A Novel Continuous Control Set Model Predictive Control for *LC*-Filtered Three-Phase Four-Wire Three-Level Voltage-Source Inverter

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***Abstract*—In this article, a novel continuous control set model predictive control (CCS–MPC) is proposed for an *LC*-filtered three-phase three-level four-wire voltage-source inverter (3P-4W-3L-VSI). The proposed MPC algorithm provides independent control of each phase of the 3P-4W-3L-VSI under various unbalanced load conditions, which shows superior performance under unbalanced loads. Furthermore, different from conventional MPC methods, the CCS–MPC achieves fixed switching frequency, hence simplifying the design of *LC* filters. In addition, dc offsets are introduced to the proposed modulation to effectively balance the neutral-point voltage of the 3P-4W-3L-VSI. Experimental results are presented to verify the effectiveness of the proposed MPC algorithm.**

***Index Terms*—Continuous control set model predictive control (CCS–MPC), fixing switching frequency, neutral-point (NP) voltage balance, three-phase four-wire three-level voltage-source inverter (3P-4W-3L-VSI).**

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I. Introduction

With the rapid progress of power electronic technologies, voltage source inverters (VSIs) have been widely utilized in distributed generation units, energy storage systems, and uninterruptible power supplies (UPS). Many control strategies have been proposed to effectively regulate the VSIs, including vector control (VC) and direct power control (DPC). For example, the VC usually employs proportional–integral controllers, which suffers from the difficulty of balancing the dynamic and steady-state control performances [1], [2]. Another example is the DPC, which possesses fast dynamics. However, it produces high output current ripples and a variable switching frequency (VSF), brining challenges to the design of harmonic filters.

In recent years, finite control set model predictive control (FCS–MPC) becomes increasingly prevalent in power electronic and motor drive applications [3], [4], [5], [6], [7], [8], [9]. Compared with the conventional VC and DPC, FCS–MPC has several advantages, such as the capability of realizing real-time optimal control while respecting system constraints, excellent steady-state and fast dynamic performances, as well as the elimination of PWM block [3], [4], [5], [6], [7], [8], [9]. In view of these advantages, different FCS–MPC algorithms are proposed for high-performance two-level VSIs. In [10], a new FCS–MPC control strategy for the single-phase two-level VSI has been proposed, which realizes seamless transition between grid-connected mode and islanded mode. Similarly, in [11], [12], [13], and [14], FCS–MPC has been applied in three-phase two-level UPS with high accuracy and fast-tracking ability. To further improve the VSI performance, different advanced FCS–MPC algorithms for multilevel VSIs have been studied. FCS–MPC methods in [15], [16], and [17] are proposed for three-phase three-level back–back converters in wind generation systems. In [18] and [19], FCS–MPC algorithms have been proposed for three-phase three-level UPS with good steady-state performance and fast dynamic response. Similarly, efficient FCS–MPC methods are proposed for three-level inverter-fed induction motor drives to enhance the torque and flux performance [20], [21]. In [22], an MPC with offset voltage injection for achieving the neutral-point (NP) voltage balance of three-phase three-level converter has been presented, which avoids employing a weighting factor. Nevertheless, the aforementioned

FCS–MPC algorithms mainly focus on three-phase balanced system and thus, may not be effective when three-phase loads are unbalanced. The circulating currents generated by three-phase unbalanced loads can result in highly distorted output voltage.

In order to supply nonlinear and unbalanced loads with improved power quality and stability, three-phase four-wire voltage-source inverters (3P-4W-VSIs) have been recommended for three-phase systems. In practice, the 3P-4W-VSIs have been widely employed in distributed generation systems, electric vehicles, and active power filters. In [23], a novel VSF frequency PWM for the 3P-4W-VSI has been presented with low current ripples and switching losses. Thus, the efficiency of the 3P-4W-VSI is improved without degrading the output current quality. Similarly, an advanced control strategy for the 3P-4W-VSI has been proposed in [24] with improved robustness against disturbance. In [25], a control strategy based on three-dimensional unbalanced coordinate transformation has been proposed for the 3P-4W-VSI, which achieves good performance with simple control structure. The abovementioned control schemes can be applied in 3P-4W-VSIs for both standalone and grid-connected operations. Different control strategies have been proposed under abnormal grid voltages, such as voltage sags [26], asymmetrical grid faults [27], and weak grid conditions [28]. Unfortunately, the abovementioned control strategies are only designed for two-level 3P-4W-VSIs, and they cannot be directly extended to three-level 3P-4W-VSIs. To effectively control the three-phase three-level four-wire voltage-source inverter (3P-4W-3L-VSI), advanced PWM schemes have been presented in recent years [29], [30].

The aforementioned control schemes for 3P-4W-VSIs utilize PWM techniques. To improve the dynamic response of the 3P-4W-VSIs, different FCS–MPC approaches have also been explored to ensure satisfactory performance. In [31] and [32], FCS–MPC with current control for the 3P-4W-2L-VSI has been presented, which can accurately track different current references under unbalanced loads. In [33], FCS–MPC for a 3P-4W-2L UPS system has been presented with excellent voltage reference tracking capacity under unbalanced loads. Furthermore, FCS–MPC can be extended to quasi-Z-source 3P-4W-2L-VSIs with unbalanced loads [34], [35]. Excellent control performance was reported. Once again, the abovementioned FCS–MPC approaches are designed for 3P-4W-2L-VSIs. Actually, Antoniewicz et al. [36] and Mohapatra and Agarwal [37] deal with 3P-4W-3L-VSIs. They utilize four power switches in the fourth wire, which increases the cost of the 3P-4W-3L-VSIs. To our best knowledge, there are few references for 4W-3P-3L T-type VSIs with MPC.

It is pointed out that all the aforementioned FCS–MPC algorithms apply only one voltage vector in each control cycle, resulting in VSFs. This brings great challenges to harmonic filter design and therefore, makes it very difficult to meet the grid standards on total harmonic distortion (THD) for grid-connected VSIs. To overcome such drawbacks, some advanced fixed switching frequency (FSF) MPC algorithms are proposed for two-level VSIs [38], [39], [40], [41], [42]. For these FSF MPC methods, there are two or more voltage vectors applied in every control period. Hence, FSF and better steady-state

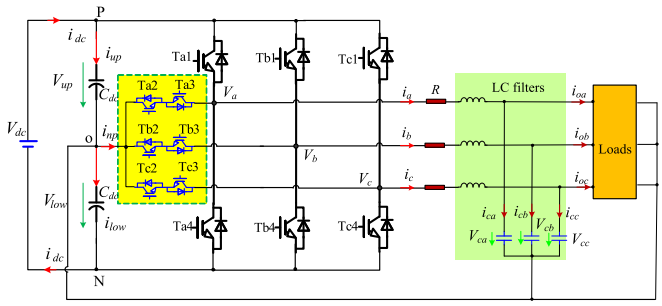

Fig. 1. Topology of the T-type four-wire three-level voltage-source inverter.

performance can be achieved. Similar FSF ideas can be extended to three-phase three-level VSIs. In [43], [44], [45], [46], [47], [48], and [49], FSF MPC algorithms for three-level VSIs have been presented, aiming at output currents tracking and the NP balancing. Unfortunately, the above FSF–MPC methods [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49] are only effective for three-phase balanced loads.

Another problem of the existing FSF–MPCs is the NP voltage balancing, which requires tedious tuning work for the NP voltage associated weighting factor in the cost function. Generally, weighting factor tuning is based on a large amount of experiments. Indeed, some articles propose MPC methods without NP voltage weighting factor. They realize the NP voltage balancing by utilizing proper small redundant voltage vectors [50], [51]. Nevertheless, these methods encounter difficulties in balancing the NP voltage in high modulation or low power factor range.

In order to obtain superior control performance for 3P-4W-3L-VSIs with unbalanced loads while achieving FSF without the NP voltage associated weighting factor, a novel continuous control set model predictive control (CCS–MPC) algorithm is proposed in this article. The proposed algorithm is developed for a T-type four-wire three-level VSI. It realizes independent control of each inverter phase with FSF. Moreover, it produces satisfying steady-state and dynamic responses under different unbalanced loads. The NP voltage is effectively balanced by injecting proper dc offset to the modulated waveforms.

The rest of this article is organized as follows: Section II presents the topology and mathematical model of 3P-4W-3L-VSIs. Then, the principle of the proposed CCS–MPC with modulated voltage vectors is illustrated in Section III. After that, the experimental evaluations have been carried out in Section VI. Finally, Section V concludes this article.

II. Topology and Mathematical Model

A. Principle of Proposed CCS–MPC

Fig. 1 shows the topology of the T-type four-wire three-level VSI, which contains four legs denoted as leg-a, leg-b, leg-c, and leg-d. Each leg of phases a, b, and c contains four power switches, whereas the leg-d is constructed by two capacitors. In Fig. 1, $V_{\rm up}$ and $V_{\rm low}$ represent the dc-link upper and lower capacitor voltage, respectively. V_{ao}, V_{bo}, and V_{co} are output voltages. i_a, i_b, and i_c are VSI output currents, and i_{ca}, i_{cb}, and i_{cc} represent currents flowing through filter capacitors. i_{oa},

TABLE I
RELATIONSHIP BETWEEN OUTPUT VOLTAGES AND SWITCHING STATES OF PHASE-X

T_{x1}	T_{x2}	T_{x3}	T_{x4}	Output voltages
1	1	0	0	V_{up}
0	1	1	0	0
0	0	1	1	$-V_{low}$

i_{ob}, and i_{oc} are load currents, i_{np} indicates the NP current, $C_{\rm dc}$ is the dc-link capacitor, R represents the filter resistance, and L and C denote the filter inductance and filter capacitance, respectively.

The relationship between switching states and the output voltage of phase-x ($x = a, b, c$) is listed in Table I, considering "O" as the reference voltage. In Table I, "1" means the power switch is turned ON and "0" represents the power switch is turned OFF. As listed in Table I, phase-x ($x = a, b, c$) outputs three different voltage levels including $V_{\rm up}$, 0, and $-V_{\rm low}$. The current paths for phase-a under different output voltages and current directions are shown in Fig. 2. Similarly, currents' paths for phase-b and phase-c can be obtained. For simplicity, only the current paths for phase-a are drawn in the article.

Noticeably, the block diagram for phase-a in s-domain can be obtained as shown in Fig. 3. Phase-b and phase-c can be obtained in a similar way.

The relationship between the output voltages and currents can be obtained from Fig. 1, which is expressed as

$$\begin{cases} V_{ao} = Ldi_a/dt + Ri_a + V_{ca} \\ V_{bo} = Ldi_b/dt + +Ri_b + V_{cb} \\ V_{co} = Ldi_c/dt + Ri_c + V_{cc}. \end{cases} \tag{1}$$

Currents flowing through the filter capacitors are written as

$$\begin{cases} i_{ca} = CdV_{ca}/dt = i_a - i_{oa} \\ i_{cb} = CdV_{cb}/dt = i_b - i_{ob} \\ i_{cc} = CdV_{cc}/dt = i_c - i_{oc}. \end{cases} \tag{2}$$

As shown in Fig. 1, the output voltage V_{xo} ($x = a, b, c$) can be obtained in terms of the dc-link voltage and switching states, which is expressed as

$$\begin{cases} V_{ao} = V_{\rm up}T_{a1}(T_{a1}{+}1)/2 - V_{\rm low}T_{a4}(T_{a4}{+}1)/2 \\ V_{bo} = V_{\rm up}T_{b1}(T_{b1}{+}1)/2 - V_{\rm low}T_{b4}(T_{b4}{+}1)/2 \\ V_{co} = V_{\rm up}T_{c1}(T_{c1}{+}1)/2 - V_{\rm low}T_{c4}(T_{c4}{+}1)/2. \end{cases} \tag{3}$$

Switching states T_{x1} ($x = a, b, c$) and T_{x4} ($x = a, b, c$) can be expressed as

$$T_{x1} = \begin{cases} 1 & \text{switch } Tx1 \text{ on} \\ 0 & \text{switch } Tx1 \text{ off} \end{cases} \quad (x = a, b, c) \tag{4}$$

$$T_{x4} = \begin{cases} 1 & \text{switch } Tx4 \text{ on} \\ 0 & \text{switch } Tx4 \text{ off} \end{cases} \quad (x = a, b, c)\ . \tag{5}$$

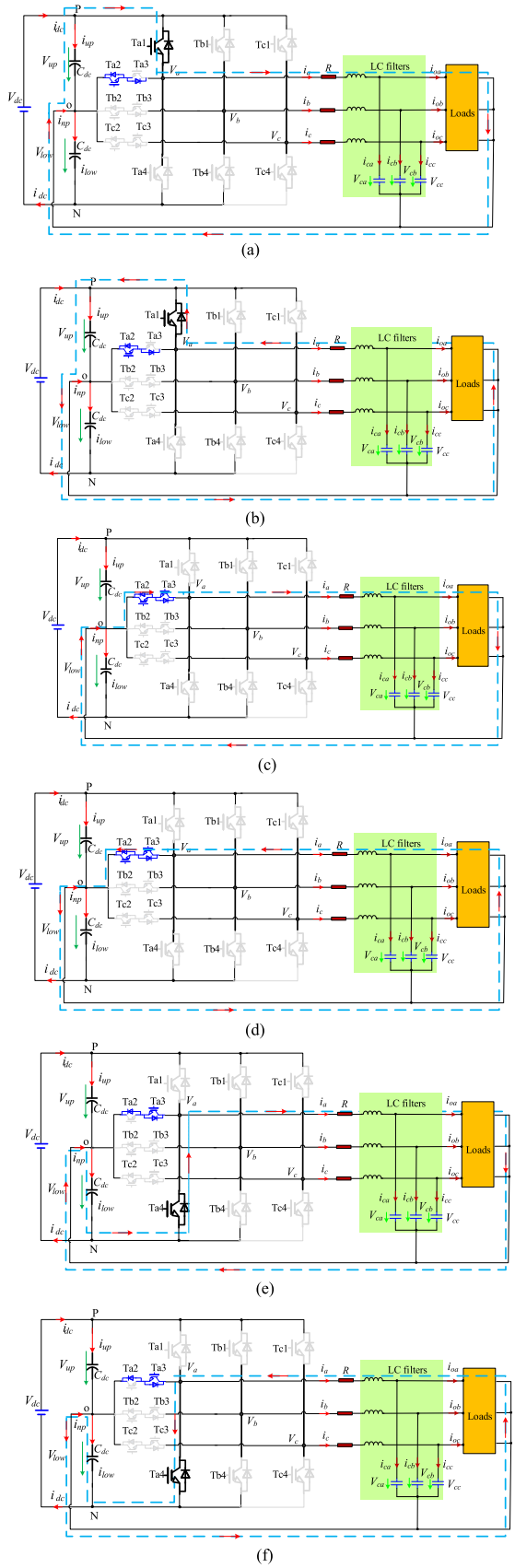

Fig. 2. Different current paths for phase-a. (a) Output $V_{\rm up}$ with $i_a > 0$. (b) Output $V_{\rm up}$ with $i_a < 0$. (c) Output zero with $i_a > 0$. (d) Output zero with $i_a < 0$. (e) Output $-V_{\rm low}$ with $i_a > 0$. (f) Output $-V_{low}$ with $i_a < 0$.

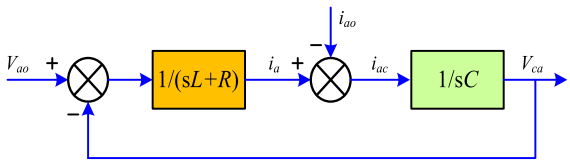

Fig. 3. Block diagram for phase-a in s-domain.

Combining (1) and (2), the system state-space representation can be obtained as

$$\frac{d}{dt}\begin{bmatrix} i_x \\ V_{cx} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix}\begin{bmatrix} i_x \\ V_{cx} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}\begin{bmatrix} V_{xo} \\ i_{ox} \end{bmatrix} \quad (x = a, b, c) \ . \tag{6}$$

Utilizing with Euler forward approximation, the predictive model at the (k+1)th instant can be obtained as

$$\begin{cases} i_x(k+1) = i_x(k) + \frac{T_s}{L}(V_{xo}(k) - V_{cx}(k) - Ri_x(k)) \\ V_{cx}(k+1) = V_{cx}(k) + \frac{T_s}{L}(i_x(k) - i_{ox}(k)) \end{cases} \quad x = a, b, c \tag{7}$$

where T_s represents the sampling period.

III. Proposed CCS–MPC Algorithms

For 3P-4W-3L-VSIs, the capacitor voltage references are given

$$\begin{cases} V_{ca}^*(t) = V_m \cos(\omega_{\text{ref}} t) \\ V_{cb}^*(t) = V_m \cos(\omega_{\text{ref}} t - 2\pi/3) \\ V_{cc}^*(t) = V_m \cos(\omega_{\text{ref}} t + 2\pi/3) \end{cases} \tag{8}$$

where $V^*{}_{cx}(t)$ ($x = a, b, c$) represents the phase-x capacitor voltage reference, V_m denotes the magnitude of capacitor voltage references, and ω_{ref} is the reference angular frequency.

The VSI aims to track the capacitor voltage references rapidly and accurately. Therefore, the cost function is constructed as

$$\begin{cases} g_{ca} = (V_{ca}^*(k+1) - V_{ca}(k+1))^2 \\ g_{cb} = (V_{cb}^*(k+1) - V_{cb}(k+1))^2 \\ g_{cc} = (V_{cc}^*(k+1) - V_{cc}(k+1))^2. \end{cases} \tag{9}$$

There is a control delay when implementing the MPC algorithm using digital signal processors (DSP) [52]. To compensate the digital control delay, the cost function is formulated as

$$\begin{cases} g_{ca} = (V_{ca}^*(k+2) - V_{ca}(k+2))^2 \\ g_{cb} = (V_{cb}^*(k+2) - V_{cb}(k+2))^2 \\ g_{cc} = (V_{cc}^*(k+2) - V_{cc}(k+2))^2. \end{cases} \tag{10}$$

As shown in (9), it is necessary to predict the capacitor output voltages of the 3P-4W-3L-VSI at the (k+2)th sampling period. From (6), it can be obtained as

$$\begin{cases} i_x(k+2) = i_x(k+1) + \frac{T_s}{L}(V_{xo}(k+1) - V_{cx}(k+1) \\ \qquad\qquad -Ri_x(k+1)) \\ V_{cx}(k+2) = V_{cx}(k+1) + \frac{T_s}{L}(i_x(k+1) - i_{ox}(k+1)) \end{cases} \quad x = a, b, c \ . \tag{11}$$

Substituting (7) into (11), the capacitor output voltage at the (k+2)th sampling period is expressed as

$$V_{cx}(k+2) = \frac{T_s^2}{LC}V_{xo}(k) + \left(1 - \frac{T_s^2}{LC}\right)V_{cx}(k) + \left(\frac{2T_s}{C} - \frac{T_s^2 R}{LC}\right)i_x(k) - \frac{T_s}{C}i_{ox}(k) - \frac{T_s}{C}i_{ox}(k+1) \quad x = a, b, c \ . \tag{12}$$

When the sampling frequency is much higher than the fundamental frequency of output voltages, the load currents of the 3P-4W-3L-VSI can be assumed to be constant within one sampling period, which is written as

$$i_{ox}(k+1) \approx i_{ox}(k) \quad x = a, b, c \ . \tag{13}$$

Substituting (13) into (12), it can be written as

$$V_{cx}(k+2) = \frac{T_s^2}{LC}V_{xo}(k) + \left(1 - \frac{T_s^2}{LC}\right)V_{cx}(k) + \left(\frac{2T_s}{C} - \frac{T_s^2 R}{LC}\right)i_x(k) - \frac{2T_s}{C}i_{ox}(k) \quad x = a, b, c \ . \tag{14}$$

To minimize the cost function, the following condition should be satisfied.

$$\begin{cases} \frac{\partial g_{ca}(V_{ao}(k))}{\partial V_{ao}(k)} = 0 \\ \frac{\partial g_{cb}(V_{bo}(k))}{\partial V_{bo}(k)} = 0 \\ \frac{\partial g_{cc}(V_{co}(k))}{\partial V_{co}(k)} = 0. \end{cases} \tag{15}$$

Combining (10) and (15), following equation is derived:

$$\begin{cases} \frac{\partial g_{ca}(V_{ao}(k))}{\partial V_{ao}(k)} = -2(V_{ca}^*(k+2) - V_{ca}(k+2))\frac{\partial V_{ca}(k+2)}{\partial V_{ao}(k)} = 0 \\ \frac{\partial g_{cb}(V_{bo}(k))}{\partial V_{bo}(k)} = -2(V_{cb}^*(k+2) - V_{cb}(k+2))\frac{\partial V_{cb}(k+2)}{\partial V_{bo}(k)} = 0 \\ \frac{\partial g_{cc}(V_{co}(k))}{\partial V_{co}(k)} = -2(V_{cc}^*(k+2) - V_{cc}(k+2))\frac{\partial V_{cc}(k+2)}{\partial V_{co}(k)} = 0. \end{cases} \tag{16}$$

Substituting (14) into (16), the output reference voltage $V_{xo}{}^*(k)$ ($x = a, b, c$) at the (k)th sampling instant is expressed as

$$V_{xo}^*(k) = \frac{2L}{T_s}i_{ox}(k) + \left(R - \frac{2L}{T_s}\right)i_x(k) + \left(1 - \frac{LC}{T_s^2}\right)V_{cx}(k) + \frac{LC}{T_s^2}V_{cx}^*(k+2) \quad x = a, b, c. \tag{17}$$

The capacitor voltage reference $V^*{}_{cx}(k+1)$ ($x = a, b, c$) at the (k+1)th sampling instant can be obtained by linear interpolation theory, which is written as

$$V_{cx}^*(k+1) = 3V_{cx}^*(k) - 3V_{cx}^*(k-1) + V_{cx}^*(k-2) \quad (x = a, b, c) \ . \tag{18}$$

Similarly, the capacitor voltage reference $V^*_{cx}(k+2)$ ($x = a, b, c$) at the (k+2)th sampling instant can be obtained as

$$V^*_{cx}(k+2) = 3V^*_{cx}(k+1) - 3V^*_{cx}(k) + V^*_{cx}(k-1) \quad (x = a, b, c) \ . \tag{19}$$

Substituting (18) into (19), it is obtained as

$$V^*_{cx}(k+2) = 6V^*_{cx}(k) - 8V^*_{cx}(k-1) + 3V^*_{cx}(k-2) \quad (x = a, b, c) \, . \tag{20}$$

Substituting (20) into (17), the output reference voltages at the (k)th sampling instant are written as

$$V^*_{xo}(k) = \left(R - \frac{2L}{T_s}\right) i_x(k) + \frac{2L}{T_s} i_{ox}(k) + \left(1 - \frac{LC}{T_s^2}\right) V_{cx}(k) + \frac{LC}{T_s^2}(6V^*_{cx}(k) - 8V^*_{cx}(k-1) + 3V^*_{cx}(k-2)) \quad x = a, b, c. \tag{21}$$

The second-order derivative of cost function (10) can be obtained as

$$\frac{\partial^2 g_{ca}(V_{ao}(k))}{\partial V_{ao}(k)^2} = \frac{\partial^2 g_{cb}(V_{bo}(k))}{\partial V_{bo}(k)^2} = \frac{\partial^2 g_{cc}(V_{co}(k))}{\partial V_{co}(k)^2} = 2\left(\frac{T_s^2}{LC}\right)^2 > 0. \tag{22}$$

Since (22) is nonnegative, the first-order derivative of cost function (10) is monotonically increasing, and it intersects with the zero axis. Thus, the output voltages in (21) are the optimal voltage vectors.

B. Balancing the NP Voltage

Carried-based pulsewidth modulation (CBPWM) owns a lot of advantages, such as easy implementation, good steady-state performance, and so on. Thus, it has been widely utilized in power converters. To balance the NP voltage for the 3P-4W-3L-VSI, zero sequence injection based CBPWM is proposed. For the 3P-4W-3L-VSI, each phase is independently controlled without coupling between different phases. Thus, only phase-a of the 3P-4W-3L-VSI is analyzed and the other phases can be analyzed in a similar way. The principle of CBPWM for the 3P-4W-3L-VSI is depicted in Fig. 4. In terms of the volt-second balance principle, the duty times of different output voltages are written as

$$\begin{cases} T_{a1} = \frac{2V^*_{ao}}{V_{\rm dc}} T_s, T_{a0} = (1 - \frac{2V^*_{ao}}{V_{\rm dc}}) T_s, T_{a-1} = 0 & (V^*_{ao} > 0) \\ T_{a1} = 0, T_{a0} = (1 - \frac{2|V^*_{ao}|}{V_{\rm dc}}) T_s, T_{a-1} = \frac{2|V^*_{ao}|}{V_{\rm dc}} T_s & (V^*_{ao} < 0) \end{cases} \tag{23}$$

where T_{az} (z = 10,−1) means the duty times of level z output voltage for phase-a of the 3P-4W-3L-VSI.

As shown in Fig. 2, it can be summarized as follows:

1) The dc-link upper capacitor is discharged with $i_a > 0$ or charged with $i_a < 0$ when the phase-a output voltage level is 1, and the corresponding dc-link lower capacitor voltage will increase or decrease due to the constant dc-link voltage.

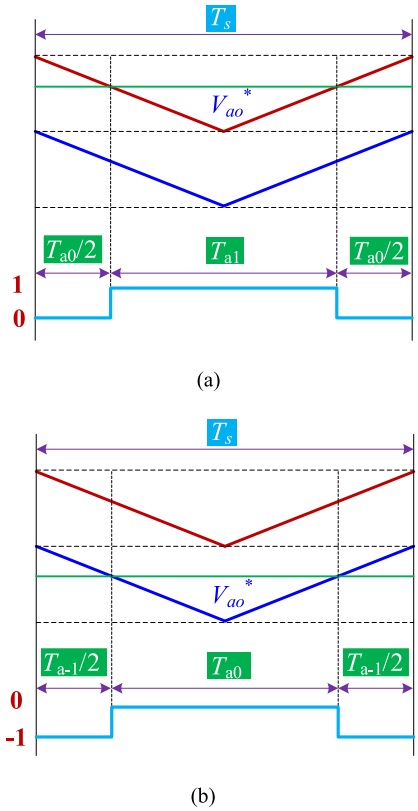

Fig. 4. Principle of CBPWM for phase-a. (a) $V_{ao} > 0$. (b) $V_{ao} < 0$.

TABLE II
INFLUENCE ON THE DC-LINK VOLTAGE WITH DIFFERENT OUTPUT LEVELS AND PHASE-A CURRENT

Output level	i_a	V_{up}	V_{low}
1	>0	decrease	increase
	<0	increase	decrease
0	>0	remain	remain
	<0	remain	remain
-1	>0	decrease	increase
	<0	increase	decrease

2) The dc-link upper and lower capacitor voltages keep unchanged when the output voltage level is zero.
3) The dc-link lower capacitor is discharged with $i_a > 0$ or charged with $i_a < 0$ when the phase-a output voltage level is −1, and the corresponding dc-link upper capacitor voltage will decrease or increase due to the constant dc-link voltage.

Based on the above analysis, the influence of i_a and the output voltage level on the dc-link upper and lower capacitor voltages are summarized in Table II.

The carrier waveform frequency of CBPWM is much higher than the fundamental frequency of the output voltages of the 3P-4W-3L-VSI. According to (23), the NP current influenced by the phase-a current $i_{{\rm NP}a}$ is expressed as

$$i_{{\rm NP}a} = \frac{2\,|V^*_{ao}|}{V_{\rm dc}} i_a. \tag{24}$$

Thus, the total NP current $i_{\rm np}$ influenced by three-phase currents is obtained as

$$i_{\rm np} = \sum_{x=a,b,c} i_{{\rm NP}x} = \frac{2}{V_{\rm dc}}(|V_{ao}^*|\, i_a + |V_{bo}^*|\, i_b + |V_{co}^*|\, i_c). \quad (25)$$

In Fig. 1, the dc-link upper and lower capacitor currents can be expressed as

$$\begin{cases} i_{c1} = C_{\rm dc}\frac{dV_{\rm up}}{dt} \\ i_{c2} = C_{\rm dc}\frac{dV_{\rm low}}{dt}. \end{cases} \quad (26)$$

In terms of (26), the NP current $i_{\rm np}$ of the 3P-4W-3L-VSI is obtained as

$$i_{\rm np} = C_{\rm dc}\frac{dV_{\rm low}}{dt} - C_{\rm dc}\frac{dV_{\rm up}}{dt} = C_{\rm dc}\frac{d(V_{\rm low}-V_{\rm up})}{dt} = C_{\rm dc}\frac{d\Delta V_{\rm NP}}{dt} \quad (27)$$

where $\Delta V_{\rm NP}$ represents the voltage difference between the dc-link upper capacitor voltage and the dc-link lower capacitor voltage.

From (27), it can be obtained as

$$\Delta V_{\rm NP} = \frac{1}{C_{\rm dc}}\int i_{\rm np}dt. \quad (28)$$

Substituting (24) into (28), the influence on $\Delta V_{{\rm NP}\,a}$ for phase-a in the current cycle is expressed as

$$\Delta V_{{\rm NP}a} = \frac{1}{C_{\rm dc}}\int_{t_1}^{t_1+T_p}\frac{2\,|V_{ao}^*|}{V_{\rm dc}} i_a dt \quad (29)$$

where T_p means the period time of phase-a current.

As seen in (29), the voltage difference $\Delta V_{{\rm NP}\,a}$ in the period time become zero if the positive cycle and negative cycle of phase-a current are symmetrical, which means the NP voltage will fluctuate with fundamental frequency. The same conclusion can be obtained for phase-b and phase-c. When zero-sequence current $I_{\rm dc}$ is injected into phase-a of the 3P-4W-3L-VSI, the influence on $\Delta V_{{\rm PN}\,a}$ for phase-a in the current cycle is expressed as

$$\begin{aligned}\Delta V_{{\rm NP}a} &= \frac{1}{C_{\rm dc}}\int_{t_1}^{t_1+T_p}\frac{2\,|V_{ao}^*|}{V_{\rm dc}}(i_a + I_{\rm dc})dt \\ &= \frac{1}{C_{\rm dc}}\int_{t_1}^{t_1+T_p}\frac{2\,|V_{ao}^*|}{V_{\rm dc}} I_{{\rm dc}sa}dt \end{aligned} \quad (30)$$

where $I_{{\rm dc}sa}$ is the sum of phase-a dc offset current and the injected zero-sequence current $I_{\rm dc}$.

From (30), it can be found that the NP voltage can be effectively controlled by injecting a proper zero sequence current. According to (21), the output reference voltages with injecting zero sequence currents at the (k)th sampling instant is expressed as

$$\begin{aligned} V_{xo}^*(k) = &\left(R - \frac{2L}{T_s}\right)(i_x(k) + I_{{\rm dc}x}(k)) \\ &+ \frac{2L}{T_s} i_{ox}(k) + \left(1 - \frac{LC}{T_s^2}\right)V_{cx}(k) \\ &+ \frac{LC}{T_s^2}(6V_{cx}^*(k) - 8V_{cx}^*(k-1) \\ &+ 3V_{cx}^*(k-2)) \quad x = a, b, c. \end{aligned} \quad (31)$$

As seen from (31), the NP voltage of the 3P-4W-3L-VSI can be effectively controlled by injecting proper zero sequence voltages [22]. This gives new output voltage references at the (k)th sampling instant as shown as

$$\begin{cases} V_{{\rm ref}a}^*(k) = V_{ao}^*(k) + V_{{\rm offset}a}(k) \\ V_{{\rm ref}b}^*(k) = V_{bo}^*(k) + V_{{\rm offset}b}(k) \\ V_{{\rm ref}c}^*(k) = V_{co}^*(k) + V_{{\rm offset}c}(k) \end{cases} \quad (32)$$

where $V^*{}_{{\rm ref}\,a}$, $V^*{}_{{\rm ref}\,b}$, and $V^*{}_{{\rm ref}\,c}$ indicate the new output voltage references, $V_{{\rm offset}\,a}$, $V_{{\rm offset}\,b}$, and $V_{{\rm offset}\,c}$ represent the offset voltage that is injected to control the NP voltage.

Three phases of the 3P-4W-3L-VSI will together influence the NP voltage. Thus, the injected zero-sequence voltages of three phases can be set to the same, which is set as

$$V_{{\rm offset}a} = V_{{\rm offset}b} = V_{{\rm offset}c} = V_{\rm offset}. \quad (33)$$

The injected zero sequence voltage $V_{\rm offset}$ should satisfy the following condition:

$$\begin{cases} -V_{\max}^* \le V_{ao}^* + V_{\rm offset} \le V_{\max}^* \\ -V_{\max}^* \le V_{bo}^* + V_{\rm offset} \le V_{\max}^* \\ -V_{\max}^* \le V_{co}^* + V_{\rm offset} \le V_{\max}^* \end{cases} \quad (34)$$

where $V^*{}_{\max}$ means the maximum amplitude of three-phase output voltages.

In terms of above analysis, the offset injection voltage $V_{\rm offset}$ can be expressed as (35) in terms of $\Delta V_{\rm NP}$. As shown in (34), it can be observed: 1) the zero-sequence current $V_{\rm offset}$ is positive when the upper capacitor voltage is larger than the lower capacitor voltage; and 2) the zero-sequence current $V_{\rm offset}$ is negative when the upper capacitor voltage is smaller than the lower capacitor voltage

$$V_{\rm offset} = \begin{cases} \frac{V_{\rm dc}}{2} - V_{\max}^* & (\Delta V_{\rm NP} \le 0) \\ -\frac{V_{\rm dc}}{2} + V_{\max}^* & (\Delta V_{\rm NP} \ge 0). \end{cases} \quad (35)$$

Following the above analysis, the control strategy for the T-type 3P-4W-3L-VSI is depicted in Fig. 5. As shown Fig. 5, the output voltage references of the VSI can be obtained by the proposed CCS–MPC according to the VSI output currents, load currents, and output capacitor voltages. Then, the pulses of the VSI power switches can be obtained by sinusoidal pulsewidth modulation. The proposed CCS–MPC can be easily implemented using common microcontrollers shown in Fig. 5.

IV. Experimental Results

To verify the effectiveness of the proposed CCS–MPC with modulated voltage vectors algorithm, an experimental platform is built based on a DSP TMS320F2808, and PWM pulses are extended by a complex programmable logic device EPM7256. It is shown in Fig. 6. The output voltages (V_{ca}, V_{cb}, V_{cc}) are sampled by LEM voltage sensors, and the inductor currents (i_a, i_b, i_c) and the load currents (i_{oa}, i_{ob}, i_{oc}) are sampled by LEM current sensors. Detailed experimental parameters are listed in Table III.

The testing conditions of the proposed CCS–MPC algorithm are listed as follows:

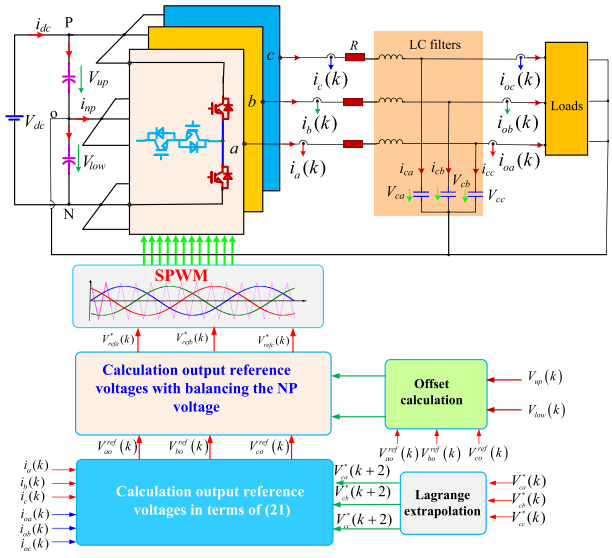

Fig. 5. Control strategy for the T-type 3P-4W-3L-VSI.

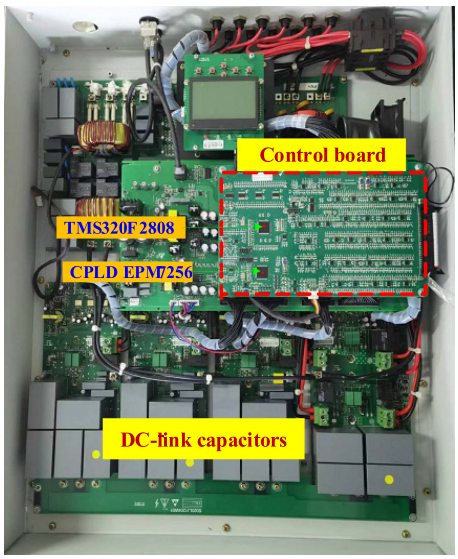

Fig. 6. Experimental platform.

TABLE III
EXPERIMENTAL PARAMETERS

Parameter	Description	Values
V_{dc}	dc input voltage	260 V
C_{dc}	dc filter capacitor	1000 μF
L	Filter inductance	3 mH
C	Output filter capacitor	4.7 μF
R	Filter total resistance	0.01Ω
f_s	Sampling frequency	16 kHz

Condition 1: The amplitude and the frequency of output voltages are set to 120 V and 50 Hz without loads ($R_a = R_b = R_c = \infty\ \Omega$), respectively.

Condition 2: The amplitude and the frequency of output voltages are set to 120 V and 50 Hz with balanced resistance loads ($R_a = R_b = R_c = 60\ \Omega$), respectively.

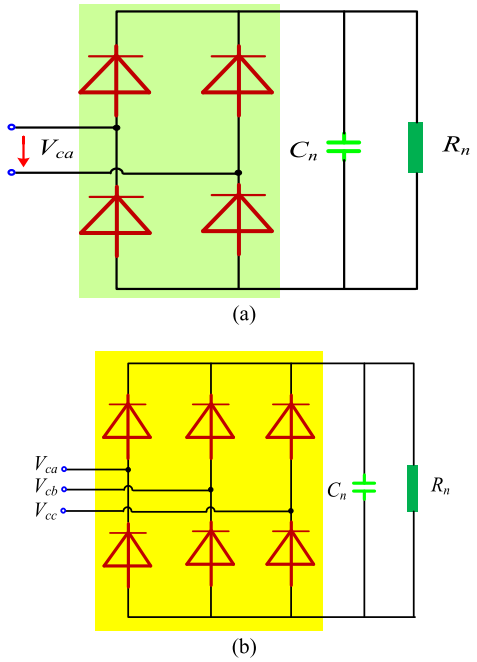

Fig. 7. Nonlinear loads. (a) Single-phase nonlinear load. (b) Three-phase nonlinear load.

Condition 3: The amplitude and the frequency of output voltages are set to 120 V and 50 Hz with balanced resistance loads ($R_a = R_b = R_c = 30\ \Omega$), respectively.

Condition 4: The amplitude and the frequency of output voltages are given as 120 V and 50 Hz with unbalanced loads, respectively. The phase-a is with nonlinear load shown in Fig. 7(a) ($C_n = 100\ \mu$F, $R_n = 23\ \Omega$), and phase-b and phase-c are with resistance loads ($R_b = R_c = 30\ \Omega$).

Condition 5: The amplitude and the frequency of output voltages are set to 120 V and 50 Hz with nonlinear load displayed in Fig. 7(b) ($C_n = 100\ \mu$F, $R_n = 23\ \Omega$), respectively.

Condition 6: The amplitude and the frequency of output voltages are kept the same with Condition 1, the balanced resistance load is stepped from 60 to 30 Ω.

Condition 7: The amplitude and the frequency of output voltages are kept the same with Condition 1, the balanced resistance load is stepped from 30 to 60 Ω.

Condition 8: The VSI operates in Condition 4, then, the phase-a load is suddenly changed from nonlinear load to no load.

Condition 9: The VSI operates in Condition 5, then, the phase-a load is suddenly changed from nonlinear load to no load.

A. Steady-State Experimental Results

The steady-state performance of the proposed CCS–MPC algorithm has been evaluated. Fig. 8 displays the steady-state output voltages (V_{ca}, V_{cb}), phase-a load current i_{oa}, the dc-link upper capacitor voltage V_{up}, and Fast , (FFT) of the phase-a voltage V_{ca} under Condition 1, Condition 2, and Condition 3. The waveform of phase-c output voltage V_{cc} is very similar to the phase-a output voltage V_{ca} with only a phase shift. Furthermore, the waveforms of phase-b and phase-c load currents (i_{ob} and i_{oc})

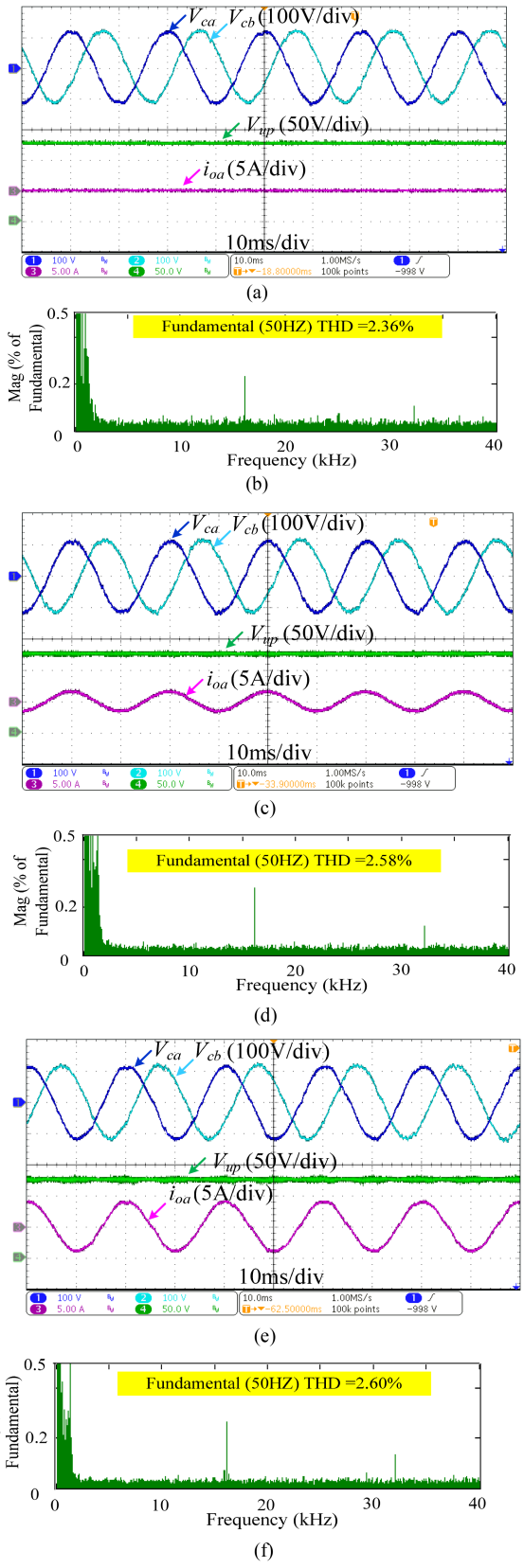

Fig. 8. Steady-state experimental results with linear loads. (a) and (b) under Condition 1. (c) and (d) under Condition 2. (e) and (f) under Condition 3.

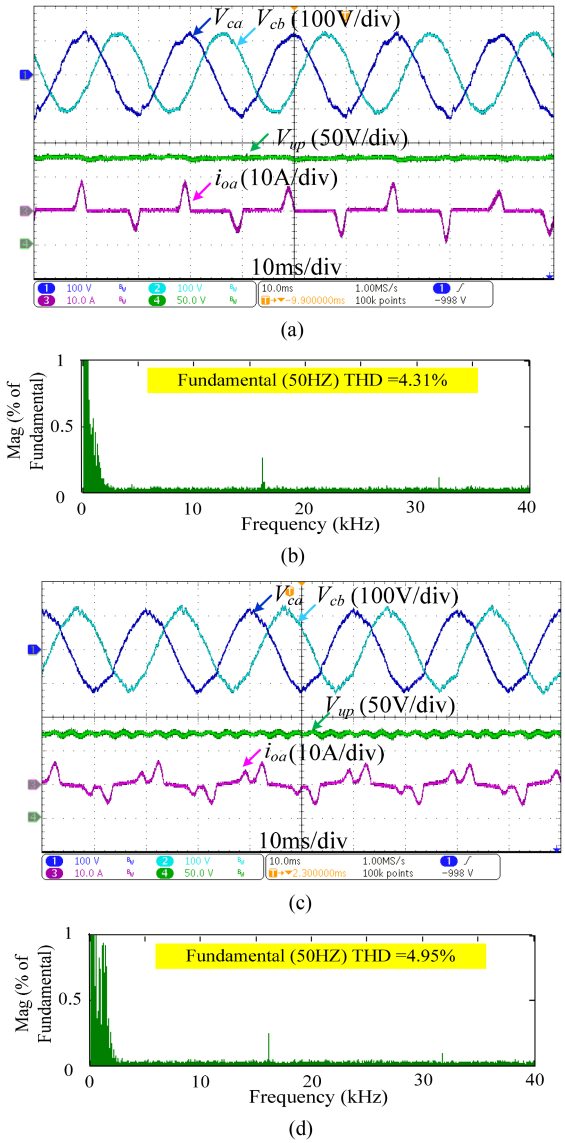

Fig. 9. Steady-state experimental results with nonlinear loads. (a) and (b) under Condition 4. (c) and (d) under Condition 5.

are very similar to the phase-a load current i_{oa} with only phase shifts. Thus, the experimental waveforms of V_{cc}, i_{ob}, and i_{oc} are not shown. The following points can be observed from Fig. 8: 1) output voltages are sinusoidal with the THD less than 3% under different loads, 2) the amplitude of output voltages is well controlled at 120 V under different loads, 3) the dc-link capacitor voltages are well balanced at 130 V with the peak-to-peak ripple less than 10 V, and 4) main high-order harmonics are concentrated at the sampling frequency and its multiples such as 16 and 32 kHz, indicating an FSF. Fig. 8 demonstrates that the proposed CCS–MPC has excellent output voltage reference tracking capacity while maintaining a well-balanced NP voltage and an FSF.

The corresponding experimental results with nonlinear loads under Condition 4 and Condition 5 are depicted in Fig. 9. The following conclusions can be drawn from Fig. 9:

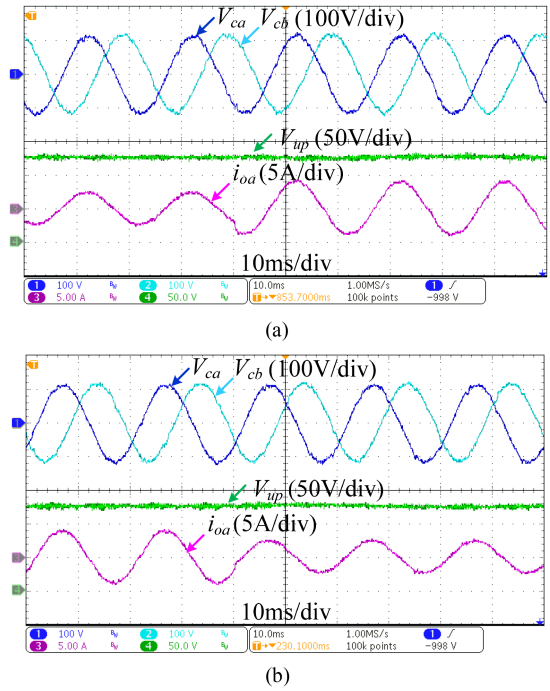

Fig. 10. Dynamic experimental results with linear loads. (a) Condition 6. (b) Condition 7.

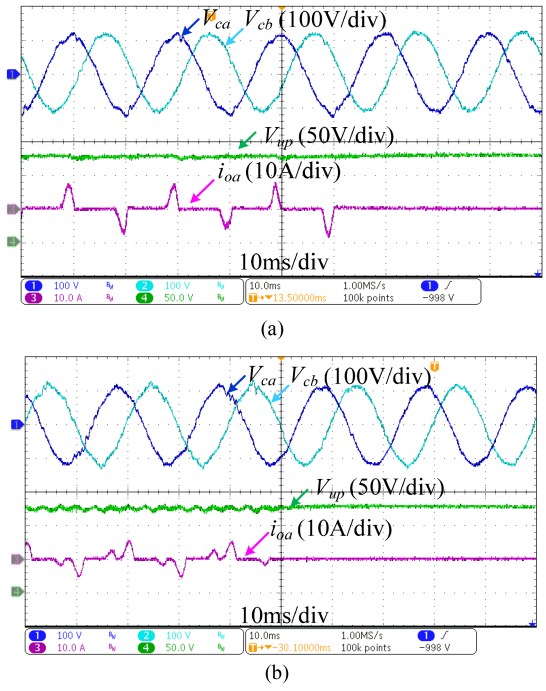

Fig. 11. Dynamic experimental results with nonlinear loads. (a) Condition 8. (b) Condition 9.

1) The output voltages are sinusoidal, and the THD values of phase-a output voltage under nonlinear loads are 4.30% and 4.95%, respectively. Compared to linear loads shown in Fig. 8, THD values become larger due to nonlinear loads with higher low-order harmonics, such as fifth and seventh harmonics.
2) The amplitude of output voltages is well controlled at 120 V.
3) The dc-link capacitor voltage is well balanced with the peak-to-peak ripple less than 15 V.

B. Dynamic Experimental Results

To further verify the validity of the proposed CCS–MPC algorithm, some dynamic tests have been carried out. Fig. 10 displays the dynamics of the output voltages (V_{ca}, V_{cb}), phase-a load output current i_{oa}, and the dc-link upper capacitor voltage $V_{\rm up}$ under Condition 6 and Condition 7. The corresponding dynamic responses under Condition 8 and Condition 9 are shown in Fig. 11.

It can be seen from Figs. 10 and 11 that 1) the output voltage waveforms remain sinusoidal under load step change, and 2) the upper capacitor voltage is well controlled at the desired voltage during dynamics. Therefore, it can be concluded that the proposed CCS–MPC endows strong robustness for load disturbances due to its fast dynamic response.

C. Experimental Results of Deadbeat Control

Deadbeat control (DBC) is widely utilized in power converters due to its simplicity and easy implementation by DSPs. DBC for the four-wire inverter proposed in [53] is utilized to compare with the proposed CCS–MPC algorithm, which can provide balanced sinusoidal output voltages under balanced and unbalanced loads. Each output voltage reference of the 3P-4W-3L-VSI at the (k)th sampling instant can be obtained in terms of DBC law, which is expressed as

$$\begin{cases} V^*_{refa}(k) = V^*_{ca}(k) + Ri_a(k) + L(i^*_a(k) - i_a(k))/T_s \\ V^*_{refb}(k) = V^*_{cb}(k) + Ri_b(k) + L(i^*_b(k) - i_b(k))/T_s \\ V^*_{refc}(k) = V^*_{cc}(k) + Ri_c(k) + L(i^*_c(k) - i_c(k))/T_s \end{cases} \tag{36}$$

$$\begin{cases} i^*_a(k) = i_{oa}(k) + C(V^*_{ca}(k) - V_{ca}(k))/T_s \\ i^*_b(k) = i_{ob}(k) + C(V^*_{cb}(k) - V_{cb}(k))/T_s \\ i^*_c(k) = i_{oc}(k) + C(V^*_{cc}(k) - V_{cc}(k))/T_s \end{cases} \tag{37}$$

where $i^*{}_x(k)$ ($x = a, b, c$) represents phase-x inductor current reference at the (k)th sampling instant.

Fig. 12 below displays the steady-state output voltages (V_{ca}, V_{cb}), phase-a load current i_{oa}, the dc-link upper capacitor voltage $V_{\rm up}$, and FFT of the phase-a voltage V_{ca} under Condition 3 and Condition 4. From Fig. 12, the following observations can be made: 1) output voltages are sinusoidal with THD values 2.70% under Condition 3 and 4.57% under Condition 4, and 2) the dc-link capacitor voltages of the 3P-4W-3L-VSI are controlled at 130 V with the peak-to-peak ripple less than 10 V. Comparing Fig. 12 with Fig. 8, it can be concluded that the proposed CCS–MPC owns better steady-state performance, which illustrates the effectiveness of the proposed MPC.

D. Parameter Sensitivity Evaluation

In practice, the filter inductance L and the filter capacitor C vary with respect to operating environment, such as temperature

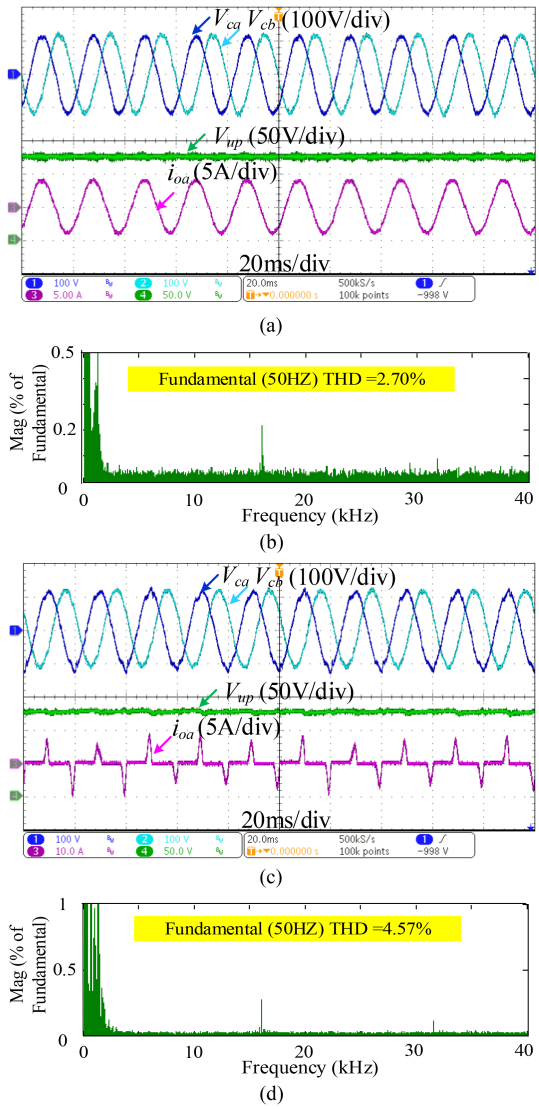

Fig. 12. Steady-state experimental results for deadbeat control in [53]. (a) and (b) under Condition 3 (c) and (d) under Condition 4.

and frequency. To evaluate the robustness of the proposed CCS–MPC algorithm, the real filter parameters of the 3P-4W-3L-VSI have been changed. The filter inductance change rate ΔL and the filter capacitor change rate ΔC are defined as

$$\begin{cases} \Delta L = \frac{L_r - L_m}{L_m} \times 100\% \\ \Delta C = \frac{C_r - C_m}{C_m} \times 100\% \end{cases} \tag{38}$$

where L_r and L_m mean the actual filter inductance value and the model filter inductance value used in the MPC algorithm, respectively. C_r and C_m represent the actual filter capacitor value and the model filter capacitor utilized in the CCS–MPC algorithm, respectively. In the system, model filter L_m and C_m are kept as $L_m = 3$ mH and $C_m = 4.7$ μF, whereas the actual filter L_r and C_r are changed under different operations. Parameter sensitivity of the phase-a output voltage THD Condition 3 for the proposed CCS MPC is listed in Table III. The following observations can be made from Table III: 1) the THD value decreases or increases with increasing or decreasing the real filters L_r and C_r, 2) the THD value is less than 4% with high-quality output voltages even with 50% filter parameter variation, and 3) the THD value has almost kept unchanged with filter parameters varying in the range from -10% to $+10\%$ that is usually considered as the practical condition. From Table IV, it can clearly illustrate that the proposed CCS–MPC endows strong robustness for filter parameters.

TABLE IV
PARAMETER SENSITIVITY EVALUATION

ΔL	-50%	-30%	-10%	0%	+10%	+30%	+50%
THD	3.38%	2.98%	2.63%	2.36%	2.28%	2.01%	1.87%
ΔC	-50%	-30%	-10%	0%	+10%	+30%	+50%
THD	3.32%	2.95%	2.63%	2.36%	2.26%	1.98%	1.81%

TABLE V
DIFFERENT MPCS COMPARISON

MPCs	Complexity	Loads	THD	Switching frequency	Dynamic response
MPC [33]	high	unbalanced loads	high	VSF	fast
MPC [34]	high	unbalanced loads	high	VSF	fast
MPC [44]	high	balanced loads	low	FSF	fast
MPC [46]	low	balanced loads	low	FSF	fast
Proposed MPC	low	unbalanced loads	low	FSF	fast

E. Comparison of Different MPC Algorithms

The performance of different MPC algorithms has been evaluated and is listed in Table V. Noticeably, term "complexity" refers to the execution time when implementing different MPC algorithms. In terms of complexity, supplying loads, THD, switching frequency, and dynamic response, it can be found that the proposed MPC has excellent performance. Thus, the proposed CCS–MPC of T-type 3P-4W-3L-VSI can be applied in distributed generation systems in the future.

V. CONCLUSION

A new MPC with modulated voltage vectors is proposed for *LC*-filtered four-wire three-level VSI in this article. Comprehensive experiments are carried out to verify effectiveness and correctness. Some conclusions are summarized as follows:

1) It contributes to producing satisfying control performance under three-phase unbalanced loads while achieving NP voltage balance and FSF.
2) Output voltages are sinusoidal with THD less than 5% under linear or nonlinear loads.
3) The proposed CCS–MPC is robust to load disturbances due to its fast dynamic response.
4) The proposed CCS–MPC has strong robustness for filter parameters, and the THD value is less than 4% with high quality of output voltages even with 50% filter parameter variation under linear loads.

In a word, the proposed CCS–MPC of 3P-4W-3L-VSIs has wide application prospects in distributed generation systems.

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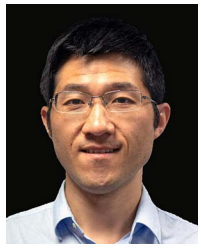

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