A Modulation Scheme Based on Virtual Voltage Levels for Capacitor Voltage Balancing of the Four-Level Diode Clamped Converter

Javad Ebrahimi, *Member, IEEE*, Shima Shahnooshi, Suzan Eren, *Member, IEEE*, and Alireza Bakhshai, *Fellow, IEEE*

***Abstract*—This article proposes a modulation scheme based on the concept of virtual voltage levels for regulating the dc-link capacitor voltages of a four-level diode clamped converter under restricted operating conditions. The proposed virtual-level space vector modulation (SVM) scheme sets the average neutral point currents to zero, which results in no net change in dc-link capacitor voltages and thereby voltage balancing. In addition, a closed-loop algorithm is developed to compensate for any voltage drift due to unideal practical conditions. Consequently, the modulation of the reference voltages results in the desired output voltages while regulating the dc-link capacitor voltages at various operating points. In the proposed modulation scheme, switching frequencies are not significantly increased, and they are lower than those in the classic virtual-vector SVM method. The simulation results demonstrate the effectiveness of the proposed modulation scheme and highlight its main benefits and features. The simulation results are verified through a laboratory-type experimental setup.**

***Index Terms*—Capacitor voltage balancing, diode-clamped converter (DCC), multilevel converter, space vector modulation (SVM).**

I. Introduction

MULTILEVEL diode-clamped converter (DCC) topologies are among the most primitive and best-known [1], [2], studied for applications requiring high-power converters at medium voltages, such as reactive power compensators [3], renewable energy systems [4], [5], and motor drives [6], [7]. Notwithstanding the three-level DCC topology, well-known as the neutral point-clamped (NPC) topology, DCC topologies with more than three voltage levels have failed to find wide industrial applications. One of the reasons is that they lack the inherent potential to achieve capacitor voltage balancing under all operating conditions when using conventional modulation techniques, including sinusoidal pulsewidth modulation and space vector modulation (SVM) [8], [9], [10]. An analytical approach has been adopted in [8] to prove the voltage-drift phenomenon of dc-link capacitors in n-level DCC topologies ($n > 3$) under operating modes with high modulation indexes and high load power factors. Particularly, the balanced area is presented in unity power factor, with modulation indexes less than 0.55 [8].

Due to the increasing power demand of commercial and industrial applications and the desire to achieve high dc-link voltage and high power quality, power converters with more than three voltage levels have received considerable attention. As a result, overcoming the balancing hurdle of the DCC topologies has been an area of research interest over the past decades. The auxiliary circuit-based solutions are considered to be the primitive studies conducted in the literature. Various efforts have been made in [11], [12], [13], and [14] to deal with the balancing challenge of DCC topologies by using auxiliary voltage balancing circuits. However, adding extra circuitry increases the volume, weight, and cost in addition to the complexity of the system. Addressing this issue, a hybrid method consisting of a flying-capacitor-based chopper and zero-sequence voltage injection has been further proposed in [15], but it still increases the cost and adds additional control requirements.

The other category of proposed strategies in the literature deals with modulation techniques to enhance the balancing performance of the conventional methods. The concept of virtual vectors (VV) derives from the linear combination of real voltage vectors to nullify the average capacitor current during the modulation period [16], [17], [18]. A VV-PWM technique was proposed in [16] for a 4L-DCC topology and then generalized to higher phase voltage levels [17]. However, defining VVs increases either memory requirements or the number of computations, and it complicates the vector location identification. Also, the average switching frequency and power losses when applying VV-PWM are considerably higher than conventional modulation methods. Authors in [19] investigated a simplified VV-PWM to lower the calculations, reduce switching transitions, and facilitate subsector determination. On the negative side, an active balancing strategy has not been developed to mitigate the influence of nonidealities in practical operation. The other strategy is to employ mathematical expressions for calculating the proper duty ratios based on the sensed dc-link capacitor voltages [20], [21]. Although the voltages of the capacitors in DCC topologies with any number of levels are actively controlled, the high switching frequency in the closed-loop control mode and intensive mathematical calculations are the main drawbacks of such methods [21]. A

Manuscript received 1 January 2022; revised 10 April 2022, 8 June 2022, 29 July 2022, and 6 October 2022; accepted 25 November 2022. Date of publication 13 December 2022; date of current version 14 February 2023. This work was supported in part by the Natural Sciences and Engineering Research Council of Canada (NSERC) and in part by the Ontario Center of Innovation (OCI). Recommended for publication by Associate Editor L. Zhang. *(Corresponding author: Javad Ebrahimi.)*

The authors are with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3N6, Canada (e-mail: javad.ebrahimi@queensu.ca; 20ss322@queensu.ca; suzan.eren@queensu.ca; alireza.bakhshai@queensu.ca).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3228482.

Digital Object Identifier 10.1109/TPEL.2022.3228482

multireference/single-carrier approach developed in [22] gives the phase voltages the freedom to switch between any number of feasible voltage levels while there is a compromise between power losses and the balancing capability of the proposed strategy.

Another set of solutions is based on model predictive control (MPC) broadly used to accomplish different control objectives in multilevel converters. In this advanced control strategy, the capacitor voltage balancing task is included in a common cost function defined to achieve different control requirements of the converter [4], [23], [24]. Therefore, the capacitor voltages are regulated around their nominal values simply by selecting a proper weighting factor. However, the number of calculations increases significantly for DCC topologies with high-voltage levels. What is more, selecting a high weighting factor for the operating points that are located in the restricted region, as discussed in [10], deteriorates other control objectives. In addition to this, due to high waveform distortion, variable switching frequency, and spread harmonic spectrum, the use of MPC for the balancing purposes of DCC topologies has become more challenging [25].

A new capacitor voltage balancing technique based on carrier-overlapped PWM (COPWM) has been proposed recently to naturally balance the dc-link capacitors of the four-level active neutral point inverter in [26], the five-level NPC inverter in [27], and DCC topologies with any number of voltage levels in [28]. This method pursues the concept of VV-PWM to set the average capacitor currents to zero over a specific interval. Despite the VV-PWM method, capacitor voltage balancing is not accomplished during each sampling period but over the fundamental period. In the case of a 4L-DCC converter, applying the COPWM method leads to equal neutral point currents and volt-second balance in each sampling period, as well as zero average capacitor current during the fundamental period in a passive way [28]. To deal with the nonidealities of practical operation, a closed-loop method based on zero voltage injection was proposed in [27]. However, the power losses are still high in this method due to the high number of switching transitions.

In [29], authors proposed a simplified VV-PWM voltage balancing technique for DCC topologies with any number of voltage levels to reduce the complexity of the SVM implementation in the conventional VV-PWM method. Compared to the VV-PWM method proposed in [17], this technique results in a lower switching frequency but a higher voltage THD. Three capacitor voltage balancing schemes based on redundant voltage levels were proposed in [30] to add extra voltage levels over the modulation period and regulate the capacitor voltages. The three balancing schemes have some advantages over each other schemes in terms of harmonic spectrum, switching frequency, dynamic response, and control complexity. For example, the second scheme has a lower dynamic response and higher switching frequency while having a more concentrated harmonic spectrum compared to schemes 1 and 3. To conclude, a proper voltage balancing strategy for DCC topologies should actively balance dc-link capacitor voltages, satisfy volt-second balance, and lead to low power losses without deteriorating the output voltages and increasing the required computations [31].

In this article, a new modulation scheme based on the concept of virtual voltage levels is proposed to regulate the dc-link capacitor voltages of the 4L-DCC topology for the operating conditions, where the classic modulation scheme cannot provide capacitor voltage balancing. The concept of virtual voltage levels was first introduced in [32] to balance the flying capacitor voltages, and in this article, this concept is developed for dc-link capacitor voltage balancing in the 4L-DCC topology. The proposed virtual levels PWM (VL-PWM) scheme deals with the voltage balancing limits of dc-link capacitor voltages in the 4L-DCC topology. Despite the previously proposed modulation schemes based on VVs, the first stages of the modulation in the proposed method, including the determination of reference voltage vector location in the space vector diagram, the determination of three adjacent voltage vectors, and duty ratios assignment, are the same as the classic SVM. In fact, the implementation of the modulation based on the classic space vector plan is one of the benefits of the proposed method compared to the VV-SVM method. Moreover, the proposed method provides the selection of appropriate redundant voltage levels corresponding to the adjacent voltage vectors to decrease the switching frequency. In addition, the reconstruction procedure of the proposed method is performed on a per-phase basis and generates virtual voltage levels, resulting in zero average neutral point currents for each fundamental period. The resultant modulation scheme generates desired output voltages and, at the same time, regulates capacitor voltages. Due to the property of zero average neutral point currents over the fundamental period, the capacitor voltages are naturally regulated at all operating points. To compensate for any voltage drift due to nonidealities or practical conditions, an additional active capacitor voltage balancing is developed. In the proposed active method, the capacitor voltages and the signs of phase currents are measured. Then, based on those, the duty ratios of voltage levels are readjusted to reduce the difference between actual capacitor voltages and their reference values. The performance of the proposed modulation technique is investigated and verified through simulation and experimentation.

The rest of this article is organized as follows. In Section II, a brief description of the 4L-DCC topology and its balancing limits are presented. In Section III, the virtual voltage levels are defined, and the proposed modulation scheme is developed for the 4L-DCC converter. In addition, simulation results are presented to validate the natural balancing performance of the proposed open-loop scheme. In Section IV, the proposed closed-loop active capacitor voltage balancing is implemented based on the measured capacitor voltages. Simulation results at various operating points are provided in Section V. In Section VI, the performance of the 4L-DCC topology using the proposed modulation scheme is experimentally validated. Finally, Section VIII concludes this article.

II. 4L-DCC Topology Description

A. Operating Principles of the 4L-DCC Topology

The three-phase schematic of the 4L-DCC topology is shown in Fig. 1, in which six identical diodes and six switching devices are the main components of each leg. As can be seen in Table I, the combinations of the ON–OFF states of the switching devices in a common leg can lead to four distinct switching modes M_{x0}, M_{x1}, M_{x2}, and M_{x3} of phase x (x= *a, b, c*). If the voltage of the negative pole of the dc-link is considered as the reference potential, each switching mode outputs a unique phase voltage at the ac terminal, and therefore four individual phase levels $l_x = \{0, 1, 2, 3\}$ corresponding to voltage values $V_{Ox} = \{0,\ V_{\rm dc}/3,\ 2V_{\rm dc}/3,\ V_{\rm dc}\}$ can be yielded at the inverter output.

The dc-link consists of three capacitors with a nominal voltage value that is one-third of the dc-link voltage. Provided that

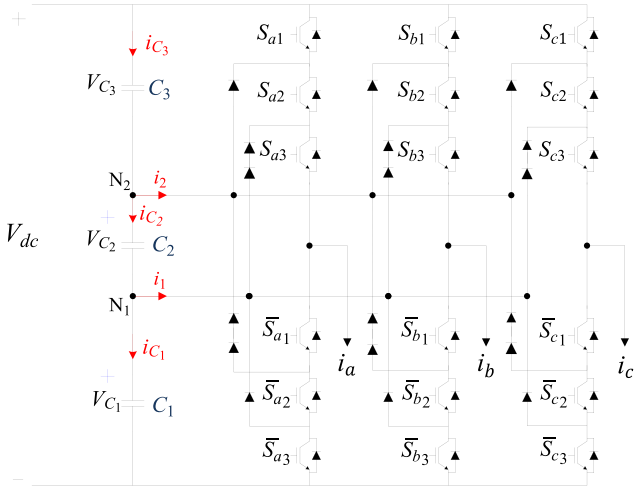

Fig. 1. Schematic of the three-phase 4L-DCC topology.

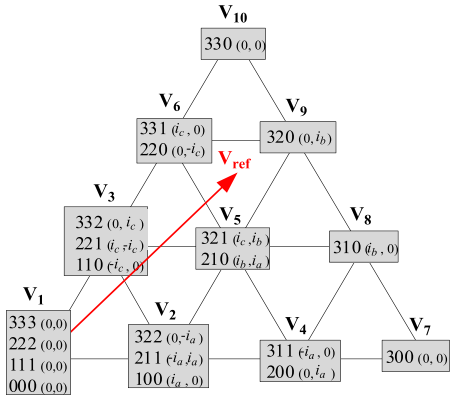

Fig. 2. Sector I of the space vector diagram for the 4L-DCC topology alongside the redundant states and the associated currents flowing out of neutral points (i_1, i_2).

TABLE I
SWITCHING MODES AND THEIR IMPACTS ON THE NEUTRAL POINTS CURRENTS

Switching modes	S_{x1}	S_{x2}	S_{x3}	$\overline{S_{x1}}$	$\overline{S_{x2}}$	$\overline{S_{x3}}$	V_{Ox}	l_x	i_1	i_2
M_{x0}	0	0	0	1	1	1	0	0	0	0
M_{x1}	0	0	1	1	1	0	$V_{dc}/3$	1	i_x	0
M_{x2}	0	1	1	1	0	0	$2V_{dc}/3$	2	0	i_x
M_{x3}	1	1	1	0	0	0	V_{dc}	3	0	0

$x = a, b, c$

the capacitor voltages are regulated around $V_{\rm dc}/3$, the voltage levels at the output will be determined by these capacitor voltages.Table I shows the effect of each switching mode on the neutral point currents i_1 and i_2, which have a direct impact on the charging/discharging status of the dc-link capacitors.

It is advantageous to express the dc-link capacitor currents in terms of the currents of the neutral points N_1 and N_2, i.e., i_1 and i_2, since these currents can be determined from the switching state used in the switching pattern and their duty ratios. According to Fig. 1, the capacitor currents are expressed as follows:

$$\begin{aligned} i_{C_3} &= i_{C_2} + i_2 \\ i_{C_2} &= i_{C_1} + i_1 \end{aligned} \tag{1}$$

where i_{C_1}, i_{C_2}, and i_{C_3} are the currents passing through dc-link capacitors C_1, C_2, and C_3, respectively. Considering a constant net dc-link voltage, following equation can be expressed:

$$\frac{dv_{C1}}{dt} + \frac{dv_{C2}}{dt} + \frac{dv_{C3}}{dt} = 0 \tag{2}$$

and

$$i_{Ck} = C_k \frac{dv_{Ck}}{dt},\ k\ =\ 1,\ 2,\ 3. \tag{3}$$

As a result of (2) and (3), the following equation is deduced:

$$i_{C1} + i_{C2} + i_{C3} = 0. \tag{4}$$

The above expression means that the common current flowing through all capacitors is not considered since it does not affect the capacitor voltages' drift. Using (1) and (4), the capacitor currents are expressed as follows:

$$\begin{bmatrix} i_{C_1} \\ i_{C_2} \\ i_{C_3} \end{bmatrix} = \begin{bmatrix} -2/3 & -1/3 \\ 1/3 & -1/3 \\ 1/3 & 2/3 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}. \tag{5}$$

With respect to Table I, if the switching modes M_{x0} and M_{x3} are selected in phase x, the phase current i_x flows out of none of the neutral points. In other words, the highest and lowest voltage levels do not change the average value of the neutral point currents and therefore capacitor currents. Whereas, the switching mode M_{x1} connects the phase x to N_1, meaning that i_x flows out of the neutral point N_1. Similarly, phase x will be connected to N_2 if M_{x2} is chosen. According to Table I, the switching mode M_{x1} occurs when the upper arm switches S_{x1} and S_{x2} are OFF and S_{x3} is ON, and the switching mode M_{x2} occurs when the upper arm switches S_{x2} and S_{x3} are ON and S_{x1} is OFF. If OFF-state and ON-state of switching devices are expressed by binary values 0 and 1, respectively, the switching modes M_{x1} and M_{x2} can be defined as

$$\begin{aligned} M_{x1} &: \left(\overline{S_{x1}}.\overline{S_{x2}}.S_{x3}\right) \\ M_{x2} &: \left(\overline{S_{x1}}.S_{x2}.S_{x3}\right). \end{aligned} \tag{6}$$

Accordingly, the neutral point currents can be defined as a function of phase currents and switching states as follows:

$$\begin{cases} i_1 = \sum_{x\ =\ a,b,c} \left(\overline{S_{x1}}.\overline{S_{x2}}.S_{x3}\right) i_x \\ i_2 = \sum_{x\ =\ a,b,c} \left(\overline{S_{x1}}.S_{x2}.S_{x3}\right) i_x \end{cases}. \tag{7}$$

B. Limits of Capacitor Voltage Balancing

In conventional voltage balancing strategies for the 4L-DCC converter, the redundant states should be utilized in order to maintain capacitor voltage balance. Fig. 2 shows sector I of the space vector diagram corresponding to the 4L-DCC converter, indicating that some voltage vectors can be synthesized by different combinations of switching modes. Also, the neutral point currents regarding each redundant state are expressed in brackets as (i_1, i_2). Redundant states can lead to dissimilar neutral point currents and consequently have distinct charging/discharging effects on the dc-link capacitors.

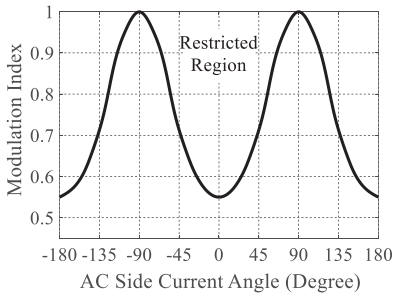

Fig. 3. Boundary of capacitor voltage balancing of the 4L-DCC converter.

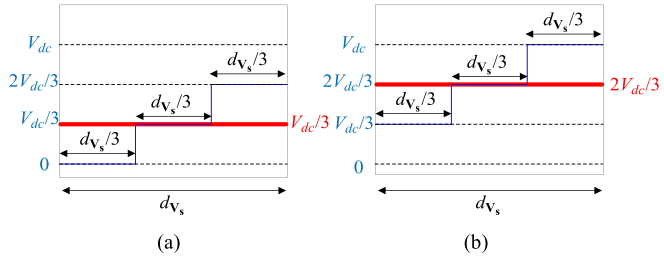

Fig. 4. Implementation of virtual levels for phase voltage levels: (a) $V_{\rm dc}/3$ and (b) $2V_{\rm dc}/3$.

In a DCC topology with more than three voltage levels, capacitor voltage balancing is restricted to operating points that depend on modulation index and power factor. Fig. 3 illustrates the voltage balancing restriction of the 4L-DCC topology as a function of the converter modulation index and the ac side current angle. The solid line in Fig. 3 indicates the boundary under which the classic SVM strategies can control and achieve balanced dc-capacitor voltages. The voltage balancing techniques are restricted to the theoretical limit derived from sinusoidal ac side currents. To attain these theoretical/practical limits, the mathematical analysis is presented in [33], [34], and [35]. Considering Fig. 3, the capacitor voltages of the 4L-DCC are not balanced and regulated around their rated values by classical modulation methods, either for high modulation indexes or high power factors. The operating conditions above the solid line correspond to the unbalanced area. This is due to the fact that redundant switching states are not adequate to maintain a balance between the charging and discharging of dc-link capacitors, and the capacitor voltages in this area deviate entirely from their nominal values. The following section will describe a new modulation method using both open-loop and closed-loop voltage balancing schemes to deal with the balancing issue within restricted region following the definition of virtual voltage levels.

III. Natural Voltage Balancing of the 4L-DCC Topology Using the Proposed VL-PWM Method

The concept of natural capacitor voltage balancing in the 4L-DCC topology is based on setting the average of the neutral point currents to zero for each fundamental period during SVM implementation. This is carried out by defining the virtual voltage levels of each phase by a linear combination of appropriate voltage levels. In this process, two main goals must be pursued as follows.

1) The average capacitor current should be zero such that the net capacitor voltage change also becomes zero.
2) The volt-second balance for synthesizing a low distortion output voltage must be satisfied.

In this section, the implementation of the proposed modulation scheme is explained.

A. Virtual Voltage Levels Definition

Assuming that $\rm V_{ref}$ is the reference voltage vector, the adjacent voltage vectors $\{\mathbf{V_u}, \mathbf{V_v}, \mathbf{V_w}\}$ and their duty ratios $\{d_u, d_v, d_w\}$ are determined by the classic SVM method as follows:

$$\mathbf{V_u}d_u+\mathbf{V_v}d_v+\mathbf{V_w}d_w = \mathbf{V_{ref}}$$

$$d_u + d_v + d_w = 1. \tag{8}$$

For further formulation, the phase voltage values are termed as ${V_{l_{xs}}}^{xs}$, which defines the voltage value of phase level l_{xs} (l_{xs}={0, 1, 2, 3}) of phase x of voltage vector$s$. It should be clarified that the variables ${V_0}^{xs}$, ${V_1}^{xs}$, ${V_2}^{xs}$, and ${V_3}^{xs}$ are equivalent to the values 0, $V_{\rm dc}/3$, $2V_{\rm dc}/3$, and $V_{\rm dc}$, respectively. After determining the adjacent voltage vectors and calculating their associated duty ratios, implementing the concept of VLs for the 4L-DCC will be expressed in the following.

The proper phase voltage level reconstruction is performed such that the following requirements are satisfied.

1) Volt-second balance in each phase is maintained. This is due to accomplish the volt-second balance for synthesizing output voltage that presented in (8).
2) The sum of duty ratios of voltage levels applied in each phase is equal to 1. This is due to accomplish the equality presented in (8).

Case I: If the switching mode M_{x1}, i.e., ${V_1}^{xs} = V_{\rm dc}/3$, is selected by any conventional modulation method for phase x (x= *a, b, c*) of voltage vector **s** (**s** = **u, v, w**), then instead of applying the chosen voltage level directly to the converter, this level is reconstructed by three nearest voltage levels ${V_0}^{xs}$, ${V_1}^{xs}$, and ${V_2}^{xs}$, and written as

$$\mathrm{V_1^{xs}}\mathrm{d_{V_s}} = \mathrm{V_0^{xs}}(\mathrm{d_{V_s}}/3) + \mathrm{V_1^{xs}}(\mathrm{d_{V_s}}/3) + \mathrm{V_2^{xs}}(\mathrm{d_{V_s}}/3)$$
$$\mathbf{s} = \mathbf{v}, \mathbf{u}, \mathbf{w}. \tag{9}$$

It should be noted that the duty ratios of three constructing levels are equal to $\mathrm{d_{V_s}}/3$ to accomplish volt-second balance. In other words, the average of ${V_0}^{xs}$, ${V_1}^{xs}$, and ${V_2}^{xs}$ with the equal duty ratios of $d_{V_s}/3$ is equal to ${V_1}^{xs}$ with the duty ratio of d_{V_s}. Fig. 4(a) shows this equivalency.

Case II: To generate voltage level $2V_{\rm dc}/3$, the adjacent voltage levels ${V_1}^{xs}$, ${V_2}^{xs}$, and ${V_3}^{xs}$ are utilized, in the same manner as the voltage level $V_{\rm dc}/3$. Therefore, instead of applying the ${V_2}^{xs} = 2V_{\rm dc}/3$ to the converter at duty ratio of d_{V_s}, this voltage level is reconstructed by three nearest voltage levels ${V_1}^{xs}$, ${V_2}^{xs}$, and ${V_3}^{xs}$, as follows:

$$\mathrm{V_2^{xs}}\mathrm{d_{V_s}} = \mathrm{V_1^{xs}}(\mathrm{d_{V_s}}/3) + \mathrm{V_2^{xs}}(\mathrm{d_{V_s}}/3) + \mathrm{V_3^{xs}}(\mathrm{d_{V_s}}/3)$$
$$\mathbf{s} = \mathbf{u}, \mathbf{v}, \mathbf{w}. \tag{10}$$

The average of ${V_1}^{xs}$, ${V_2}^{xs}$, and ${V_3}^{xs}$ with the equal duty ratios of $d_{V_s}/3$ is equal to ${V_2}^{xs}$ with the duty ratio of d_{V_s}. The equivalence of the left-side and right-side of (10) is depicted in Fig. 4(b).

Case III: The highest and lowest phase voltage levels do not have any virtual forms, given the fact that the main objective of defining virtual voltage levels is achieving capacitor voltage

balancing for the 4L-DCC converter, and the switching modes ${V_0}^{xs}$ and ${V_3}^{xs}$ do not contribute to capacitor voltage deviation.

The initial implementation of the proposed VL-SVM method is based on equal distributing the total duty cycle of each voltage level between the three nearest adjacent voltage levels. It will accomplish natural capacitor voltage balancing in the 4L-DCC topology for different modulation indexes and load power factors. However, an additional active capacitor voltage balancing method should be implemented in a practical system to compensate for any voltage drift due to unideal practical conditions. The implementation of the active capacitor voltage balancing in the second step of the proposed method (Section IV) results in an unequal distribution of the total duty cycle. However, the requirements mentioned above remain satisfied.

B. Redundant Switching States Selection

It can be seen from Fig. 2 that there is a redundancy associated with space vectors. For example, given the reference voltage is located in the triangle shown in Fig. 2, the space vector $\mathbf{V_5}$ has the redundant switching states [321] and [210], the space vector $\mathbf{V_6}$ has the redundant switching states [331] and [220], and the space vector $\mathbf{V_9}$ has the redundant switching state [320]. The selection of proper switching states is important in optimizing the switching frequency as explained in this section.

In the proposed VL-PWM method, the switching states associated with each space vector is selected with the target of minimizing the switching frequency. Considering sector I, as shown in Fig. 2, if the upper switching state in each gray box is chosen, the voltage level of phase a would remain at 3 throughout this sector. For instance, if $\mathbf{V_{ref}}$ is located in sector I and surrounded by three voltage vectors $\mathbf{V_5}$, $\mathbf{V_6}$, and $\mathbf{V_9}$, then the desired switching states will be [321], [331], and [320], respectively. It can be shown that if any other combination of switching states is applied in this sector, the phase levels would change in such a way that it would result in a higher switching frequency. Due to the symmetry, the same approach is adopted for other sectors of the space vector diagram.

C. Determination of Duty Ratios of Voltage Levels

After determining the switching states corresponding to the adjacent voltage vectors and their associated duty ratios, the voltage level reconstruction is separately applied to each phase to implement the VL-PWM scheme. For example, the primary state [322] corresponding to voltage vector $\mathbf{V_2}$ with duty ratio d_{V_2} turns into three reconstructing states [333], [322], and [311]. It is evident that by applying [322] to the converter, the reverse current of phase a $(-i_a)$ flows out of the second neutral point N_2 during the $d_{V_2}T_s$ interval, as T_s defines the sampling period. However, by turning [322] into three mentioned reconstructing states, $-i_a$ passes through both neutral branches, N_1 and N_2, over a $(d_{V_2}/3)T_s$ interval. Therefore, applying VLs to a 4L-DCC topology leads to similar currents flowing out of two neutral points N_1 and N_2.

The reconstructing states related to voltage vectors $\mathbf{V_1}$–$\mathbf{V_{10}}$ of sector I alongside their resultant neutral point currents are expressed in Table II. The same approach can be taken in other sectors of the space vector diagram using the proposed VLs concept.

In order to formulate Table II for three adjacent voltage vectors, the space vectors, their related switching states, and the resultant neutral point currents are nominated as

TABLE II
IMPLEMENTATION OF VIRTUAL LEVELS IN SECTOR I OF THE SPACE VECTOR DIAGRAM

Voltage vectors	Primary state $[l_a\ l_b\ l_c]$ neutral currents (i_1, i_2)	Reconstructed states $[l_a\ l_b\ l_c]$ neutral currents (i_1, i_2)			Resultant neutral currents (i_1, i_2)
$\mathbf{V_1}$	[333] (0, 0)	[333] (0, 0)	[333] (0, 0)	[333] (0, 0)	(0, 0)
$\mathbf{V_2}$	[322] $(0, -i_a)$	[333] (0, 0)	[322] $(0, -i_a)$	[311] $(-i_a, 0)$	$(-i_a, -i_a)$
$\mathbf{V_3}$	[332] $(0, i_c)$	[333] (0, 0)	[332] $(0, i_c)$	[331] $(i_c, 0)$	(i_c, i_c)
$\mathbf{V_4}$	[311] $(-i_a, 0)$	[322] $(0, -i_a)$	[311] $(-i_a, 0)$	[300] (0, 0)	$(-i_a, -i_a)$
$\mathbf{V_5}$	[321] (i_c, i_b)	[332] $(0, i_c)$	[321] (i_c, i_b)	[310] $(i_b, 0)$	$(-i_a, -i_a)$
$\mathbf{V_6}$	[331] $(i_c, 0)$	[332] $(0, i_c)$	[331] $(i_c, 0)$	[330] (0, 0)	(i_c, i_c)
$\mathbf{V_7}$	[300] (0, 0)	[300] (0, 0)	[300] (0, 0)	[300] (0, 0)	(0, 0)
$\mathbf{V_8}$	[310] $(i_b, 0)$	[320] $(0, i_b)$	[310] $(i_b, 0)$	[300] (0, 0)	(i_b, i_b)
$\mathbf{V_9}$	[320] $(0, i_b)$	[330] (0, 0)	[320] $(0, i_b)$	[310] $(i_b, 0)$	(i_b, i_b)
$\mathbf{V_{10}}$	[330] (0, 0)	[330] (0, 0)	[330] (0, 0)	[330] (0, 0)	(0, 0)

$$\begin{aligned}
\mathbf{V_u}&: [l_{au}\, l_{bu}\, l_{cu}],\ (i_{1u}, i_{2u})\\
\mathbf{V_v}&: [l_{av}\, l_{bv}\, l_{cv}],\ (i_{1v}, i_{2v})\\
\mathbf{V_w}&: [l_{aw}\, l_{bw}\, l_{cw}],\ (i_{1w}, i_{1w})
\end{aligned} \tag{11}$$

where l_{xs} ($l_{xs} = \{0, 1, 2, 3\}$) is the level of phase x ($x = a, b, c$) of voltage vector $\mathbf{s}$ ($\mathbf{s} = \mathbf{u, v, w}$). Also, i_{1s} and i_{2s} are the resultant neutral point currents associated with voltage vectors.

The total duty ratios of each voltage level in each phase are calculated by adding the duty ratios of the corresponding level of three selected voltage vectors as follows:

$$\begin{aligned}
d_{x0} &= \sum_{s=u,\ v,\ w} (l_{xs} == 0)\, d_{V_s} + (l_{xs} == 1)\, d_{V_s}/3\\
d_{x1} &= \sum_{s=u,\ v,\ w} (l_{xs} == 1)\, d_{V_s}/3 + (l_{xs} == 2)\, d_{V_s}/3\\
d_{x2} &= \sum_{s=u,\ v,\ w} (l_{xs} == 1)\, d_{V_s}/3 + (l_{xs} == 2)\, d_{V_s}/3\\
d_{x3} &= \sum_{s=u,\ v,\ w} (l_{xs} == 2)\, d_{V_s}/3 + (l_{xs} == 3)\, d_{V_s}
\end{aligned} \tag{12}$$

where d_{x0}, d_{x1}, d_{x2}, and d_{x3} are the total duty ratios of voltage levels 0, $V_{\rm dc}/3$, $2V_{\rm dc}/3$, and $V_{\rm dc}$ of phase x, respectively.

Once the duty ratios associated with each phase level have been determined, it is necessary to arrange the duty ratios within one sampling period. The voltage levels are typically applied in the following sequence for different phases in one sampling period: 3–2–1–0–1–2–3.

To clarify the proposed procedure, a numerical example is provided. It is assumed that the reference voltage $\mathbf{V_{ref}}$ is surrounded by three adjacent voltage vectors $\mathbf{V_u} = \mathbf{V_5}$, $\mathbf{V_v} = \mathbf{V_6}$, and $\mathbf{V_w}$

$= \mathbf{V_9}$, as shown in Fig. 2. The duty ratios of the corresponding voltage vectors are calculated using (8) and are considered equal to 0.5, 0.2, and 0.3, respectively. As explained in Section III-B, the redundant switching states $[l_{au}l_{bu}l_{cu}] = [321]$, $[l_{av}l_{bv}l_{cv}] = [331]$, and $[l_{aw}l_{bw}l_{cw}] = [320]$ are selected to keep switching frequency at minimum. To achieve capacitor voltage balancing, the reconstruction procedure is implemented on the mentioned voltage levels, as expressed in (12).

1) For phase *a* of the considered adjacent voltage vectors $\mathbf{V_5}$, $\mathbf{V_6}$, and $\mathbf{V_9}$, the voltage level of phase *a* is the same for three vectors and is equal to 3. It meets one of the conditions of d_{a3} in (12), i.e., $(l_{a5} == 3) = (l_{a6} == 3) = (l_{a9} == 3) = 1$. Hence, $d_{a3} = d_{V_5} + d_{V_6} + d_{V_9} = 0.5 + 0.2 + 0.3 = 1$, and the duty ratio of other voltage levels of phase *a* are 0. In other words, the voltage level 3 is not changed throughout the reconstruction stage.
2) The voltage levels of phase *b* are 2, 3, and 2 for the corresponding voltage vectors $\mathbf{V_5}$, $\mathbf{V_6}$, and$\mathbf{V_9}$, respectively. According to (10), the voltage level 2 of phase *b* of vector $\mathbf{V_5}$ is reconstructed by three nearest voltage levels V_1^{b5}, ${V_2}^{b5}$, and V_3^{b5}. It also meets the condition $(l_{b5} == 2)$ in (12). In addition, the voltage level 2 of phase *b* of vector $\mathbf{V_9}$ is reconstructed by three nearest voltage levels V_1^{b9}, V_2^{b9}, and ${V_3}^{b9}$. Therefore, the duty ratio of voltage vectors $\mathbf{V_5}$ and $\mathbf{V_9}$ is distributed equally among the voltage levels 1, 2, and 3 for phase *b*. Regarding the voltage vector $\mathbf{V_6}$, its voltage levels remain unchanged as it is equal to 3. Using (12), the sum of duty ratios corresponding to the three mentioned voltage vectors are obtained after reconstruction as

$$d_{b0} = 0,$$
$$d_{b1} = d_{b2} = d_{V_5}/3 + d_{V_9}/3 \ = 0.5/3 + 0.3/3 = 0.8/3,$$
$$d_{b3} = d_{V_5}/3 + d_{V_6} + d_{V_9}/3 = 0.5/3 + 0.2 + 0.3/3 = 1.4/3.$$

3) For phase *c* of the mentioned adjacent voltage vectors, l_{c5}, l_{c6}, and l_{c9} are equal to 1, 1, and 0, respectively. According to (9), the voltage level 1 of phase *c* of vector $\mathbf{V_5}$ is reconstructed by three nearest voltage levels ${V_0}^{c5}$, ${V_1}^{c5}$, and ${V_2}^{c5}$ with equal duty ratios of $d_{V_5}/3$. Moreover, the voltage level 1 of phase *c* of vector $\mathbf{V_6}$ is reconstructed by three nearest voltage levels ${V_0}^{c6}$, ${V_1}^{c6}$, and ${V_2}^{c6}$ with equal duty ratios of $d_{V_6}/3$. The voltage level 0 of the voltage vector $\mathbf{V_9}$ remains unchanged. Using (12), the duty ratios of voltage levels of phase *c* after reconstruction procedure are calculated as follows:

$$\begin{aligned} d_{c0} &= d_{V_5}/3 + d_{V_6}/3 + d_{V_9} \\ &= 0.5/3 + 0.2/3 + 0.3 \ = \ 1.6/3, \\ d_{c1} &= d_{c2} = d_{V_5}/3 + d_{V_9}/3 \\ &= 0.5/3 + 0.2/3 = 0.7/3, \\ d_{c3} &= 0. \end{aligned}$$

D. Demonstration of the Natural Capacitor Voltage Balancing

The total neutral point currents by considering three adjacent voltage vectors are calculated as follows:

$$\begin{aligned} i_{1t} &= i_{1u} + i_{1v} + i_{1w} \\ i_{2t} &= i_{2u} + i_{2v} + i_{2w} \end{aligned} \tag{13}$$

where i_{1t} and i_{2t} are the total currents of neutral points N_1 and N_2 over one sampling period, respectively. Obviously, if the resultant neutral point currents regarding each voltage vector are equal after implementing VLs, then $i_{1t} = i_{2t}$.

Gaining equal neutral points currents by using VLs is a key feature to achieve natural capacitor voltage balancing for the 4L-DCC converter, irrespective of its operating condition. By substituting $i_1 = i_2 = i_{1t} = i_{2t}$ into (5), the capacitor currents are obtained as follows:

$$\begin{cases} i_{C_1} = -i_{1t} = -i_{2t} \\ i_{C_2} = 0 \\ i_{C_3} = i_{1t} = i_{2t}. \end{cases} \tag{14}$$

This means that the charging/discharging status of capacitor C_1 is the opposite of the status of capacitor C_3, and the average current passing through the middle dc-link capacitor is always zero under ideal conditions. Therefore, natural voltage balancing can be easily achieved for the capacitor C_2 without any additional requirements. It is worth noting that the average current of capacitors C_1 and C_3 is not zero during the sampling period. However, they can be set to zero over the fundamental frequency by selecting proper redundant switching states associated with the adjacent voltage vectors. In other words, the effect on neutral point currents caused by the selected switching states in each sector of the space vector diagram can be compensated if proper switching states are selected in the adjacent sector. Due to symmetry, the concept is explained for the adjacent sectors I and II and can be generalized to other voltage vectors of the 4L-DCC converter.

It is assumed that the reference voltage vector is located in sector I and is surrounded by the voltage vectors $\mathbf{V_5}$, $\mathbf{V_6}$, and $\mathbf{V_9}$, as shown in Fig. 2. According to the switching state selection explained in Section II, [321], [331], and [320] are the chosen switching states corresponded to the adjacent voltage vectors in the same order. After applying the VLs concept to the mentioned switching states, as can be seen in Table II, the currents flowing out of the neutral points N_1 and N_2 are ($-{i_a}^I$, $-{i_a}^I$), (${i_c}^I$,${i_c}^I$), and (${i_b}^I$,${i_b}^I$), respectively. The superscript *I* is used to refer to sector I. For example, if the duty ratio of $\mathbf{V_5}$ is $\mathrm{d_{V5}}$, the reverse current of phase *a* ($-i_a$) flows out of two neutral points of the 4L-DCC topology during this interval. To examine the compensating capability of the adjacent sector II, the reference voltage vector should move circularly in such a way that its location in sector II has a 60° phase shift with its primary location in sector I. As a result, the switching states [120], [020], and [130] synthesize the shifted voltage vector in sector II. By repeating the same reconstructing procedure for the voltage vectors of sector II, it is concluded that the resultant neutral point currents associated with the selected switching states are ($-{i_c}^{II}$, $-{i_c}^{II}$), (${i_b}^{II}$,${i_b}^{II}$), and (${i_a}^{II}$, ${i_a}^{II}$). The superscript II refers to sector II. To achieve natural capacitor voltage balancing during the fundamental period, it should be proved that the neutral point currents produced by the switching states in sector II are the reverse of those produced by the corresponded switching states in sector I. Assuming that ω is angular velocity, *t* denotes time, and φ is load angle, α is defined as

$$\alpha \ = \ \omega t - \varphi \tag{15}$$

and is used to define the instantaneous values of the phase currents. The symmetric three-phase currents ${i_a}^I$, ${i_b}^I$, and ${i_c}^I$ in sector I are expressed as follows:

$${i_a}^I = I_m \sin(\alpha)$$

$$i_b^I = I_m \sin(\alpha - 2\pi/3)$$
$$i_c^I = I_m \sin(\alpha + 2\pi/3) \quad (16)$$

where I_m is the peak amplitude of the phase currents. To obtain three-phase currents i_a^{II}, i_b^{II}, and i_c^{II}, a 60° phase shift is needed to apply to the phase currents in (16) for mapping them to sector II as follows:

$$\begin{aligned} i_a^{II} &= I_m \sin(\alpha + \pi/3) = I_m \sin(\alpha + \pi - 2\pi/3) = -i_b^I \\ i_b^{II} &= I_m \sin(\alpha - 2\pi/3 + \pi/3) \\ &= I_m \sin(\alpha - \pi + 2\pi/3) = -i_c^I \\ i_c^{II} &= I_m \sin(\alpha + 2\pi/3 + \pi/3) = I_m \sin(\alpha + \pi) = -i_a^I. \end{aligned} \quad (17)$$

As it is concluded from (17), the phase currents in the adjacent sector II are the reverse of those in sector I, and this is the key to accomplishing capacitor voltage balancing in each 120° interval of the main period. To clarify, the capacitor currents for the switching state [321] in sector I and its corresponding switching state [120] in sector II are calculated by using (17) as follows:

$$\begin{cases} i_{C_1}^I = i_a^I \\ i_{C_2}^I = 0 \\ i_{C_3}^I = -i_a^I \end{cases} \quad (18)$$

$$\begin{cases} i_{C_1}^{II} = i_c^{II} = -i_a^I = -i_{C_1}^I \\ i_{C_2}^{II} = 0 \\ i_{C_3}^{II} = -i_c^{II} = i_a^I = -i_{C_3}^I \end{cases} \quad (19)$$

where $i_{C_1}^I$, $i_{C_2}^I$, and $i_{C_3}^I$ are the capacitor currents produced by the switching states in sector I ([321] in (18)), and $i_{C_1}^{II}$, $i_{C_2}^{II}$, and $i_{C_3}^{II}$ refer to the capacitor currents when applying the switching states in sector II ([120] in (19)). It is proven by (18) and (19), as an example, that the adjacent sectors have the reverse effect on the charging/discharging status of the dc-link capacitors, and therefore, the dc-link capacitor voltages are regulated around their nominal value during the fundamental period. In the following section, simulation results are conducted to show the natural balancing capability of the proposed VL-PWM method.

E. Simulation Results

The 4L-DCC topology connected to an *RL* load has been simulated in PSIM software to validate the control performance of the proposed VL-PWM method. The system parameters are included in Table III, and the selected operating condition is located in the restricted region. Fig. 5 shows the three-phase currents over two fundamental periods. As expected according to Table III, the rms value of the currents is 110 A, and the current THD is calculated to be 0.72%.

Fig. 6 shows the phase voltage when implementing the VL-PWM method on the 4L-DCC inverter. As can be seen, the phase voltage is fixed to levels 3 and 0, respectively, within each of the positive and negative half-cycles at intervals of one-six of the fundamental period. As explained in part B of this section, this results from the adoption of the redundant switching state selection approach. The line voltage waveform and its harmonic spectrum are shown in Figs. 7 and 8, respectively. The voltage THD is calculated as 33.67% in the simulated operating conditions.

The proposed VL-PWM method has an advantage in terms of natural capacitor voltage balancing as shown in Fig. 9. It can be seen that the dc-link capacitors C_1 and C_3 charge during one-sixth of the fundamental period and discharge over the next 60° interval, and this is repeated three times in each fundamental period.

TABLE III
SIMULATED SYSTEM PARAMETERS

System parameters	Value
Input dc voltage	3 kV
DC-link capacitors	1 mF
Modulation index	0.95
Load power factor	0.9
Load current (rms)	110 A
Output frequency	50 Hz
Sampling frequency	5 kHz

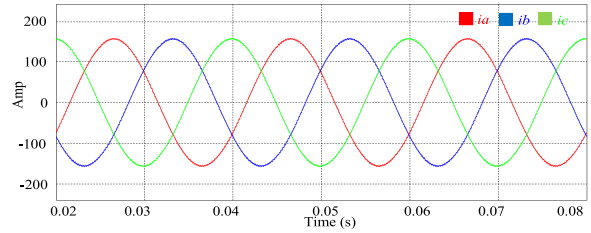

Fig. 5. Simulation results of three-phase currents of the proposed VL-PWM method.

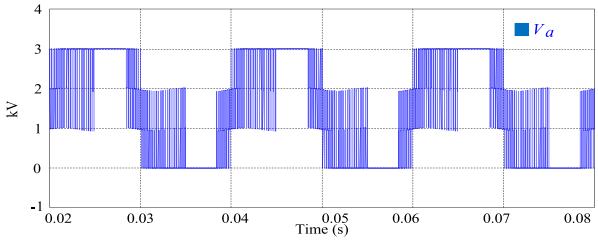

Fig. 6. Simulation results of phase voltage of the proposed VL-PWM method.

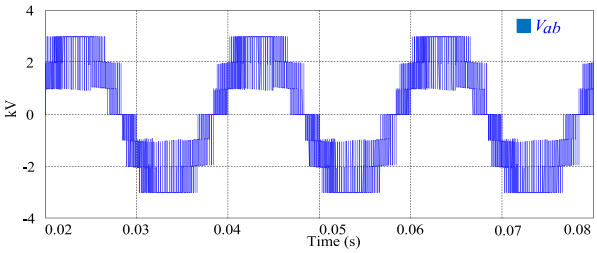

Fig. 7. Simulation results of line voltage of the proposed VL-PWM method.

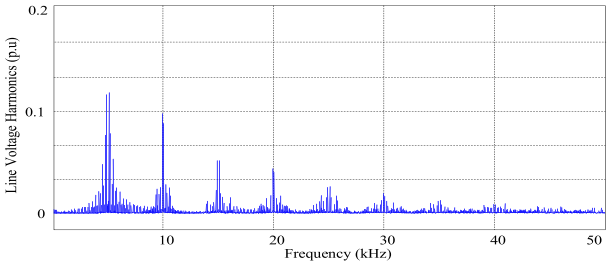

Fig. 8. Simulation results of line voltage harmonics of the proposed VL-PWM method.

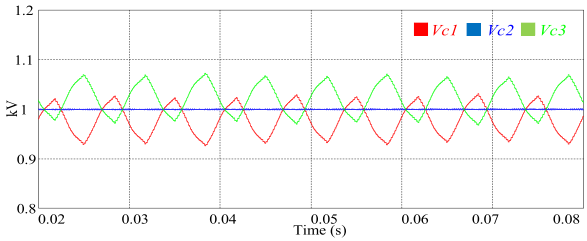

Fig. 9. Simulation results of dc-link capacitor voltages of the proposed VL-PWM method.

IV. Proposed Active Voltage Balancing VL-PWM Method

The proposed open-loop VL-PWM scheme ideally results in capacitor voltage balancing. However, under practical operating conditions, the natural capacitor voltage balancing properties of the open-loop VL-PWM method can gradually become degraded. Therefore, an additional active capacitor voltage balancing method needs to be implemented in a practical system to compensate for any voltage drift due to unideal practical conditions.

As only the phase voltage levels $V_{\rm dc}/3$ and $2V_{\rm dc}/3$ can alleviate the undesired balancing situations, their duty ratios should be adjusted based on the measured capacitor voltages. First, similar to the natural voltage balancing VL-PWM method, the identical duty ratios of these voltage levels are calculated using (12). Next, the duty ratios are readjusted in favor of reducing the difference between actual capacitor voltages and their reference value. Finally, the duty ratios of voltage levels 0 and $V_{\rm dc}$ must change to accomplish volt-second balance of the modulation scheme. It is not necessary to get all three dc-link capacitor voltage feedbacks assuming the total $V_{\rm dc}$ is known. In the proposed scheme, the capacitors C_1 and C_2 are considered for voltage balancing. Considering $i_{1t} = i_{2t}$ after implementing the open-loop VL-PWM scheme, the readjustment process of active voltage balancing of capacitors C_1 and C_2 is conducted in order to compensate the following statuses:

Status I: $V_{C_1} > V_{C_{\rm ref}}$

If the sign of i_x is positive, and the voltage level of phase x (l_x) is either 1 or 2, then the current passing through capacitor C_1 is negative according to (5). This means that the capacitor C_1 discharges, and its voltage is modified per se. However, if the duty ratio of both levels increases and/or phase level 1 is applied to the converter for a longer duration than voltage level 2, the balancing behavior of the control scheme will be augmented.

TABLE IV
Active Voltage Balancing Requirements of Capacitor C_1

Condition	Required Change of d_{x1}	Required Change of d_{x2}	Necessities
Δ_1=1	$+\varepsilon_1$	$+\varepsilon_2$	$\varepsilon_1>0$ & $\varepsilon_1 \geq \varepsilon_2$
Δ_1=−1	$-\varepsilon_1$	$-\varepsilon_2$	$\varepsilon_1>0$ & $\varepsilon_1 \geq \varepsilon_2$

In other words, since i_1 appears with a bigger coefficient in the equation of the C_1 current, [see (5)], making d_{x1} bigger than d_{x2} leads to the negative amplitude of the capacitor current increasing. Therefore, C_1 discharges with a sharper slope.

On the other hand, if i_x is negative, it can be concluded that the duty ratios should become lower and/or d_{x2} should be bigger than d_{x1} to decrease the positive amplitude of i_{C_1} and increase the effectiveness of the balancing strategy.

Status II: $V_{C_1} < V_{C_{\rm ref}}$

Under this situation, the positive phase current increases the difference between the actual capacitor voltage and the reference value, making it even worse due to the negative current passing through capacitor C_1. In order to lower the amplitude of capacitor current, instead of applying voltage levels 1 and 2 during identical time intervals, they should make up lower intervals and/or voltage level 1 should constitute a lower portion of the sampling period compared to voltage level 2. Nevertheless, if the sign of the phase current is negative, the favorable approach from the standpoint of capacitor voltage balancing is raising the duty ratios of the middle voltage levels and/or selecting a higher duty ratio for voltage level 2 than voltage level 1.

By defining the logic variable *SI*, $V_{\rm diff1}$, and Δ_1 as

$$V_{\rm diff1} = \begin{cases} 1, & (V_{C_1} - V_{C_{\rm ref}}) > 0 \\ -1, & (V_{C_1} - V_{C_{\rm ref}}) < 0 \end{cases} \tag{20}$$

$$\text{SI} = \begin{cases} 1, & \text{sign}\,(i_x) > 0 \\ -1, & \text{sign}\,(i_x) < 0 \end{cases} \tag{21}$$

$$\Delta_1 = SI \times V_{\rm diff1} \tag{22}$$

the required compensation of statuses I and II, needed to fulfill capacitor C_1 voltage balancing, are summarized in Table IV. Note that ε_1 and Δ_2 are the required changes that should be made to $d_{x1}$and d_{x2}.

Regarding capacitor C_2, the required compensation for statues III and IV are expressed in the following:

Status III: $V_{C_2} > V_{C_{\rm ref}}$

Like the aforementioned statuses, the duty ratios of phase levels 1 and 2 of phase *x* should be readjusted, given the relationship between the C_2 current and neutral point currents [see (5)], the polarity of phase *x* current, and the voltage value of capacitor C_2 at the beginning of the sampling period. If the voltage deviation is positive, the capacitor current should be negative to help maintain voltage balance, meaning that, according to (5), the duty ratio of voltage level $V_{\rm dc}/3$ should be lower than that of voltage level $2V_{\rm dc}/3$. Therefore, the negative term of the equation of C_2 current dominates the positive one. Contrarily, for a negative phase current, applying voltage level $2V_{\rm dc}/3$ for a shorter duration than voltage level $V_{\rm dc}/3$ can contribute to voltage balancing.

TABLE V
ACTIVE VOLTAGE BALANCING REQUIREMENTS OF CAPACITOR C_2

Condition	Required Change of d_{x1}	Required Change of d_{x2}	Necessities
$\Delta_2=1$	$-\varepsilon_1'$	$+\varepsilon_2'$	$\varepsilon_1'>0$ & $\varepsilon_2'>0$
$\Delta_2=-1$	$+\varepsilon_1'$	$-\varepsilon_2'$	$\varepsilon_1'>0$ & $\varepsilon_2'>0$

Status IV: $V_{C_2} < V_{C_{\text{ref}}}$

If the C_2voltage is lower than the nominal value, the current passing through the capacitor should be positive to reduce the difference between the actual voltage and the rated value. Assuming positive phase current, the proper compromise between the duty ratios of the middle voltage levels is to select a longer duration for phase level 1 than 2. In contrast, the equation of i_{C_2} in (5) indicates that for a negative sign of phase current, the duty ratio of phase level 2 should have more prominence over the existing sampling period.

After defining the logic variables V_{diff2} and Δ_2 as follows, the required compensation of statuses III and IV are expressed in Table V:

$$V_{\text{diff2}} = \begin{cases} 1, & (V_{C_2} - V_{C_{\text{ref}}}) > 0 \\ -1, & (V_{C_2} - V_{C_{\text{ref}}}) < 0 \end{cases} \tag{23}$$

$$\Delta_2 = \text{SI} \times V_{\text{diff2}}. \tag{24}$$

In order to satisfy statuses I and II, i.e., accomplishing active voltage balancing for capacitor C_1, the modified duty ratios d'_{x0}, d'_{x1}, d'_{x2}, and d'_{x3} are written below with regards to Table IV

$$\begin{aligned} d'_{x0} &= d_{x0} - \Delta d/2 \\ d'_{x1} &= d_{x1} + \Delta d \\ d'_{x2} &= d_{x2} - \Delta d/2 \\ d'_{x3} &= d_{x3} \end{aligned} \tag{25}$$

where Δd is calculated as

$$\Delta d = \Delta_1 \times d_{x,\,\min} \tag{26}$$

where $d_{x,\,\min}$ is the minimum value among d_{x0} , d_{x1}, d_{x2}, and d_{x3}.

The next step is to adjust the duty ratios given in (25) to guarantee capacitor C_2 voltage balancing by performing requirement III and IV, as follows:

$$\begin{aligned} d''_{x0} &= d'_{x0} \\ d''_{x1} &= d'_{x1} - k \times \Delta d'/2 \\ d''_{x2} &= d'_{x2} + k \times \Delta d' \\ d''_{x3} &= d'_{x3} - k \times \Delta d'/2 \end{aligned} \tag{27}$$

where $\Delta d'$ is calculated as

$$\Delta d' = \Delta_2 \times d_{x,\,\min} \tag{28}$$

and k is the balancing coefficient with a value between 0.5 and 1. The parameter k is required to perform the active voltage balancing of all dc-link capacitors at the same time. By assuming k is not included in (27), the duty ratios for phase levels 1 and 2 will be equal in the case of equal values of $\Delta_1$and Δ_2. This is the same as the natural capacitor voltage balancing properties of the open-loop VL-PWM method. As a result, the capacitor voltage variations are not actively compensated. Therefore, coefficient k should be considered less than 1. On the other hand, the proposed active balancing scheme is less capable of regulating the capacitor C_2 voltage at lower values of k. Accordingly, the lower limit of coefficient k is set to 0.5.

TABLE VI
REQUIRED CHANGES TO THE DUTY RATIOS AFTER READJUSTMENT PROCESS

Condition	Required changes of voltage level duty ratios			
	d_{x0}	d_{x1}	d_{x2}	d_{x3}
$\Delta_1=1$ $\Delta_2=1$	$-\frac{1}{2}\times d_{x,\,min}$	$+\left(1-\frac{k}{2}\right)\times d_{x,\,min}$	$-\left(\frac{1}{2}-k\right)\times d_{x,\,min}$	$-\frac{k}{2}\times d_{x,\,min}$
$\Delta_1=1$ $\Delta_2=-1$	$-\frac{1}{2}\times d_{x,\,min}$	$+\left(1+\frac{k}{2}\right)\times d_{x,\,min}$	$-\left(1+\frac{k}{2}\right)\times d_{x,\,min}$	$+\frac{1}{2}\times d_{x,\,min}$
$\Delta_1=-1$ $\Delta_2=1$	$+\frac{1}{2}\times d_{x,\,min}$	$-\left(1+\frac{k}{2}\right)\times d_{x,\,min}$	$+\left(1+\frac{k}{2}\right)\times d_{x,\,min}$	$-\frac{1}{2}\times d_{x,\,min}$
$\Delta_1=-1$ $\Delta_2=-1$	$+\frac{1}{2}\times d_{x,\,min}$	$-\left(1-\frac{k}{2}\right)\times d_{x,\,min}$	$+\left(\frac{1}{2}-k\right)\times d_{x,\,min}$	$+\frac{k}{2}\times d_{x,\,min}$

After a readjustment of the duty ratios, the main requirement is to maintain the volt-second balance of the modulation scheme over the entire sampling period. Considering phase x ($x = a, b, c$), this condition has been satisfied in (25) and (27) and can be written as follows:

$$\begin{aligned} &0\times d'_{x0}+V_{\text{dc}}/3\times d'_{x1}+2V_{\text{dc}}/3\times d'_{x2}+V_{\text{dc}}\times d'_{x3}=V_{\text{ref}-x} \\ &\quad d'_{x0}+d'_{x1}+d'_{x2}+d'_{x3}=1 \end{aligned} \tag{29}$$

$$\begin{aligned} &0\times d''_{x0}+V_{\text{dc}}/3\times d''_{x1}+2V_{\text{dc}}/3\times d''_{x2}+V_{\text{dc}}\times d''_{x3}=V_{\text{ref}_{-x}} \\ &\quad d''_{x0}+d''_{x1}+d''_{x2}+d''_{x3}=1. \end{aligned} \tag{30}$$

According to (25) and (27), Table VI shows the final modifications to the duty ratios so that the dc-link capacitor voltages are actively controlled, and the volt-second balance requirement is confirmed.

Fig. 10 shows the whole procedure of the proposed modulation and control algorithm. In this modulation technique, the duty ratios of the corresponded phase voltage levels (d_{x0}, d_{x1}, d_{x2}, d_{x3}) are rearranged such that the generation of the proper voltage levels at the converter's terminals and natural voltage balancing of the dc-link capacitors are guaranteed at the same time. To compensate for unbalances of the dc-link capacitor voltages, the active balancing scheme is applied. Accordingly, the capacitor voltages and the phase currents are measured, and the duty ratios are readjusted to provide active capacitor voltage balancing and simultaneously meet the volt-second balance requirement.

V. SIMULATION RESULTS

To validate the control capabilities of the proposed active voltage balancing VL-PWM method, it has been implemented on the 4L-DCC inverter within the PSIM software using the system parameters in Table III. In the following subsections, two kinds of changes are applied to the operating conditions to show the control performance of the proposed method.

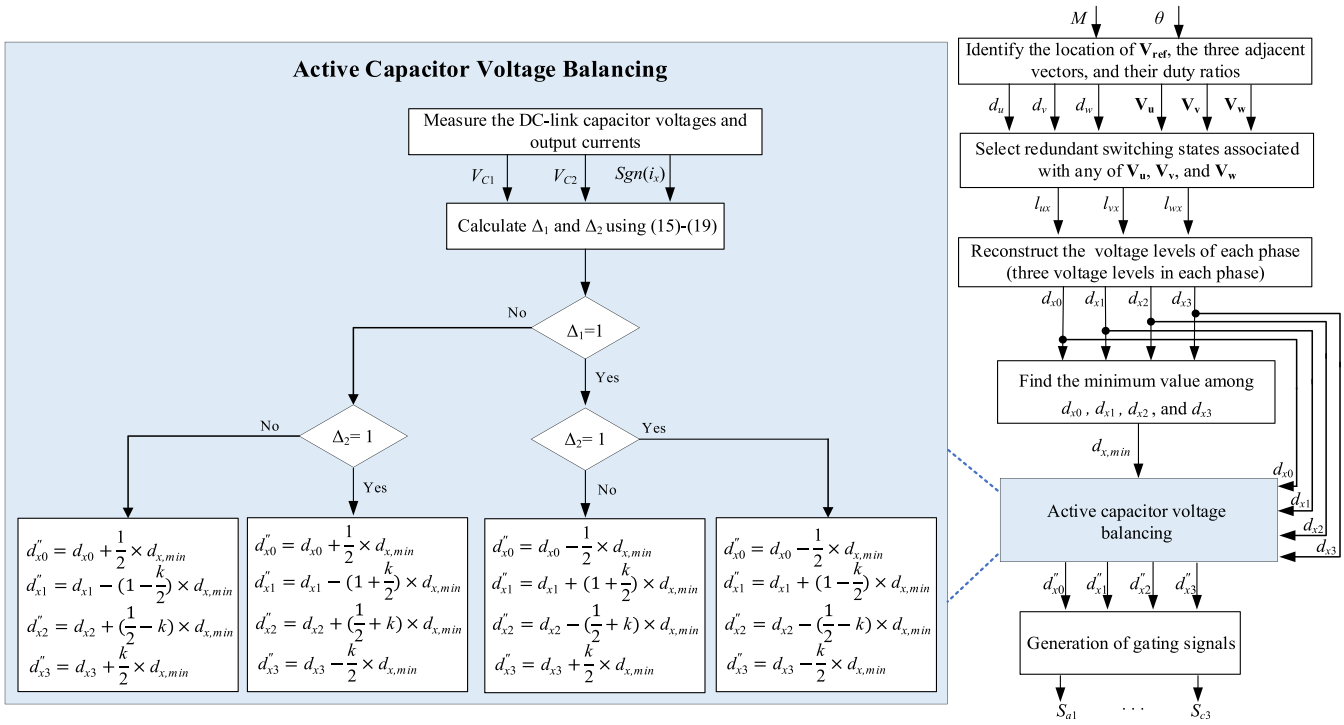

Fig. 10. Flowchart of the proposed modulation and capacitor voltage balancing method for the 4L-DCC topology.

A. Modulation Index Change

Since the worst case of the imbalanced region of the DCC topologies occurs during unity power factor for modulation indexes higher than 0.55, the minimum value of the modulation index is selected to be 0.6 throughout the evaluation of the proposed method. In other words, when the operating conditions are located in the balanced area, the conventional modulation techniques along with classic balancing schemes are adopted. Otherwise, the proposed VL-PWM method is applied to the converter over the restricted region.

First, the load power factor is set to 0.9, and the system performance is evaluated for two consecutive step changes in modulation index. The first step change is from $m = 0.95$ to $m = 0.75$, and the second one is from $m = 0.75$ to $m = 0.6$.

Considering the applied changes, Fig. 11 shows the simulation results of the three-phase currents, line voltage, and dc-link capacitor voltages. The rms value of the phase currents is 110 A during the primary operating condition, then it decreases to 85.7 and 68.6 A for $m = 0.75$ and $m = 0.6$, respectively. The current THD for the three aforementioned operating conditions is calculated to be 0.67%, 1%, and 1.28%, respectively. Fig. 11 also shows the dc-link capacitor voltage being regulated around one-third of the dc-link voltage. It is apparent from the comparison of the dc-link capacitor voltages when applying natural voltage balancing and active voltage balancing VL-PWM methods, i.e., Figs. 9 and 11, that the charging and discharging patterns are the same. However, the voltage drift existing in Fig. 9 has been mitigated in Fig. 11. Also, the capacitor voltage ripple is reduced from 9.8% to 8.4%.

The harmonics spectrum of the line voltage is shown in Fig. 12 with the voltage THD equaling 36.71%, 45.83, and 60.85% for $m = 0.95$, $m = 0.75$, and $m = 0.6$, respectively. Fig. 13 shows the simulation results of the phase voltage. The average switching

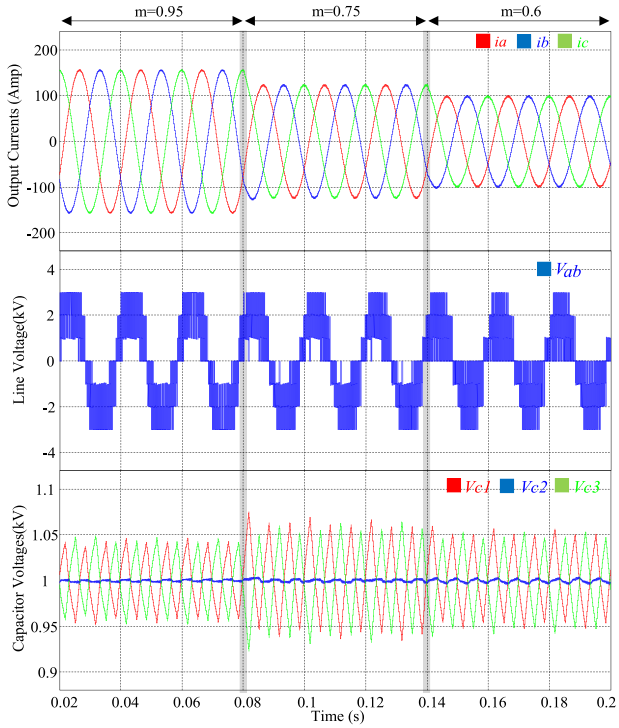

Fig. 11. Simulation results of output currents, line voltage, and capacitor voltages under two step changes in modulation index using the proposed VL-PWM.

frequency has the lowest value when the modulation index is 0.95, and it is equal to 2.46 kHz. Under the same condition, the switching frequency of the natural voltage balancing VL-PWM

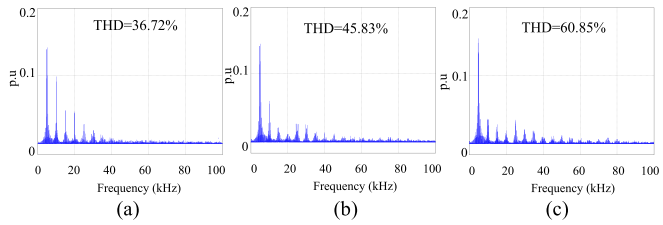

Fig. 12. Harmonic spectrum of line voltage for different modulation indexes: (a) $m = 0.95$, (b) $m = 0.75$, and (c) $m = 0.6$.

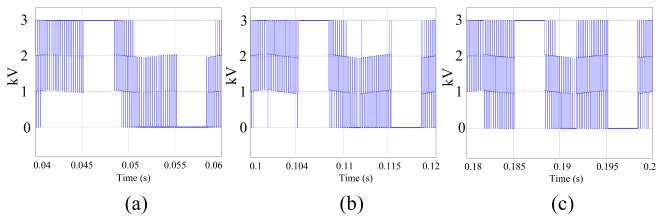

Fig. 13. Simulation results of phase voltage for different modulation indexes: (a) $m = 0.95$, (b) $m = 0.75$, and (c) $m = 0.6$.

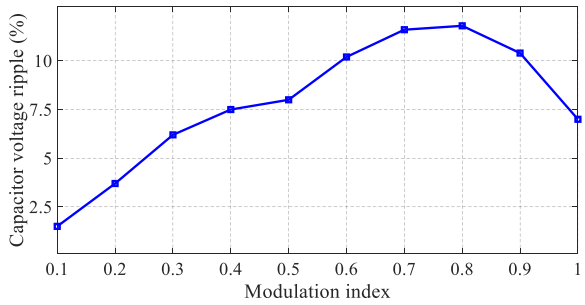

Fig. 14. Variation of the upper and lower dc-link capacitor voltage ripples versus modulation index.

method presented in Section III equals 2.2 kHz and is slightly lower. Considering operating conditions with $m = 0.75$ and $m = 0.6$ when applying the closed-loop VL-PWM method, the average switching frequency is 2.55 and 2.97 kHz, respectively. The 4L-DCC topology connected to an *RL* load has been simulated in PSIM software under different modulation indexes to examine the variation of the upper and lower dc-link capacitors. Fig. 14 shows how the voltage ripple of dc-link capacitors vary by changing the modulation index, stating that the voltage ripple has the highest values for intermediate values of modulation index (around $m = 0.8$), while it reduces to lower values as modulation index moves toward higher and lower values than 0.8.

B. Load Power Factor Change

For the next step, the modulation index remains fixed at 0.95, and the system response is assessed under two changes to the load power factor from 0.9 to 0.6, and then from 0.6 to 0.2. Three fundamental periods are allocated to each operating condition in the corresponding simulation results.

Fig. 15 shows the output current for the three applied power factors. The current THD increases when applying lower power factors, equaling 0.67% for PF = 0.9 and increases to 1.4% when the PF is set to 0.2. As can be seen in Fig. 15, the line voltage levels are properly produced during different power factors.

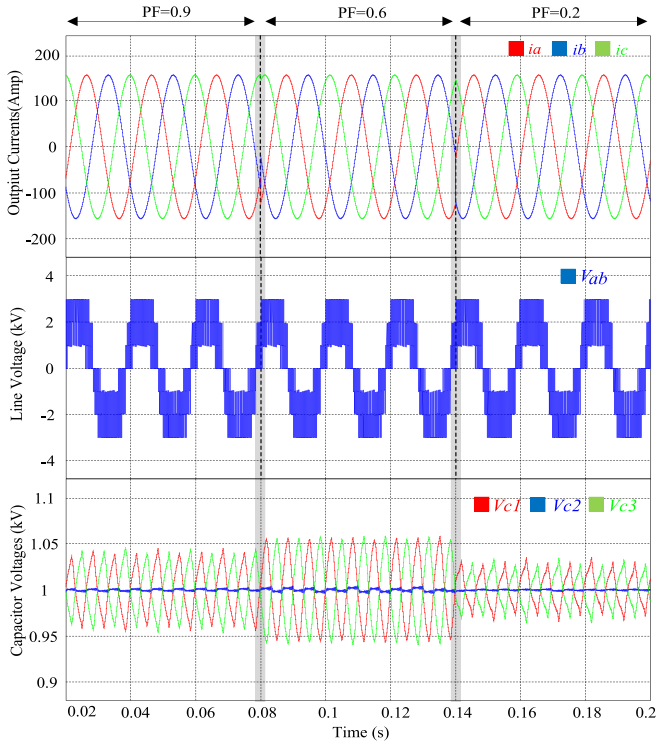

Fig. 15. Simulation results of three-phase currents, line voltage, dc-link capacitor voltages during two step changes in load power factor using the proposed VL-PWM.

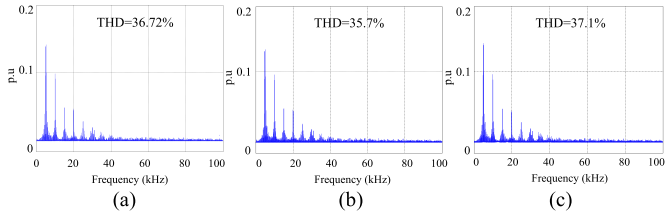

Fig. 16. Harmonic spectrum of line voltage for different load power factors: (a) PF = 0.9, (b) PF = 0.6, and (c) PF = 0.2.

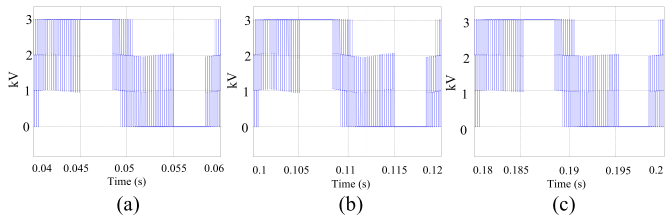

Fig. 17. Simulation results of phase voltage for different load power factors: (a) PF = 0.9, (b) PF = 0.6, and (c) PF = 0.2.

Also, the active voltage balancing VL-PWM method satisfies the balancing requirements under various load power factors, as shown in Fig. 15. However, the voltage ripple has the highest value among the presented conditions, equaling 12%, when the load power factor is 0.6.

Fig. 16 shows the harmonic spectrum of the line voltage for three different values of the load power factor, and the voltage THD is relatively the same over the depicted intervals and equals 36%. The phase voltage is shown in Fig. 17 during the same

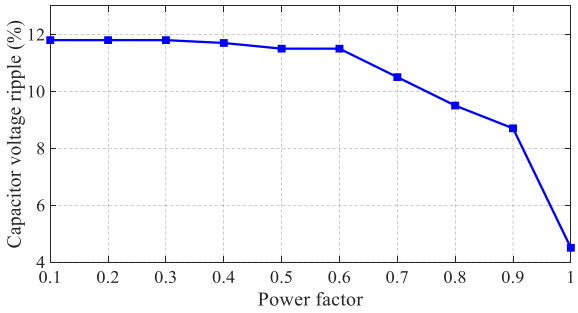

Fig. 18. Variation of the upper and lower dc-link capacitor voltage ripples versus power factor.

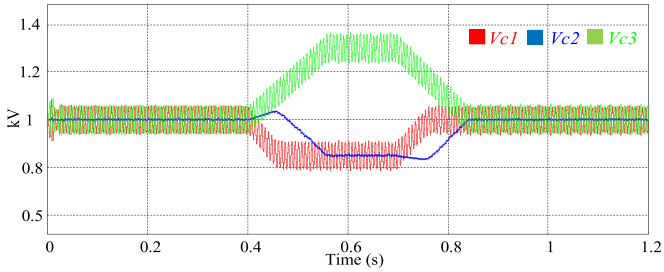

Fig. 19. Simulation results for a step change in the reference of capacitor voltages.

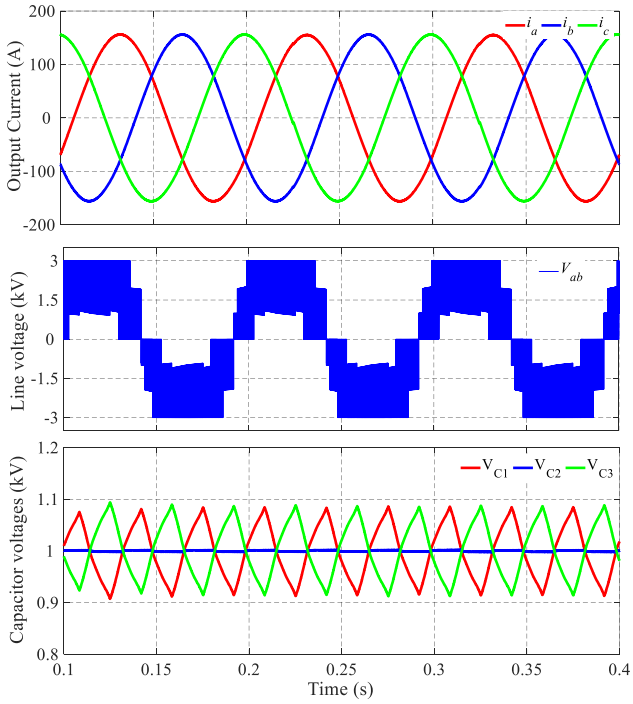

Fig. 20. Simulation results of the proposed VL-PWM technique at output frequency of 10 Hz.

changes in the power factor. Note that the average switching frequency remains relatively unchanged under step changes to the load power factor and is calculated to be 2.4 kHz. Fig. 18 shows the variation of capacitor voltage ripples versus different values of load power factors. It can be seen that the capacitor voltage ripples have the highest values when the load is mainly inductive and reduces as the load power factor becomes close to unity power factor.

C. Step Change in Reference Capacitor Voltages

To confirm the effectiveness of the active voltage balancing VL-PWM method, a step change is applied to the reference values of the dc-link capacitor voltages. As shown in Fig. 19, the capacitor voltages are regulated around the nominal voltage, i.e., one-third of dc-link voltage, before $t = 0.4$ s. A step change occurs at $t = 0.4$ s so that the reference voltage of the top dc-link capacitor rises from 1 to 1.3 kV, while the reference voltage of the bottom and the middle capacitors decrease to 0.85 kV. After implementing the described step changes, the capacitor voltages are stabilized at the new reference values. At $t = 0.7$ s, the reference voltages are changed to their primary values, and as can be seen in Fig. 16, the capacitor voltages are balanced again at one-third of the dc-link voltage.

D. Operation at Low Output Frequency

For motor drive applications, modulation schemes face several challenges, one of which is their performance at lower fundamental frequencies [38]. In the present article, the performance of the proposed scheme is evaluated at a 10 Hz output frequency. Fig. 20 illustrates the results of this simulation. DC-link capacitors are balanced, but they have the higher voltage deviation at this low output frequency as they do at higher output frequencies. The reason for this is that the reference vector is retained in each sector for a much longer period of time, although in the proposed active voltage balancing scheme, duty ratios are readjusted each sampling period.

E. Current Controller

The proposed VL-PWM scheme is tested under closed-loop operation conditions. The closed-loop control scheme is based on the current controller in the *DQ* frame. In this approach, the line current is tightly regulated by a dedicated current-control scheme, through generating the appropriate voltage at ac terminal [36]. It is responsible for producing three-phase sinusoidal modulating waveforms by adjusting both the modulation index and the frequency to match the reference currents. In fact, this is a three-phase *DQ* frame current controller [37]. In the *DQ* frame, the transferred reference load currents are subtracted from the three-phase ac load currents. Then, a PI controller processes the error signals to generate the reference voltages [36], [37]. Consequently, the reference modulation index, M, and the reference angle, θ, are calculated, and they will be utilized in the proposed modulation scheme. From this, the appropriate switching signals for the converter will be generated. Fig. 21 illustrates the simulation results for implementing the proposed VL-PWM scheme in conjunction with the closed-loop current control. The reference current is initially set to 110 A. After that, it becomes 58 A and then 92 A. As can be seen in Fig. 21, the proper output voltages are generated, and the dc-link voltage are well balanced using the implementation of the closed-loop current control.

VI. Comparison

As a way of comparing active voltage balancing VL-PWM and the classic VVPWM method in terms of voltage THD and

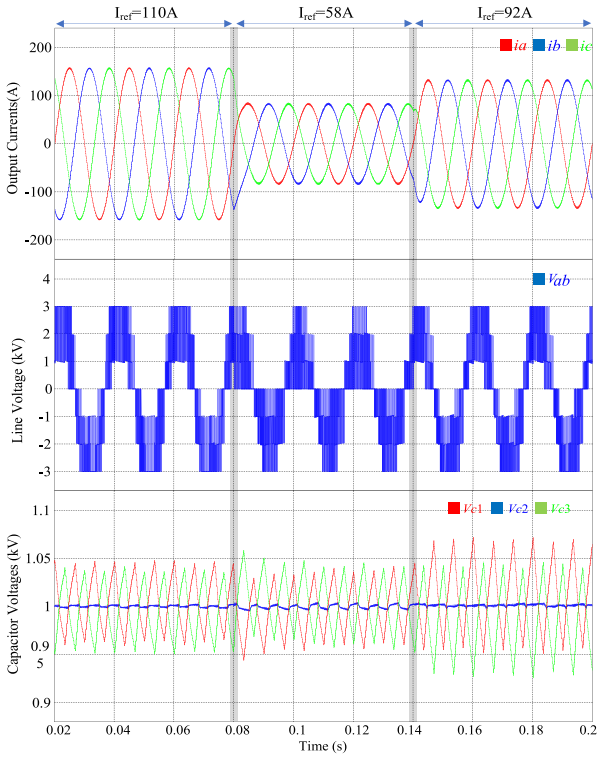

Fig. 21. Simulation results of the implementation of the proposed VL-PWM method alongside the closed-loop current control.

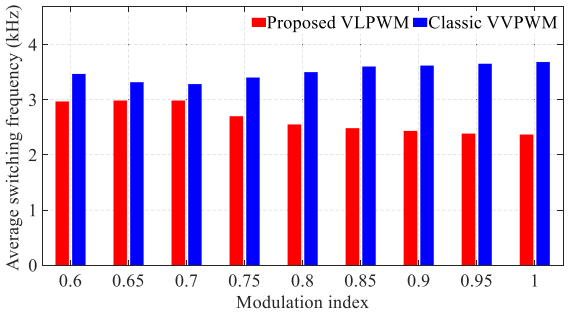

Fig. 22. Comparison of switching frequencies of the proposed VL-PWM and VVPWM methods.

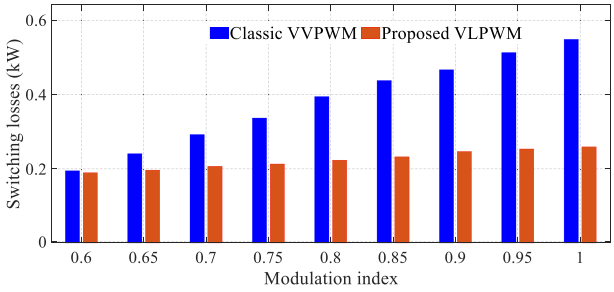

Fig. 23. Comparison of switching losses of the proposed VL-PWM and VVPWM methods.

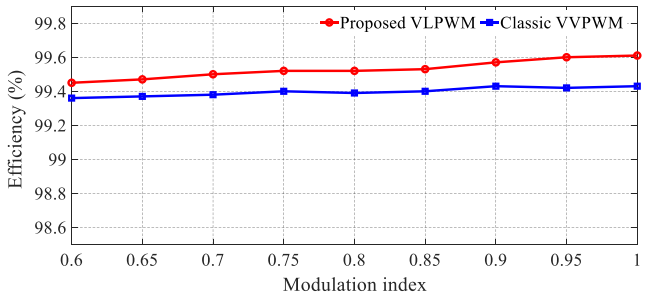

Fig. 24. Comparison of efficiency of the proposed VL-PWM and VVPWM methods.

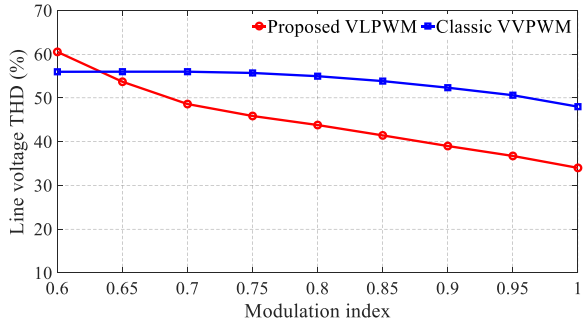

Fig. 25. Comparison of the line voltage THD of the proposed VL-PWM and the classic VVPWM methods.

switching frequencies, both methods were evaluated for a modulation index range from 0.6 to 1, which falls within the range in which basic PWM cannot provide capacitor voltage balancing. Note that the proposed method in this article is an alternative for conventional modulation methods when capacitor voltage balancing cannot be accomplished in the 4L-DCC topology (refer to Fig. 3). As a matter of fact, employing classic PWM or SVM techniques for modulation indexes lower than 0.55 presents lower complexity, lower voltage distortion, and lower switching transitions while there is no concern about voltage balancing.

Fig. 22 compares the switching frequencies of the proposed VL-PWM and classic VVPWM techniques for different modulation indexes. The reported values are the average switching frequency of three switching devices in each phase during one fundamental output cycle. Under all operating conditions considered, the switching frequency of the proposed method is lower than that of the VVPWM method. This effect is even greater for higher modulation indexes. With a modulation index of 0.95, using the proposed VL-PWM method, the switching frequencies of switches S_{a1}, S_{a2}, and S_{a3} (indicated in Fig. 1) are 2, 3.25, and 2.05 kHz, respectively.

A comparison of switching losses and efficiency of the 4L-DCC topology under the implementation of the proposed VL-PWM and VVPWM techniques are shown in Figs. 23 and 24, respectively. In comparison with the VVPWM method, the proposed method results in lower switching losses for different modulation indexes over the unbalanced area. Due to the lower switching losses of the proposed VL-PWM method, it also results in higher converter efficiency than the classic VVPWM under different operating conditions. In Fig. 25, the comparison of voltage THD shows that the proposed VL-PWM method performs better than classical VVPWM for modulation indexes greater than 0.62. The comparison results of Figs. 22–25 are presented for the modulation indexes between 0.6 and 1. The reason for this is that the 4L-DCM converter has voltage balancing issues in these modulation indexes with power factors close to unity, as illustrated in Fig. 3.

TABLE VII
EXPERIMENTAL SYSTEM PARAMETERS

System parameter	Value
Switching devices	MOSFET IRF640
Current and voltage ratings of the MOSFETs	18 A, 200 V
DSP	TMS320F28335
DC source voltage (V_{dc})	200 V
Capacitance of dc-link capacitors	470 µF
Sampling frequency	5 kHz
Reference voltage frequency (f_o)	50 Hz
Load resistance and inductance (R, L)	20 Ω, 32 mH

It is evident the classic SVM is suitable for lower modulation indexes, considering its simplicity and lower switching frequency.

It should be noted that the active capacitor voltage balancing scheme has been implemented in the proposed method, whereas the VV-SVM scheme is devoid of this feature and only provides natural voltage balancing. However, when comparing the proposed natural voltage balancing scheme presented in Section III, it is evident that the proposed method requires less computational time. Despite the VV-SVM schemes based on VVs, the initial stages of modulation in the proposed natural voltage balancing method, including the location of reference voltage vector in the space vector diagram, the identification of three adjacent voltage vectors, and the assignment of duty ratios, are identical to the classic SVM. As a matter of fact, the proposed method has the advantage of implementing the modulation using the classical space vector plan as opposed to the VV-SVM method. Therefore, the proposed VL-SVM scheme has a lower computational burden than the VV-SVM scheme.

In addition, the proposed method is implemented on a digital platform. However, in real-world implementation, there are many optimizations and tricks that can affect the computational time of an algorithm. More importantly, the computational power of the processor also plays an important role in this figure. On the other hand, in real MV applications, the converter parameters, such as switching frequency, are selected based on the design criteria and available components. For these applications, the sampling frequency is in the range of a few KHz, and the sampling interval is large enough to allow for the computation time required for all operations of active capacitor voltage balancing within a sample interval.

VII. EXPERIMENTAL RESULTS

A low-power prototype of the three-phase 4L-DCC topology was implemented to evaluate the practicality of the proposed voltage balancing VL-PWM method. Table VII gives the experimental system parameters. A digital signal processor is utilized to execute the proposed modulation scheme and generate switches' gate signals. The amplitude of the dc voltage is 200 V as this was just a proof-of-concept verification.

Fig. 26 shows the measured waveforms when the modulation index is set to 0.95. As can be seen in Fig. 26(a), the phase to neutral voltage waveforms have four levels and a peak-to-peak amplitude equal to the dc-link voltage. The dc-link capacitor voltages are balanced, which leads to accurate output voltage levels. The amplitude of the dc-link voltage is 200 V, as can be seen in Fig. 26(c), and the dc-link capacitor voltages are well regulated at $V_{\rm dc}/3$, i.e., 67 V. Fig. 26(b) and (d) shows the three-phase line voltages and load currents, respectively. The experimental results are in good agreement with the simulation results.

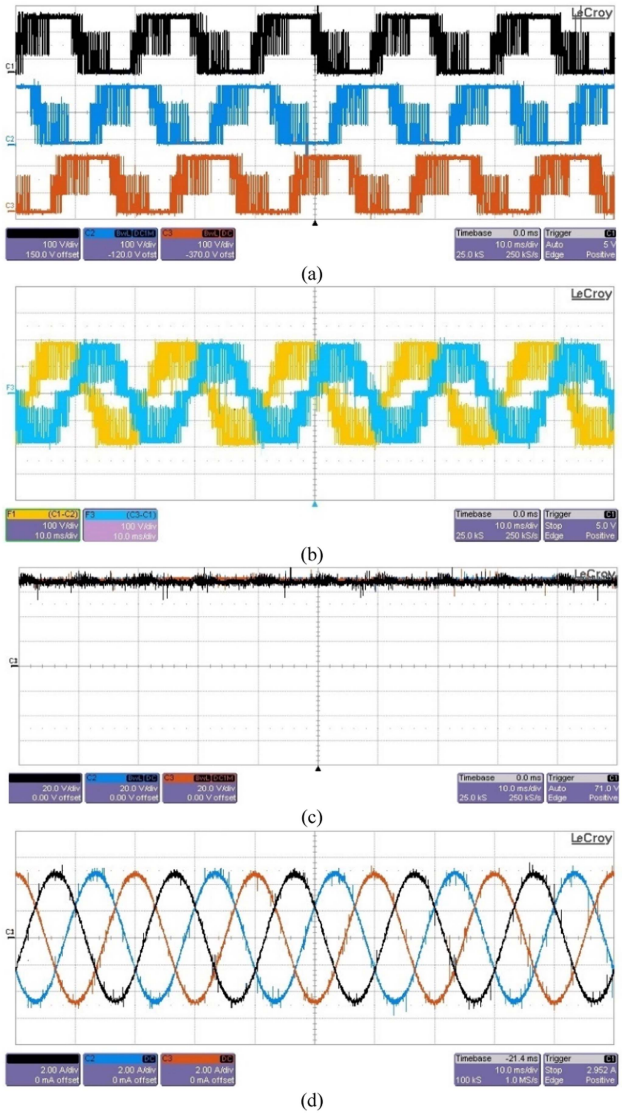

Fig. 26. Experimental results at $M = 0.95$: (a) phase voltages v_{aN}, v_{bN}, and v_{cN}, (b) line voltages v_{ab} and v_{ca}, (c) dc-link capacitor voltages, and (d) three-phase load currents.

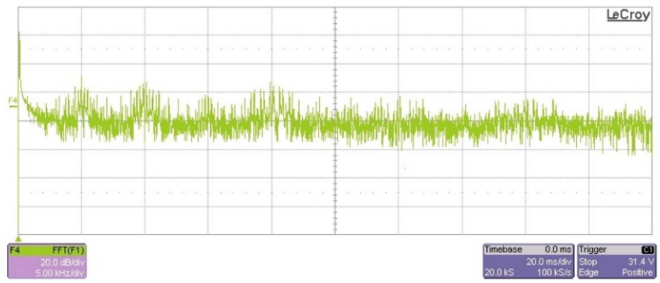

Fig. 27. Frequency spectra of the output line voltage.

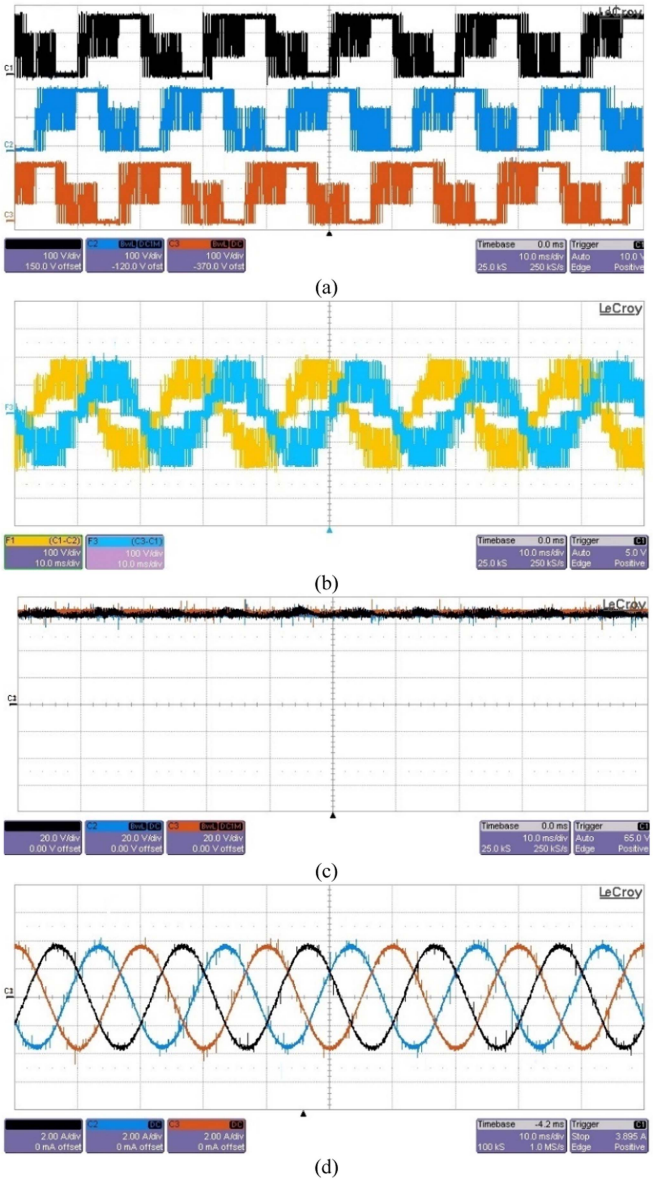

Fig. 28. Experimental results at $M = 0.75$: (a) phase voltages v_{aN}, v_{bN}, and v_{cN}, (b) line voltages v_{ab} and v_{ca}, (c) dc-link capacitor voltages, and (d) three-phase load currents.

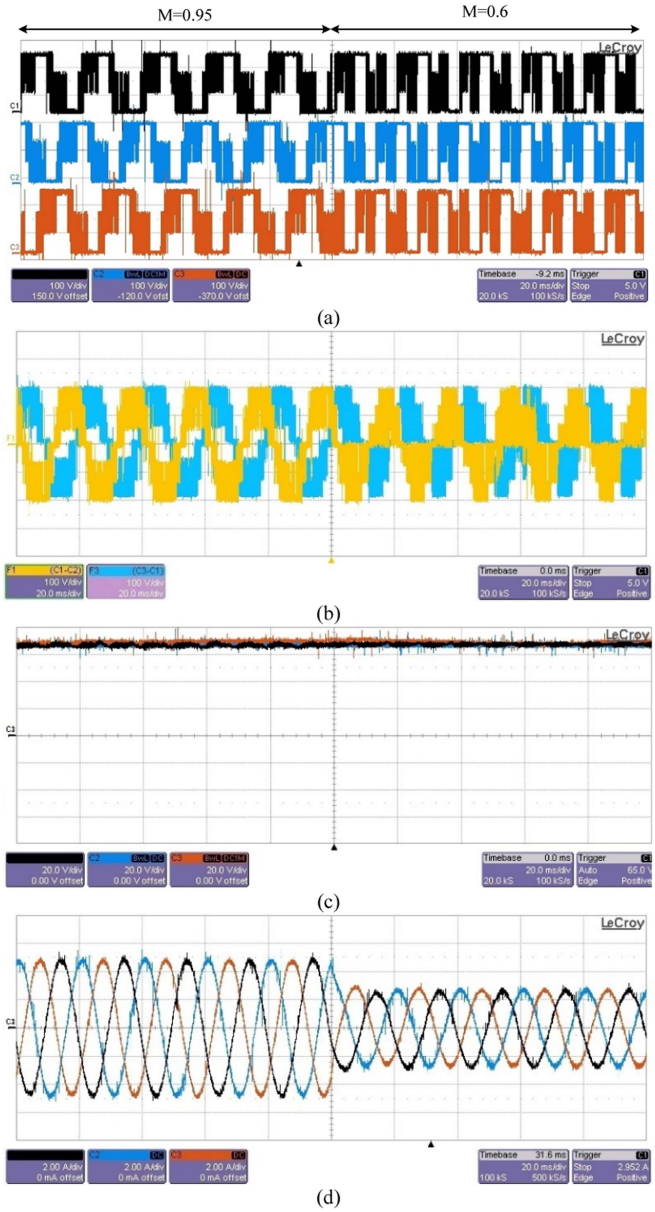

Fig. 29. Experimental results when modulation index changes from $M = 0.95$ to $M = 0.6$: (a) phase voltages v_{aN}, v_{bN}, and v_{cN}, (b) line voltages v_{ab} and v_{ca}, (c) dc-link capacitor voltages, and (d) three-phase load currents.

Fig. 27 shows the FFT of the output line voltage V_{ab}. The sideband harmonics of the output voltage are centered around the sampling frequency of 5 kHz and its multiplications. The THD of the line voltage is approximately 45%, while the THD of the load current is approximately 1.4%. These values are slightly higher than those obtained by the simulations.

The performance of the proposed modulation scheme is evaluated at a different operating point, in which the modulation index is set to the $M = 0.75$. The measured phase voltages, line voltages, dc-link capacitor voltages, and load currents are shown in Fig. 28. The phase voltage waveforms in Fig. 28(a) have four levels and as explained in the proposed scheme, the phase voltage waveforms are fixed to levels 0 and 4 during two 60° intervals of each output voltage cycle. This is due to the method of redundant switching states selection in the proposed scheme. The phase voltages provide the seven-level line voltages at the load terminals as shown in Fig. 28(b). It is evident from the experimental results that the proposed modulation scheme performs capacitor voltage balancing for DCC topologies when the operation points are located in the restricted area (refer to Fig. 3). The capacitor voltages in Fig. 28(c) are regulated around their nominal values, leading to the proper operation of the converter.

To show the performance of the proposed VL-PWM scheme with capacitor voltage balancing during transient conditions, a step change from $M = 0.95$ to $M = 0.6$ is applied. The resulting phase voltages, line voltages, dc-link capacitor voltages, and load currents are shown in Fig. 29. The phase voltages generation is based on the proposed scheme at different modulation indexes. The active voltage balancing scheme properly regulates the dc-link capacitor voltages during the step change. As can

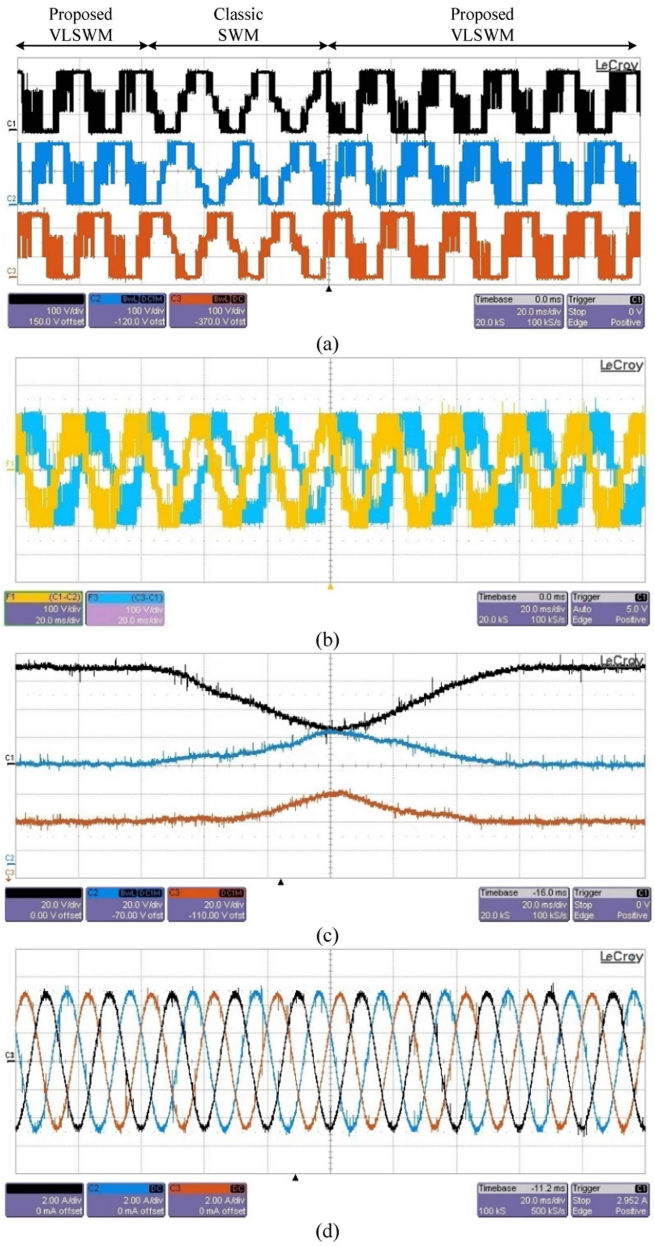

Fig. 30. Experimental results of imbalance dynamics when the modulation method changes: (a) phase voltages v_{aN}, v_{bN}, and v_{cN}, (b) line voltages v_{ab} and v_{ca}, (c) dc-link capacitor voltages, and (d) three-phase load currents.

be seen in Fig. 29(c), the capacitor voltages are maintained at the nominal values with modulation index changes. The line voltages v_{ab} and v_{ca} are shown in Fig. 29(b), which have seven-level voltage waveforms. The amplitudes of load currents are decreased because of the reduction of the output voltage amplitude at a lower modulation index.

Fig. 30 shows the experimental results of imbalance dynamics for dc-link capacitors. Initially, the active voltage balancing VL-PWM method is applied to the 4L-DCC, and the voltages of dc-link capacitors are balanced at one-third of the dc-link voltage. After this, the classic SVM method is employed to produce the desired output voltage. As can be seen in Fig. 30(a) and (b), the phase voltage and line voltage display staircase

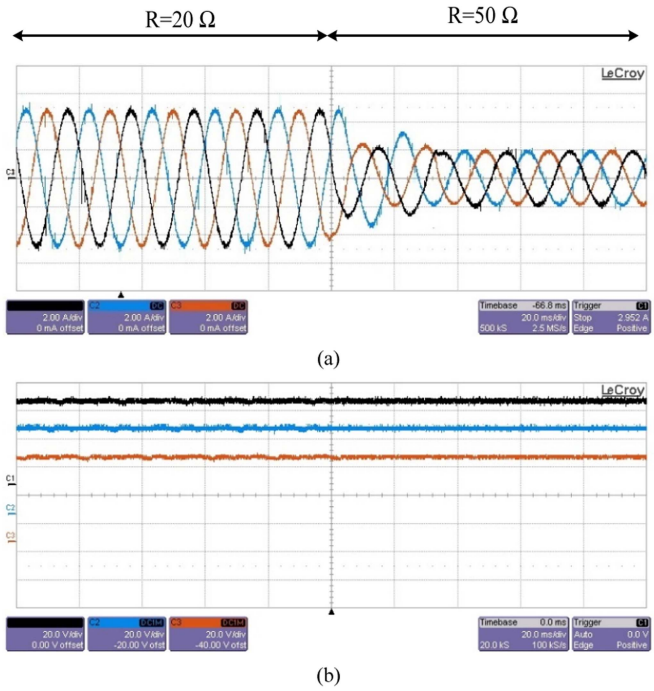

Fig. 31. Experimental results at load power factor change: (a) three-phase load currents and (b) dc-link capacitor voltages.

waveforms, which correspond to the classic SVM scheme. However, the voltage of the middle capacitor, C_2, is decreased, whereas the voltages of the top and bottom capacitors, C_1 and C_3, are raised. In this way, the voltage waveforms deviate. Three output cycles later, the proposed VL-PWM scheme is activated again, and the capacitor voltages return to the desired values.

Fig. 31 shows the experimental waveforms for changing load power factors. In the beginning, the load resistance and inductance are equal to 20 Ω and 32 mH, respectively, and the voltages of dc-link capacitors are balanced at one-third of the dc-link voltage. Thereafter, the resistance of the load is increased from 20 to 50 Ω. As a result, the power factor is changed from 0.89 to 0.98. It is evident that the dc-link capacitor voltages are well regulated at their desired levels during loads power factor changes. As expected, the capacitor voltage ripples are smaller at lower output currents.

VIII. Conclusion

This article presents a modulation scheme for dc-link capacitor voltage balancing of the 4-level DCC topology. This strategy deals with the voltage balancing restrictions of the 4L-DCC topology under the implementation of classic modulation techniques. The modulation scheme is implemented on the basis of using virtual voltage levels, which enables the average neutral point currents over the fundamental period to be zero. This results in low capacitor voltage ripples and low line voltage THDs, which are the other advantages of the proposed VL-PWM method. To decrease the switching frequencies, the switching states are rearranged, and appropriate space vectors are selected during the proposed VL-PWM implementation. In addition, to compensate for any voltage drift due to unideal

practical conditions, an additional closed-loop procedure is developed. In this procedure, the duty ratios of the voltage levels are readjusted in favor of reducing the difference between the actual capacitor voltages and their reference values. As a result, the dc-link capacitor voltages are actively balanced. Simulation and experimental results show the effectivenessof the proposed modulation scheme.

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Javad Ebrahimi (Member, IEEE) received the Ph.D. degree in power electronics from the Isfahan University of Technology, Isfahan, Iran, in 2017.

He is currently a Postdoctoral Fellow with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada. From 2017 to 2019, he was an R&D Director with the Behrad Consulting Engineers Company, Isfahan, Iran, where he was working closely with utilities and industries, and was actively involved in research in the areas of power electronics and power systems. His research interests include topology design, modulation, and control of power electronic converters, multilevel converters, electric vehicles, and the application of power electronics in power systems.

Shima Shahnooshi received the B.Sc. and M.Sc. degrees in power electronics and electric machines from the Isfahan University of Technology, Isfahan, Iran, in 2017 and 2020, respectively. She is currently working toward the Ph.D. degree in power electronics and electric machines with the Queen's University, Kingston, ON, Canada.

Her research interests include the control of multilevel converters, predictive control, and the control of microgrids.

Suzan Eren (Member, IEEE) received the B.Sc. (Hons.), M.Sc., and Ph.D. degrees in electrical engineering from the Queen's University, Kingston, ON, Canada, in 2006, 2008, and 2013, respectively.

She is currently an Assistant Professor with the Department of Electrical and Computer Engineering, Queen's University, and a member of the ePOWER, the Queen's Centre for Energy and Power Electronics Research Group. Her industrial experience includes collaboration with SPARQ Systems in developing their highly efficient solar microinverter. Her research interests include control and signal processing techniques for power converters used in microgrid and renewable energy applications.

Alireza Bakhshai (Fellow, IEEE) received the B.Sc. and M.Sc. degrees from the Isfahan University of Technology, Isfahan, Iran, in 1984 and 1986, respectively, and the Ph.D. degree from the Concordia University, Montreal, QC, Canada, in 1997, all in electrical engineering.

He is currently a Faculty Member with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, and a Licensed Professional Engineer in Ontario. From 1986 to 1993 and from 1998 to 2004, he was a Faculty Member with the Department of Electrical and Computer Engineering, Isfahan University of Technology. His research interests include high-power electronics, distributed energy generation and conversion, microgrid and smart grid systems, and advanced control theories applied to power electronics converters.