A High-Frequency Isolated Four-Switch Single-Phase Quasi-Z-Source AC–AC Converter With Inherent Commutation and Step-Changed Frequency Operation

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***Abstract*—In this article, a high-frequency isolated single-phase quasi-Z-source ac–ac converter is proposed. This converter can generate a broad range of output voltage while also allowing the output frequency to be changed. The configuration is divided into two similar subcircuits in a way that only one unidirectional switch exists in each subcircuit, and complementary switches are removed. Therefore, the proposed converter has inherent commutation without the necessity to apply any delays or, safe commutation strategies. Two switches on the output side are responsible for changing the frequency. So, voltage regulation and changeable frequency are obtained with only four unidirectional switches and a simple switching strategy. Electrical isolation is also acquired via employing a compact-sized high-frequency transformer. All the aforementioned features result in the proposed converter's small size, compact structure, low cost, high reliability, and high power density. A comprehensive analysis of the circuit operation principles is discussed. Then, a 100 V_{rms}/50 Hz laboratory prototype is implemented to indicate the accuracy of theoretical results.**

***Index Terms*—Continuous input current, high-frequency transformer (HFT), inherent commutation, quasi-Z-source ac–ac converter, step-changed frequency.**

I. Introduction

FOR a long time, ac–ac converters have captured special attention due to their ability to deliver ac voltage with variable amplitude and frequency. For output voltage regulation only, in applications such as dynamic voltage restorers [1], the direct PWM ac–ac converters [2] are utilized. Variable frequency operation is also desired, which is needed in various ac–ac conversion applications, such as traction systems [3], wind turbines [4], induction heating [5], etc. These applications require voltage with both varying amplitude and frequency. There are two conventional converter topologies to meet this demand. The first topology is indirect variable frequency converters (ac–dc–ac) [6], [7]. Such converters comprise two conversion stages.

A dc-link capacitor is settled between stages to smooth the dc voltage. This capacitor is bulky, heavy, and has a short life. Furthermore, power losses in each power converting stage decrease efficiency and reliability. The second topology is matrix converters (MCs) [8], [9]. The MCs deliver single-stage, direct ac–ac conversion without any interface dc link. The first MC is presented in [10]. Due to the lack of energy storage components in this MC structure, they could only perform voltage amplitude step-down operations. The issues of MCs in terms of voltage gain have been solved by introducing the Z-source ac–ac converters [11], [12]. As a result, by incorporating Z-source networks into MCs, a wide range of buck-boost output voltages and variable frequency is obtained [13]. Complementary bidirectional switches are utilized in the MCs and Z-source ac–ac converters. Overlapping or dead time may occur between them due to different lags in the gate driver circuits of these PWM switches. So, current and voltage spikes are unavoidable if these switches have delays, resulting in damage to the switches and the converter performance. To solve these commutation problems, a safe commutation strategy is investigated for Z-source ac–ac converters in [14], [15] and MCs in [16]. This strategy is complicated and becomes more so when there are several bidirectional complementary switches in the converter structure. A theory called "switching cells" was recently presented in [17]. In this concept, by separating the circuit structure into two identical cells, bidirectional switches are replaced with unidirectional switches and diodes. Then, a simple switching strategy is required to control and provide a current path for inductors. This concept can be applied to MCs and direct PWM Z-source ac–ac converters [18], [19], [20].

All of the above-mentioned ac–ac converters are not isolated. In [21], an isolated multiconverter is introduced. This converter provides electrical isolation by employing a line-frequency transformer, which is directly connected to the ac input source. However, due to their heavy and bulky iron cores and thick copper windings, such transformers are voluminous, costly, have higher losses, and decreased efficiency and power density [22]. Therefore, inserting a high-frequency transformer (HFT) is a proper alternative for achieving electrical isolation, high power density, and high efficiency all at the same time [23], [24]. Various high-frequency isolated (HFI) single-phase Z-source ac–ac converters in [25], modified topology in [26], and HFI trans-Z-source in [27] are presented. However, these converters have higher power losses and complicated safe commutation

Manuscript received 10 August 2022; revised 24 October 2022; accepted 28 November 2022. Date of publication 13 December 2022; date of current version 14 February 2023. Recommended for publication by Associate Editor B. Li. *(Corresponding author: Ebrahim Babaei.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3228939.

Digital Object Identifier 10.1109/TPEL.2022.3228939

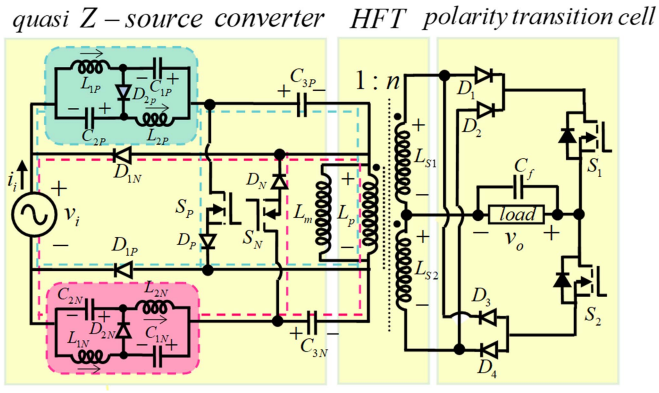

Fig. 1. Proposed HFI quasi-Z-source AC–AC converter.

strategies. Furthermore, the variable frequency of the output voltage is something that is lacking. To include variable frequency in addition to HFI, converter topologies such as MCs with HFI must be given special attention. In [28] an HFI MC is presented. But it has a discontinuous input current and can only operate in buck mode. The converter presented in [29] improves on the previous converter [28] by including a boost feature and a continuous input current. However, the structure employs an H-bridge on each primary and secondary side of the HFT, bringing the total number of switches to eight, which increases the cost.

To solve the shortcomings of the previously mentioned converters, a HFI single-phase quasi-Z-source ac–ac converter with step-changed frequency operation is proposed in this article to provide all the following properties as enumerated.

1) With the contribution of two freedom degrees, including the duty cycle (D) and the turn ratio (n) of HFT, a wide range of boost or buck-boost voltage gain is provided.
2) The proposed converter offers symmetric bipolar voltage gain. So, it can carry out both inverting and noninverting operations. With the help of this attribute, this converter has a step-changed frequency operation.
3) A compact volume HFT provides electrical isolation.
4) By separating the structure into two symmetric subcircuits with only one unidirectional switch, any overlap between the switches, or any dead time cannot be created.
5) The proposed converter uses only four switches, which is significantly low.
6) The input current is continuous and does not require large filters. Also, the waveform quality is improved by providing a continuous input current.

II. Proposed HFI Quasi Z-Source AC–AC Converter

A. Topology Clarification of the Proposed Converter

The circuit structure of the proposed HFI quasi-Z-source ac–ac converter is shown in Fig. 1. The circuit structure of the quasi-Z-source converter section is divided into two subcircuits, positive and negative. They are considered for performance in the positive half-cycles and negative half-cycles of the input voltage source, respectively. The positive subcircuit is indicated with the dashed blue line and the negative subcircuit with the dashed red line. There is also a high-frequency PWM unidirectional switch in each subcircuit. S_P and S_N are modulated by high-frequency PWM signals.

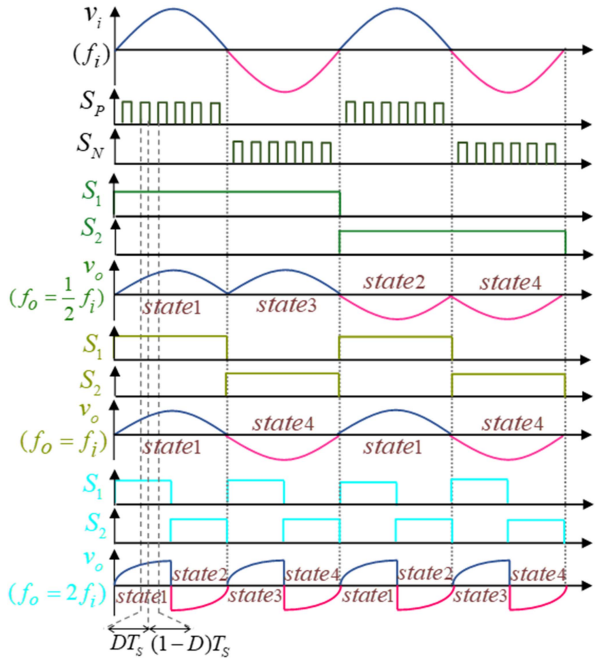

Fig. 2. Switching strategy of the proposed converter for producing three several frequencies at the output.

Each of these switches creates two operation modes and has the task of adjusting the output voltage amplitude. After HFT, on the output side, S_1 and S_2 are used as switches that transit the output voltage polarity toward the input voltage to create one of the two inverting or noninverting output voltage modes. The operation frequency of these two switches is low and depends on the desired frequency of the output voltage.

B. Switching Strategies and Operation Principles

As long as the input voltage source is in its positive half-cycles, S_P is switched ON and OFF. Then, considering which of the S_1 or S_2 in the polarity transition cell is turned ON, one of the states 1 or 2 will be formed at the output. When S_1 is turned ON, the input voltage is transferred to the output completely in-phase, resulting in a noninverted output (state 1) but when S_2 is turned ON, it transfers the input voltage to the output entirely out-of-phase, creating an inverted output (state 2). Similarly, when S_N is switched ON and OFF in negative half-cycles, regarding which of S_1 or S_2 is turned ON, states 3 or 4 will be created. By permuting these four states, different frequencies can be extracted at the output. The available output frequency range can be divided into two parts. The step-up output frequencies which follow the $f_o = kf_i$ and the step-down output frequencies which follow the $f_o = \frac{1}{k} f_i$ where k can be any positive integer ($k = 1$, 2, 3, 4, …). The proposed converter simple switching strategy for all four switches is shown in Fig. 2 for creating the three output frequencies. Each switching cycle, as shown in Fig. 2, only involves one unidirectional high-frequency PWM switch, which is not complementary to the other low-frequency switch. Therefore, deliberate dead times are not required to prevent short-circuits and current spikes. Furthermore, the current path for inductors is inherently provided by the structure itself. For this reason, safe commutation strategies, which provide a current path during these dead times (open-circuit) to prevent voltage spikes, are eliminated. The following assumptions are taken into account when analyzing the proposed converter. (a) The

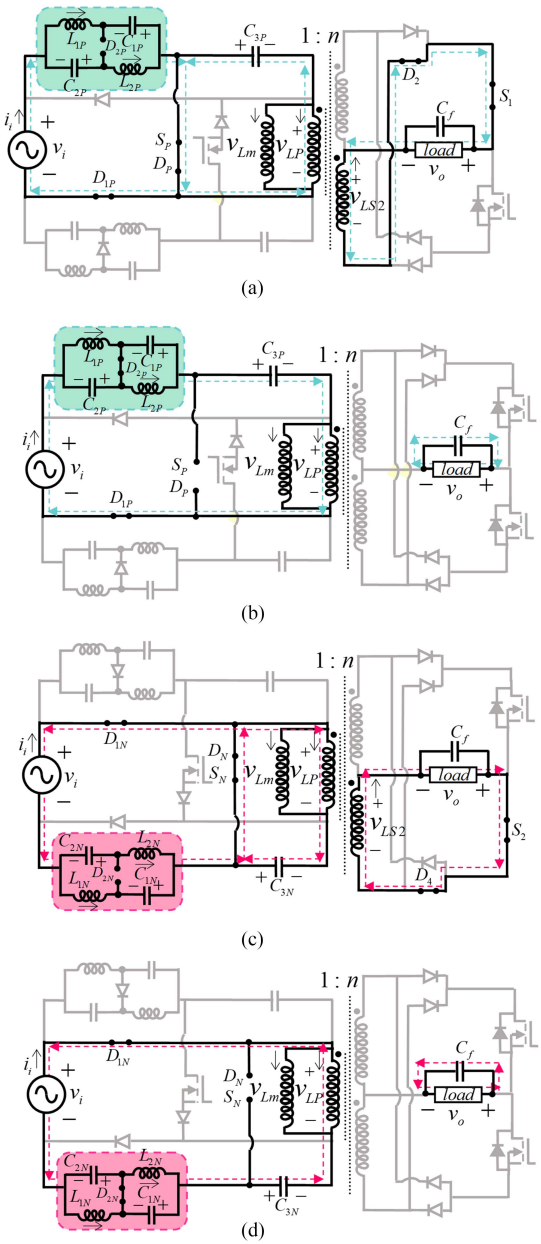

Fig. 3. Equivalent circuits of the proposed converter. (a) Mode I of state 1. (b) Mode II of state 1. (c) Mode I of state 4. (d) Mode II of state 4.

proposed converter operates in continuous conduction mode. (b) The proposed converter's inductors and capacitors are all ideal. (c) Both secondary windings of the HFT have the same turn ratio toward the primary winding. As illustrated in Fig. 2, the generation of the output voltage with the frequency of $f_o = f_i$ uses two states (states 1 and 4) throughout one cycle of the input voltage source. Each of these states consists of two operation modes. The duration of mode I and mode II are (DT_S) and (1-D)T_S, respectively, where Ts is the switching period.

1) State 1:

a) Mode I: Fig. 3(a) depicts the equivalent circuit. In this mode, S_P is switched ON and the D_P and D_{1P} are forward-biased, but D_{2P} is reversed and does not lead the flow. The energy stored in the C_{1P}, C_{2P} is discharged to L_{1P}, L_{2P}. The C_{3P} stored energy is inversely discharged across the primary winding of the HFT (L_P) through the S_P and D_P ($v_{LP} = -v_{C3P} < 0$). Therefore, according to the selected directions for the HFT, $v_{LS1}, v_{LS2} = nv_{LP} < 0$ is realized on the secondary side of the HFT. In state 1, the S_1 is turned ON, causing the D_2 to conduct and the energy stored in the capacitor C_{3P} to be transferred to the output load. By applying KVL, it can be written

$$v_{L1P} = v_i + v_{C1P} \tag{1}$$

$$v_{L2P} = v_i + v_{C2P} \tag{2}$$

$$v_{Lm} = -v_{C3P} \tag{3}$$

$$v_{LS1-LS2} = -nv_{C3P} \tag{4}$$

$$v_o = -v_{LS2}. \tag{5}$$

b) Mode II: The equivalent circuit of mode II is shown in Fig. 3(b). In this mode, a positive voltage is placed on the D_{2P} so it can conduct the flow. D_{1P} has still retained forward-biased. C_{1P} and C_{2P} are charged by L_{1P} and L_{2P} via the free-wheeling path provided by D_{2P}. C_{3P} is charged from the path of the V_i, L_{1P}, D_{2P}, L_{2P}, L_m, and D_{1P}. The output current path is blocked by D_1. By applying KVL, it can be written

$$v_{L1P} = -v_{C2P} \tag{6}$$

$$v_{L2P} = -v_{C1P} \tag{7}$$

$$v_{Lm} = v_i + v_{C1P} + v_{C2P} - v_{C3P}. \tag{8}$$

By applying the volt-second balancing law for inductors L_{1P}, L_{2P}, and L_m with the help of (1)–(3) and (6)–(8), the voltage across the capacitors is obtained as follows:

$$\begin{cases} v_{C1P-C2P} = +\frac{D}{1-2D}v_i \\ v_{C3P} = +\frac{1-D}{1-2D}v_i \end{cases}. \tag{9}$$

By replacing (9) in (4) and (5), voltage gain is calculated as follows:

$$\frac{v_o}{v_i} = +\frac{1-D}{1-2D}n = +G. \tag{10}$$

The positive sign in the voltage gain equation means that the voltage polarity does not change at the output.

2) State 4:

a) Mode I: Fig. 3(c) depicts the equivalent circuit. In this mode, S_N is switched ON. D_N and D_{1N} conduct. The C_{3N} stored energy is discharged to L_P ($v_{LP} = v_{C3N} > 0$). Therefore, $v_{LS1}, v_{LS2} = nv_{C3N} > 0$ is realized on the secondary side of the HFT. In state 4, the S_2 is turned ON, causing the diode D_4 to conduct. So, the energy stored in the C_{3N} is transferred to the output load. By applying KVL, it can be written

$$v_{L1N} = -v_i + v_{C1N} \tag{11}$$

$$v_{L2N} = -v_i + v_{C2N} \tag{12}$$

$$v_{Lm} = v_{C3N} \tag{13}$$

$$v_{LS1-LS2} = nv_{C3N} \tag{14}$$

$$v_o = -v_{LS2}. \tag{15}$$

The polarity of v_{LS2} is positive. So, according to (15) the output voltage polarity will be negative, which is in-phase (noninverting) toward the negative input voltage source.

b) Mode II: The equivalent circuit is shown in Fig. 3(d). In this mode, S_N is switched OFF. Both D_{1N} and D_{2N} conduct the flow. The capacitor C_{3N} is charged from the path of the V_i, L_{1N}, D_{2N}, L_{2N}, L_m, and D_{1N}. The output current path is blocked by

TABLE I
CURRENT PEAK AND RMS VALUES ACROSS THE SWITCHES, INDUCTORS, DIODES, AND CAPACITORS

Switches	
Peak	**RMS**
$I_{SP-SN}=\frac{\sqrt{2}}{D}\frac{P_O}{V_{i-rms}}$	$I_{SP-SN}=\frac{1}{\sqrt{2D}}\frac{P_O}{V_{i-rms}}$
$I_{S1-S2}=\frac{\sqrt{2}(1-2D)}{nD(1-D)}\frac{P_O}{V_{i-rms}}$	$I_{S1-S2}=\frac{1-2D}{n\sqrt{2D}(1-D)}\frac{P_O}{V_{i-rms}}$
Inductors	
Peak	**RMS**
$I_{L1P,N-L2P,N}=\frac{\sqrt{2}P_O}{V_{i-rms}}$	$I_{L1P,N-L2P,N}=\frac{1}{\sqrt{2}}\frac{P_O}{V_{i-rms}}$
$I_{Lm}=\frac{\sqrt{2}(1-2D)}{1-D}\frac{P_O}{V_{i-rms}}$	$I_{Lm}=\frac{(1-2D)}{1-D}\frac{P_O}{V_{i-rms}}$
Diodes	
Peak	**Average**
$I_{D1P,N}=\frac{2\sqrt{2}P_O}{V_{i-rms}}$, $I_{DP,N}=\frac{\sqrt{2}}{D}\frac{P_O}{V_{i-rms}}$	$I_{D1P,N}=\frac{2\sqrt{2}P_O}{\pi V_{i-rms}}$, $I_{DP,N}=\frac{\sqrt{2}P_O}{\pi V_{i-rms}}$
$I_{D2P,N}=\frac{\sqrt{2}}{1-D}\frac{P_O}{V_{i-rms}}$	$I_{D2P,N}=\frac{\sqrt{2}P_O}{\pi V_{i-rms}}$
$I_{D1-D4}=\frac{\sqrt{2}(1-2D)}{nD(1-D)}\frac{P_O}{V_{i-rms}}$	$I_{D1-D4}=\frac{\sqrt{2}(1-2D)}{n\pi(1-D)}\frac{P_O}{V_{i-rms}}$
Capacitors	
Peak	**RMS**
$I_{C1P,N-C2P,N}=\frac{\sqrt{2}P_O}{V_{i-rms}}$	$I_{C1P,N-C2P,N}=\sqrt{\frac{D}{2-2D}}\frac{P_O}{V_{i-rms}}$
$I_{C3P,N}=\frac{\sqrt{2}(1-2D)}{D}\frac{P_O}{V_{i-rms}}$	$I_{C3P,N}=\frac{(1-2D)}{\sqrt{2D(1-D)}}\frac{P_O}{V_{i-rms}}$

TABLE II
VOLTAGE GAIN DETERMINATION

f_o	v_i	v_o	State	f_o	v_i	v_o	State	f_o	v_i	v_o	State
$2f_i$	+	$+GV_i$	1	f_i	+	$+GV_i$	1	$f_i/2$	+	$+GV_i$	1
	+	$-GV_i$	2						−	$-GV_i$	3
	−	$-GV_i$	3		−	$+GV_i$	4		+	$-GV_i$	2
	−	$+GV_i$	4						−	$+GV_i$	4

D_3. By applying KVL, it can be written

$$v_{L1N} = -v_{C2N} \tag{16}$$

$$v_{L2N} = -v_{C1N} \tag{17}$$

$$v_{Lm} = v_i - v_{C1N} - v_{C2N} + v_{C3N}. \tag{18}$$

By applying the volt-second balancing law for L_{1N}, L_{2N}, and L_m with the help of (11)–(18), the voltage across the capacitors and state 4 voltage gain is obtained as follows:

$$\begin{cases} v_{C1N-C2N} = -\frac{D}{1-2D}v_i \\ v_{C3N} = -\frac{1-D}{1-2D}v_i \\ \frac{v_o}{v_i} = +\frac{1-D}{1-2D}n = +G \end{cases}. \tag{19}$$

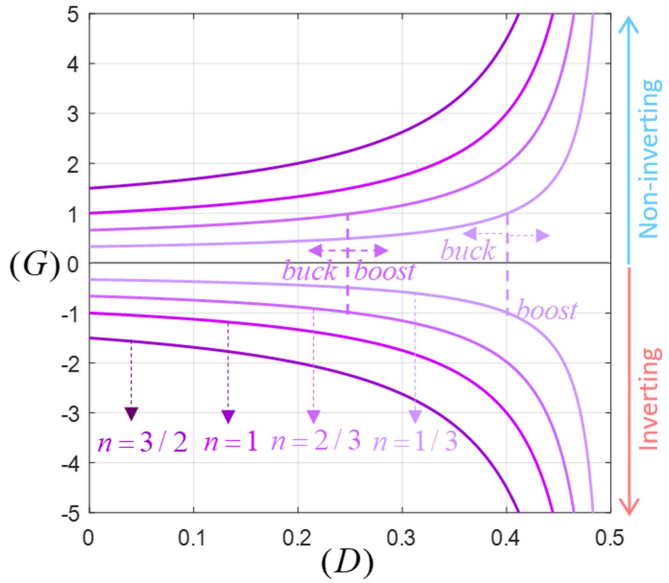

Fig. 4. Voltage gain versus duty cycle curves for four different HFT turn ratios.

For other states, the voltage gain can be derived similarly. In Table II, the voltage gain determination for three output frequencies is revealed. The voltage gain curves of the proposed converter for both positive voltage gain values (noninverting) and negative voltage gain values (inverting) are plotted in Fig. 4.

III. SELECTION OF SEMICONDUCTORS, DESIGN OF PASSIVE COMPONENTS, AND EFFICIENCY CALCULATION

A. Semiconductor Selection

The peak voltage across the switches and diodes and the peak current through them are required to select these devices. Therefore, the maximum voltage stresses of semiconductors are given in the following in terms of D, n, and $V_{i\text{-}rms}$:

$$\begin{cases} V_{SP-SN} = \frac{\sqrt{2}}{1-2D}V_{i-rms} \\ V_{S1-S2} = \frac{2\sqrt{2}n(1-D)}{1-2D}V_{i-rms} \\ V_{D1P,N} = -\frac{\sqrt{2}(2-3D)}{1-2D}V_{i-rms} \\ V_{D2P,N} = -\frac{\sqrt{2}}{1-2D}V_{i-rms} \\ V_{D1-D4} = -\frac{2\sqrt{2}n(1-D)}{1-2D}V_{i-rms} \end{cases}. \tag{20}$$

Then, the maximum current stresses of semiconductors are summarized in Table I in terms of D, n, P_O, and $V_{i\text{-}rms}$.

B. Passive Component Design

The inductor's required value is calculated based on

$$L = \frac{|V_L|\,\Delta t}{\Delta I_L}. \tag{21}$$

The voltage applied to the inductor during Δt interval is denoted by $|V_L|$. Δt is considered as DT_S. The maximum allowable current ripple, ΔI_L, is determined to be $x_L\%$ of the peak current value passing through the inductor ($\Delta I_L = x_L\% I_{L-peak}$) which is provided in Table I. Therefore, the required inductance value of the proposed converter can be determined by

$$\begin{cases} L_{1P,N} - L_{2P,N} \geq \frac{D(1-D)}{1-2D}\frac{V_{i-rms}^2}{x_L\% f_S P_o} \\ L_m \geq \frac{D(1-D)^2}{(1-2D)^2}\frac{V_{i-rms}^2}{x_L\% f_S P_o} \end{cases}. \tag{22}$$

The capacitor's required value can be derived as follows:

$$C = \frac{|I_C|\,\Delta t}{\Delta V_C} \tag{23}$$

where $|I_C|$ is the current flowing through the capacitor during $\Delta t = DT_S$, ΔV_C denotes the maximum allowable voltage ripple, as $\Delta V_C = x_C\%V_C$ and V_C is the peak voltage value of capacitor, which can be calculated using (9) and (19). So, the requirement of capacitors can be obtained as follows:

$$\begin{cases} C_{1P,N} - C_{2P,N} \geq (1-2D)\frac{P_o}{x_C\%f_S V_{i-rms}^2} \\ C_{3P,N} \geq \frac{(1-2D)^2}{1-D}\frac{P_o}{x_C\%f_S V_{i-rms}^2} \end{cases}. \tag{24}$$

The maximum permitted ripple of the output filter capacitor is shown in the following equation:

$$\Delta V_{Cf} = x_C\%V_o = x_C\%\frac{\sqrt{2}n\,(1-D)}{1-2D}V_{i-rms}. \tag{25}$$

The designed value of output capacitance is as regards

$$C_f \geq \frac{(1-2D)^2}{n^2(1-D)}\frac{P_o}{x_C\%f_S V_{i-rms}^2}. \tag{26}$$

C. Calculation of Loss and Efficiency

The converter's efficiency can be expressed in the form

$$\eta = \frac{P_o}{P_o + P_{Loss}}. \tag{27}$$

P_{Loss} is comprised of conduction loss (P_{cond}), switching loss, and core loss (P_{fe}). So, this can be written as follows:

$$P_{Loss} = P_{cond} + P_{switching} + P_{fe}. \tag{28}$$

The voltage and current ripples of the inductors and capacitors are neglected. If r_L signifies the resistance of inductors and HFT winding, r_C specifies capacitors ESR, r_S denotes switches conduction resistance, and V_F denotes the forward voltage of diodes, then P_{cond} can be represented as follows:

$$\begin{aligned} P_{cond} &= P_{cond,L} + P_{cond,C} + P_{cond,S} + P_{cond,D} \\ &= (r_L I_{L-rms}^2) + (r_C I_{C-rms}^2) + (r_S I_{S-rms}^2) \\ &\quad + (V_F I_{D-avg}). \end{aligned} \tag{29}$$

The RMS and average current values are calculated for a line period which are presented in Table I.

The switching losses of high-frequency PWM switches when they are turned ON and OFF which involves two switches S_P and S_N can be defined as follows:

$$P_{switching} = \frac{1}{6}V_{S-rms}I_{S-rms}f_s\,(t_r + t_f) \tag{30}$$

where f_s is the S_P and S_N switching frequency, t_r is the turning-ON cross-over time, and t_f is the turning-OFF cross-over time.

Core loss is defined as follows:

$$P_{fe} = k_{fe}B_{\max}^{\beta}A_C l_m \tag{31}$$

the core loss coefficient is K_{fe}, the peak ac flux density is $B_{\max}$, and the core loss exponent constant is β. l_m is the magnetic path length, and A_C is the core cross-section area [30]. The proposed converter's power loss curves are depicted in Fig. 5 in terms of the duty cycle and HFT turn ratio in order to clarify their effects on the power loss of the proposed converter.

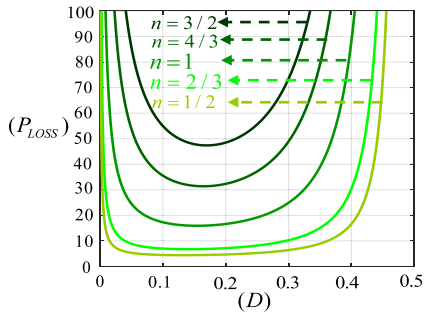

Fig. 5. Power loss versus duty cycle curves for different HFT turn ratios.

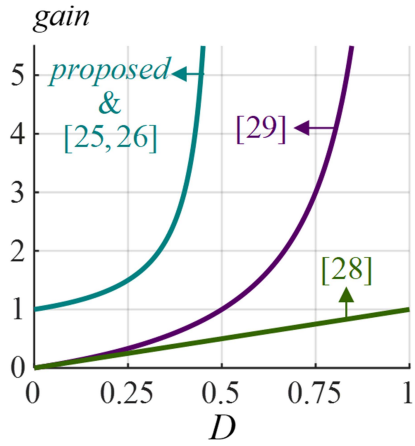

Fig. 6. Voltage gain comparison of the proposed converter with other HFI AC–AC converters.

IV. Comparative Analysis

The proposed converter and other isolated ac–ac converters have been compared in several factors, and the outcomes are outlined in Table III. The main advantages of the proposed converter over the most recent HFI variable frequency ac–ac converters of [28], [29] are that it provides a higher voltage gain along with the step-changed frequency operation only with the total number of four unidirectional switches. In [21], by choosing a certain value for n, a certain output voltage is determined. This voltage gain is not flexible because there is no freedom degree as a duty cycle to adjust the output voltage. Due to the existence of a Z-source network in the HFI ac–ac converters of [25], [26], they provide the same voltage gain as the proposed converter. However, they cannot provide identical bipolar voltage gain and variable frequency. The voltage gain curves of the proposed converter and other HFI ac–ac converters in noninverting mode and $n = 1$ are plotted in Fig. 6. As can be seen, [28] and [29] demand a greater duty cycle for a given voltage gain. Raising the duty cycle to generate greater voltages, increases the conduction loss, and both voltage stresses and current stresses on semiconductors. The simulations of the proposed converter and the most recent variable-frequency converters have been performed to verify the comparison in terms of total harmonic distortion (THD). All the results are summarized in Table IV. The proposed converters' improved input current THD values are due to the continuous sinusoidal input current waveforms. Whereas the input current of other converters such as the [28], [18], and [20] is discontinuous or quasi-continuous.

TABLE III
COMPARISON OF THE PROPOSED CONVERTER WITH OTHER ISOLATED AC–AC CONVERTERS

References	[21]	[25, 26]	[28]	[29]	Proposed
Voltage gain	$\pm n$	$\frac{n(1-D)}{1-2D}$	$\pm nD$	$\pm\frac{nD}{1-D}$	$\pm\frac{n(1-D)}{1-2D}$
Symmetrical bipolar operation	Yes	No	Yes	Yes	Yes
Buck-boost operations	Buck or boost	Buck-boost	buck	Buck-boost	Buck-boost
Transformer type	LF	HF	HF	HF	HF
Input current	Continuous	Continuous	Discontinuous	Continuous	Continuous
Step-changed frequency operation	Yes	No	Yes	Yes	Yes
Inherent commutation	Yes	No	No	No	Yes
Additional commutation strategy	No	Yes	Yes	Yes	No
Number of high-frequency switches	2	6	6	8	2

TABLE IV
COMPARISON OF THE PROPOSED CONVERTER THD VALUES WITH OTHER VARIABLE-FREQUENCY AC–AC CONVERTERS BASED ON SIMULATION RESULTS

		THD of V_o						THD of I_{in}					
		25 Hz		50 Hz		100 Hz		25 Hz		50 Hz		100 Hz	
		Buck	Boost	Buck	Boost	Buck	Boost	Buck	Boost	Buck	Boost	Buck	Boost
HFI variable frequency converters	[Proposed]	62.99%	62.94%	2.17%	2.15%	62.71%	62.6%	3.39%	3.18%	3.35%	3.16%	7.04%	5.85%
	[28]	63.05%	-	1.82%	-	65.47%	-	14.1%	-	3.58%	-	18.11%	-
	[29]	62.54%	62.5%	0.52%	0.61%	60.84%	59.71%	4.32%	4.72%	3.93%	3.7%	5.76%	6.49%
Non isolated variable frequency converters	[18]	58.61%	59.71%	5.28%	4.41%	60.73%	62.92%	10.41%	12.34%	10.38%	12.21%	22.04%	30.12%
	[19]	61.02%	59.7%	1.79%	3.4%	63.51%	64.55%	2.36%	3.5%	2.35%	4.23%	34.55%	54.89%
	[20]	62.43%	62.45%	1.04%	1.46%	63.66%	64.02%	5.04%	2.52%	5.05%	2.12%	4.96%	14.94%

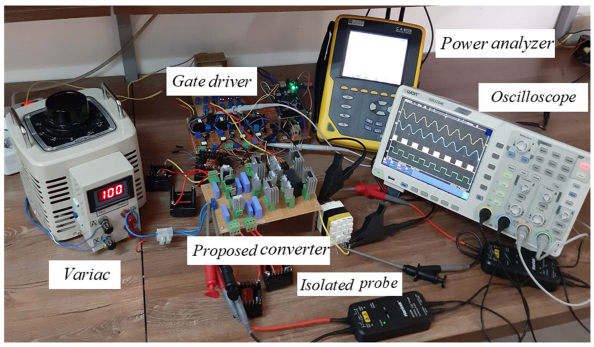

Fig. 7. Laboratory prototype of the proposed converter.

V. EXPERIMENTAL RESULTS

A prototype of the proposed converter, as illustrated in Fig. 7, is installed in the laboratory. The proposed converter is examined on the occasion that $V_{i\text{-}rms} = 100, f_i = 50$ Hz, $n = 1, D = 0.25$, and $R = 110$. In this case, the output voltage will be regulated to 150 V_{rms}. The switching frequency is 100 kHz. With the help of relationships (22)–(26), the required values for the converter parameters are chosen as $C_{1P,N\text{-}2P,N\text{-}3P,N} = 2.2\mu$F, $C_f = 0.5\mu$F, $L_{1P,N\text{-}2P,N} = 800\mu$H, and $L_m = 400\mu$H.

The waveforms of the output voltage, output current, input voltage, and input current for three output frequencies, including 50 Hz, stepped up 100 Hz, and stepped down 25 Hz are illustrated in Fig. 8 to validate the experimental outcomes for step-changed frequency operation. As demonstrated in Fig. 8, the measured peak value of the output voltage for all three different output frequencies is $V_{o\text{-}peak} = 202$ V which agrees with the calculated value of $V_{o\text{-}peak} = 212$ V when $V_{i\text{-}peak} = 142$ V with $D = 0.25$ by voltage gain equation given in (10), proving appropriate accordance between the experimental and theoretical results in terms of voltage gain. The voltage stress waveforms of the capacitors, switches, and diodes are shown in Fig. 9 for a 50 Hz output frequency. These voltage stress waveforms clearly reveal that there are no spikes in the circuit operation, as it was foreseeable due to the inherent commutation capability of the proposed converter. The prototype of the proposed converter is exposed to the R-L load in order to evaluate how the topology performs under a nonresistive load. The output load is determined to be $R = 110\ \Omega$ and $L = 100$ mH. Both input and output waveforms are depicted in Fig. 10.

Fig. 11 depicts the input and output waveforms for $f_o = 50$ Hz as the load resistor steps down from 150Ω to 70Ω. Due to the absence of spikes, the proposed converter entirely retains its safe commutation ability when it undergoes a load transition. The quality evaluation via THD is measured by a power analyzer and Table V contains the results. Eventually, the measured THD values occurring within the permitted range, the output voltages being symmetric, and the sinusoidal input current for different output frequencies, which are shown in Table V and Fig. 8, respectively, confirm the good quality of waveforms. This clearly demonstrates the great performance of the proposed converter. Fig. 12(a) depicts the efficiency curves of the proposed converter and other HFI ac–ac converters in the same circumstance of constant input voltage, $f_o = 50$ Hz, and fixed load for varying output power. The switching loss increases as the number of switching devices grows. The proposed converter has fewer switches than any of the recently investigated HFI ac–ac converters. Furthermore, a lower duty cycle requirement for creating the same output power results in less conduction loss of components. Fig. 12(b) provides power loss distribution for $P_o = 204.5$ W.

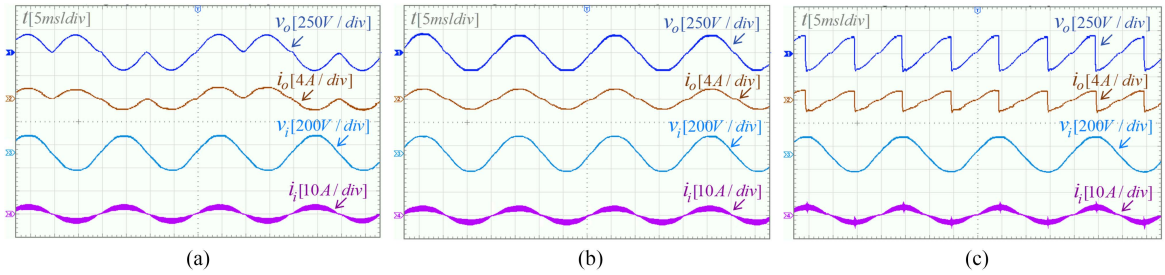

Fig. 8. Experimental results of output voltage, output current, input voltage, and input current waveforms. (a) For $f_o = 25$ Hz. (b) For $f_o = 50$ Hz. (c) For $f_o = 100$ Hz.

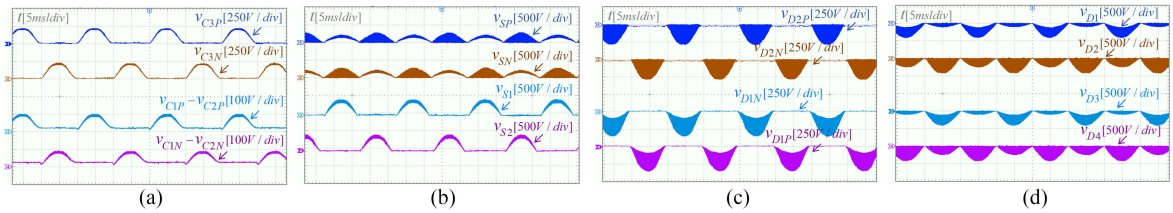

Fig. 9. Experimental results of voltage stress waveforms. (a) On the capacitors. (b) On the switches. (c) and (d) On the diodes.

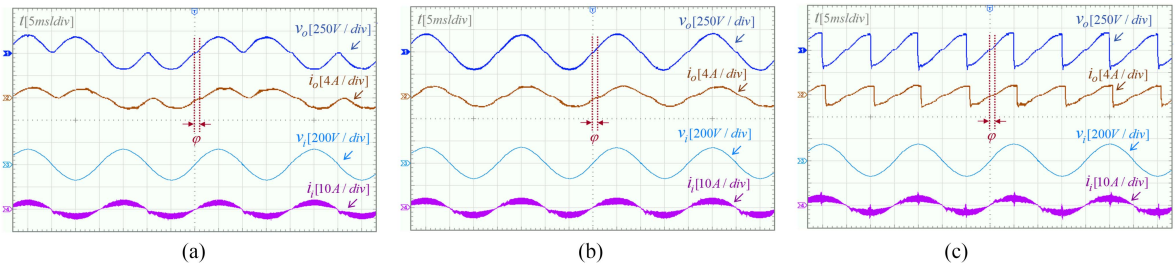

Fig. 10. Experimental results of output voltage, output current, input voltage, and input current waveforms under a nonresistive load (R-L load). (a) For $f_o = 25$ Hz. (b) For $f_o = 50$ Hz. (c) For $f_o = 100$ Hz.

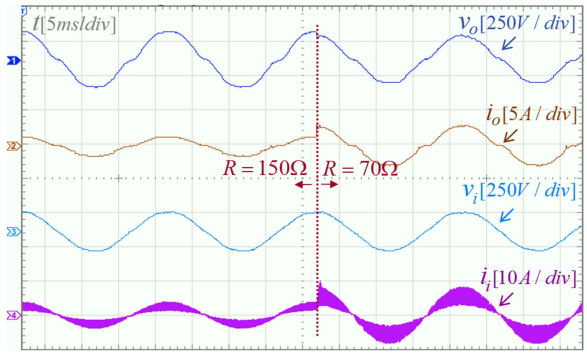

Fig. 11. Experimental results of output and input waveforms under a transient load from 150 to 70 Ω for $f_o = 50$ Hz.

TABLE V
MEASURED THD VALUES FOR THREE DIFFERENT OUTPUT FREQUENCIES

THD	25 Hz	50 Hz	100 Hz
THD of i_i	3.6%	3.57%	5.97%
THD of v_o	63.3%	2.38%	62.85%

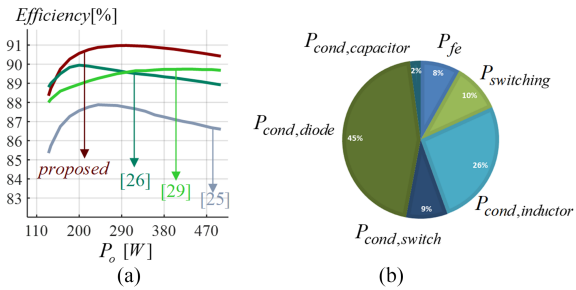

Fig. 12. Efficiency evaluation of the proposed converter. (a) For varying output power in comparison to other HFI AC–AC converters. (b) Power loss distribution of the proposed converter for the output power of $P_o = 204.5$ W.

VI. CONCLUSION

In this article, an HFI four-switch single-phase quasi-Z-source ac–ac converter has been proposed. Along with the duty cycle, the transformer turn ratio adds another freedom degree to generate a wide range of output voltage. The proposed converter also eliminates the output H-bridge and just needs two unidirectional switches to change the frequency. The proposed converter, in contrast to other existing HFI converters, does not face commutation problems. This inherent commutation capability is clearly visible in the experimental waveforms of the switches without spikes. Moreover, a continuous input current has potentially been provided. The accuracy of theoretical claims has been demonstrated by a laboratory prototype.

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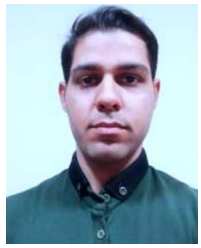

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