A Compact Model Extending the BSIM3 Model for Silicon Carbide Power MOSFETs

Lixi Yan, Kanuj Sharma, and Ingmar Kallfass

***Abstract*—This article presents an approach adopting and extending the industry-standard BSIM3 model with necessary extensions to build an accurate compact model for 1.2-kV silicon carbide (SiC) power MOSFETs. The BSIM3 model is adopted to describe the controlled channel part of the power MOSFETs. Compared with the models provided by the device vendors, the standard model shows higher fidelity in the simulation. Considering the vertical MOSFET structure and the special properties of SiC, the proposed model extensions include the thermal drift region, the body diode, and the drain–gate capacitance. The pulsed current–voltage characteristics considering the thermal effects, the voltage-dependent capacitance, and the transient behavior of the body diode are measured and serve as the reference for the model parameter extraction. The specific parameter extraction strategy is provided. The method is exemplified on different commercially available SiC power MOSFETs. Finally, the model is validated through the comparison of measured and modeled switching loss energy and switching transitions from a double-pulse test at 600 V and different load current levels up to 26 A and temperatures up to 90 °C.**

***Index Terms*—BSIM3, characterization, modeling, power MOSFET, silicon carbide (SiC).**

I. Introduction

POWER transistors based on wide-bandgap semiconductors are essential to the required miniaturization of high-efficiency switched-mode power converters. Silicon carbide (SiC) is one of the most promising candidates among all the wide-bandgap semiconductor materials [1], [2], which enable power devices to operate at higher switching frequencies and higher temperatures compared to conventional silicon devices [3]. Power MOSFETs are the most commonly used power devices due to their low gate drive power, small device size, fast switching speed, and superior paralleling capability. Therefore, there is a continuously increasing need for accurate and compact models for SiC power MOSFETs, which can be used for device evaluation, circuit design, and system behavior prediction.

For circuit-level-oriented models, some studies are carried out for vertical SiC power MOSFETs. The model proposed by McNutt et al. [4] is considered as the pioneering work in the field of SiC power MOSFET modeling. They provided a physics-based model with a unique channel current expression, which includes the formulation of the lower gate voltage as well as the enhanced linear region transconductance. In the past 20 years, several SiC MOSFET models have been published; Mantooth et al. [3] reviewed these models in detail and categorized them into five levels based on the model complexity . In recent years, there has also been some new modeling methods that involve machine learning, e.g., Lee et al. [5] have presented an equivalent circuit simulation behavior model for SiC MOSFETs based on a neural network. However, currently, there is still a lack of accurate and convergence-robust industry-standard models for vertical SiC power MOSFETs. On the other hand, such standard models exist already for CMOS logic devices, like the BSIM family models, which are proven to be highly accurate and robust. However, these standard models cannot be directly applied for power MOSFETs, since the device structure of vertical power MOSFETs is typically very different from standard lateral CMOS or even LDMOS-type transistors for logic/signal processing. Also, there does not exist precise definition in the standard CMOS models for the specific structures such as the drift region or the body diode, which play significant roles in power MOSFETs.

Moreover, models provided by device manufacturers and vendors often contain some deficiencies, e.g., do not describe enough nonlinear effects such as voltage dependent capacitance (C-V) and transient performance like reverse recovery. To the best of the authors' knowledge, currently, there exist no vendor models that are able to describe the transient reverse recovery performance for SiC power MOSFETs under different operating conditions with deviation below 15%, and our simulation result with vendor models shows that, in many cases, the deviation is even higher than 20%. The lack of precise definition for these effects would cause an underestimation of the device power loss in the simulation, and some electromagnetic compatibility issues cannot be predicted accurately. Especially, with the increase in switching frequency and power density of state-of-the-art power electronic circuits, accurate simulations are becoming critical and necessary in the field of high-efficiency and compact electronic design.

Furthermore, the customized vendor models are typically implemented as custom SPICE netlists, which are often not robust enough with respect to convergence. Therefore, a standard model is chosen as the model core, which is continuous, scalable, and computationally robust over different regions of operations and adapted it for vertical power SiC MOSFETs.

Manuscript received 12 April 2022; revised 30 July 2022 and 22 October 2022; accepted 13 December 2022. Date of publication 27 December 2022; date of current version 14 February 2023. Recommended for publication by Associate Editor K. Sheng. *(Corresponding author: Lixi Yan.)*

The authors are with the Institute of Robust Power Semiconductor Systems, University of Stuttgart, 70569 Stuttgart, Germany (e-mail: lixi.yan@ilh.uni-stuttgart.de; kanuj.sharma@ilh.uni-stuttgart.de; ingmar.kallfass@ilh.uni-stuttgart.de).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3232376.

Digital Object Identifier 10.1109/TPEL.2022.3232376

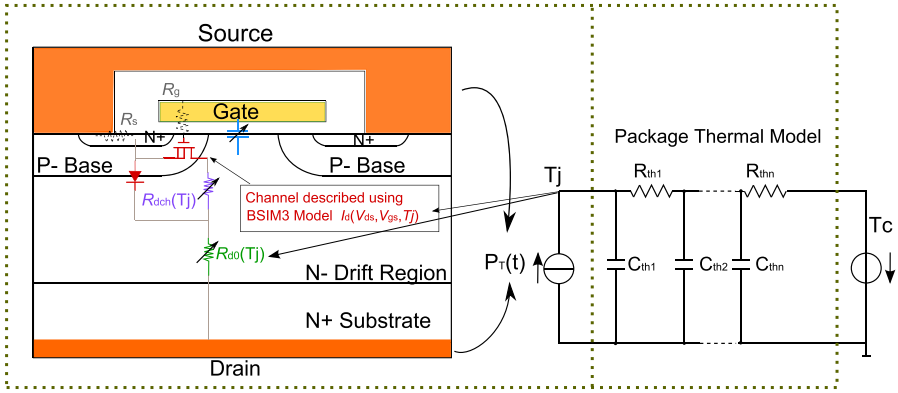

Fig. 1. Vertical power MOSFET structure with the connected thermal model based on power losses.

This article presents an approach to characterize SiC power MOSFETs and proposes a compact model derived from the BSIM3 model, which describes the static characteristics considering thermal effects, parasitic capacitance, and dynamic performance. Compared with the previous BSIM model versions, the BSIM3 model is more precise and more widely integrated in various simulation platforms. The later version models of the BSIM family, e.g., BSIM4, define more physical effects into the model expression; however, many of the expressions defined for CMOS devices are not necessarily applicable for power MOSFETs, and the complicated definition also involves more parameters, which increases the complexity of parameter extraction. Therefore, the BSIM3 model is selected here and adopted as the core channel model.

In our previous work, the extended BSIM3 model is successfully adapted for Si vertical power MOSFETs [6]. However, it is observed that the model extension method for Si power MOSFET, e.g., drift resistance, parasitic capacitance, and body diode, is not suitable for SiC power MOSFETs, because of their different material property and voltage classes in application [7], [8]. Therefore, in this article, the specific device properties of SiC power MOSFETs are analyzed, and the suitable model extension method is proposed. The detailed definition is explained in Section II.

In this article, the model parameters are extracted based on the device measurement, in order to obtain more detailed characteristics of the target device. The measurement equipment and methods are introduced in Section III for each characteristic. With the modeling method in this article, the deviation between the simulation and the measurement is below 4% for static characteristics and less than 10% for transient characteristics. The comparison between the performance of the model in this article and the previous method for Si devices as well as the vendor model is also shown in Section III. Although the tolerance of the product also needs to be taken into consideration, it needs to be noticed that the deficiencies in the model definition, which exist in many of the vendor models, fundamentally lead to their inability to accurately describe the device characteristics. These deficiencies cannot be compensated by adjusting the constant values, but by using a more appropriate definition method, as we introduced in this article.

II. Modeling Method

A. Drift Resistance

Similar to Si MOSFETs, the drift resistance coming from the low-doped epi-layer of SiC power MOSFETs for the current through the channel and body diode is different, because of their different current paths [9]; therefore, the drift resistance is defined containing two parts: the individual drift resistance R_{dch}, which is mainly contributed by the accumulation resistance and the JFET resistance [7] only related to the channel, and the common resistance R_{d0} coming from the deep drift region and the drain substrate region, which has the same influence on both the channel and the body diode, as shown in Fig. 1.

The wide-bandgap material property makes the drift region of SiC MOSFETs capable to be much shorter than that in Si MOSFETs for the same breakdown voltage. Consequently, for power transistors, SiC technology is mostly applied for high-voltage MOSFETs with a high breakdown voltage of more than 1 kV [8], [10]. With the increase in the device breakdown voltage, the relative contribution of the drift region resistance to the ON-resistance of power MOSFETs becomes higher [10]. Therefore, compared to Si MOSFETs, which are widely used in low-voltage applications under 100 V, the drift region of 1200-V SiC MOSFETs contributes a major percentage of the total ON-resistance of the device. The resistance contributed by the drift region is nonlinear voltage dependent, and it is observed that for SiC MOSFETs using a constant auxiliary resistance to describe the drift resistance of the body diode current path as introduced in [6] for Si power MOSFETs is not sufficient; therefore, an extra nonlinear resistance is required to describe this resistance.

To describe the nonlinear resistance, the following expression, which is introduced in the EKV-HV model [11], is used in this article:

$$R_{\mathrm{dch}} = R_{\mathrm{drift0}} \left[\frac{1 + \left(\frac{V_{\mathrm{drift}}}{V_{\mathrm{SAT,L}}} \right)^{\alpha_{\mathrm{vsat}}}}{1 + \theta_{\mathrm{acc}} \cdot |V_{\mathrm{gs}}|} \right]. \tag{1}$$

The parameter R_{drift0} is the initial constant drift resistance and V_{drift} is the voltage across the drift region. The parameters $V_{\mathrm{SAT,L}}$ and α_{vsat} are the velocity saturation parameters. In the original equation defined in [11], the parameter $V_{\mathrm{SAT,L}}$ is defined as a

drift-length-dependent variable, and here, it is simplified as a parameter. Since the planar channel structure is often used in SiC devices, the influence coming from the gate bias also needs to be taken into account. The parameter θ_{acc} in (1) is the gate bias modulation parameter (effect of accumulation charge sheet on drift resistance due to gate biasing) and V_{gs} is the applied gate voltage.

B. Parasitic Capacitance

Similar to Si power MOSFETs, the drain–gate capacitance in vertical SiC power MOSFETs has also the structure as the oxide capacitance between the gate and the drain in series with the depletion-layer capacitance under the gate oxide. However, in the measurement result of SiC power MOSFETs, which is shown in Section III, it is observed that in the low-V_{ds} region, there is a steep drop in the capacitance curve, which is more visible in logarithmic scale.

This phenomenon sometimes also appears in Si MOSFET devices but is inconspicuous and normally negligible in the capacitance model definition [12]. However, in SiC devices, the two-stage capacitance drop becomes nonnegligible. It can be induced by the ion implantation in the JFET region below the gate terminal [13]. Since the doping concentration in the JFET region is higher than that in the drift layer close to the drain side, the charging/discharging of the drain–gate capacitance is slower when the drain–gate voltage is lower than the JFET pinch-off voltage [14]. In the new generation of SiC MOSFETs, the trench structure is adopted to reduce the JFET effect; however, this phenomenon is still noticeable in SiC MOSFETs.

Moreover, the drain–gate capacitance of SiC MOSFETs may also be influenced by the transition layer at the interface of nonannealed SiC-SiO_2 [15], which causes surface roughness scattering [2]. The surface roughness scattering in Si is attributed to surface traps and residual unoxidized silicon particles at the interface. However, in SiC, the situation is more complex. SiC can be thermally oxidized in the same manner as silicon, except that the chemical reaction produces both SiO_2 and CO. During this process, there can also exist unoxidized carbon, and there is evidence for a transition layer at the interface, where the chemical composition changes gradually from pure SiC to pure SiO_2 over a distance of several nanometers [15]. The surface layer of the SiC also exhibits some structural disorders resulting from the oxidation process, and the first monolayers of SiO_2 contain excess carbon [15].

Considering these effects, the expression of the voltage-dependent capacitance between the gate and drain terminals of SiC MOSFETs is extended from the capacitance, which is used for Si power MOSFETs [6] and defined as

$$C_{\text{dg}} = C_{\text{dg}C0} + C_{\text{dg}0}\left(1 + C_q \cdot (V_{\text{dg}} - V_{fbgd})\right)^{-N_c} + C_{\text{dg}1}\left(1 + \tanh\left(\theta\left(V_{\text{dg}} - V_0\right)\right)\right). \quad (2)$$

The first term of expression (2) is a constant capacitance, which represents the bias-independent outer fringing capacitance. Since the SiC power MOSFETs are normally utilized in high-voltage application, the constant term is necessary to avoid the underestimation of the capacitance at high-V_{ds} bias caused by the V_{dg} dependence definition of the capacitance. The second term is a modified MOS capacitance model, which is constructed by the gate oxide capacitance in series with the semiconductor capacitance under the gate oxide. It is a physics-based definition, but considering that the process parameters may not be available to model users, the process-parameter-based calculated values in the original definition are replaced by empirical parameters. The detailed process of the derivation is discussed in [6]. This expression is successfully adapted to Si power MOSFETs but not sufficient to describe the steep drop in the low-V_{ds} region in the capacitance curve of SiC power MOSFETs, which is caused by the JFET effect and surface roughness scattering as analyzed before. The capacitance curves are shown in Section III-B. Therefore, an empirical extension is defined to describe the C_{dg} capacitance curve in the low-V_{ds} region, which is the third term in (2).

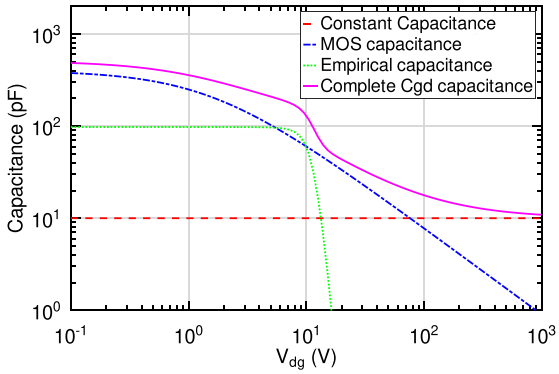

Fig. 2. Different terms defined in drain–source capacitance.

Fig. 2 shows the contributions of each term in (2). It can be noticed that the empirical term only effects the capacitance in the low-voltage region especially for the steep capacitance drop. With the increasing bias voltage, the capacitance is mainly defined by the physics-based fringing and MOS capacitance expression. Compared with a pure empirical capacitance definition, the advantage of the physics-based with empirical auxiliary definition is that it can not only ensure the accuracy of the device behavior in a certain region but also keeps the model prediction capability for a larger operating range, while the accuracy of a pure empirical definition is limited in the range of the available characterization result.

For the gate–source capacitance of SiC MOSFETs, a constant capacitance model is used, since it shows negligible V_{ds} dependence. The drain–source capacitance is dominated by the junction of the body diode, which is introduced in Section II-C in detail.

C. Body Diode

In the structure of vertical power MOSFETs, the p-n junction between the n+ source region and the p-base region is shorted by overlapping the source metal across the junction, as shown in Fig. 1, in order to suppress the parasitic BJT effect formed in the MOSFET structure [7]. This structure constructs a p-i-n SiC body diode for the reverse current [16]. In the BSIM3 model, there is a junction expression defined between the bulk and

drain terminals, but the drift resistance effect is not considered. Moreover, the thermal effects observed in SiC diodes are also different from that of Si devices. Therefore, for SiC MOSFET models, the junction diode definition defined in the BSIM3 model needs to be deactivated, and an extended body diode model is defined.

The static current of the body diode model can be defined by the Shockley diode equation. However, because of the wide bandgap of SiC material, the forward conduction voltage drop of SiC p-i-n diodes is higher than that of Si p-i-n diodes; therefore, the parameters need to be adapted for the SiC junction.

The capacitance of the body diode contains the depletion capacitance and diffusion capacitance of the junction. The depletion capacitance accounts for most of the junction capacitance when the junction is reverse biased, i.e., the MOSFET is forward biased. When the junction is forward biased, there is an additional contribution to the junction capacitance from the rearrangement of the stored charges in the neutral region, which is the diffusion capacitance [17]. These two capacitances together induce the reverse recovery phenomenon.

With the conventional definition for the diode capacitance in the SPICE model [18], the reverse recovery at a relatively low current level can be fitted; however, at higher currents, a deviation appears between the simulation and the measurement of the reverse recovery current, because in the high injection case, the conventional SPICE diode model is not able to describe the diffusion capacitance accurately [12]. Therefore, to precisely describe the reverse recovery behavior of SiC power MOSFETs, a more accurate model that can correctly predict the stored charge behavior during the transient, especially for the diffusion capacitance, is required.

The simple stored charged model [19] is successfully utilized for Si power MOSFETs in our previous work [12]. The charge definition is defined as a lumped unit in the simple charge control model; however, it is realized that this simplification is not suitable for the SiC body diode. Therefore, in this article, the charge distribution model with the three-point lumped charge method [20] is used for a more detailed and precise definition.

The equations of the lumped-charge-based analytical model are derived from simplified fundamental device physics equations using the nodal arrangement and transformed into lumped charge equations [20], [21], [22].

Different from the simple stored charge model, which defines all the carrier charge at one internal node, in the lumped-charge-based analytical model, five critical regions are defined, and the total charge in each region is lumped into the corresponding node. One charge node is defined individually in the heavily doped p+ and n+ regions, as shown in Fig. 3 [20]. For the lightly doped n region, three nodes are defined. Nodes 2 and 4 are connection nodes and node 3 is the charge storage node.

In the lumped-charge-based analytical model, the electron and hole charges are considered separately. For the drift region nodes, the current-transport equations are defined as [22]

$$i_{p(i,i+1)} = \frac{q_{p(i)} - q_{p(i+1)}}{T_p} + \frac{q_{p(i+1)}}{2T_p} \cdot \frac{V_{(i,i+1)}}{v_t} \tag{3}$$

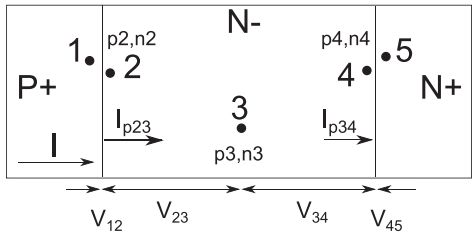

Fig. 3. Lumped charge node distribution in the body diode structure [20].

$$i_{n(i,i+1)} = \frac{q_{n(i)} - q_{n(i+1)}}{T_n} + \frac{q_{n(i+1)}}{2T_n} \cdot \frac{V_{(i,i+1)}}{v_t}. \tag{4}$$

The current continuity equation for the stored charge node is defined as [21], [22]

$$i_{p(i-1,i)} - i_{p(i,i+1)} = \frac{q_{p(i)} - Q_{p0}}{\tau_i} + \frac{dq_{p(i)}}{dt}. \tag{5}$$

The charge neutrality equations are defined as [21]

$$q_{n(i)} = Q_B + q_{p(i)}. \tag{6}$$

Together with the junction equation (Boltzmann relations), these equations above are summarized as the fundamental device equations describing the carrier distribution and transportation between the charge nodes in the device.

Finally, for the terminal voltage and current constraints [Kirchhoff's circuit law (KVL) and Kirchhoff's current law (KCL)], we have

$$V = \sum_{i=1}^{i=n-1} V_{(i,i+1)} \tag{7}$$

$$I = \sum_{i=1}^{i=n-1} i_{n(i,i+1)} = \sum_{i=1}^{i=n-1} i_{p(i,i+1)}. \tag{8}$$

The KVL and KCL equations connect internal variables of the model equation to the device terminal current and voltage.

The lumped charge model is implemented as a voltage-controlled current source and placed in parallel to the channel described by the BSIM3 model, as shown in Fig. 1. The junction diode definition defined in the BSIM3 model is deactivated.

Compared with the simple stored charge model, the lumped-charge-based analytical model has a more detailed definition for the stored charge distribution, which makes the model more flexible and accurate but also more complex. The complicated definition and increased number of model parameters can lead to some potential convergence problems and increase the parameter extraction complexity.

D. Thermal Behavior

The resistivity of SiC MOSFETs also mainly depends on the carrier density and the carrier mobility. However, different from Si, in SiC material (4H-SiC) with typical doping concentration ($1 \times 10^{15} \sim 1 \times 10^{17}\text{cm}^{-3}$), the thermal influence to the carrier concentration is nonnegligible in the operating temperature range (200–450 K) [2]. The carrier density increases with increasing temperature, while the carrier mobility decreases with

increasing temperature. The temperature effects to the carrier mobility and the carrier density together influence the ON-state resistance of SiC MOSFETs, which cause the resistance not to monotonically increase with temperature like in the Si MOSFET case.

An empirical second-order temperature effect model, as shown in (9) [23], is used for both the channel and the common drift resistance definition. The variable $T_{\rm j}$ is the device junction temperature, T_0 is the reference temperature, and $R_{\rm drift}(T_0)$ is the drift resistance at the reference temperature T_0. The parameters α and β are the first- and second-order temperature coefficients of resistance. This model is successfully utilized for Si devices in our previous work [6], but for SiC MOSFETs, the thermal model parameters need to be defined differently, and the results are shown in Section III

$$R_{\rm drift}(T) = R_{\rm drift}(T_0)\left[1+\alpha\left(T-T_0\right)+\beta\left(T-T_0\right)^2\right]. \quad (9)$$

The temperature dependence of the carrier mobility and concentration in the SiC body diode is also different from that in Si diodes. In order to decrease the model complexity and to obtain correct simulation results, the temperature-dependent saturation current of the body diode is defined in (10), which is simplified from [24]. In this expression, $I_{\rm satSiC0}$ is the saturation current and TempE is the temperature coefficient

$$I_{\rm satSiC}(T) = \left(1+{\rm TempE}\left(\frac{T}{T_0}-1\right)\right)\cdot I_{\rm satSiC0}. \quad (10)$$

To represent the dynamically changing junction temperature during the device operation, the dynamic thermal model [6] is adopted in this article. In this method, the junction temperature $T_{\rm j}$ is modified from a system parameter to a variable and implemented as a voltage node, as shown in Fig. 1. The voltage at node $T_{\rm j}$ is calculated based on the power loss of the intrinsic device at each time step during the simulation and can communicate with the package thermal model. The thermal model of the package is built based on the definition provided by the device vendor. $T_{\rm c}$ is the case temperature at the surface of the device package.

III. Device Characterization and Parameter Extraction

A. I–V Characteristics

In this article, the model parameters are extracted based on the measurement of commercially available SiC MOSFETs.

The measurement of the I–V characteristics is carried out with the Keysight curve tracer B1505A at different case temperatures. Fig. 4 shows the comparison of the measured and simulated output characteristic at room temperature of the 1200-V 36-A SiC power MOSFET C2M0080120D [25]. It shows that the extended BSIM3 model with the proposed extension methods for SiC MOSFETs is able to describe the I–V characteristics of the target device accurately. With the external nonlinear drift resistance definition, the transition from the linear regime to the saturation regime in the output characteristics of the SiC device can be correctly depicted. Moreover, the current saturation tendency at high $V_{\rm gs}$ values is also precisely described.

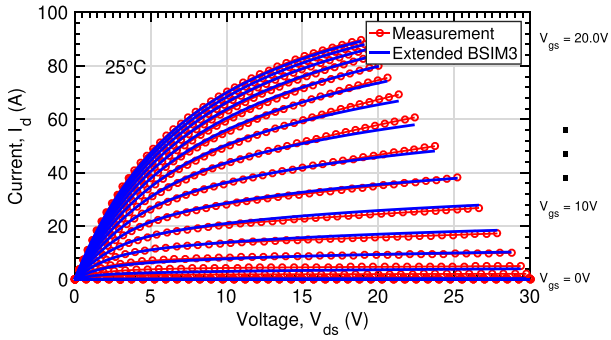

Fig. 4. Output characteristics of the 1200-V SiC mosfet C2M0080120D.

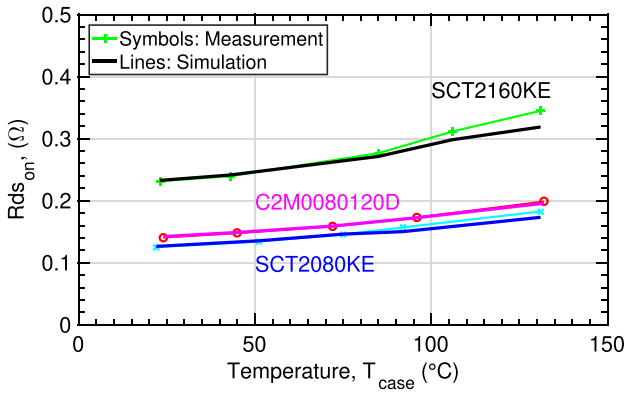

Fig. 5. ON-state resistance of three different 1200-V SiC MOSFETs when $V_{\rm gs}$ is at 20 V.

To evaluate the general applicability of the proposed model for various SiC MOSFET process technologies, two more devices with different current levels and from different vendors are selected here for parameter extraction. Here, the 1200-V 40-A SCT2080KE [26], which has a similar current level but is from a different manufacturer, and the 1200-V 22-A SCT2160KE [27], which has higher ON-state resistance and lower current level, are selected as the target devices for the verification and comparison of the proposed model. The C2M0080120D has a planar gate structure, while the SCT2080KE and SCT2160KE are with a trench gate structure. Different gate process techniques can influence the ON-state resistance and the parasitic capacitance characteristics. The ability of the model to describe the devices with different process technologies is checked in the following by using the proposed model to fit different devices.

The thermal effects play a significant role in the device performance of power MOSFETs. The temperature-dependent parameters are extracted based on the I–V measurement at different case temperatures. To make a clear and more precise comparison, instead of plotting the I–V curves of each device at different case temperatures, Fig. 5 shows the comparison of the simulated and measured ON-state resistances of the three selected devices when $V_{\rm ds}$ is 10 V and $V_{\rm gs}$ is 20 V. In this figure, we can observe that the devices C2M0080120D and SCT2080KE have similar application range and, therefore, very close ON-state resistance at the same operation points. At the same bias voltage, the device SCT1260KE, which works in a

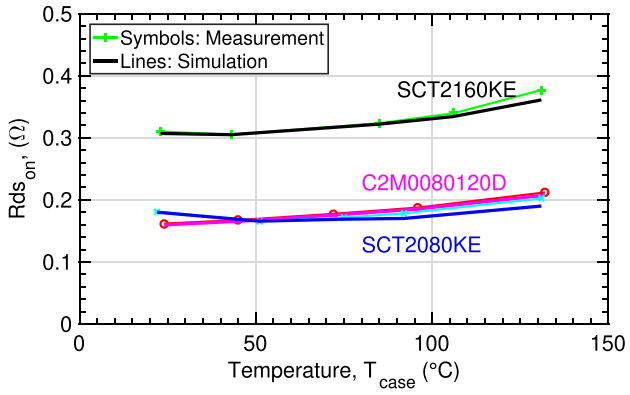

Fig. 6. ON-state resistance of three different 1200-V SiC MOSFETs when V_{gs} is at 16 V.

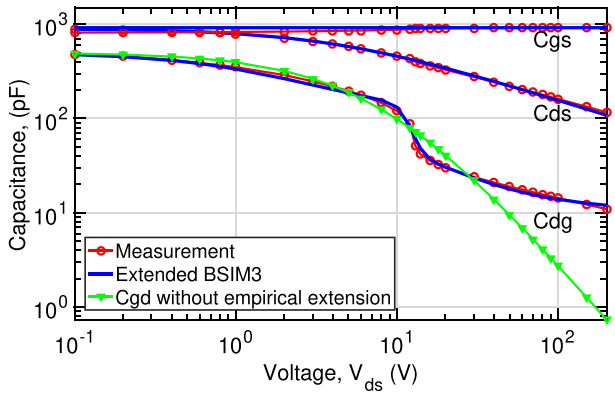

Fig. 7. C–V characteristics of the 1200-V SiC MOSFET C2M0080120D with and without empirical expression in the double logarithmic scale.

lower current range, has relatively higher ON-state resistance. Furthermore, the ON-state resistance of all the three selected devices increases with the case temperature at this bias voltage condition. These behaviors are able to be described accurately by the proposed extended BSIM3 model.

As analyzed in Section II, the thermal effect on the resistance of SiC MOSFETs is a combination of the temperature-dependent carrier density and the carrier mobility during the temperature profile in the application. Therefore, different from Si devices, the resistance of SiC devices is not monotonically increasing with the temperature over the operation range. Moreover, the tendency also varies with different process technologies. This behavior can be more clearly observed with lower V_{gs} bias. Fig. 6 shows the simulated and measured ON-state resistances of the three selected devices when the gate bias voltage is 16 V. It can be observed that the lowest R_{dson} point of the Rohm devices SCT2080KE and SCT1260KE is at around 45 °C, which is not the lowest temperature point in the measured range, while R_{dson} of the Cree device C2M0080120D monotonically increases with the temperature. This difference can be caused by the device process technology, since the SCT2080KE and SCT1260KE have a trench gate structure and the C2M0080120D is with a planar gate structure.

In general, the temperature dependence of the ON-state resistance of SiC MOSFETs is complicated and depends on the combination of multiple factors, but it still follows the power function tendency, and the simulation results in Figs. 5 and 6 show that the thermal definition introduced in Section II is able to depict the dynamic temperature dependence precisely.

For the static I–V characteristics, the root-mean-square deviation (RMSD) between the measurement and the simulation result is less than 4% for all the compared devices in this article, which is better than the conventional requirement.

B. C–V Characteristics

One of the significant advantages of SiC power MOSFETs is the high switching speed. For the switching performance, the parasitic capacitance plays a critical role. Similar to Si devices, the gate–source parasitic capacitance of SiC power MOSFETs has little V_{ds} dependence, and the voltage dependence of the drain–source capacitance for the forward bias V_{ds} condition is also similar to Si devices. However, the capacitance between the gate and drain terminals, especially in the low-V_{ds} region of SiC MOSFETs, is special because of the JFET region and the oxidation process of the SiO_2. For the capacitance characterization, the two-port S-parameter measurement method is used in this article to avoid the frequency dependence, which may appear in measurements [6].

As mentioned in Section II-B, the characteristic of the capacitance between the drain and gate terminals of SiC power MOSFETs is different from that of Si power MOSFETs. Fig. 7 shows the comparison of the capacitance between the measurement and the simulation with and without the empirical supplementary definition for the drain–gate capacitance.

It can be observed that there exists a nonnegligible steep drop in the C_{dg} curve, which cannot be described by the MOS capacitance model. It signifies that the MOS capacitance model for Si devices is insufficient for the SiC drain–gate capacitance, and the modification of the MOS capacitance model is necessary.

Considering the SiC MOSFET condition, based on the MOS capacitance model, an additional empirical expression is introduced in (2), as explained in Section II. Fig. 7 shows that with the empirical expression the accuracy of the drain-gate capacitance model is increased, especially for the region where the capacitance steeply decreases with increasing V_{ds} (10 to 20 V).

The steep drop tendency and the voltage dependence of the drain–gate capacitance for different processing technologies can differ from each other. Fig. 8 shows the parameter extraction result of the trench gate MOSFET SCT2080KE. It can be observed that because of the trench structure, the influence coming from the differently doped JFET region to the drain–gate capacitance of the SCT2080KE declines.

The fitting result illustrates that the proposed model is able to describe various process technologies accurately. The RMSD between the measurement and the simulation result can be lower than 5% for all the compared devices in this article.

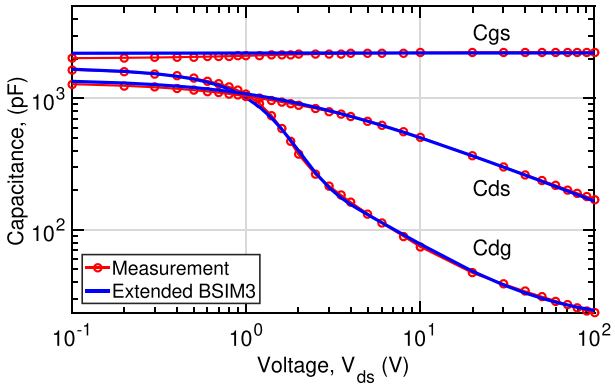

Fig. 8. C–V characteristics of the 1200-V SiC MOSFET SCT2080KE with empirical expression in the double logarithmic scale.

C. Reverse Characteristics of the Body Diode

The reverse behavior of SiC MOSFETs is different from that of Si devices because of the SiC body diode property, especially regarding the thermal effects.

In the static reverse characterization, the reverse current of the C2M0080120D is measured with the curve tracer B1505A at room temperature of 24 °C, when V_{gs} sweeps from −8 to 2 V with 1-V steps. It can be observed that there is still current flowing through the channel when the bias voltage V_{gs} is at 2 V or at even negative values. The channel is closed when V_{gs} is lower than −4 V, which is much lower than the threshold voltage for the forward current in the first quadrant of the output characteristics. It is caused by the body-effect phenomenon, which can be defined by the BSIM3 model for the channel [12].

Regarding the thermal effects, the measurement for the reverse current through the body diode of the target device is carried out at different case temperatures. To ensure that the current only flows through the body diode, V_{gs} is kept at −8 V, at which the channel is closed.

Fig. 9(a) shows the simulated and measured reverse current when V_{gs} sweeps from −8 to 2 V at room temperature. The asymmetric channel performance [12] can be described correctly as shown in the parameter extraction result. Some deviation appears at the high current region, when there is current flowing through both the channel and the body diode, which can still be improved by a more considerate definition of the body effect to the channel. However, considering the model complexity, the BSIM3 definition is used for the body effect.

Fig. 9(b) shows the reverse current flowing through the body diode at different case temperatures, while the channel is in OFF-state with −8 V gate bias. The comparison between the measurement and the simulation indicates that the modified temperature effect model for the SiC body diode is able to fit the device dynamic thermal performance well.

To characterize the transient reverse recovery behavior of the body diode in SiC MOSFETs, a group of double-pulse tests (DPTs) is carried out with the Cree (Wolfspeed) SiC evaluation board KIT8020-CRD-8FF1217P-1. In the DPT setup, the same DUTs are used for both the high and low sides, while the high-side

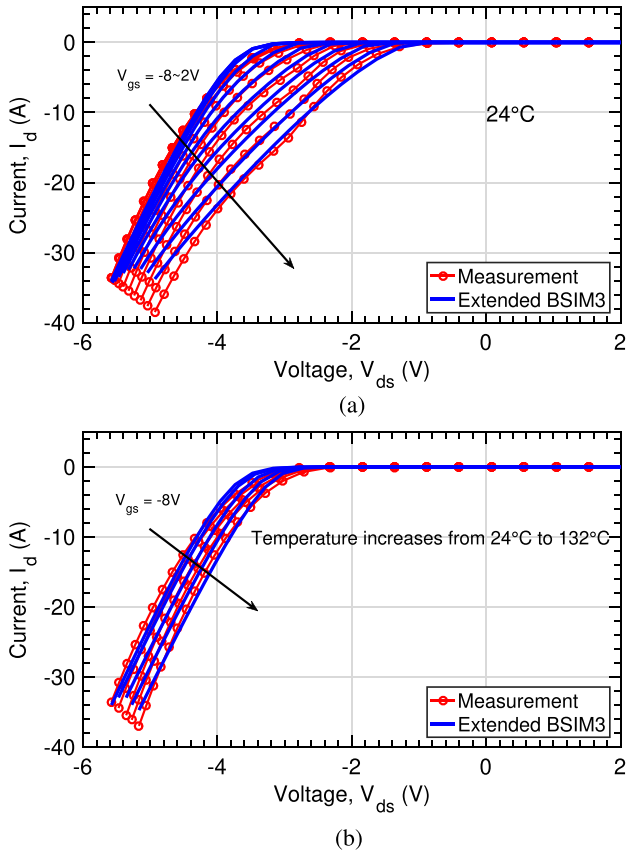

Fig. 9. Reverse I–V characteristics of the 1200-V SiC MOSFET C2M0080120D. (a) Sweeping V_{gs} at room temperature. (b) Sweeping temperature when V_{gs} at −8 V.

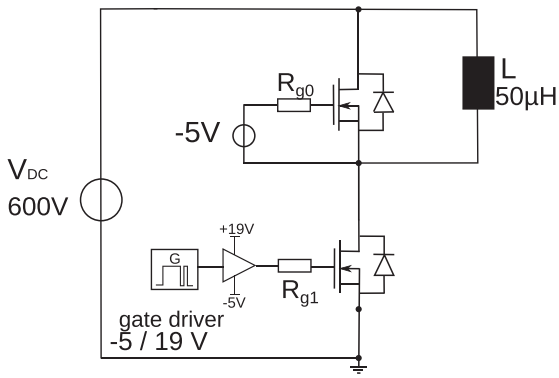

Fig. 10. Sketch of the DPT setup for SiC devices.

MOSFET is kept in OFF-state to act as the freewheeling diode. The transient current is measured by a coaxial shunt [28] at the source terminal of the low-side device. Fig. 10 depicts the DPT setup.

In this analysis, the 1200-V SiC MOSFET SCT2080KE is selected as the target device. Considering the margin of safety, the dc-link voltage is chosen as 600 V, and a 50-µH air coil is used as the inductive load to create the current steps. Both the high- and low-side DUTs are the target devices. The high-side device is kept OFF with −5 V gate bias, at which the channel of the DUT is ensured to be closed in the reverse case. The

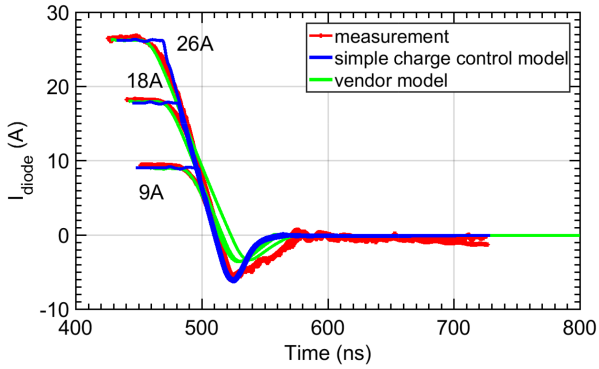

Fig. 11. Measured reverse recovery waveform of the SiC body diode at different current levels and simulation result with the vendor model and with the simple charged controlled model.

positive turn-ON gate voltage for the low-side device is set as 19 V according to the device datasheet.

The reverse recovery behavior can be influenced by the operating scenario [29], e.g., the operating temperature, loading current, dc-link voltage, etc. To observe the influence on the reverse recovery behavior coming from the current level and the temperature, the DPT is carried out at 9.8, 18.2, and 26.7 A when the case temperature is at 25, 65, and 90 °C, respectively.

For the diffusion capacitance of the body diode, the simple charge control model, which is successfully applied for Si power MOSFETs, is initially tried to be utilized to describe the reverse recovery behavior of the body diode. The comparison of the measurement and the simulation result at room temperature is shown in Fig. 11. It can be observed that the slope of the recovery term of the SiC device is also different from that of conventional Si MOSFETs. Moreover, it is realized that with the simple stored charge model, when the reverse recovery current peak is fitted, the reverse recovery time cannot be simulated precisely at the same time. Because the charge definition is defined as a lumped unit in the simple charge control model, although this definition can accurately describe the reverse recovery performance of Si power MOSFETs [12], this simplification is not suitable for modeling the body diode of SiC power MOSFETs.

Fig. 11 also shows the simulation result of the vendor model. It can be observed that the reverse recovery peak is not precisely described, and the reverse recovery charge is also underestimated.

Therefore, the charge distribution model with the lumped charge method needs to be adopted for a more detailed and precise definition. Fig. 12 shows the simulation result of the reverse recovery current at different case temperatures and at different current levels. At room temperature in Fig. 12(a), it can be observed that the load current almost does not influence the reverse recovery current, but with increasing temperature, as shown in Fig. 12(b) and (c), the current waveform and the current peak along with the reverse recovery charge increase. Moreover, the difference between different load currents also appears at higher temperatures. The physical definition of the charge distribution model has the ability to describe these behaviors accurately. In the simulation, the parasitic effect of the setup

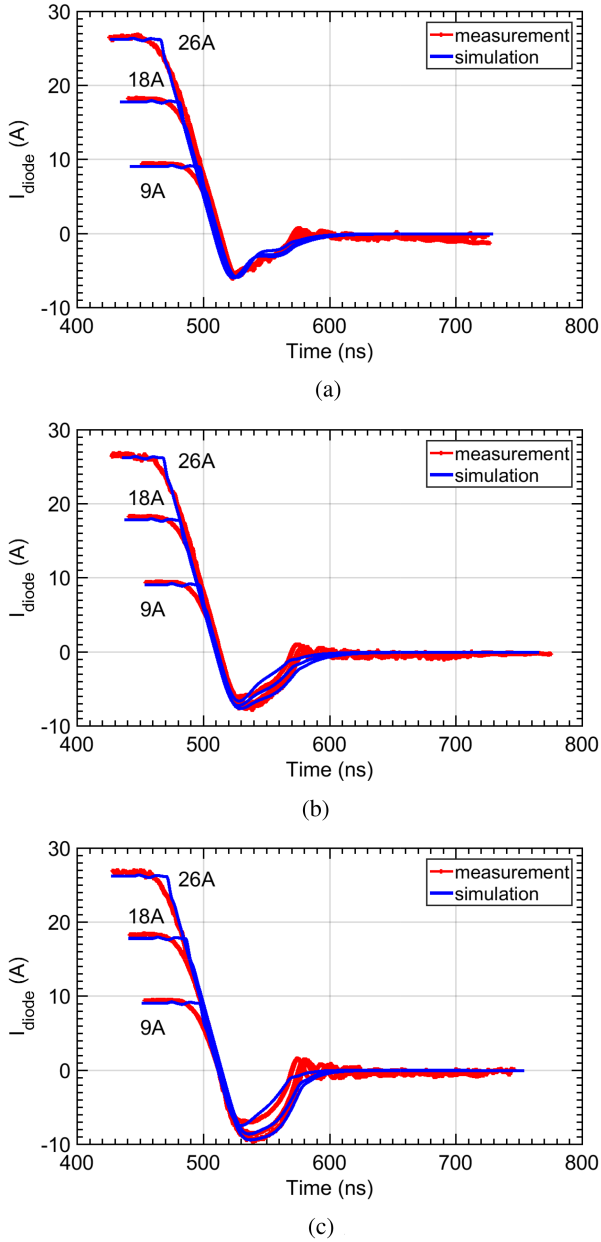

Fig. 12. Measured reverse recovery waveform of the SiC body diode at different current levels and different case temperatures compared with the simulation result with the charge distribution model. (a) 25 °C. (b) 65 °C. (c) 90 °C.

is modeled as a lumped inductor in series with a resistor. The accuracy of the description of the parasitic effect coming from the setup is limited in this article by using the evaluation board. To improve the accuracy, an electromagnetic simulation can be carried out for the definition of the parasitic effects coming from the DPT setup.

The waveform of the active-side device during the turn-ON transient is also recorded. Fig. 13 shows the active device transient waveform at 90 °C when the load current is 26 A. From the application point of view, the switching loss of the active device during the reverse recovery transition at different current levels is also calculated. The comparison between the measurement and simulation, when the case temperature is at

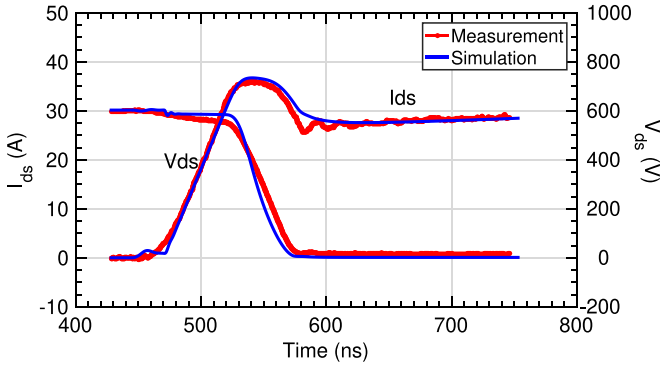

Fig. 13. Transient waveform of the active device during turn-ON at 90 °C case temperature.

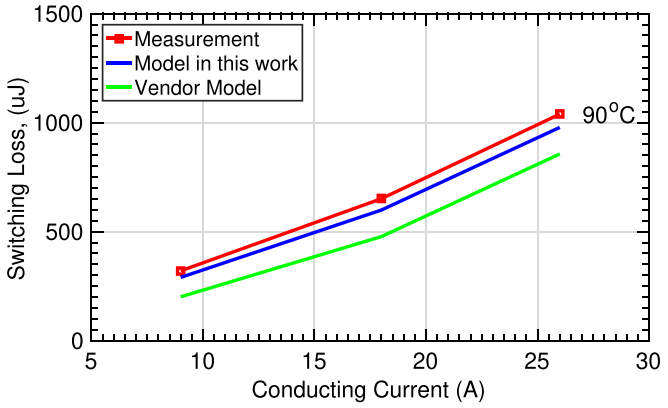

Fig. 14. Switching loss of the active device during the reverse recovery of the passive device at 90 °C case temperature.

TABLE I
SWITCHING LOSS OF THE ACTIVE DEVICE AT DIFFERENT CURRENT LEVELS AND TEMPERATURES

Operating Condition		Measurement	Simulation	Error
25°C	9A	279 μJ	253 μJ	9.32 %
	18A	559 μJ	511 μJ	8.59 %
	36A	911 μJ	841 μJ	7.68 %
90°C	9A	320 μJ	290 μJ	9.38 %
	18A	651 μJ	599 μJ	7.99 %
	36A	1039 μJ	978 μJ	5.87 %

90 °C, is shown in Fig. 14. According to [30], the switching loss is calculated by integrating the switching power from the time when the current reaches 10% of the load current until the voltage drops to 10% of the dc-link voltage. Compared with the vendor model, the modeling method proposed in this article can increase the accuracy of the simulation of the transient switching loss by around 20%.

To validate the model performance at different temperatures and load current levels, the measurement and simulation results of the switching loss during the switching on transient at different operating points, as mentioned above, are compared. The measured and simulated results and the error between them are listed in Table I. It can be seen that the deviation between the measured and the simulated switching loss at all the operating points is lower than 10%. And the accuracy can be further improved when the parasitic effects coming from the measurement setup can be described more precisely.

From the parameter extraction result, it can be deduced that to model SiC MOSFETs, the specific model extensions proposed in this article are accurate and necessary.

IV. CONCLUSION

This article proposed and analyzed a method to extend the industry-standard BSIM3 model to describe SiC vertical power MOSFETs. The simulation results showed that the proposed model can depict the characteristics of SiC power MOSFETs at different electrical and thermal operating points precisely. The switching behavior influenced by the parasitic capacitances was also accurately defined by the proposed extended model. Finally, the transient simulation tests validated the performance of the proposed model. For future work, the model can still be improved to describe the V_{gs}-dependent capacitance for a more precise description of the dynamic behavior, while the tradeoff between the model accuracy and the model complexity always needs to be taken into consideration. In addition, the proposed model extension strategy can be further developed for novel SiC MOSFET structures.

REFERENCES

[1] J. L. Hudgins, G. S. Simin, E. Santi, and M. A. Khan, "An assessment of wide bandgap semiconductors for power devices," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 907–914, May 2003.
[2] T. Kimoto and J. Cooper, *Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications*. Hoboken, NJ, USA: Wiley, 2014.
[3] H. A. Mantooth, K. Peng, E. Santi, and J. L. Hudgins, "Modeling of wide bandgap power semiconductor devices—Part I," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 423–433, Feb. 2015.
[4] T. R. McNutt, A. R. Hefner, H. A. Mantooth, D. Berning, and S. Ryu, "Silicon carbide power MOSFET model and parameter extraction sequence," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 353–363, Mar. 2007.
[5] Y. H. Lee, M. Zhang, P. J. Niu, P. F. Ning, L. Liu, and S. S. Lee, "Simplified silicon carbide MOSFET model based on neural network," in *Semiconductors: Silicon Carbide and Related Materials* (ser. Materials Science Forum), vol. 954. Wollerau, Switzerland: Trans Tech Publications, 2019, pp. 163–169.
[6] L. Yan and I. Kallfass, "Adopting the BSIM3 model with thermal extension for a Si vertical power MOSFET," in *Proc. IEEE 19th Int. Power Electron. Motion Control Conf.*, 2021, pp. 68–74.
[7] B. Baliga, *Fundamentals of Power Semiconductor Devices*. New York, NY, USA:Springer, 2010.
[8] Y. Tanimoto et al., "Power-loss prediction of high-voltage SiC-MOSFET circuits with compact model including carrier-trap influences," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4509–4516, Jun. 2016.
[9] L. Yan and I. Kallfass, "Adopting the BSIM3 model to describe the DC-IV characteristics of a vertical power MOSFET," *in Proc. IEEE Int. Power Electron. Appl. Conf. Expo.*, 2018, pp. 1–6.
[10] W. Choi and D. Kim, "New PowerTrench® MOSFET with shielded gate technology increases system efficiency and power density in synchronous rectification applications," Fairchild Semicond., 2013.
[11] Y. S. Chauhan, F. Krummenacher, and A. M. Ionescu, *Modeling of High Voltage MOSFETs Based on EKV (HV-EKV)*. Dordrecht, The Netherlands: Springer, 2010, pp. 95–127.
[12] L. Yan, T. Li, and I. Kallfass, "Characterization and modeling of the reverse behavior of a vertical power MOSFET," *Microw. Opt. Technol. Lett.*, vol. 63, no. 8, pp. 2090–2096, 2021.
[13] J. Wang et al., "Characterization, modeling, and application of 10-kV SiC MOSFET," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 1798–1806, Aug. 2008.

[14] H. Ding, J. J. Liou, C. R. Cirba, and K. Green, "An improved junction capacitance model for junction field-effect transistors," *Solid-State Electron.*, vol. 50, no. 7, pp. 1395–1399, 2006.
[15] J. Taillon et al., "Systematic structural and chemical characterization of the transition layer at the interface of NO-annealed 4H-SiC/SiO_2 metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 113, 2013, Art no. 044517.
[16] K. Chen, Z. Zhao, L. Yuan, T. Lu, and F. He, "The impact of nonlinear junction capacitance on switching transient and its modeling for SiC MOSFET," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 333–338, Feb. 2015.
[17] S. Sze and K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, 2006.
[18] N. Arora, *SPICE Diode and MOSFET Models and Their Parameters*. Vienna, Austria: Springer, 1993, pp. 536–562.
[19] K. J. Tseng and S. Pan, "Modified charge-control equation for simulation of diode reverse recovery," *Electron. Lett.*, vol. 32, no. 4, pp. 404–406, 1996.
[20] C. L. Ma, P. O. Lauritzen, and J. Sigg, "Modeling of power diodes with the lumped-charge modeling technique," *IEEE Trans. Power Electron.*, vol. 12, no. 3, pp. 398–405, May 1997.
[21] C. L. Ma, P. O. Lauritzen, and P. Y. Lin, "A physically-based lumped-charge P-nu-N diode model," in *Proc. 5th Eur. Conf. Power Electron. Appl.*, 1993, vol. 2, pp. 23–28.
[22] P. O. Lauritzen and C. L. Ma, "A simple diode model with reverse recovery," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 188–191, Apr. 1991.
[23] F. Kerrour, A. Boukabache, and P. Pons, "Modelling of thermal behavior N-doped silicon resistor," *J. Sens. Technol.*, vol. 3, no 3, pp. 132–137, 2012.
[24] L. Hernandez, A. Claudio-Sanchez, M. Cotorogea, J. Aguayo, and M. A. Rodriguez, "4H-SiC PiN diode electrothermal model for conduction and reverse breakdown for simulator," in *Proc. IEEE 11th Int. Power Electron. Congr.*, 2008, pp. 192–197.
[25] Rev.D., Sep. 2019. [Online]. Available: https://www.wolfspeed.com/downloads/dl/file/id/167/product/643/c2m0080120d.pdf
[26] Rev.001, Mar. 2021. [Online]. Available: https://fscdn.rohm.com/en/products/databook/datasheet/discrete/sic/mosfet/sct2080ke-e.pdf
[27] Rev.001, Mar. 2021. [Online]. Available: https://fscdn.rohm.com/en/products/databook/datasheet/discrete/sic/mosfet/sct2160ke-e.pdf
[28] P. Baranov, V. Borikov, and E. Tsimbalist, "Measurement of the current transfer function for power transducers of current to voltage," *Appl. Mech. Mater.*, vol. 756, pp. 615–621, 2015.
[29] Z. Wang, J. Ouyang, J. Zhang, X. Wu, and K. Sheng, "Analysis on reverse recovery characteristic of SiC MOSFET intrinsic diode," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 2832–2837.
[30] *Semiconductor Devices. Discrete Devices. Field-Effect Transistors*, IEC 60747-8, 2011.

Lixi Yan received the B.Sc. degree in electrical engineering from Southeast University, Nanjing, China, in 2012, and the M.Sc. degree in information technology in 2016 from the University of Stuttgart, Stuttgart, Germany, where she is currently working toward the Ph.D. degree with the Institute of Robust Power Semiconductor Systems.

She is working on the circuit-design oriented modeling and simulation of modern power transistors with the Institute of Robust Power Semiconductor Systems, University of Stuttgart. Her current research interests include characterization of power transistors and physics-based modeling for vertical Si and SiC power MOSFETs.

Kanuj Sharma received the B.Tech. degree in electronics and communication engineering from Maharishi Dayanand University, Rohtak, India, in 2011, the M.Sc. degree in international business management with marketing from Heriot-Watt University, Edinburgh, U.K., in 2013, and the M.Sc. degree in micro- and optoelectronics in 2017 from the University of Stuttgart, Stuttgart, Germany, where he is currently working toward the Ph.D. degree with the Institute of Robust Power Semiconductor Systems.

His technical research interests include the physics and characterization of wide-bandgap transistor technologies.

Ingmar Kallfass received the Dipl.-Ing. degree in electrical engineering from the University of Stuttgart, Stuttgart, Germany, in 2000, and the Dr.-Ing degree on the topic of nonlinear modelling of dispersive heterostructure field effect transistors and their MMIC applications from the University of Ulm, Ulm, Germany, in 2005.

In 2001, he was a Visiting Researcher with the National University of Ireland, Dublin, Ireland. In 2002, he joined the Department of Electron Devices and Circuits, University of Ulm, as a Teaching and Research Assistant. In 2005, he joined the Fraunhofer Institute for Applied Solid-State Physics, Breisgau, Germany. From 2009 to 2012, he was a Professor with the Karlsruhe Institute of Technology, Karlsruhe, Germany. Since 2013, he has been a Chair for Robust Power Semiconductor Systems with the University of Stuttgart. His major research interests include compound-semiconductor-based circuits and systems for power and microwave electronics.