A 13.56-MHz Wireless Power Transfer System With a Wide Operating Distance and Load Range for Biometric Smartcards

Hongkyun Kim, *Student Member, IEEE*, Yechan Park, *Student Member, IEEE*, and Chul Kim, *Senior Member, IEEE*

***Abstract*—This article presents a wireless power transfer system for an increased dynamic range of link distance and load with extended controllability of transmitting power. Under wide link distance and load variation, rectification and regulation in a single-stage to provide a stable 3-V dc voltage V_L from a 13.56-MHz sinusoidal waveform at the receiver (RX) LC tank is performed. For high end-to-end power transfer efficiency and robust operation under link and load variations, the transmitting power P_{TX} is controlled by the reflected impedance from the RX to the transmitter (TX). To extend the controllability of the P_{TX}, antennae with high quality factors and a series-connected RX LC tank structure are applied. A working-only-when-needed rising edge detector and a $\Delta\Sigma$-based falling edge detector for low power and accurate zero current detection are presented. A digital $\Delta\Sigma$-based voltage regulation controller is adopted for stable dc supply with fast transient response. The implemented IC in a standard 65-nm CMOS process measures 0.14-mm^2 active silicon area. The proposed work operates under a wide range of link distance (30–185 mm) with a large load dynamic range (10000×, 60 Ω–600 kΩ).**

***Index Terms*—Biometric smartcard, inductive link, reflected impedance, wide distance and load variation, wireless power transfer (WPT).**

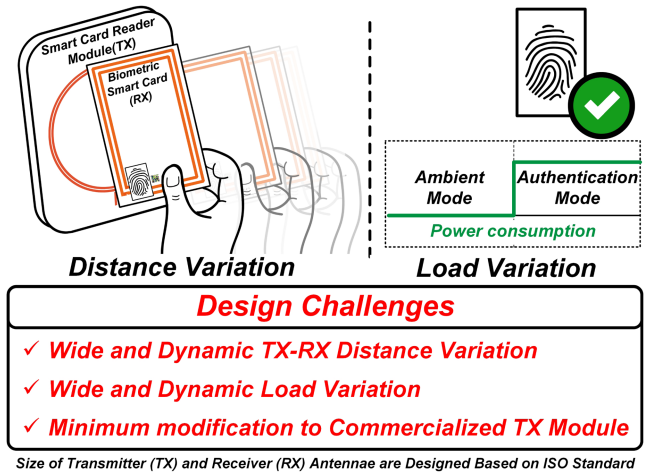


Fig. 1. Conceptual diagram and design challenges for a biometric smartcard with fingerprint authentication.

I. Introduction

THE importance of contactless biometric smartcards has been increased with emerging concerns about the spread of epidemics, security issues, and user convenience [1], [2], [3]. Unlike previous contactless memory cards which only store data passively, biometric smartcards with enhanced security using biometric authentication demand a power budget greater than 100 mW, large enough to run an installed processing unit. Fig. 1 illustrates conceptual diagrams of a biometric smartcard with design challenges. A biometric smartcard (RX) can operate while consuming power delivered from a card reader module (TX). For the convenient operation of the RX, designing a wireless power receiver (WPR) that supplies stable power under wide and dynamic link distance variation is essential. Also, a fast load transient response for mode transitions from ambient mode to authentication mode is required as an instantaneous increase in current from load may fail constant voltage regulation of the supply. Also, zero or at most minimum modification to commercialized TX module is needed for wide reuse of installed card reader modules.

Fig. 2(a) shows a conventional multistage voltage-mode (VM) WPR structure that has been widely used [4], [5], [6]. AC voltage at an RX antenna is rectified and regulated through an ac–dc converter, and a dc–dc converter. This structure works well at a short link distance at the expense of cumulative power loss. However, at the long link distance, the coupling between TX and RX link weakens and it may fail to generate enough dc voltage due to limited received power at the RX antenna. To increase operating link distance, current-mode (CM) WPR was developed for wireless power delivery through a loosely coupled link, as depicted in Fig. 2(b) [7]. It accumulates energy at the RX LC tank during a build-up phase and after enough accumulation,

Manuscript received 13 June 2022; revised 18 November 2022; accepted 20 December 2022. Date of publication 28 December 2022; date of current version 14 February 2023. This work was supported in part by the ANSYS Korea, IDEC, the National Research Foundation of Korea (NRF) Grant funded by the Korea government (MSIT) under Grants 2020R1C1C1009878, 2021M3H4A1A03048661, and 2022M3E5E9018349. Recommended for publication by Associate Editor K.-H. Chen. *(Corresponding author: Hongkyun Kim.)*

Hongkyun Kim and Chul Kim are with the Bio and Brain Engineering, KAIST, Daejeon 34141, South Korea (e-mail: hongkyun.kim@kaist.ac.kr; kimchul@kaist.ac.kr).

Yechan Park is with the School of Electrical Engineering, KAIST, Daejeon 34141, South Korea (e-mail: yechan.park@kaist.ac.kr).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3232609.

Digital Object Identifier 10.1109/TPEL.2022.3232609

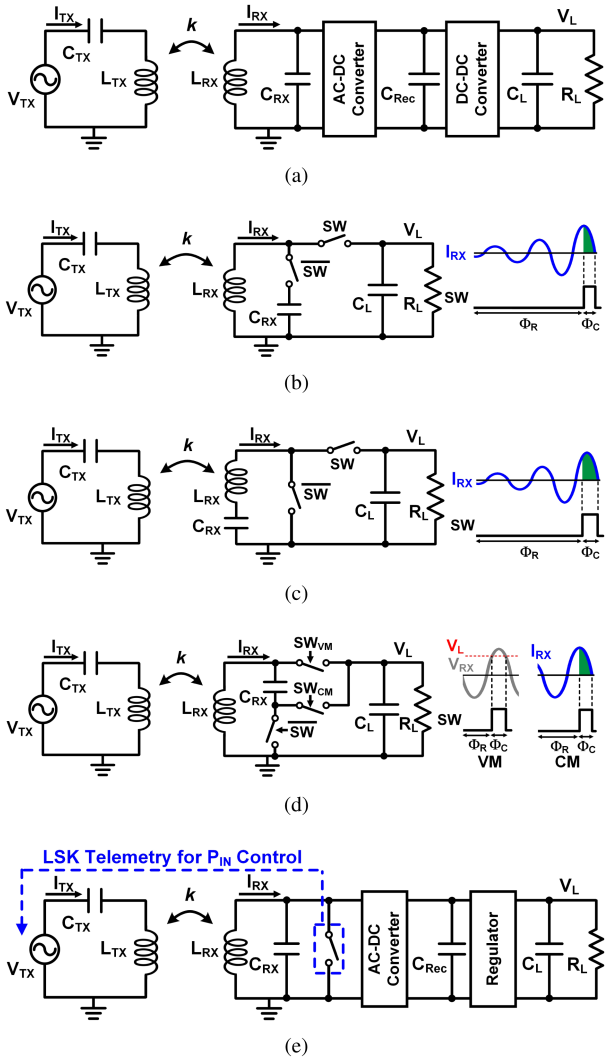


Fig. 2. Simplified circuit models of previous wireless power transfer and receiver systems with key waveforms. (a) 3-stage wireless power receiver. (b) Current mode (CM). (c) CM with a charging mode control for minimum residual energy at the RX LC tank. (d) WPR with adaptive VM-CM conversion. (e) WPT system with an up-link telemetry for P_{IN} control.

charges the battery for regulating rectification in single stage. Although its maximum power at the RX LC tank is limited by the breakdown voltage of power switches connected to the LC tank high-impedance node, this structure shows great performance when receiving power at the RX LC tank P_{RX} is small.

To further improve performance at this link condition, a series-connected CM WPR structures have been developed [8], [9], [10], [11], [12]. CM WPR designs with structure illustrated in Fig. 2(c) discharges the LC tank energy to the battery for maximum power delivered to the load (PDL) [8], [9], [10], [11]. Since PDL per switching is inherently defined by the LC tank for discharge, it requires an additional regulator for voltage regulation. Fig. 2(d) shows a reconfigurable VM/CM WPR that adaptively reconfigures to VM/CM depending on P_{RX}, supporting relatively wide distance and load variation [13]. However, it also has power switches connected to the high-impedance node of the LC tank, limiting the P_{RX} due to the voltage stress and creating a dead zone at mode transitions [14]. Fig. 2(e) shows a wireless power transfer (WPT) system with global feedback to actively control transmitting power, and thus, receiving power P_{RX} for stable operation even under dynamic link variation [15], [16], [17], [18], [19]. However, the P_{RX} control speed of the global feedback is somewhat slow for fast dynamic link applications, such as smartcards, and adopting a load-shift keying (LSK) telemetry demands severe modification on the TX module and communication protocol [8], [9], [10], [11]. To break through all the limitations above, we present a WPT system working over an increased dynamic range of link distance and load with extended controllability of transmitting power (WIDE). The dynamic range of link distance is 30–185 mm and that of the load is 60 Ω–600 kΩ. To overcome the operation limit aroused by the trait of the WPT system, such as vulnerability to link distance and load variations, the transmitting power is instantly controlled by modifying reflected resistance at the TX from the RX side. To extend controllability of transmitting power, the RX LC tank should accommodate large energy, and thus, series compensated high Q-factor RX antenna sustaining strong coupling between the TX and the RX antennae in wide link distance is adopted. Furthermore, the presented WIDE performs rectification and regulation simultaneously to develop a 3-V load voltage from 13.56-MHz ac voltage at the RX LC tank. For this purpose, a precise zero current detector and a $\Delta\Sigma$-based voltage regulator controller are proposed. The rest of this article is organized as follows. Section II explains the operation principle of WIDE with theoretical analysis, and Section III describes the system architecture. The measurement results are shown in Section IV. Finally, Section V concludes this article.

II. Operation Principle of WIDE

This section covers the operation principles and theoretical analysis of WIDE, revealing that WIDE is superior under wide and dynamic link distance and load variation. Fig. 3(a) illustrates the overall lumped schematic of WIDE with energy delivery between TX and RX. A sinusoidal voltage source V_{TX} supplies TX current, I_{TX} to the TX LC tank by L_{TX}-C_{TX}, and delivers energy over a wireless link in a form of a 90° phase shifted dependent voltage source, $j\omega M I_{\mathrm{TX}}$ to series-connected RX L_{RX} and C_{RX}. In reverse, RX current, I_{RX} is reflected to the TX LC tank with another 90° phase shift, which is expressed as $Z_{\mathrm{Reflected}}$. It eventually reduces I_{TX} and input power P_{TX}. This relationship between I_{TX} and I_{RX} is beneficial to end-to-end (E2E, from input power P_{TX} to load power P_L) wireless power transfer efficiency (PTE) and regulation. Both LC tanks resonate at f_{res}, 13.56 MHz. Effective series resistance (ESR) at the TX and RX are modeled as an R_1 and an R_2, respectively. Two power switches S_{N} and S_{P} are controlled to adjust P_{TX} and regulate the amount of PDL to the load R_{L} in parallel with C_{L} under wide and dynamic link distance and load variation.

WIDE operates in two distinct modes, the resonance mode and charging mode shown in Fig. 3(b). At resonance mode, the V_{X} node connects to GND through S_{N} to receive and store energy at high-Q RX LC tank. At charging mode, the V_{X} node connects to the load through S_{P} during half of $1/f_{\mathrm{res}}$ by precise zero current

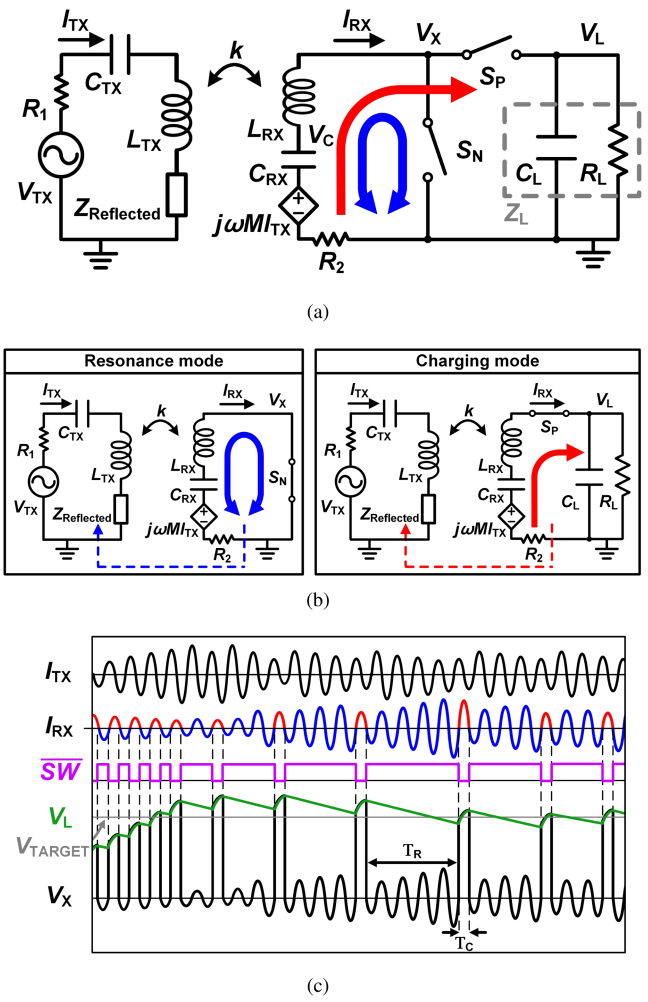


Fig. 3. (a) Simplified schematic diagram of WIDE. (b) Operation modes: resonance and charging modes. (c) Key waveforms of WIDE in operation.

detection, to deliver maximum energy from the RX LC tank to the load per switching and sustain regulated V_{L}. The energy stored at the RX LC tank is projected to the TX LC tank in form of $Z_{\mathrm{Reflected}}$, which eventually increases or decreases P_{TX}. Fig. 3(c) shows key waveforms of WIDE, including I_{TX}, I_{RX}, a gate driving signal $\overline{SW}$ for power switches, voltage waveforms at node V_{L} and V_{X}. The V_{L} is regulated by $\Delta\Sigma$-based voltage regulation control. The controller monitors V_{L} at the frequency of 13.56 MHz and, when V_{L} is greater (lower) than the V_{TARGET}, decreases (increases) the portion of charging mode until V_{L} reaches V_{TARGET}.

A. Theoretical Analysis

In the resonance mode, $Z_{\mathrm{Reflected}}$ under the steady-state condition can be found from

$$Z_{\mathrm{Reflected\text{-}RES}} = \frac{\omega^2 M^2}{R_2 + R_{\mathrm{N}}} \tag{1}$$

where $\omega = 1/\sqrt{L_{\mathrm{TX}} C_{\mathrm{TX}}} = 1/\sqrt{L_{\mathrm{RX}} C_{\mathrm{RX}}}$, M is the mutual inductance between the TX and RX link, R_1, R_2 consists of ESR from the inductor and capacitor, and R_{N} is the on-resistance of S_{N}. The current from fixed voltage source V_{TX} can be written as

$$I_{\mathrm{TX}} = \frac{V_{\mathrm{TX}}}{R_1 + \frac{\omega^2 M^2}{R_2 + R_{\mathrm{N}}}}. \tag{2}$$

The amplitude of voltage V_{C} induced at C_{RX} is calculated from

$$|V_{\mathrm{C}}| = \omega M I_{\mathrm{TX}} Q_{\text{2-RES}} \tag{3}$$

where $Q_{\text{2-RES}} = \omega L_{\mathrm{RX}}/(R_2 + R_{\mathrm{N}})$. The energy stored at the RX LC tank is found from

$$E_{\text{RX-RES}} = \frac{1}{2} C_{\mathrm{RX}} \left(\omega M \frac{V_{\mathrm{TX}}}{R_1 + \frac{\omega^2 M^2}{R_2 + R_{\mathrm{N}}}} Q_{\text{2-RES}} \right)^2. \tag{4}$$

When $R_1(R_2 + R_{\mathrm{N}}) \ll \omega^2 M^2$, (4) can be simplified to

$$E_{\text{RX-RES}} \simeq \frac{1}{2} C_{\mathrm{RX}} \left(\frac{V_{\mathrm{TX}}(R_2 + R_{\mathrm{N}})}{\omega M} Q_{\text{2-RES}} \right)^2. \tag{5}$$

In (5), energy stored at the RX LC tank is inversely proportional to M^2. Utilizing the relationship, energy delivered to the RX is controlled to compensate link distance variation. For example, when the link distance becomes longer or angular misalignment increases, and thus, M decreases, $E_{\text{RX-RES}}$ increases. Although it would be difficult to implement the optimal load in the RX due to design challenges, such as wide link distance and load range, the optimal load can further improve $E_{\text{RX-RES}}$ [20]. The voltage V_{X} in the resonance mode is

$$V_{\text{X-RES}} = I_{\mathrm{RX}} \times R_{\mathrm{N}}. \tag{6}$$

In the charging mode, the impedance reflected at the TX $Z_{\mathrm{Reflected}}$ in a steady state is written as

$$Z_{\text{Reflected-CHG}} = \frac{\omega^2 M^2}{R_2 + R_{\mathrm{P}} + Z_{\mathrm{L}}} \tag{7}$$

where R_{P} is the on-resistance of S_{P}, and $Z_{\mathrm{L}} = C_{\mathrm{L}} || R_{\mathrm{L}}$. Comparing (1) and (7), $Z_{\mathrm{Reflected}}$ decreases in the charging mode, and thus I_{TX} and P_{TX} increase for fast charging. The V_{X} at the charging mode is significantly different from V_{X} at the resonance mode shown in (6). $V_{\text{X-CHG}}$ is calculated as

$$V_{\text{X-CHG}} = I_{\mathrm{RX}} \times R_{\mathrm{P}} + V_{\mathrm{L}}. \tag{8}$$

The equivalent reflected impedance $Z_{\text{Reflected-EQ}}$ can be calculated with the ratio of T_{R} and T_{C}

$$D = \frac{T_{\mathrm{R}}}{T_{\mathrm{R}} + T_{\mathrm{C}}} \tag{9}$$

$$Z_{\text{Reflected-EQ}} = \frac{\omega^2 M^2}{R_2 + R_{\mathrm{N}} D + (R_{\mathrm{P}} + Z_{\mathrm{L}})(1 - D)} \tag{10}$$

where T_{R} and T_{C} are the resonance mode time period and charging mode time period, respectively.

To satisfy the condition $R_1(R_2 + R_{\mathrm{N}}) \ll \omega^2 M^2$, the TX and RX antennae are designed to have high quality factors. However, the use of high-Q RX antenna amplifies variation in V_{C} under wide link distance variation between the TX and RX according to (5). For extending controllability of P_{TX} from the RX by increasing the amount of energy in the RX LC tank without breakdown of MOSFETs, L_{RX} and C_{RX} are connected in series to isolate the V_{C} node from any MOSFETs. By comparing (3) with

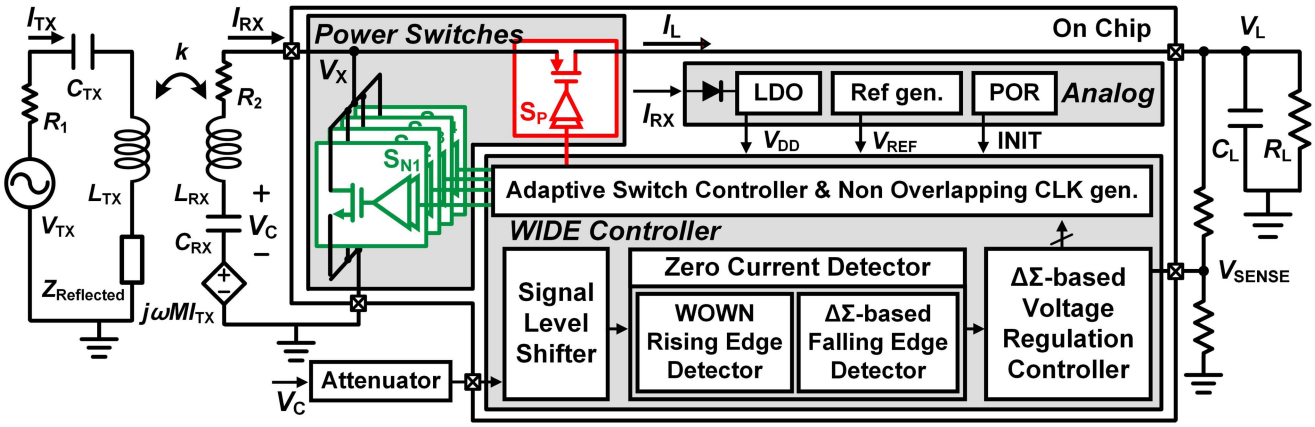


Fig. 4. Overall system block diagram of WIDE.

(6) and (8), the amount of reduction in voltage stress can be calculated. Therefore, the MOSFETs are always in safe voltage range without the use of overvoltage protection circuits.

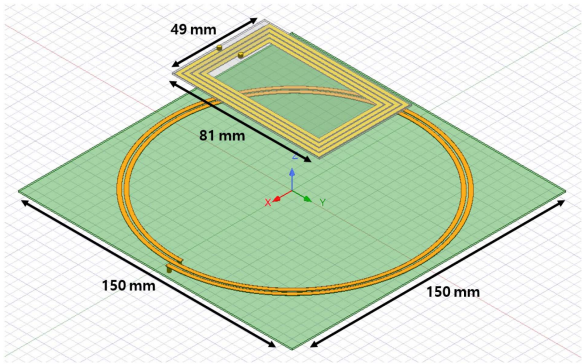
The mode transition from the resonance mode to the charging mode decreases energy stored at the RX LC tank and decreases $Z_{\text{Reflected}}$. It eventually increases I_{TX} and P_{TX} instantaneously, which is a driving force to recover I_{RX} at the next cycle of switching. This additionally helps voltage and power regulation at V_{L} increasing dynamic operating link distance.

III. System Architecture

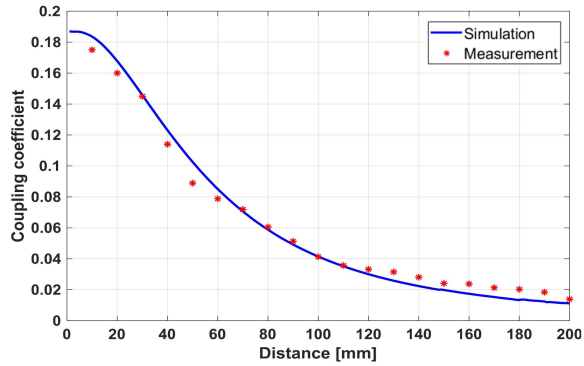
Fig. 4 shows the overall system of WIDE. WIDE consists of a voltage source, two high-Q TX, RX antennae with series connected 13.56-MHz resonance compensation capacitors and WIDE chip. In WIDE chip, there is an analog block, WIDE controller and power switches for operation. In the analog block, a small diode connected with a linear low-dropout regulator (LDO), an internal reference generator, and a power-on-reset (POR) are implemented to generate V_{DD}, reference voltages, and a start-up signal, respectively. The 1.2-V V_{DD} is the supply voltage of WIDE controller. In the WIDE controller, a working only when needed (WOWN) rising edge detector finds negative to positive zero current crossing points with attenuated and level shifted V_{C}. $\Delta\Sigma$ error integration concept is utilized for a falling edge detector finding positive-to-negative zero current crossing points, and a voltage regulation controller generating gate driving signals for fast load voltage regulation. There are four parallel NMOS power switch units and a single PMOS power switch controlled by a non-overlapping clock generator and an adaptive switch controller for minimizing conduction and switching losses.

A. Antenna Design

As introduced in Section II, the design of high-Q TX and RX antennae for the condition $R_1(R_2 + R_{\text{N}}) \ll \omega^2 M^2$ is essential for compensating link distance variation by controlling energy delivered to the RX LC tank. As shown in Fig. 5, the size of the TX and RX antennae follow the ISO/IEC 10373-6 standard [21] and the ISO/IEC 14443-1 PICC class 1 standard [22],



(a)



(b)

Fig. 5. (a) Illustration of Q3D model for TX and RX antennae design. (b) Comparison of coupling coefficient by Q3D extraction and measurement results with different link distance.

while Q-factors are 170 and 160, respectively. The electrical parameters of the designed antennae are extracted in Ansys Q3D. Simulated and measured coupling coefficient between the TX and RX antennae under link distance variation from 0 to 200 mm are compared in Fig. 5(b).

B. Zero Current Detector

To increase both E2E PTE and PDL, design of a precise zero current detector is required. If the charging mode starts

earlier than the negative to positive zero current crossing point (t_{NP}) or ends after the positive to negative zero current crossing point (t_{PN}), the reverse current from the load to the RX LC tank flows, significantly reducing E2E PTE. In opposite, if the charging mode starts later than the t_{NP} or ends before the t_{PN}, PDL per switching decreases [8]. This subsection covers how the WOWN rising edge detector and the $\Delta\Sigma$-based falling edge detector efficiently and accurately finds t_{NP} and t_{PN}, respectively. The robustness of zero current detector against PVT variation is shown by the Monte Carlo simulation results of the zero current detector along with its internal power supply generator.

1) WOWN Rising Edge Detector: Finding a t_{NP} in a 13.56-MHz sinusoidal waveform without significant delay requires conventional continuous comparators to consume high power. Although a dynamic comparator works energy-efficiently per comparison, it needs to know the exact timing for comparison, which is not viable. Alternatively, a dynamic comparator should make frequent comparisons with a high clock frequency to find a t_{NP}. However, it consumes huge power again like a continuous comparator due to large number of comparisons. Here, a self-clocked dynamic comparator with an up to 1.25-GHz comparison frequency only near t_{NP} is presented. As such, it has high accuracy for finding t_{NP} points and is energy efficient since it works only when it is needed. This self-clocked dynamic comparator is named as WOWN rising edge detector.

Fig. 6 illustrates the full schematic diagram of the designed WOWN rising edge detector with key waveforms and Monte Carlo simulation result. V_C' is generated by attenuating and level-shifting V_C. Its dc bias voltage is slightly smaller than the threshold voltage of M_1. Therefore, only when V_C' is larger than the threshold voltage of M_1, current begins to flow to power up the dynamic comparator for operation. Since V_C is 90° earlier in phase than V_X (and thus, I_{RX}), the dynamic comparator operates near t_{NP} only. After making a comparison with a small systemic offset, positive or negative comparison output (OUTP or OUTN) generates a CLK_{WOWN} which is fed back with small delay for next comparison of the own dynamic comparator. This enables variable clock frequency generation since the dominant delay factor of the loop is the dynamic comparator and its decision time which is a function of V_C'. The clock frequency, CLK_{WOWN} is up to 1.25-GHz near t_{NP} when V_C' is close to its peak voltage. The first OUTP is latched to point out t_{NP} and to generate rising edge of CLK_{ZCS}. As such, the WOWN rising edge detector finds t_{NP} precisely while consuming less than 30 μW from internally generated 1.2-V V_{DD} from the LDO. As V_X and I_{RX} are in-phase in the resonance mode, V_X is compared to ground rather than I_{RX} for finding t_{NP}. Monte Carlo simulation result in Fig. 6(c) shows the accuracy of rising edge detector against PVT variation.

2) $\Delta\Sigma$-Based Falling Edge Detector: Fig. 7 illustrates the simplified schematic of the $\Delta\Sigma$-based falling edge detector consuming less than 15 μW, its key waveforms and the Monte Carlo simulation result. A rising edge of the 13.56-MHz CLK_{RST}, generated from the WOWN rising edge detector, begins the falling edge detection process. When CLK_{Delay} becomes logic high, the voltage V_{INT} falls down from V_{DD} until V_{INT} reaches the logic threshold V_{TH} of the activation inverter owing to current flow from the IDAC. Then, output of the activation inverter resets

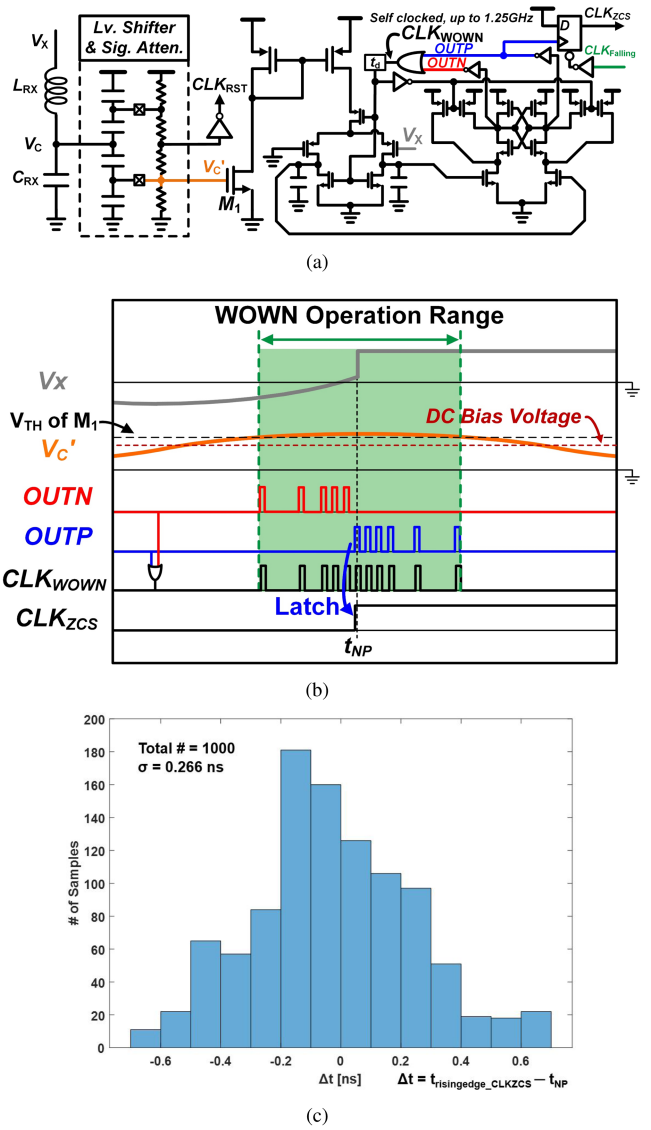


Fig. 6. (a) Schematic diagram of WOWN rising edge detector for negative to positive zero current crossing detection. (b) Key waveforms. (c) Monte Carlo simulation result.

the D flip-flop, and generates a short pulse $CLK_{Falling}$. This is the timing for resetting CLK_{ZCS} to logic low. Due to reset of the D flip-flop, CLK_{Delay} becomes logic low for discharging C_{INT} until V_{INT} reaches V_{DD} again. When the power switch S_P (in Fig. 3) is turned OFF, $\overline{SW}$ is inverted and generates CLK_{SPOFF}. The dynamic latch comparator starts to compare V_X and GND at the rising edge of CLK_{SPOFF}. By observing the comparison result of the dynamic latch comparator [23], the falling edge detector checks whether falling edge of CLK_{ZCS} is generated before or after the zero current crossing point t_{PN}. Then, the output of the comparator Δ, is accumulated at the UP/DN counter to increase or decrease the amount of current controlled by the IDAC. For instance, if V_X is lower than GND due to negative current of I_{RX}, it means that CLK_{ZCS} falls down later than t_{PN}, and thus, the IDAC current should be increased. Through the feedback process, the time delay from 14 to 24 ns, with a resolution

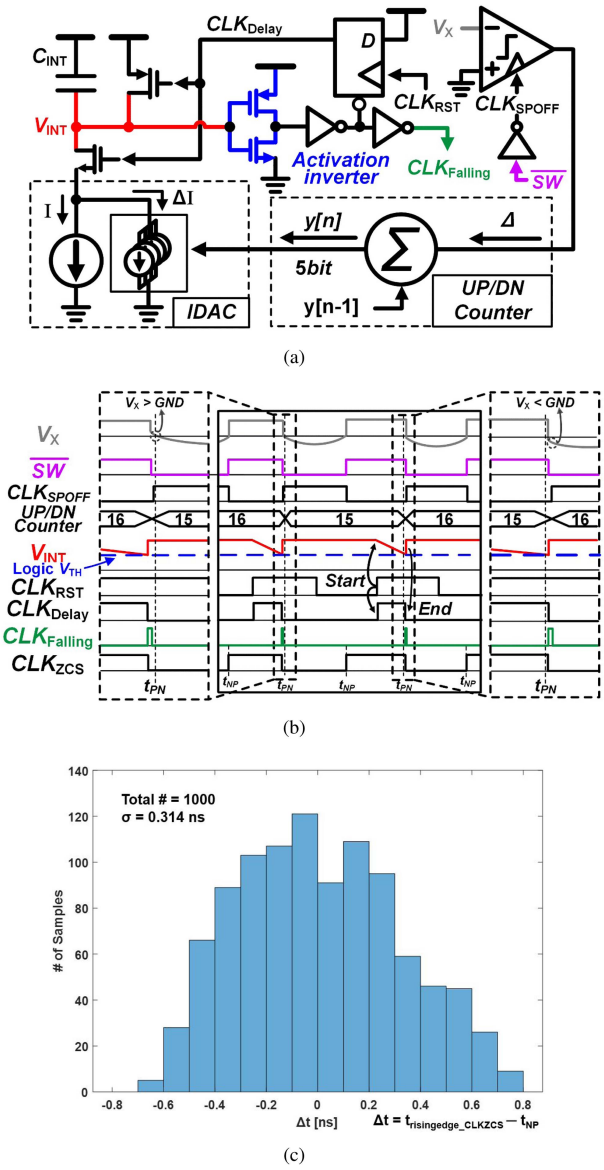


Fig. 7. (a) Schematic diagram of ΔΣ-based falling edge detector for positive to negative zero current crossing detection. (b) Key waveforms. (c) Monte Carlo simulation result.

Δ of 300 ps is controlled for detection of t_{PN}. Two timing parameters, t_{NP} and t_{PN} develop a zero current sensing clock $\mathrm{CLK_{ZCS}}$. Fig. 7(c) shows the accuracy of ΔΣ-based falling edge detector against PVT variation by the Monte Carlo simulation result.

C. Fully Digital ΔΣ-Based Voltage Regulation Controller

For load voltage regulation at target voltage, a fully digital ΔΣ-based voltage regulation controller is designed, as shown in Fig. 8. Unlike a conventional analog error integration controller which requires a continuous power consuming error amplifier for error integration and a large area capacitor for dominant pole compensation [20], [24], the digital ΔΣ-based voltage

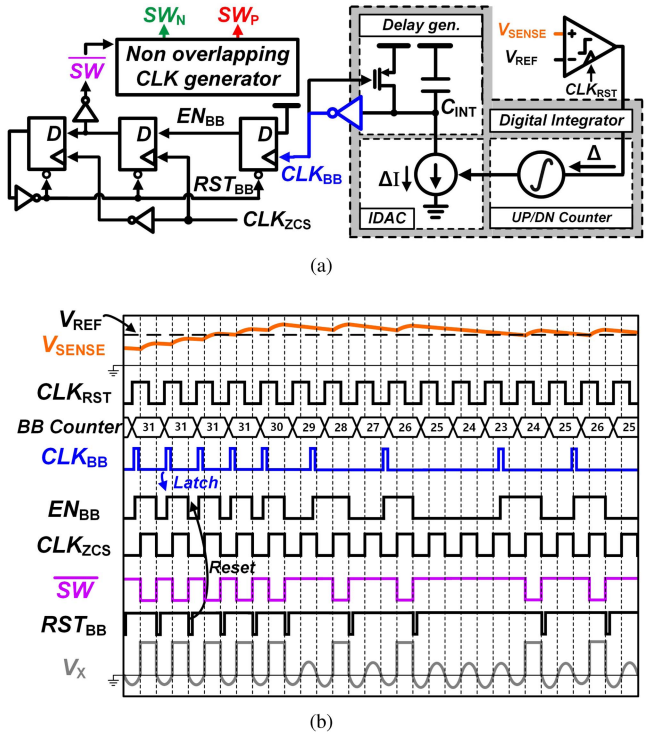


Fig. 8. (a) Building blocks for ΔΣ-based voltage regulation controller, and (b) key waveforms.

regulation controller adopts a dynamic comparator and a digital integrator enabling no dc error without area-hungry capacitor and static power consumption. It consumes switching power which is linearly proportional to switching frequency, and at a 13.56-MHz $\mathrm{CLK_{RST}}$, the average power consumption of the dynamic comparator is 1 μW. Depending on switching frequency, a conventional analog controller may consume less power. The dynamic comparator compares an internally generated V_{REF} with V_{SENSE} that is a sensed voltage from V_{L} to determine whether V_{L} has reached its target value of 3 V. The comparison output is delivered and accumulated to the digital integrator, a 5-bit up/down counter. The output of digital integrator controls the delay block which is a similar design in Fig. 7. This controlled delay sets a switching frequency of power switches by producing variable clock CLK_{BB} that generates EN_{BB}. When EN_{BB} is high, $\mathrm{CLK_{ZCS}}$ generates $\overline{SW}$. The $\overline{SW}$ is delivered to nonoverlapping clock generator for gate driving signals SW_{P} and SW_{N}, while all the D flip-flops are reset for the next clock cycle. The digital ΔΣ-based voltage regulation controller consumes 20 μW.

D. Adaptive Switch Controller

The power losses due to the switching loss and conduction loss from power switches should be alleviated for improving E2E PTE. For adaptive power loss management, the number of active power NMOS units are controlled based on switching frequency set by the ΔΣ-based voltage regulation controller. When switching frequency increases, the switching loss becomes a

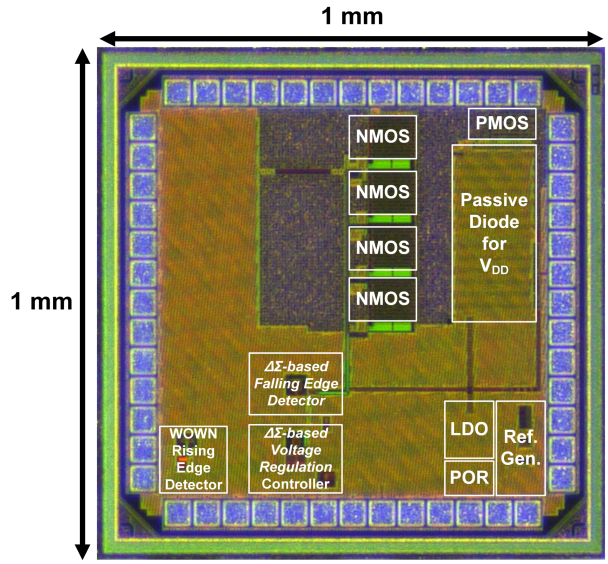


Fig. 9. Chip micrograph.

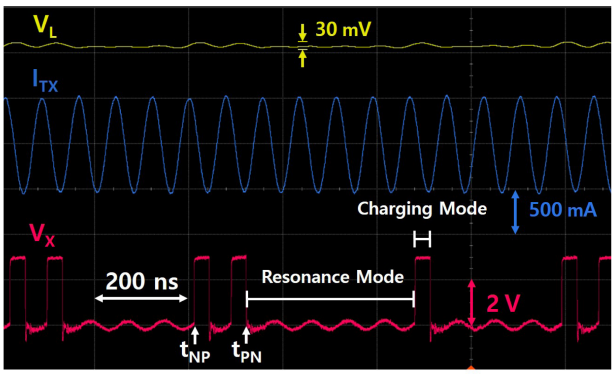


Fig. 10. Measured waveforms of V_L, I_{TX}, and V_X at 100-mm link distance between TX and RX.

dominant loss factor, and thus, the number of active power NMOS units is decreased to reduce the switching loss. Inversely, when switching frequency decreases, the number of active power NMOS units increases for conduction loss reduction. Through this adaptive switch control, E2E efficiency is improved by around 3%.

IV. Measurement Results

WIDE was fabricated in a standard 65-nm CMOS process, occupying an active area of 0.14 mm^2 shown in the chip micrograph in Fig. 9. The TX and RX antennae are fabricated on printed circuit boards (PCBs). A high speed high output current drive amplifier (ADA4870) is used as the input voltage source V_{TX} to supply 13.56-MHz current to the TX LC tank.

Fig. 10 shows the measured waveforms of V_L, I_{TX}, and V_X operating at link distance of 100 mm, with 200-Ω load. It is clearly visible in the node of V_X and V_L that at charging mode, the RX LC tank energy is delivered to V_L during half period. This half period charging is enabled by the on-chip precise zero current sensing block that detects the zero current points t_{NP}

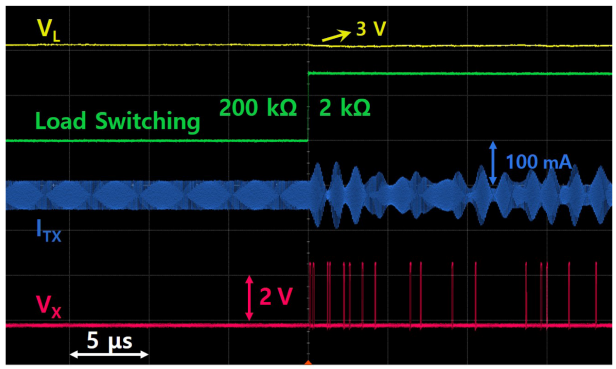


Fig. 11. Load transient response: measured waveforms of V_L, I_{TX}, and V_X.

and t_{PN}. As such, right before the rising edge of V_X and after the falling edge of V_X, negative phase of a sinusoidal waveform stops and starts, respectively, with small switching noise. WIDE successfully rectifies and regulates V_L to 3 V with a ripple voltage of less than 30 mV at $C_L = 2.2$ µF, owing to the ΔΣ-based voltage regulation controller.

In order to see the regulation performance and the effect of $Z_{reflected}$ in the I_{TX}, a load transient response of WIDE at 50 mm of link distance is measured by inducing load transition from 200 to 2 kΩ, as shown in Fig. 11. While almost no switching in V_X is observed at the light load condition, the RX LC tank energy is frequently delivered to the heavy load, leading to negligible voltage drop in V_L. Please note that I_{TX} is varying accordingly: whenever the V_X is connected to V_L for energy delivery from the RX LC tank to the load, the energy of RX LC tank is reduced and as a result, I_{TX} increases owing to reduced $Z_{reflected}$.

Measured results and setups for load regulation from 60 Ω to 600 kΩ at 30-mm and 185- mm distance, worst load, and distance conditions are shown in Fig. 12. With a 2.2-µF decoupling capacitor C_L, WIDE showed a load regulation performance of 1.89 mV/mA with a 20-µs settling time at the 30-mm distance, and a 2.09 mV/mA with a 22-µs settling time at 185-mm distance. It is clearly seen that I_{TX} is maximized (minimized) at long (short) link distance. To decrease the switching loss, only the single power NMOS is activated on 30-mm distance, while all power NMOSs are activated to decrease conduction loss at 185-mm distance. This measurements shows that WIDE regulates V_L successfully even with this wide load and distance variation.

The left figure in Fig. 13 shows the measured V_L at steady state for various load and distance conditions. A 60-Ω load limits the operating link distance up to 185 mm. The state of the arts are compared with WIDE using normalized distance by the area of both TX and RX antennae for fair comparison [18], [25]. Among the state of the arts, WIDE clearly has wide operating link distance and load range. The P_{TX}, P_{OUT}, and E2E PTE are shown on the right side of Fig. 13. Surprisingly, E2E PTE is greater than 5% even at 180-mm distance. The Table I summarizes and compares the presented WIDE with recent state-of-the-art WPT systems supporting wide distance and load variations. With the presented design, up to 150-mW PDL at 185-mm distance which is enough to support the biometric smartcard

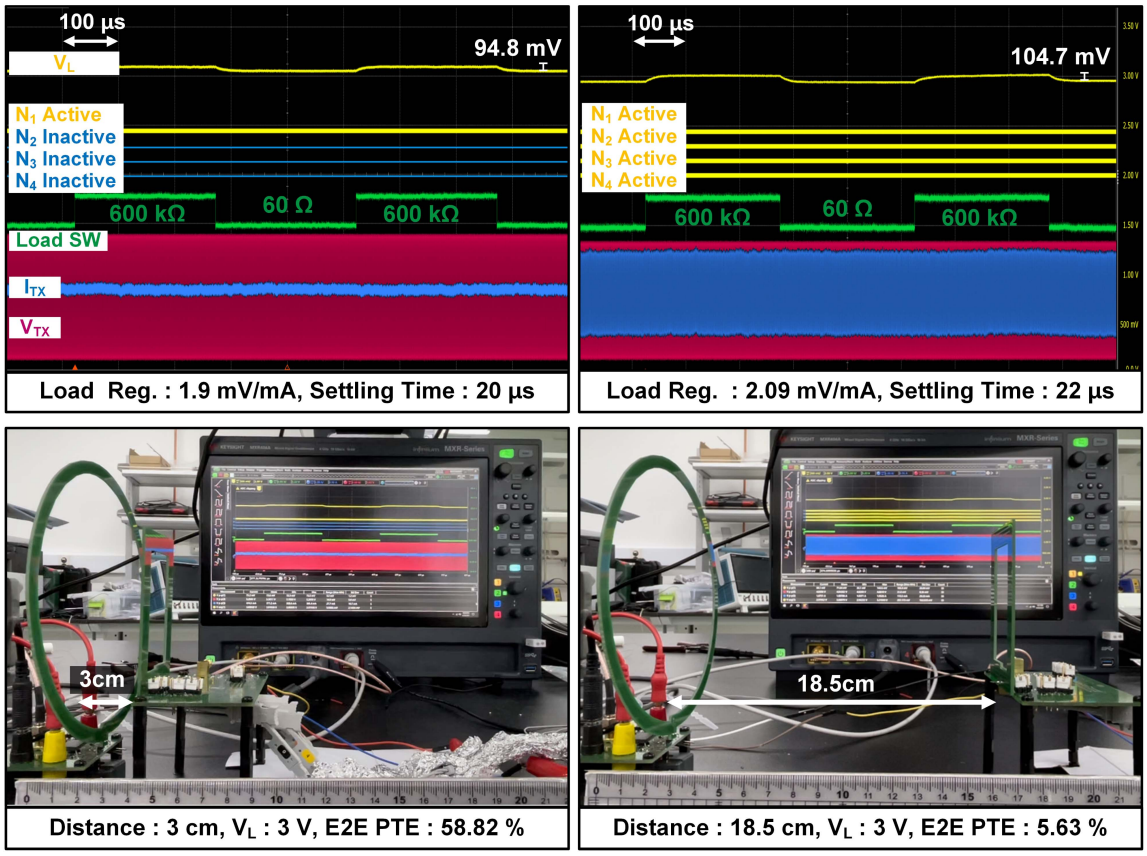


Fig. 12. Measured waveforms and setups for load transients varying from 60 Ω to 600 kΩ at two different link distances 30 and 185 mm.

TABLE I
COMPARISON TABLE

	JSSC'15 [15]	ISSCC'15 [16]	JSSC'18 [17]	JSSC'19 [18]	JSSC'17 [13]	TPE'21 [12]	TPE'22 [8]	ASSCC'21 [11]	This Work	
Max. Distance w/ V_L Reg. [mm] (no regulation***)	20	18.5	11.5	42	135	16	N/A (32***)	N/A	185	
Normalized Max. Distance (no regulation***)	1.02*	0.849*	0.43*	1.4	1.675	0.44	N/A (1.32***)	N/A	1.791	
Load Range w/ V_L Reg. [Ω] @ Distance	216 – 1296 (6×) @ 10 mm	N/A	120 – 15k (125 ×) @ 6 mm	22.5 – 900 (40×) @ 20 mm	512 – 102k (200×) @ 45 mm	5.5 – 275 (50×) @ 12 mm	N/A	N/A	60 – 600k (10000×) @ 185 mm	
Transient Load Reg. @ Load Conditions [Ω] (Load Variation)	3.62 mV/mA @ 216 – 1296 (6×)	2.06 mV/mA @ 136.9 –1369 (10×)	0.9 mV/mA @ 150 – 15k (100×)	N/A	83.3 mV/mA (VM) 244 mV/mA (CM) @ 10k – 100k (10×)	1.06** mV/mA @ 5.5 – 275 (50×)	N/A	N/A	30 mm Dist.	1.89 mV/mA @ 60–600k (10000×)
									185 mm Dist.	2.09 mV/mA @ 60–600k (10000×)
Max. P_{OUT} [mW] @ Distance	102 @ 3 mm	30 @ 18.5 mm 234 @ 3 mm	49.4 @ N/A	93.8 @ N/A	20 @ N/A	1980 @ 12 mm	112 @ 10 mm	257** @ N/A	150 @ 185 mm 150 @ 30 mm	
Rx Structure	VM	VM	VM	VM	VM-CM	CM	CM	CM	CM	
TX Power Adjustment Method	Active / LSK	Active / LSK	Active / LSK	Active / TX Freq. Tracking	N/A	N/A	N/A	N/A	Passive / Reflected Impedance	
Active Area [mm²]	2.143**	2.344**	0.464	0.39**	0.52	0.652	0.54	0.41	0.14	
Settling Time for Load Reg. @ Distance	130 µs @ 10 mm	2000 µs	0	N/A	N/A	2.5** µs @ 12mm	N/A	N/A	20 µs @ 30 mm 22 µs @ 185 mm	
Freq. (MHz)	13.56	13.56	13.56	1.7 to 30	1	6.78	5	27.12	13.56	
CMOS Tech.	350	350	65	180	350	180	180	180	65	

Normalized distance : $d/\sqrt{4r_{TX}r_{RX}}$ (d : distance between TX-RX antennae, r_{TX} : radius of TX antenna, r_{RX} : radius of RX antenna)
Square coils normalized to circular shape with the same area
* Include detection coil
** Value extracted from included figure
*** No voltage regulation

	TX	RX
Outer Antenna Size	15 cm (diameter)	55 mm × 86 mm
Inductance @ 13.56 MHz	1.71 µH	2.12 µH
Quality Factor @ 13.56 MHz	167	177

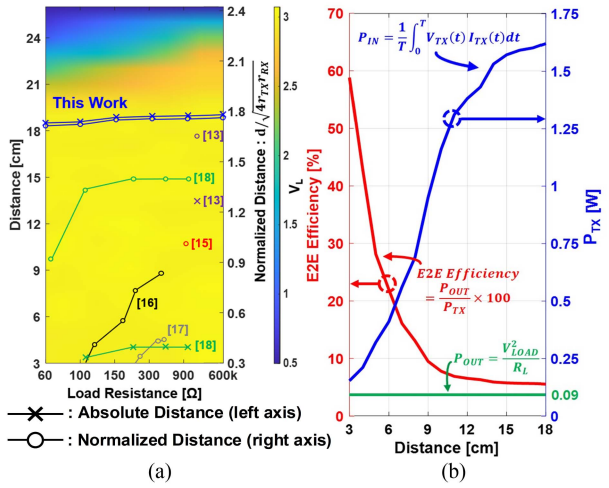


Fig. 13. (a) Measured V_{L} with various distance and load conditions. x and o are marked at the maximum absolute and normalized distance, respectively, driving a load with successful voltage regulation to target voltages. (b) E2E PTE, P_{TX}, and P_{L} are measured at various absolute link distance with a regulated V_{L} to 3 V.

application is achieved. Table I gives a comparison summary with state-of-the-art works. WIDE achieves the widest distance, load range with V_{L} regulation, and fast settling time.

V. Conclusion

This article presents a WPT system working over an increased dynamic range of link distance and load with extended controllability of transmitting power. To widen operating link distance and load range, P_{TX} is controlled from the RX that accommodates large energy owing to the series-connected LC tank. For mode transitions between resonance and charging modes, WIDE supports accurate and energy-efficient zero current detection owing to the presented WOWN rising edge detector and the $\Delta\Sigma$-based falling edge detector from a 13.56-MHz sinusoidal waveform. Furthermore, the $\Delta\Sigma$-based voltage regulation controller allows single-stage rectification and regulation with fast transient response under wide link distance and load variation. The presented WIDE is fabricated in a 65-nm standard CMOS process, occupying 0.14-mm^2 active area. Measurement results show its superiority in supporting wide link distance and load dynamic range along with fast transient responses.

References

[1] M. Ghovanloo and K. Najafi, "A wideband frequency-shift keying wireless link for inductively powered biomedical implants," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 12, pp. 2374–2383, Dec. 2004.

[2] P. Rakers, L. Connell, T. Collins, and D. Russell, "Secure contactless smartcard ASIC with DPA protection," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 559–565, Mar. 2001.

[3] P. K. Chan, C. S. Choy, C. F. Chan, and K. P. Pun, "Preparing smartcard for the future: From passive to active," *IEEE Trans. Consum. Electron.*, vol. 50, no. 1, pp. 245–250, Feb. 2004.

[4] Y. Lu and D. B. Ma, "Wireless power transfer system architectures for portable or implantable applications," *Energies*, vol. 9, no. 12, 2016.

[5] K.-G. Moh et al., "12.9 A fully integrated 6 W wireless power receiver operating at 6.78 MHz with magnetic resonance coupling," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Techn. Papers*, 2015, pp. 1–3.

[6] J.-H. Choi, S.-K. Yeo, S. Park, J.-S. Lee, and G.-H. Cho, "Resonant regulating rectifiers (3R) operating for 6.78 MHz resonant wireless power transfer (RWPT)," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 2989–3001, Dec. 2013.

[7] M. Choi, T. Jang, J. Jeong, S. Jeong, D. Blaauw, and D. Sylvester, "A current-mode wireless power receiver with optimal resonant cycle tracking for implantable systems," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2016, pp. 372–373.

[8] H.-S. Lee et al., "A power-efficient resonant current mode receiver with wide input range over breakdown voltages using automated maximum efficiency control," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8738–8750, Jul. 2022.

[9] S.-W. Hong, "A 13.56 MHz current-mode wireless power and data receiver with efficient power extracting controller and energy-shift keying technique for loosely coupled implantable devices," in *Proc. IEEE Int. Solid- State Circuits Conf.*, 2020, pp. 486–488.

[10] H. S. Gougheri and M. Kiani, "Current-based resonant power delivery with multi-cycle switching for extended-range inductive power transmission," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 9, pp. 1543–1552, 2016.

[11] Z. Luo and H. Lee, "A 87.2%-Efficiency 27.12 MHz current-mode wireless power receiver with ramp-assisted energy delivery controller for implantable devices," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2021, pp. 1–3.

[12] J. Lin, C. Zhan, and Y. Lu, "A 6.78-MHz single-stage wireless power receiver with ultrafast transient response using hysteretic control and multilevel current-wave modulation," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 9918–9926, Sep. 2021.

[13] M. Sadeghi Gougheri and H. Kiani, "Self-regulated reconfigurable voltage/current-mode inductive power management," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 3056–3070, Nov. 2017.

[14] H. Sadeghi Gougheri and M. Kiani, "An inductive voltage-/current-mode integrated power management with seamless mode transition and energy recycling," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 874–884, Mar. 2019.

[15] X. Li, C.-Y. Tsui, and W.-H. Ki, "A 13.56 MHz wireless power transfer system with reconfigurable resonant regulating rectifier and wireless power control for implantable medical devices," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 978–989, Apr. 2015.

[16] C.-Y. Li, X. Tsui, and W.-H. Ki, "Wireless power transfer system using primary equalizer for coupling- and load-range extension in bio-implant applications," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2015, pp. 1–3.

[17] C. Huang, T. Kawajiri, and H. Ishikuro, "A 13.56-MHz wireless power transfer system with enhanced load-transient response and efficiency by fully integrated wireless constant-idle-time control for biomedical implants," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 538–551, Feb. 2018.

[18] J. Pan, A. A. Abidi, W. Jiang, and D. Marković, "Simultaneous transmission of up to 94-mw self-regulated wireless power and up to 5-Mb/s reverse data over a single pair of coils," *IEEE J. Solid-State Circuits*, vol. 54, no. 4, pp. 1003–1016, Apr. 2019.

[19] J. Tang, L. Zhao, and C. Huang, "33.6 A wireless power transfer system with Up-to-20% light- load efficiency enhancement and instant dynamic response by fully integrated wireless hysteretic control for bioimplants," in *Proc. IEEE Int. Solid- State Circuits Conf.*, vol. 64, 2021, pp. 470–472.

[20] C. Kim, S. Ha, J. Park, A. Akinin, P. P. Mercier, and G. Cauwenberghs, "A 144-MHz fully integrated resonant regulating rectifier with hybrid pulse modulation for mm-sized implants," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 3043–3055, Nov. 2017.

[21] *Identification Cards-Contactless Integrated Circuit(s) Cards-Proximity Cards*, ISO/IEC standard 10373, Geneva, Switzerland.

[22] *Identification Cards-Contactless Integrated Circuit(s) Cards-Proximity Cards*, ISO/IEC standard 14443, Geneva, Switzerland.

[23] C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs, "Sub-μVrms-Noise Sub-μW/Channel ADC-Direct neural recording with 200-mV/ms transient recovery through predictive digital autoranging," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3101–3110, Nov. 2018.

[24] C. Kim et al., "A 3 mm $\times$3 mm fully integrated wireless power receiver and neural interface system-on-chip," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 6, pp. 1736–1746, Dec. 2019.

[25] D. Ahn, S. Kim, J. Moon, and I.-K. Cho, "Wireless power transfer with automatic feedback control of load resistance transformation," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7876–7886, Nov. 2016.

Hongkyun Kim (Student Member, IEEE) received the B.S. degree in electrical engineering from Kyunghee University, Suwon, South Korea, in 2016, and the M.S. degree in 2018 from the Graduate School for Green Transportation Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, where he is currently working toward the Ph.D. degree in bio and brain engineering.

His research interests include wireless power transfer system and power management ICs.

Yechan Park (Student Member, IEEE) received the B.S. degree in electrical engineering from Ajou University, Suwon, South Korea, in 2017, and the M.S. degree in electrical engineering in 2020 from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, where he is currently working toward the Ph.D. degree in electrical engineering with KAIST.

His research interests include the design of integrated circuits and systems for emerging biomedical applications, including wireless power transmission ICs, wireless communication ICs, and power management ICs.

Dr. Park was the recipient of the Bronze Prize in the 27th Humantech Paper Award from Samsung Electronics, Suwon, South Korea, in 2021.

Chul Kim (Senior Member, IEEE) received the Ph.D. degree in bioengineering from the University of California San Diego, La Jolla, CA, USA, in 2017.

He is currently an Assistant Professor with the Department of Bio and Brain Engineering, and the Program of Brain and Cognitive Engineering, Korea Advanced Institute of Science and Technology, Daejeon, South Korea. From 2009 to 2012, he was with SK HYNIX, Icheon, South Korea, where he designed power management circuitry for dynamic random-access memory. From 2017 to 2019, he was a Postdoctoral Fellow with the University of California. His current research interests include the design of energy-efficient integrated circuits and systems for fully wireless brain-machine interfaces and unobtrusive wearable sensors.

Dr. Kim was the recipient of the Gold Prize in the 16th Humantech Thesis Prize Contest from Samsung Electronics, Suwon, South Korea, in 2010, 2018 Shunichi Usami Ph.D. Thesis Design Award from the Bioengineering Department, UC San Diego, and 2017–2018 IEEE Solid-State Circuits Society Predoctoral Achievement Award. He was the Guest Editor of IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS for the special issue of ISCAS2020. Since 2020, he has been an Associate Editor for IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, and the Technical Program Committee for IEEE Custom Integrated Circuits Conference (CICC). He is the Co-Editor of the High-Density Integrated Electrocortical Neural Interfaces: Low-Noise Low-Power System-on-Chip Design Methodology (Academic Press, 2019).