Virtual Admittance Reshaping Based Input Current Phase Shift Suppression Method for Totem-Pole Bridgeless PFC Converter

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***Abstract*—Grid-side current phase shift (GCPS) is an important issue in totem-pole bridgeless power factor correction (TBPFC) converters. In this article, a virtual admittance reshaping based GCPS suppression method is proposed based on the establishment of the admittance model of the TBPFC converter including the EMI filter. The virtual admittance reshaping does not need additional current and voltage sensors and can realize complex admittance through a control algorithm. Thus, the current phase error can be adjusted to zero with the optimal design. The inherent admittance of the system is analyzed from the perspective of system frequency characteristics to extract leading-phase admittance. Then, the parallel admittance is produced through the inductance current for canceling it. The current reference and the modulation voltage are combined to realize obtaining the equivalent virtual admittance and meanwhile reduce the burden of the current regulator. The sensitivity of the system parameters is analyzed, and the saturation effect of the inductor and the error of the EMI filter parameters have little effect on admittance reshaping. Besides, the research method does not need to adjust parameters according to the load. The effectiveness of the proposed method is verified by experiments on a TBPFC converter platform.**

***Index Terms*—Admittance model, grid-side current phase shift (GCPS), high power factor, totem-pole bridgeless PFC (TBPFC) converter, virtual admittance.**

I. Introduction

TOTEM-POLE bridgeless power factor correction (PFC) topology has the advantages of low electromagnetic interference (EMI), simple main circuit structure, and high device utilization [1], [2], [3], [4], [5], so it has a good application prospect in high efficiency and high power density occasions. Due to the rapid development of wide-bandgap devices, the use of GaN power devices enables the totem-pole bridgeless PFC (TBPFC) topology to operate in the continuous conduction mode (CCM). This topology can be applied to higher power occasions and it can improve converter efficiency [6], [7], [8], [9]. In applications such as variable-frequency air conditioners, the converter operates in a heavy load state at the beginning and a light load state for more time, so it is important to improve the power quality of the converter under light load.

Due to the bandwidth limitation of the current controller, as well as the EMI filter, the grid-side current phase shift

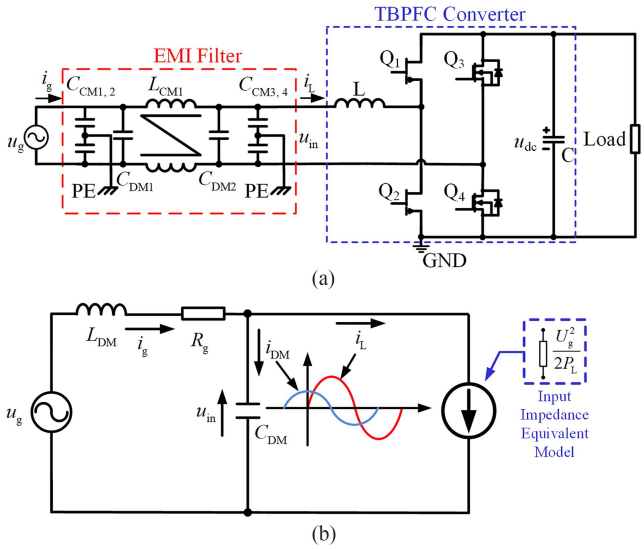

Fig. 1. Topology and equivalent model of the TBPFC converter. (a) Topology circuit. (b) Equivalent model.

TABLE I
TBPFC Converter Parameters

Parameters	Value
Rated power (W)	1500
Switching frequency (kHz)	150
Grid frequency (Hz)	50
Boost inductance (μH)	500
Dc-link capacitance (μF)	940
Differential capcitance (μF)	4
Differential inductance (μH)	80
Common mode capacitance (nF)	5.1
Common mode inductance (mH)	4

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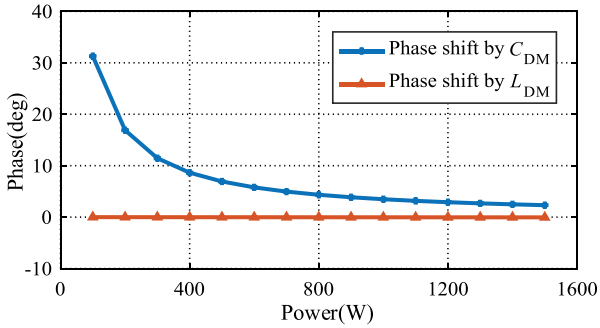

Fig. 2. GCPS caused by EMI filter in different load conditions.

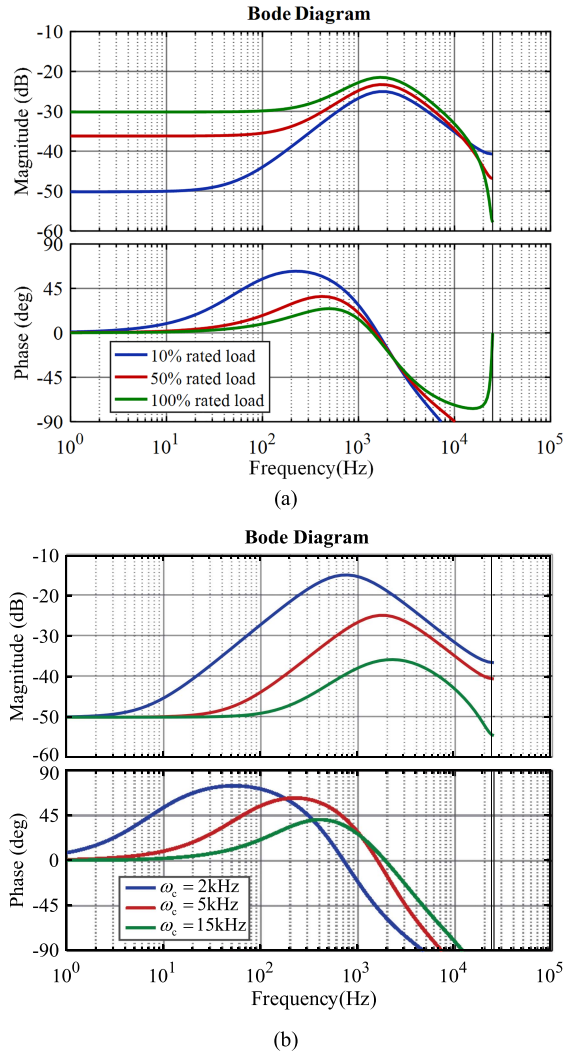

Fig. 3. Bode diagrams of system input admittance. (a) Under different loads. (b) Under different current loop bandwidths.

(GCPS) and zero-crossing point distortion become more serious at light load conditions. Hence, the power factor and total harmonic distortion (THD) of the TBPFC converter with the average current control strategy get deterioration. In the CCM boost PFC converter, the GCPS phenomenon occurs when the ratio of the input current control bandwidth to the power frequency is low. This is because the input admittance contains a leading-phase admittance term, and its amplitude at the power frequency increases as the control bandwidth decreases.

The commonly used suppression measures for the GCPS can be classified into two categories: increasing the control bandwidth and modifying the control loop. Increasing control bandwidth based methods can reduce the proportion of the leading-phase admittance term, thus suppressing the GCPS. The traditional implementation method is to redesign the boost converter according to the control objective, such as reducing the boost inductance, increasing the switching frequency, etc. With these measures, the current loop has a higher bandwidth, but these measures may lead to lower converter efficiency. In such methods of increasing the control bandwidth, using the nonlinear controller is a kind of effective way to suppress the current phase shift [10], [11], [12], [13], [14], [15], [16], [17]. In [11], a predictive control algorithm with conduction-mode detection for PFC converter was proposed. This method can reduce the line current distortion and approach a unity PF. However, the calculation time of this method is large [18]. Besides, the current tracking performance is dependent on the accuracy of the component parameters. For the application of air-conditioning compressor drive, the microcontroller not only controls the PFC stage but also controls the compressor.

Modifying control loop based methods can use a linear controller and design a reasonable additional admittance compensator to cancel out the leading phase admittance. It is more suitable for the application of holding little calculation resources. Most methods are achieved by an additive duty-cycle feedforward controller. The causes of current distortion were analyzed by modeling the input admittance and the compensation admittance was designed in [19] and [20]. The virtual admittance reshaping method does not need additional sensors and the calculation time is short, which does not affect the control of the compressor. In [19], a leading-phase admittance cancellation method based on virtual admittance reshaping was investigated. However, this method ignores the influence of the input filter.

The admittance characteristics of the system were analyzed under different operating modes, and a feedforward component was designed to reduce the current distortion of the converter in discontinuous current mode (DCM) [21]. Applying duty cycle feedforward can reduce the burden of the current loop regulator. At the same time, it has a good effect on suppressing GCPS in average current control, even if the current control bandwidth is lower than several thousand Hertz. Besides, it can reduce the zero-crossing distortion of input current caused by the difference of current regulation ability between DCM and CCM, and maintain the stability of input impedance [21], [22], [23]. However, they cannot compensate the circulating filter current, since the underdamped characteristics of the current control closed-loop system will lead to current oscillation [19].

However, these models ignored the EMI filter, which cannot accurately reflect the GCPS, especially for the GaN-based

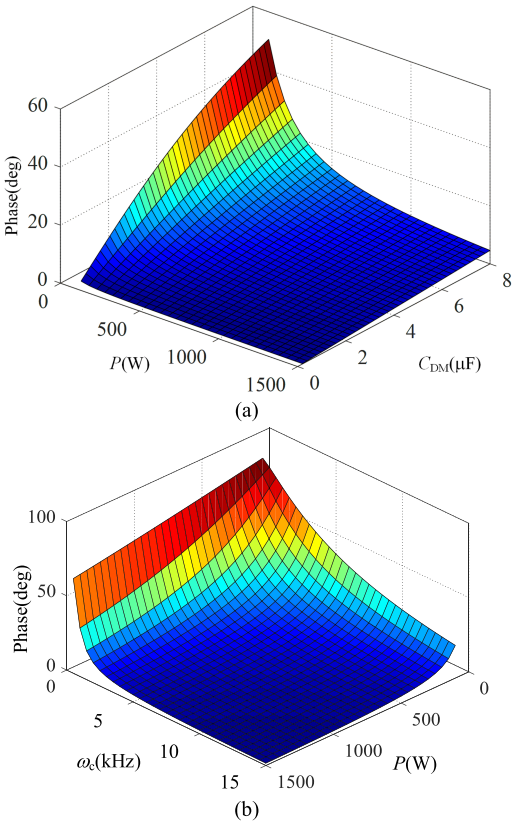

Fig. 4. Relationship among C_{DM}, φ_{g1}, φ_{g2}, and ω_{c} in various load conditions. (a) φ_{g1} versus C_{DM}. (b) φ_{g2} versus ω_{c}.

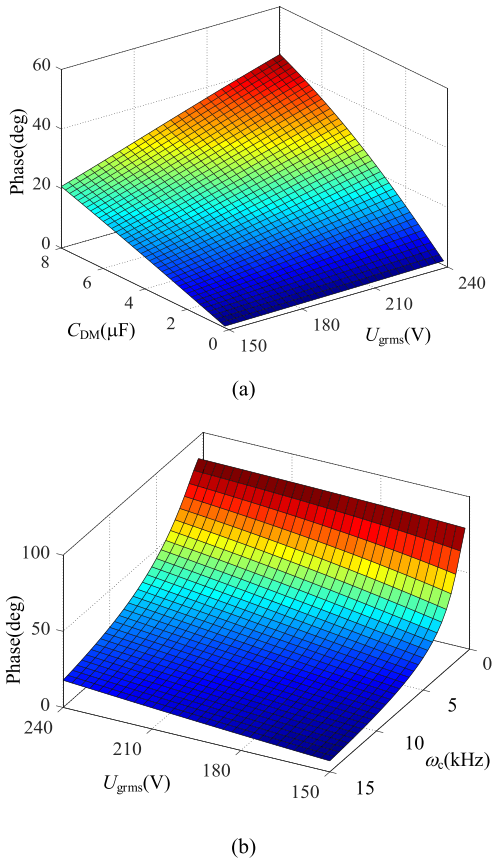

Fig. 5. Relationship among C_{DM}, φ_{g1}, φ_{g2}, and ω_{c} in various grid-side voltage conditions. (a) φ_{g1} versus C_{DM}. (b) φ_{g2} versus ω_{c}.

TBPFC converter. Because of the high switching speed, the component values of the EMI filter are larger than those in the conventional boost PFC converter. The influence of the EMI filter can no longer be ignored so it is necessary to consider the EMI filter when modeling the current phase shift. To solve this problem, researchers have proposed a variety of differential mode capacitor current compensation strategies [24], [25], [26], [27], [28], [29]. The phase-leading filter current compensation methods were researched in [24], [25], and [27]. The strategy in [24] also considered the current offset but the parameters need to be determined according to the actual test. The performance in DCM mode and CRM mode were concerned in [25] and [27]. The above-mentioned methods can effectively suppress GCPS caused by differential mode capacitor current. In all, the methods are analyzed and designed based on time-domain, which causes the influence principle indeterminacy and needs to be researched in advance under the different operating conditions.

This article proposes a GCPS suppression method based on virtual admittance reshaping for the TBPFC converter to deal with the phase-leading phenomenon. Compared with the previous works, the proposed method establishes an input admittance model considering the input filter and the nonideal behaviors of the digital current controller. It can accurately estimate the current phase shift at different loads. Based on it, the influence principles of the EMI filter and the current loop bandwidth limitation are revealed and the reasonable virtual admittance is designed and paralleled with the system equivalent admittance. Besides, the sensitivity of the above-mentioned two factors is analyzed. The expected virtual admittance current is generated by using the sampled value of the input voltage. Then, the equivalent virtual admittance current is obtained by configuring the combination of the current reference and the modulation voltage. Through this measure, the command complexity and the burden of the current regulator can be reduced. The sensitivity of the admittance reshaping effect to the inductance saturation effect and EMI filter parameter error is analyzed. The proposed method has strong adaptability to parameters, without adjusting parameters according to load changes and adding additional current and voltage sensors.

This article is organized as follows. In Section II, the principles of GCPS caused by the EMI filter and current loop bandwidth limitation are analyzed. Then, the input admittance model of the system is established in Section III. Moreover, the virtual admittance reshaping based GCPS suppression strategy is introduced. Finally, experimental results are provided in Section IV to verify the effectiveness and feasibility of the proposed method.

II. Analysis of GCPS Phenomenon in TBPFC Converter

A. GCPS Caused by EMI Filter

The topology of the TBPFC converter is shown in Fig. 1(a). The CCM PFC converter adopts a C-L-C structure EMI filter with a simple structure and small magnetic components. When

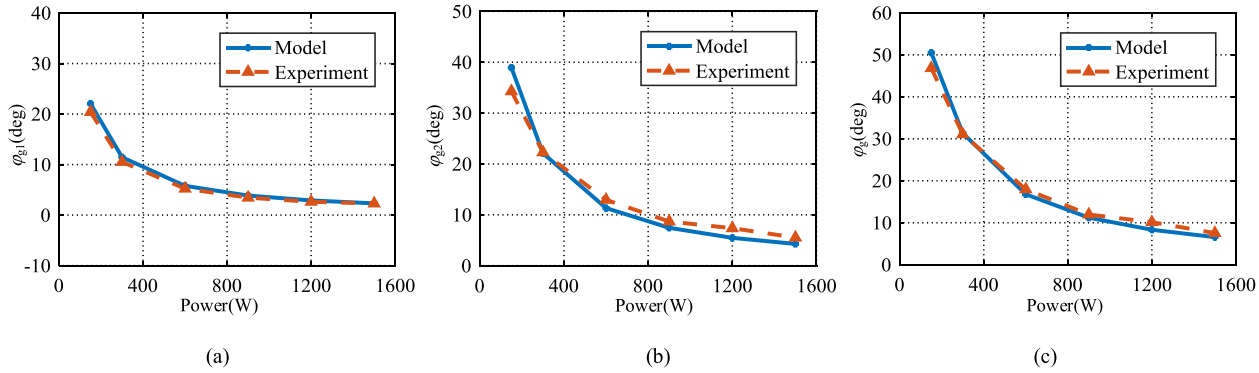

Fig. 6. Comparisons of the model analysis results and experimental results of φ_{g}, φ_{g1}, and φ_{g2}. (a) Comparison of φ_{g1}. (b) Comparison of φ_{g2}. (c) Comparison of φ_{g}.

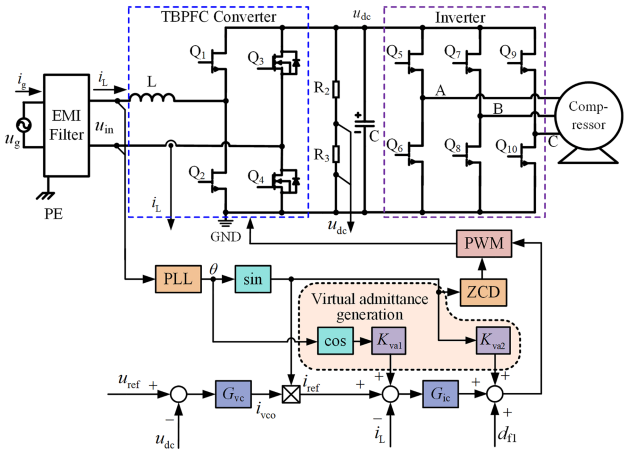

Fig. 7. Control diagram of TBPFC converter based on virtual admittance reshaping.

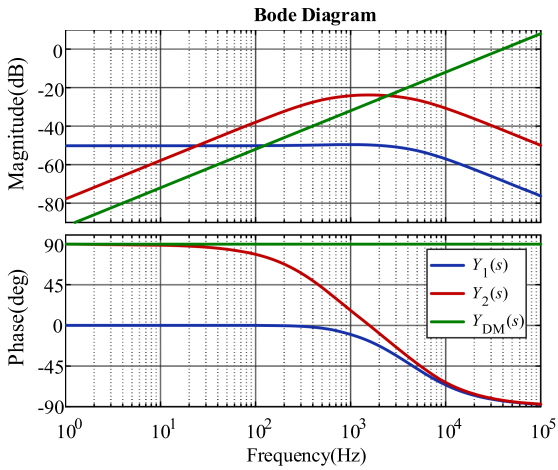

Fig. 9. Bode diagrams of $Y_1(s)$, $Y_2(s)$, and $Y_{\mathrm{DM}}(s)$.

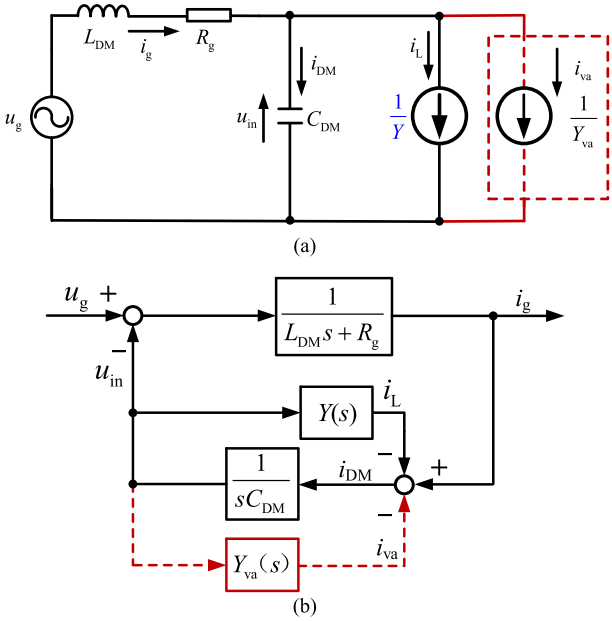

Fig. 8. Proposed GCPS suppression strategy based on virtual admittance reshaping. (a) Equivalent model. (b) Control block diagram.

the current flows through the common-mode inductance, the current generates opposite magnetic fields in the inductive coils wound in the same phase and cancels each other out [17]. At the same time, due to the limitation of the leakage current value allowed in the relevant safety standards, the common-mode capacitor is generally at the nanofarad level. Therefore, the influence of the common mode capacitor and common mode inductance in the EMI filter on the current phase can be ignored. To sum up, the influence of the EMI filter on the current phase is mainly determined by the differential mode capacitance and differential mode inductance.

In order to analyze the influence of the EMI filter on GCPS, the following assumption is made firstly: The TBPFC converter after the EMI filter is regarded as an approximately constant power load and operating under ideal power factor conditions [25]. In this condition, the topology in Fig. 1(a) can be equivalent to the equivalent model of the converter shown in Fig. 1(b). The state equation of the system can be expressed as follows:

$$\begin{cases} L_{\mathrm{DM}} \frac{di_{\mathrm{g}}}{dt} = u_g - R_{\mathrm{g}} i_{\mathrm{g}} - u_{\mathrm{in}} \\ C_{\mathrm{DM}} \frac{du_{\mathrm{in}}}{dt} = i_{\mathrm{g}} - i_{\mathrm{L}} \end{cases} \tag{1}$$

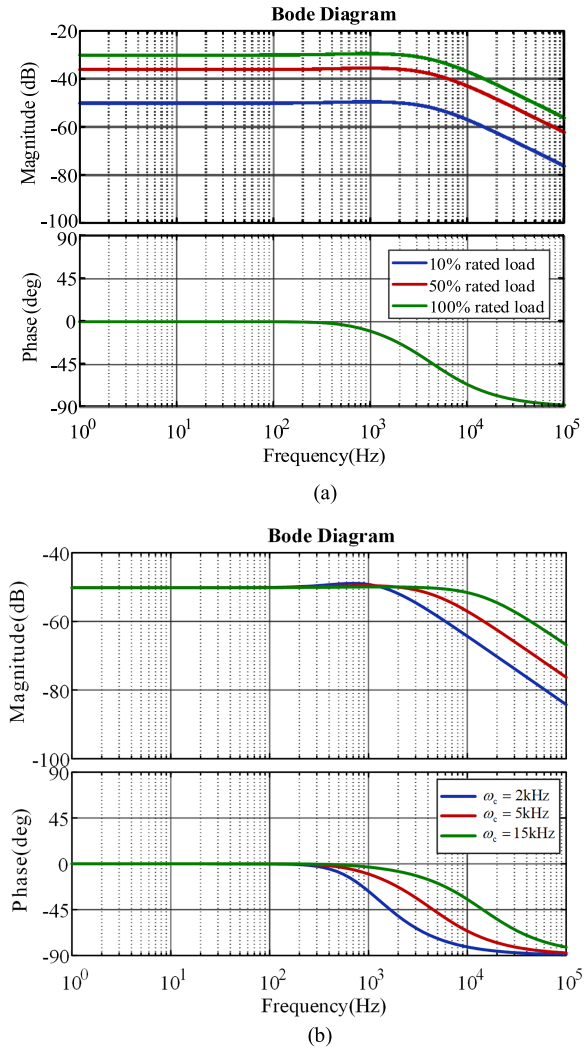

Fig. 10. Bode diagrams of system input admittance after enabling the proposed method. (a) Under different loads. (b) Under different current loop bandwidth.

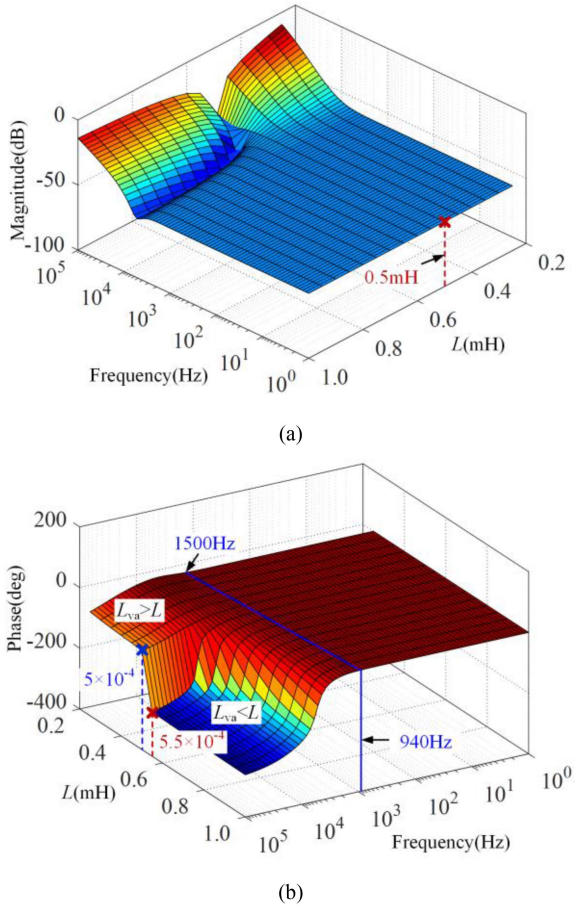

Fig. 11. System frequency characteristics when paralleling virtual elements under different boost inductance. (a) Magnitude diagram. (b) Phase diagram.

where u_g, u_{in}, i_g, and i_L are the grid-side voltage, the PFC converter input voltage, the grid-side current, and the inductor current, respectively. L_{DM}, R_g, and C_{DM} are the differential mode inductance, the circuit resistance, and the differential mode capacitance, respectively.

According to the approximate constant power characteristic of the converter, the input current of the PFC converter can be expressed as follows:

$$i_L = u_{in}\frac{2P_L}{U_g^2} \tag{2}$$

where P_L is the power of load, and U_g is the magnitude value of the grid-side voltage.

The system admittance can be expressed as follows:

$$Y_g(s) = i_g/u_g = (sC_{DM}U_g^2 + 2P_L)/(s^2L_{DM}C_{DM}U_g^2 + s(R_gC_{DM}U_g^2 + 2P_LL_{DM}) + 2P_LR_g + U_g^2). \tag{3}$$

$$Y_g(s) \approx \frac{sC_{DM}U_g^2 + 2P_L}{s(R_gC_{DM}U_g^2 + 2P_LL_{DM}) + U_g^2} \approx \frac{2P_LU_g^2 + s(C_{DM}U_g^4 - 4P_L^2L_{DM})}{(R_gC_{DM}U_g^2 + 2P_LL_{DM})^2\omega_g^2 + U_g^4}. \tag{4}$$

Since $2P_LR_g \ll U_g^2$, ignoring $2P_LR_g$ and higher-order terms, (3) is reduced to (4) where ω_g is the frequency of grid-side voltage.

From (4), the relationship among the system admittance phase φ_{g1}, the differential mode inductance, and differential mode capacitance can be obtained as follows:

$$\tan(\varphi_{g1}) = \omega_gC_{DM}\frac{U_g^2}{2P_L} - \omega_gL_{DM}\frac{2P_L}{U_g^2}. \tag{5}$$

Fig. 2 shows the GCPS caused by C_{DM} and L_{DM} when the grid voltage frequency is 50 Hz, where the grid voltage is 220 V and the converter power range is 100–1500 W. As is known that GaN device has a higher switching speed than Si-based MOSFET and IGBT, thus the switching noise is more serious, which leads to higher requirements for EMI filter. In the EMI filter design process, the design examples in [30] and [31] are referred. In order to reduce the common mode inductance, they choose double stage EMI filter topology. The same topology is

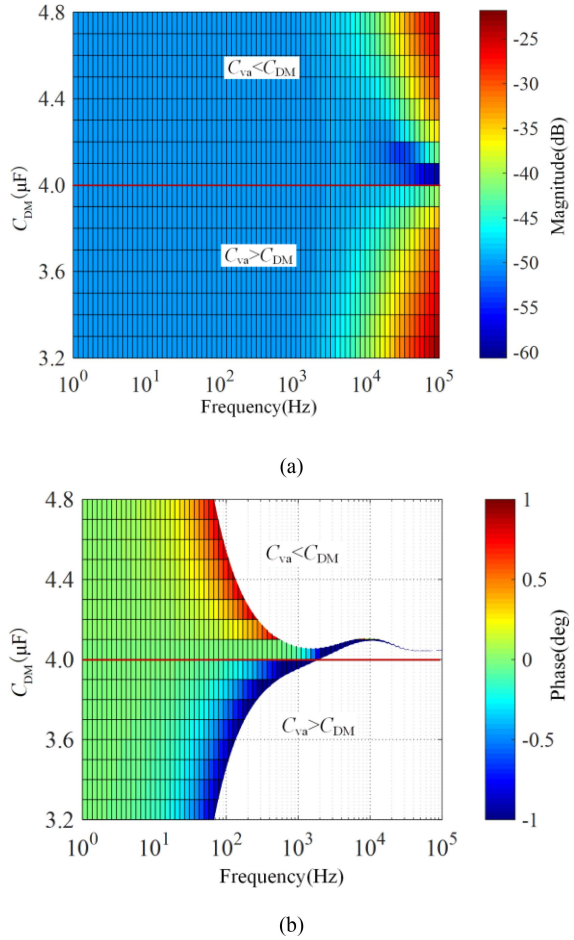

Fig. 12. System frequency characteristics when paralleling virtual elements under different C_{DM}. (a) Magnitude diagram. (b) Phase diagram.

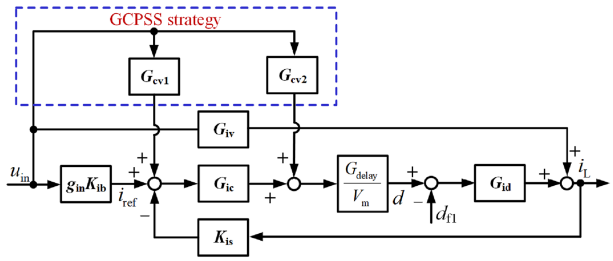

Fig. 13. Block diagram of the current loop with equivalent virtual admittance.

selected in this study. The differential capacitances of them are 4 μF and 5.3 μF, respectively. Corresponding with them, the C_{DM} is composed of two 1 μF and one 2 μF capacitors. The parameters of the EMI filter are shown in Table I.

From (5) and Fig. 2, it can be seen that the current phase shift caused by the differential mode inductance can be ignored. On the other hand, the differential mode capacitance has a greater effect on GCPS, especially under light load conditions. Therefore, the differential mode capacitor is the main cause of the GCPS in the EMI filter, and the differential mode inductance will be ignored in the subsequent analysis.

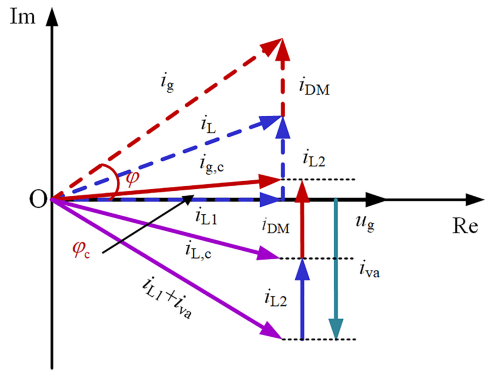

Fig. 14. Schematic diagram of the GCPS phenomenon suppression.

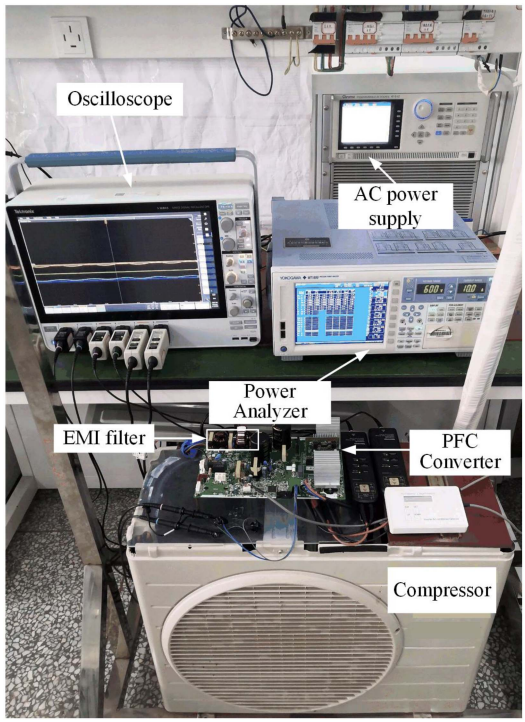

Fig. 15. Experimental platform of TBPFC converter.

B. GCPS Caused by Current Regulator Bandwidth

The current reference of the TBPFC converter using the average current control strategy in CCM is the product of the voltage loop output and the per-unit value of the grid-side voltage. Under steady operation, the output of the voltage loop is considered as a dc value, and then the current reference i_{ref} of the inductor current can be expressed as follows:

$$i_{\mathrm{ref}} = i_{\mathrm{vco}} u_{\mathrm{g\_pu}} = g_{\mathrm{in}} K_{\mathrm{ib}} u_{\mathrm{in}} \tag{6}$$

where i_{vco}, $u_{\mathrm{g\_pu}}$, g_{in}, and K_{ib} are the voltage loop output, the per-unit value of the grid-side voltage, the input admittance, and the reciprocal of the current reference value, respectively.

In the modeling process, the time delay can be equivalent to an inertia element, i.e., $G_{\mathrm{delay}}(s) = e^{-1.5T_s s} \approx 1/(1.5T_s s + 1)$.

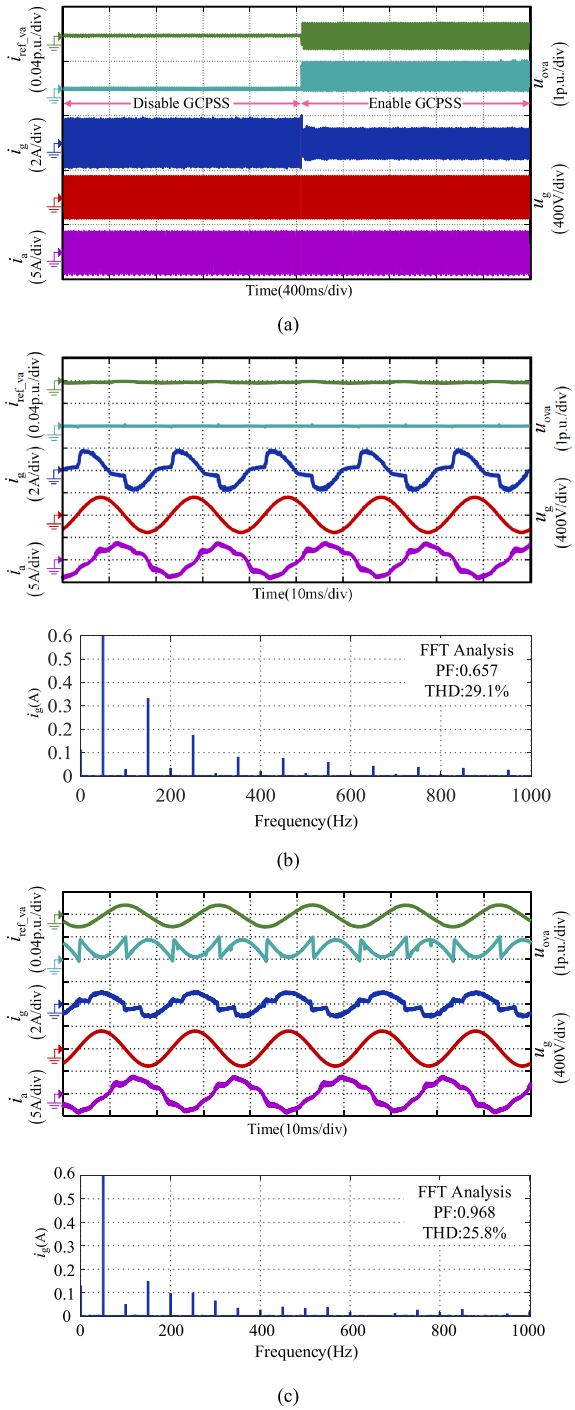

Fig. 16. Experimental results without and with applying the proposed GCPS suppression strategy, when the compressor speed is 15 Hz and the power is 150 W. (a) Process of enabling the proposed GCPS suppression strategy. (b) Without GCPS suppression strategy. (c) With GCPS suppression strategy.

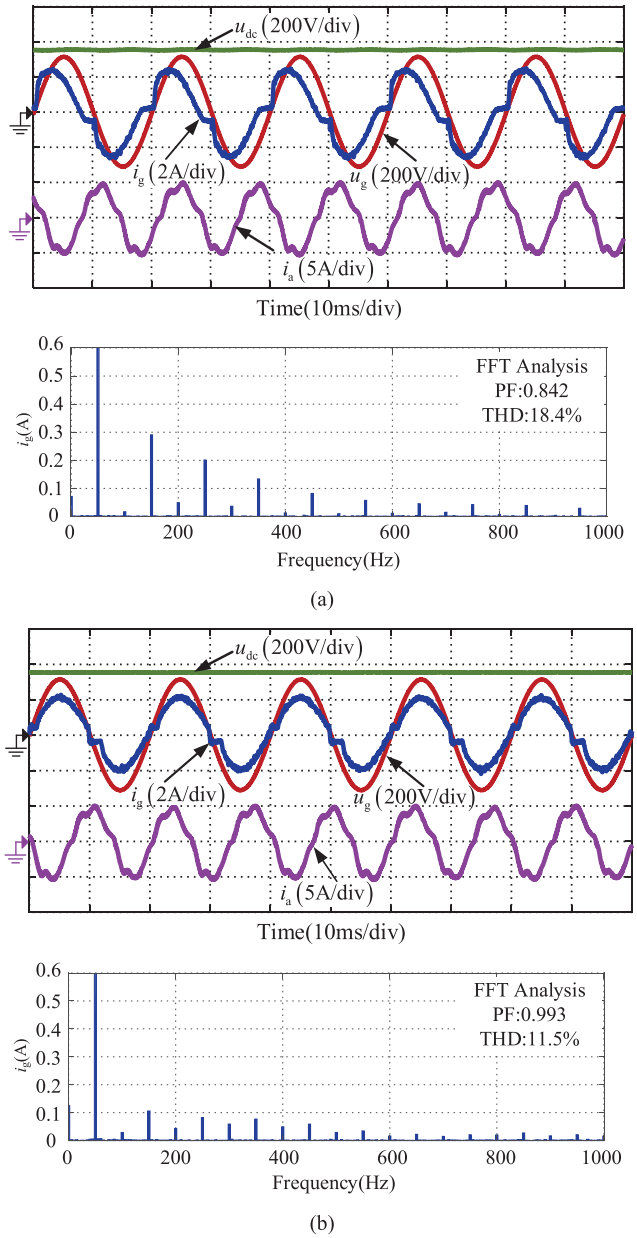

Fig. 17. Experimental results without and with applying the proposed GCPS suppression strategy, when the compressor speed is 25 Hz and the power is 300 W. (a) Without GCPS suppression strategy. (b) With GCPS suppression strategy.

The duty cycle of the main switch can be expressed as follows:

$$D(s) = \frac{U_{\text{ico}}(s)G_{\text{delay}}(s)}{V_{\text{m}}} = \frac{[I_{\text{ref}}(s) - K_{\text{is}}I_L(s)]G_{ic}(s)G_{\text{delay}}(s)}{V_{\text{m}}} \quad (7)$$

where U_{ico}, $1/V_{\text{m}}$, K_{is}, and G_{ic} are the current loop output, the modulator gain, the current feedback gain, and the current loop regulator, respectively.

According to the average model of the inductor current of the PFC converter, the following can be obtained:

$$\frac{di_{\text{L}}}{dt} = \frac{1}{L}[u_{\text{in}}d + (u_{\text{in}} - u_{\text{dc}})(1-d)] = \frac{1}{L}[u_{\text{in}} - u_{\text{dc}}(1-d)] \quad (8)$$

where u_{dc}, L, and d are the dc-link voltage, the value of the boost inductor, and the duty cycle, respectively. According to

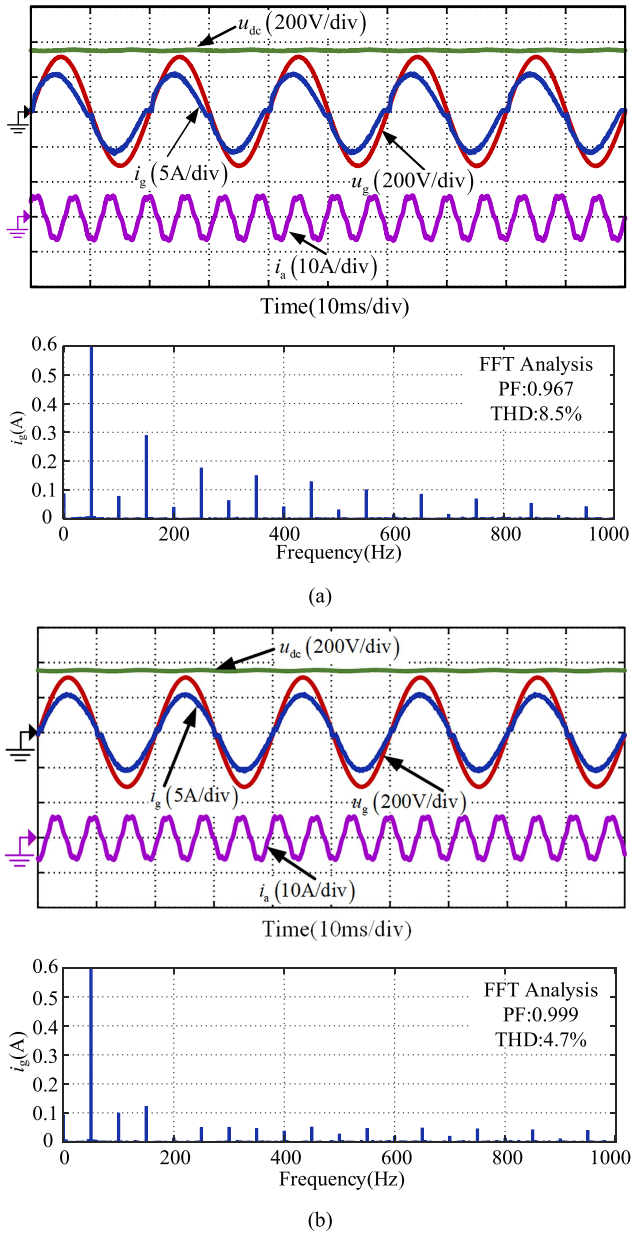

Fig. 18. Experimental results without and with applying the proposed GCPS suppression strategy, when the compressor speed is 53 Hz and the power is 800 W. (a) Without GCPS suppression strategy. (b) With GCPS suppression strategy.

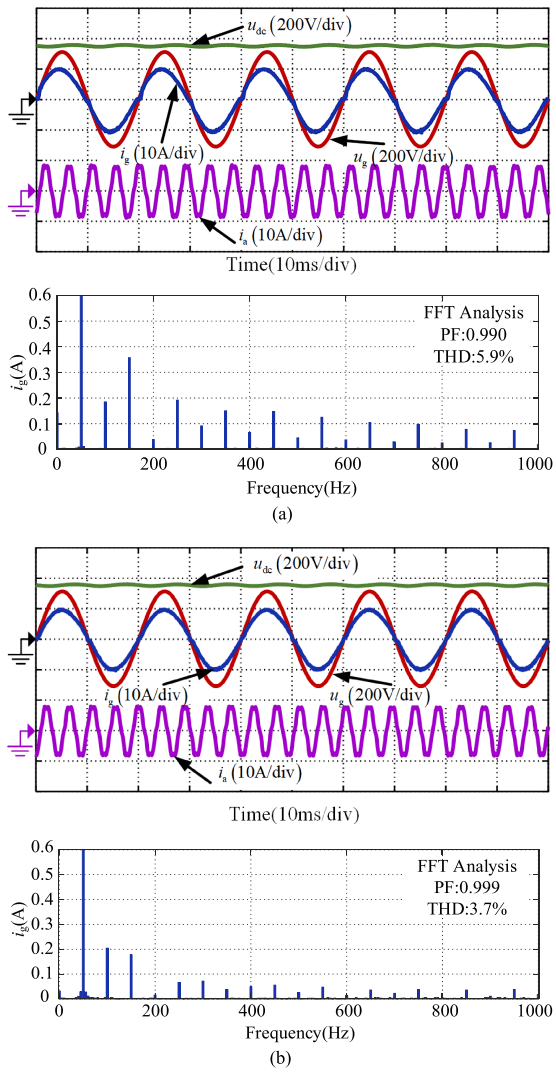

Fig. 19. Experimental results without and with applying the proposed GCPS suppression strategy, when the compressor speed is 75 Hz and the power is 1500 W. (a) Without GCPS suppression strategy. (b) With GCPS suppression strategy.

the Laplace transform of (8), $I_{\mathrm{L}}(s)$ can be expressed as follows:

$$I_{\mathrm{L}}(s) = G_{\mathrm{iv}}(s)U_{\mathrm{in}}(s) + G_{id}(s)\left(D(s) - \frac{1}{s}\right) \tag{9}$$

where $G_{\mathrm{iv}}(s) = 1/(sL)$, $G_{\mathrm{id}}(s) = U_{\mathrm{dc}}/(sL)$, and U_{dc} is the dc component of the dc-link voltage.

The dc-link capacitance is 940 μF. It is large enough that it can be seen as a constant voltage source in the steady state [19], [32]. In addition, the bandwidth of the voltage loop is designed to be 10 Hz to reduce the effect of the output voltage ripple [3]. THD and power factor (PF) are concerned in a steady state. Besides, the process of load change is short, which has little effect on the current THD and PF. In order to simplify the admittance model, the load changes can be ignored as [28], [26].

Ignoring the influence of voltage control loop and load changes, substituting $I_{\mathrm{ref}}(s) = g_{\mathrm{in}}K_{\mathrm{ib}}U_{\mathrm{in}}(s)$ into (7), and substituting $D(s)$ into (9), the relationship between $I_{\mathrm{L}}(s)$ and $U_{\mathrm{in}}(s)$ can be obtained as follows:

$$I_{\mathrm{L}}(s) = \frac{G_{\mathrm{iv}}}{1+T_{\mathrm{i}}}U_{\mathrm{in}}(s) + \frac{g_{\mathrm{in}}K_{\mathrm{ib}}G_{ic}G_{\mathrm{delay}}G_{id}}{V_{\mathrm{m}}(1+T_{\mathrm{i}})}U_{\mathrm{in}}(s) - \frac{G_{\mathrm{id}}}{s(1+T_{\mathrm{i}})} \tag{10}$$

where T_{i} is the loop gain transfer function, $T_{\mathrm{i}} = G_{\mathrm{ic}}G_{\mathrm{delay}}G_{\mathrm{id}}K_{\mathrm{is}}/V_{\mathrm{m}}$.

According to (10), the input admittance of TBPFC converter can be expressed as follows:

$$Y(s) = \frac{I_{\mathrm{L}}(s)}{U_{\mathrm{in}}(s)} = Y_1(s) + Y_2(s) \tag{11}$$

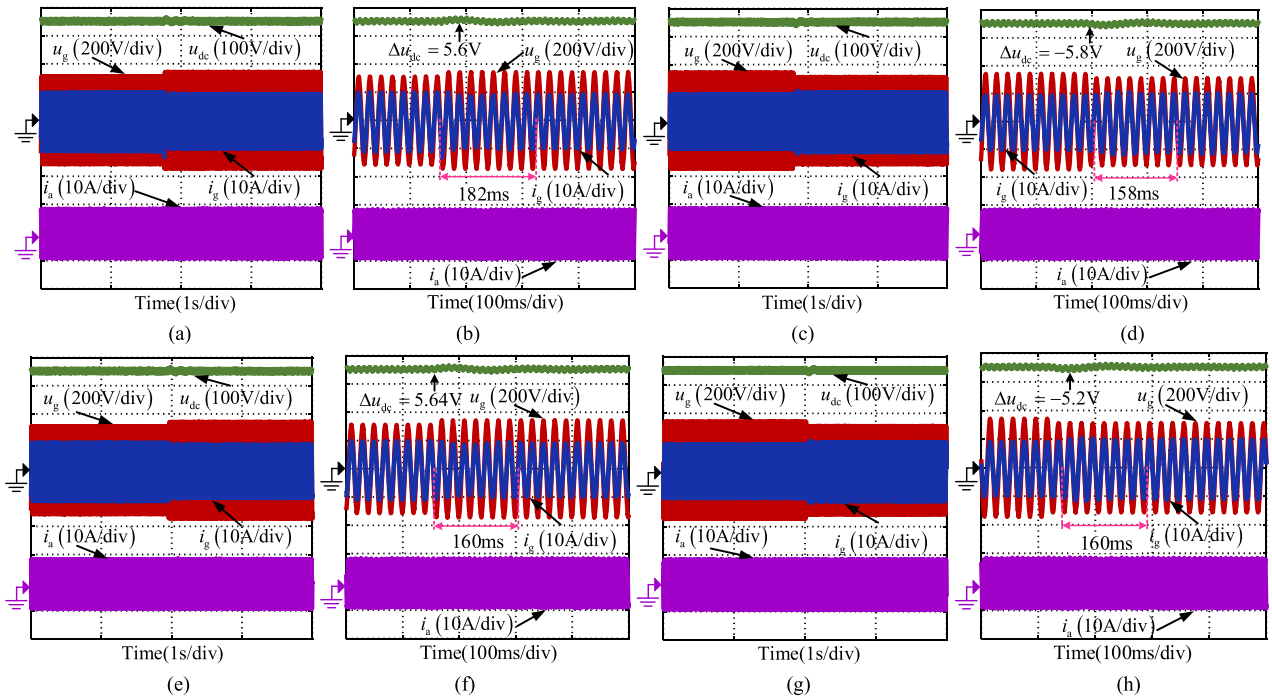

Fig. 20. Experimental waveforms of the PFC converter input voltage step between 220 and 242 V. (a) 220 to 242 V without GCPS suppression strategy. (b) Enlarged view of (a). (c) 242 to 220 V without GCPS suppression strategy. (d) Enlarged view of (c). (e) 220 to 242 V with GCPS suppression strategy. (f) Enlarged view of (e). (g) 242 to 220 V with GCPS suppression strategy. (h) Enlarged view of (g).

where

$$\begin{cases} Y_1(s) = \frac{g_{\text{in}} K_{\text{ib}} G_{\text{ic}} G_{\text{delay}} G_{\text{id}}}{V_{\text{m}}(1+T_{\text{i}})} \\ Y_2(s) = \frac{G_{\text{iv}}}{1+T_{\text{i}}} \end{cases}. \tag{12}$$

It can be seen from the above-mentioned analysis that the relationship between the inductor current and the input voltage of the TBPFC converter based on the average current control strategy satisfies (11). The phase difference between i_{L} and u_{in} is closely related to the current controller G_{ic} and the input admittance g_{in}. The input admittance g_{in} is determined by the load.

In this study, the proportional-integral controller is selected as the current regulator. In order to guarantee an adequate phase margin, the corner frequency f_{L} of the PI controller is chosen to be sufficiently less than the crossover frequency f_{ci}. At frequencies less than f_{L}, the PI compensator improves the rejection of disturbances. Usually, the bandwidth of the current loop is taken as one-tenth of the switching frequency. However, in this study, the switching frequency is 150 kHz, and the control frequency is 50 kHz. Considering the interrupt frequency limitation, 5 kHz is chosen as the current loop bandwidth. The corner frequency f_{L} is designed as one-tenth of the crossover frequency f_{ci}. The f_{ci} is selected as 3.5 kHz. Since f_{L} is sufficiently lower than the f_{ci} then the phase margin is unchanged. Due to the switching frequency being 150 kHz, which is far higher than the current loop bandwidth 5 kHz, the system open loop gain at 150 kHz is lower than −60 dB, thus the high frequency current ripple has been suppressed significantly.

The input admittance model is discretized by the backward difference method. The Bode diagrams of the input admittance of the TBPFC converter are obtained under different load conditions when the current loop bandwidth is set to 5 kHz, as shown in Fig. 3(a). It can be seen that as the power decreases, the phase shift of the inductor current increases from 12° to 24° and 60°. Therefore, the phase shift of the inductor current is more serious under light load conditions. In addition, when the load is 10% of the rated load, the Bode diagram of the PFC converter at different current loop bandwidths is shown in Fig. 3(b). It can be seen that when the current loop bandwidth is reduced, the phase shift of the inductor current is further intensified, rising from 33° to 60° and 75°. Therefore, in order to achieve a high power factor in a wide load range, it is necessary to add a GCPS suppression strategy based on average current control.

$$G(s) = \frac{(g_{\text{in}} K_{\text{ib}} K_{\text{p}} U_{\text{dc}} + V_{\text{m}})s + K_{\text{i}} g_{\text{in}} K_{\text{ib}} U_{\text{dc}} - \omega_{\text{g}}^2 V_{\text{m}} T_{\text{d}}}{(K_{\text{i}} U_{\text{dc}} K_{\text{is}} T_{\text{d}} - \omega_{\text{g}}^2 L V_{\text{m}} T_{\text{d}} + U_{\text{dc}} K_{\text{is}} K_{\text{p}})s + K_{\text{i}} U_{\text{dc}} K_{\text{is}} - \omega_{\text{g}}^2 L V_{\text{m}} - \omega_{\text{g}}^2 U_{\text{dc}} K_{\text{is}} K_{\text{p}} T_{\text{d}}} \tag{14}$$

$$G(s) = \frac{[K_{\text{i}} V_{\text{m}} - K_{\text{i}}^2 g_{\text{in}} K_{\text{ib}} U_{\text{dc}} T_{\text{d}}]s + g_{\text{in}} K_{\text{ib}} U_{\text{dc}} (K_{\text{i}}^2 + \omega_{\text{g}}^2 K_{\text{p}}^2) + \omega_{\text{g}}^2 V_{\text{m}} K_{\text{p}}}{U_{\text{dc}} K_{\text{is}} [\omega_{\text{g}}^2 (K_{\text{i}} T_{\text{d}} + K_{\text{p}})^2 + (K_{\text{i}})^2]}. \tag{15}$$

The GCPS, the part caused by the EMI filter, and the part caused by current loop bandwidth limitation are defined as $\varphi_{\rm g}$, $\varphi_{\rm g1}$, and $\varphi_{\rm g2}$, respectively. The relationship among them is

$$\varphi_{\rm g} = \arctan(\tan(\varphi_{\rm g1}) + \tan(\varphi_{\rm g2})). \tag{13}$$

According to the model in (11), the relationship between $I_{\rm L}(s)$ and $U_{\rm in}(s)$ can be rewritten as follows, (14) and (15) shown at the bottom of the previous page.

Since $K_{\rm i}U_{\rm dc}K_{\rm is} \gg \omega_{\rm g}^2 LV_{\rm m}$, $K_{\rm i} \gg \omega_{\rm g}^2 K_{\rm p}T_{\rm d}$, (14) can be simplified as (15). According to it, the relationship between $\varphi_{\rm g2}$ and the current controller can be expressed as follows:

$$\tan(\varphi_{\rm g2}) = \frac{(K_{\rm i}V_{\rm m} - K_{\rm i}^2 g_{\rm in}K_{\rm ib}U_{\rm dc}T_{\rm d})\omega_{\rm g}}{g_{\rm in}K_{\rm ib}U_{\rm dc}(K_{\rm p}^2\omega_{\rm g}^2 + K_{\rm i}^2) + V_{\rm m}K_{\rm p}\omega_{\rm g}^2}. \tag{16}$$

Based on the above-mentioned analysis, the relationship between $C_{\rm DM}$ and $\varphi_{\rm g1}$, $\omega_{\rm c}$, and $\varphi_{\rm g2}$ in various load conditions are shown in Fig. 4(a) and (b), respectively. As shown in Fig. 4(a), at light load conditions, $\varphi_{\rm g1}$ is sensitive to $C_{\rm DM}$, but at heavy load, $C_{\rm DM}$ has little effect on $\varphi_{\rm g1}$. For example, when $C_{\rm DM}$ increases from 0.2 μF to 8 μF, $\varphi_{\rm g1}$ increases from 1.16° to 39.02° at 150 W, however, $\varphi_{\rm g1}$ increases from 0.11° to 4.48° at 1500 W. As shown in Fig. 4(b), at light load conditions, when $\omega_{\rm c}$ is lower than 8 kHz, $\varphi_{\rm g2}$ is sensitive to $\omega_{\rm c}$. At heavy load conditions, $\varphi_{\rm g2}$ is sensitive to $\omega_{\rm c}$, when $\omega_{\rm c}$ is lower than 3 kHz. In general, increasing $\omega_{\rm c}$ to higher than 3 kHz, the sensitivity of $\varphi_{\rm g2}$ reduces significantly. For example, at 1500 W, $\omega_{\rm c}$ increases from 500 Hz to 3 kHz, $\varphi_{\rm g2}$ reduces from 63.75° to 8.37°, however, $\omega_{\rm c}$ increases from 3 to 15 kHz, $\varphi_{\rm g2}$ reduces only 6.7°.

In various grid-side voltage conditions, the relationships among the phase shift, the EMI filter, and the current loop bandwidth are shown in Fig. 5. As shown in Fig. 5(a), the sensitivity of $C_{\rm DM}$ increases with the increase of the grid-side voltage. However, in different grid-side voltage conditions, the sensitivity of $\omega_{\rm c}$ is almost unchanged. Thus, the phase shift caused by the EMI filter is sensitive to grid-side voltage, but the phase shift caused by the current loop bandwidth limitation is scarcely influenced.

In order to verify the accuracy of the model, compare the modeling results with experimental results at different loads. The comparison results are shown in Fig. 6. It can be seen that the model error at light load is no more than 4°, when the load increase, the model error reduces. The model accuracy can satisfy the requirement and can reflect the experimental results, and the error.

III. Proposed Virtual Admittance Reshaping Based GCPS Suppression Method

The control diagram of the TBPFC converter based on virtual admittance reshaping is shown in Fig. 7. Normally, the output signal of the current regulator is modulated as the control signal of the TBPFC converter. In order to reshape the admittance, the current reference component is obtained according to $u_{\rm in}$. It is superimposed on the current reference, thereby changing the inductor current and suppressing the GCPS. In addition, considering the bandwidth limitation of the current controller, the modulation voltage component is also superimposed on the output of the current regulator, so that the actual current is in the same direction as the current reference vector. In this method, the design of virtual admittance is important. The optimal design of virtual admittance will improve the regulation ability of the current regulator, and the tracking error will be the smallest in this case.

A. Input Admittance Reshaping for PFC Converter

In order to improve the power factor of the PFC converter, the parallel admittance mode at both ends of the differential mode capacitor is considered to suppress the GCPS. This method can reshape the input admittance of the PFC converter so that the impedance at the grid-side voltage frequency exhibits a resistive characteristic. Different from direct parallel components, the virtual admittance method requires no additional components and can achieve complex impedance characteristics. The virtual admittance reshaping based equivalent model of the TBPFC converter is shown in Fig. 8(a), where $1/Y$ is the input impedance of the PFC converter considering the current controller, and $i_{\rm va}$ is the virtual admittance branch circuit current. The control block diagram is shown in Fig. 8(b), and the virtual admittance branch current is generated by sampling the input voltage.

According to Fig. 8(a), the grid-side current can be expressed as follows:

$$\begin{aligned} i_{\rm g} &= i_{\rm DM} + i_{\rm L} + i_{\rm va} \\ &= u_{\rm g}\frac{Y(s) + Y_{DM}(s) + Y_{va}(s)}{[Y(s) + Y_{DM}(s) + Y_{va}(s)](L_{\rm DM}s + R_g) + 1} \end{aligned} \tag{17}$$

where $Y_{\rm va}(s)$ and $Y_{\rm DM}(s)$ are the virtual admittance and the differential capacitance admittance, respectively. $Y_{\rm DM}(s) = sC_{\rm DM}$.

According to the analysis in the previous section, the influence of $L_{\rm DM}$ and $R_{\rm g}$ on the phase of $i_{\rm g}$ can be ignored. The Bode diagrams of the system admittances $Y_1(s)$, $Y_2(s)$, and $Y_{\rm DM}(s)$ are shown in Fig. 9, from which it can be seen that the phase of the admittance $Y_1(s)$ is zero, and the phase of the admittance $Y_2(s)$ and $Y_{\rm DM}(s)$ is about 90° near the power frequency. Therefore, the currents $i_{\rm L2}$ and $i_{\rm DM}$ generated by the input voltage through admittance $Y_2(s)$ and $Y_{\rm DM}(s)$ are the phase shift components of $i_{\rm g}$, leading the input voltage phase by about 90°. In order to reduce the GCPS of the TBPFC converter including the EMI filter, a virtual admittance term $Y_{\rm va}(s)$ needs to be designed to cancel the admittances $Y_2(s)$ and $Y_{\rm DM}(s)$. The expected virtual admittance term $Y_{\rm va}(s)$ is shown in the following equation:

$$Y_{\rm va}(s) = -C_{\rm va}s - \frac{V_{\rm m}}{V_{\rm m}L_{\rm va}s + U_{\rm dc}K_{\rm is}G_{\rm ic}G_{\rm delay}}. \tag{18}$$

When $C_{\rm va} = C_{\rm DM}$ and $L_{\rm va} = L$, the leading admittance in the original system can be completely canceled, and the PFC converter including EMI filter has zero-phase leading admittance. Thus, $i_{\rm g}$ and $u_{\rm g}$ are in the same phase. After the virtual admittance reshaping based GCPS suppression strategy is adopted, the Bode diagram of the system is shown in Fig. 10. It can be seen that after admittance reshaping, the GCPS can be suppressed, and the phase characteristics are consistent under different load conditions. With the increase of current loop

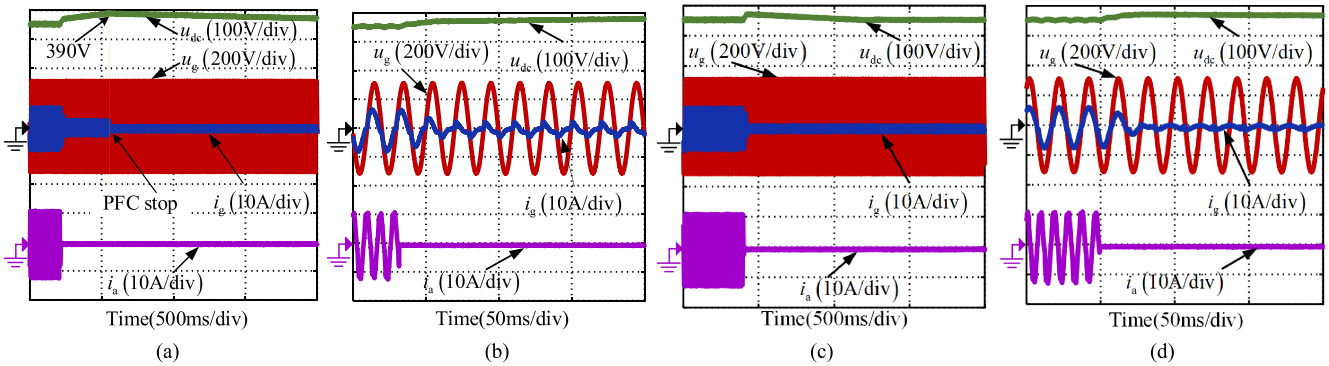

Fig. 21. Experimental waveforms of the PFC converter load step from 500 W to zero. (a) Without GCPS suppression strategy. (b) Enlarged view of (a). (c) With GCPS suppression strategy. (d) Enlarged view of (c).

TABLE II
COMPARISONS WITH PREVIOUS WORKS

Load(%)	Results in [25]			Results without GCPS suppression			Results with GCPS suppression		
	PF	THD(%)	Efficiency(%)	PF	THD(%)	Efficiency(%)	PF	THD(%)	Efficiency(%)
10	0.9078	12.2	97.65	0.6570	29.05	91.25	0.9683	25.78	90.11
20	0.9699	7.40	98.00	0.8423	18.39	96.20	0.9935	11.46	95.51
50	0.9880	5.48	98.31	0.9672	8.53	98.41	0.9988	4.66	98.14
100	0.9972	3.38	98.21	0.9896	5.86	98.81	0.9993	3.69	98.66

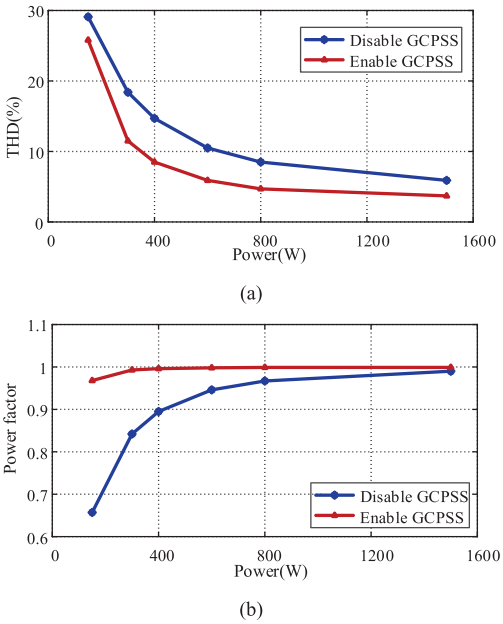

Fig. 22. Grid-side current THD and system power factor without and with applying the proposed GCPS suppression strategy under different loads. (a) Grid-side current THD. (b) System power factor.

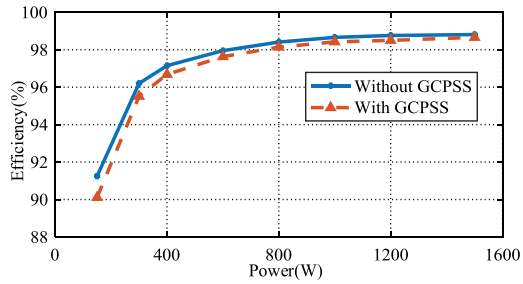

Fig. 23. Efficiencies with and without the GCPS suppression strategy.

control bandwidth, the effect of phase shift suppression can be improved.

In practical applications, due to the error between the actual and the nominal values of the components, as well as the saturation effect of the boost inductor, there will be errors between the designed virtual admittance term and the phase-leading admittance term in the actual system. In order to analyze the influence of different errors on the admittance reshaping effect, the input admittance frequency characteristic diagram of the system is drawn. As shown in Figs. 11 and 12, the differential mode capacitor is set to 0.8∼1.2 times the nominal value, and the boost inductance is 0.5∼2 times the nominal value.

It can be seen from Fig. 11 that the nominal inductance value is used to reshape the admittance. When the system inductance changes, at least in the range of 1–940 Hz, the system input admittance phase is within ±1°. The change of L has little effect on the admittance reshaping effect in the low frequency range, and mainly affects the response of the system to the high frequency signal (Frequency>5 kHz). It can be seen from the figure that when $L_{va} \neq L$, the high frequency admittance amplitude increases.

Fig. 12 shows the frequency characteristics of the system after admittance reshaping when the differential mode capacitance changes. It can be found that the input admittance phase of the system is symmetrical along the center of $C_{va} = C_{DM}$. When $C_{va} < C_{DM}$, the phase leads, and when $C_{va} > C_{DM}$, the phase lags. When the capacitance error is within the range of 20%, the phase error at the power frequency after admittance reshaping does

not exceed $\pm 1°$. When $C_{\rm va} \neq C_{\rm DM}$, the amplitude is the same as when L changes and the admittance amplitude increases at high frequency. Since the high-frequency components in the power grid are small, selecting the nominal values of the inductance and capacitance to reshape the admittance is hardly affected by component errors. Moreover, the current harmonics in the IEC6100-3-2 standard only pay attention to harmonics below the 40th order.

B. Implementation Method of Virtual Admittance

Admittance reshaping can be realized by controlling the inductance current $i_{\rm L}$. Due to the bandwidth limitation of the current loop, it is complex to generate the current reference alone, which increases the burden of the controller and is difficult to achieve good results. Therefore, the sampling value of the input voltage is used to generate the virtual admittance current, which is then transformed into the current reference and the modulation voltage. Through the combination of the two, the equivalent virtual admittance current is obtained to realize the effect of admittance reshaping.

After considering the time delay of the digital control system, the current loop block diagram of the TBPFC converter with virtual admittance reshaping is shown in Fig. 13. The GCPS suppression scheme based on virtual admittance reshaping is integrated into the average current control algorithm of the TBPFC converter. The equivalent admittance generated by current reference and modulation voltage are

$$\begin{cases} Y_{\rm va1}(s) = \frac{G_{\rm va1} G_{\rm ic} G_{\rm id}}{V_{\rm m}(1+T_{\rm i})} \\ Y_{\rm va2}(s) = \frac{G_{\rm va2} G_{\rm id}}{V_{\rm m}(1+T_{\rm i})} \end{cases}. \tag{19}$$

Since enabling the proposed GCPS suppression method does not change the open loop transfer function, i.e., the characteristic equation of the closed-loop system does not change. Thus, the phase margin is unchanged. Besides, the discretization method in this study is the backward difference method, which does not change the stability of the system.

According to the analysis in the previous part, the sum of the equivalent admittances $Y_{\rm va1}$ and $Y_{\rm va2}$ is equal to the required virtual admittance $Y_{\rm va}$. Therefore, the expressions of $G_{\rm va1}$ and $G_{\rm va2}$ can be calculated as follows:

$$\begin{cases} G_{\rm va1}(s) = -sC_{\rm DM}K_{\rm is} \\ G_{\rm va2}(s) = -\frac{V_m(s^2 L C_{DM}+1)}{U_{\rm dc}} \end{cases}. \tag{20}$$

In this study, the backward difference method is chosen to get the time domain discrete model of the system and realize digital control on the microcontroller.

The component superimposed on the current reference is $I_{\rm com} = G_{\rm va1} u_{\rm in}$. The discretization process is as follows.

It can be seen from Fig. 13 and (20) that the component superimposed on the current reference is

$$\begin{aligned} I_{\rm com}(s) &= -sC_{\rm DM}K_{\rm is}u_{\rm in}(s) \\ s &= \frac{z-1}{zT_{\rm s}} \\ \Rightarrow I_{\rm com}(z) &= -\frac{z-1}{zT_{\rm s}} C_{\rm DM}K_{\rm is}u_{\rm in}(z). \end{aligned} \tag{21}$$

Convert it into a differential equation as follows:

$$I_{\rm com}(k) = -C_{\rm DM}K_{\rm is}\left[u_{\rm in}(k) - u_{\rm in}(k-1)\right]/T_{\rm s}. \tag{22}$$

Similarly, the expression of the modulated voltage component can be obtained as follows:

$$\begin{aligned} d_{\rm com}(k) = &-\frac{V_{\rm m}LC_{\rm DM}}{U_{\rm dc}T_{\rm s}^2}\left[u_{\rm in}(k) - 2u_{\rm in}(k-1) + u_{\rm in}(k-2)\right] \\ &- \frac{V_{\rm m}}{U_{\rm dc}}u_{\rm in}(k). \end{aligned} \tag{23}$$

The relationship between each voltage and current vector is shown in Fig. 14. The dotted lines show the relationship between the current vectors of each branch before applying the suppression strategy, where $i_{\rm L1}$ and $i_{\rm L2}$ are the current components of the inductor current in the voltage direction and the vertical voltage direction, respectively. $i_{\rm DM}$ is the differential mode capacitor current. It can be seen from Fig. 14 that before the strategy is applied, the phase difference between $i_{\rm g}$ and $u_{\rm g}$ is φ. After applying the suppression strategy, it is equivalent to superimposing $i_{\rm va}$ on $i_{\rm L1}$. The superimposed current is superimposed with $i_{\rm L2}$ to obtain the compensated inductor current $i_{\rm L,c}$, and then superimposed with $i_{\rm DM}$ to obtain the compensated grid-side current $i_{\rm g,c}$, The phase difference between $i_{\rm g,c}$ and $u_{\rm g}$ is $\varphi_{\rm c}$, which is directly related to the compensation current $i_{\rm va}$.

IV. Experimental Results

The experimental platform of the TBPFC converter is shown in Fig. 15. The Renesas RX62T is adopted. The compressor drive system is used as the load of the experimental platform, and the load is adjusted by adjusting the compressor speed. The main parameters of the TBPFC converter are shown in Table I, and the rated load is 1500 W. In this article, a virtual admittance reshaping based GCPS suppression strategy is implemented on this platform.

The experimental results under 10% rated load are shown in Fig. 16. In Fig. 16, $i_{\rm ref\,va}$, $u_{\rm ova}$, and $i_{\rm a}$ represent the current reference component, the modulation voltage component, and the compressor A-phase current, respectively. As can be seen, when the GCPS suppression strategy is disabled, the per-unit value of $i_{\rm ref\,va}$ and $u_{\rm ova}$ is 0. At this time, the GCPS occurs, and the grid-side current amplitude is large, due to the differential mode capacitance and the bandwidth limitation of the PFC converter. From the Fourier analysis results of the grid-side current in Fig. 16(b), it can be seen that the dominant current harmonics, viz. the third, fifth, and seventh harmonics are larger, the THD is 29.1%, the current phase lead angle is 46.8°, and the power factor is only 0.657. The power quality of the grid side is poor. The low power factor is mainly caused by the displacement factor because the differential mode capacitors in this study are 4 μF. It has a great influence on the power factor of the converter at light load. When the strategy of suppressing GCPS based on virtual admittance reshaping is enabled, the relevant experimental results are shown in Fig. 16(c). It can be seen from the experimental results that the GCPS is suppressed and the current amplitude is reduced. Fourier analysis results show that the amplitudes of the third, fifth, and seventh current harmonics are significantly lower than those when the strategy

is disabled. The THD of the input current is 25.8%, the current phase lead angle is 0.54°, and the power factor raises to 0.968. The power quality on the grid side is significantly improved. The correctness of this method is further verified. It can be seen from Fig. 16(b) and (c) that after suppressing the phase shift, the power factor is improved significantly. However, enabling the proposed method leads to the phase shift of the inductor current being changed to −20.47°, and the diode limits the current direction. The distortion around zero crossing cannot be suppressed significantly, which leads to the grid-side current THD only decreasing from 29.1% to 25.8%.

In order to verify the effectiveness of the virtual admittance reshaping based GCPS suppression strategy, experiments were carried out under different load conditions. The experimental results under the conditions of 1/5 load, 1/2 load, and full load are shown in Figs. 17–19. Consistent with the above-mentioned analysis, due to the increase of the load power, the GCPS phenomenon on the grid side can be alleviated. Especially when the load reaches full load, the current phase advance angle is reduced to within 10°. When the proposed strategy is applied, the THD is further reduced, and the power quality is improved. The superior adaptability and universality for applications of this method are further verified.

Fig. 20 shows the input voltage step with and without the proposed method at full load (1500 W). The input voltage step between 220 and 242 V (110% of 220 V) is compared. In this process, the dc-link voltage overshoot and drop are around 5.5 V with and without the proposed method. According to Fig. 20, compared with disabling the proposed method, enabling the method can reduce the current adjustment time from 182 to 160 ms during the input voltage steps from 220 to 242 V. When the input voltage steps from 242 to 220 V, the current adjustment times are both 160 ms. The experimental results are similar when the input voltage step between 220 and 198 V (90% of 220 V).

In the operating state that the load steps from 500 W to zero-load (stop the compressor), the converter without the proposed method will stop operation due to the overshoot of dc-link voltage. In this process, it is higher than 390 V and triggers over-voltage protection. The experimental results are shown in Fig. 21. It can be seen from Fig. 21(b), the PFC converter stops when the dc-link voltage arrives at 390 V, then the inductance current is zero, the grid-side current is the same as the EMI filter current. On the other hand, the dc-link voltage overshoot of the converter with the proposed method is only 371 V, and the over-voltage protection will not be triggered. According to the experimental results in Fig. 21, the proposed method has a stronger strategy to control the dc-link voltage and improve the robustness of the converter.

Based on the above-mentioned experimental results and analysis, the proposed GCPS suppression strategy will not influence the dynamics of the system in a negative way. In addition, it can improve some performance such as the current adjustment time in input voltage increase and the robustness in load step compared with disabling the method.

Fig. 22 shows the experimental measurement results of the grid-side current THD and power factor before and after enabling the proposed GCPS suppression method. After enabling the proposed method, when the load reaches more than half load, the input current power factor reaches 0.999, and the input current THD drops to 5.32%. When the load is light, the power factor and THD are improved more obviously than before the strategy is adopted, and the power quality of the grid side is improved. The effectiveness and feasibility of the proposed compensation method are further verified.

The efficiencies of the PFC converter before and after enabling the proposed method are shown in Fig. 23. It can be seen that the efficiency increases from light load to heavy load, and with the power increase, the efficiency errors decrease. However, the experimental results of efficiency decrease a little with the GCPS suppression strategy. The reason is as follows: The RMS of the inductor current with GCPS suppression strategy is smaller than that of the inductor current without GCPS suppression strategy, which leads to lower conduction losses. However, the average value of the inductor current with GCPS suppression strategy is larger than that of the inductor current without GCPS suppression strategy. Besides, the efficiencies without GCPS were measured after cooling and the efficiencies with GCPS were measured without cooling. Thus, the switching losses increase after enabling the proposed method. The GaN HEMTs are used as high-frequency power devices in the TBPFC converter. The switching frequency is 150 kHz. Due to the small drain-to-source resistance, and the high switching frequency of the device, the main losses at light load are switching losses [33], [34], [35]. Thus, the efficiencies decrease a little with the GCPS suppression strategy.

The comparison of the PF, THD, and efficiency is shown in Table II. The method proposed in [25] compensates the duty ratio in DCM mode, thus, at light load, PF and THD performance is better than the method proposed in this article. However, in CCM mode, the method proposed in this article has a higher PF, due to the current loop limitation being compensated. The efficiency is more related to the power device, inductor, switching frequency, and topology.

V. Conclusion

Aiming at the phenomenon of GCPS caused by EMI filter and current regulator bandwidth limitation, the equivalent input admittance model and frequency domain model of the totem-pole PFC converter have been established in this article, and the principle of GCPS caused by the above-mentioned factors has been revealed. A virtual admittance reshaping based GCPS suppression strategy has been proposed. The equivalent virtual admittance has been designed based on the average current control architecture of the PFC converter, which can offset the equivalent leading-phase admittance terms of the system. This method has low sensitivity to the converter parameters, which improves the robustness of the system and simplifies the algorithm. The GCPS is near 0° under different load conditions when the proposed method has been adopted without adjusting parameters. The effectiveness of the proposed method has been verified through experiments.

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