Simultaneous Power and Data Transmission Using Combined Three Degrees of Freedom Modulation Strategy in DC–DC Converters

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***Abstract*—Power and signal dual modulation (PSDM) modulates both power and data at the same time, making it an appropriate communication method for power electronics' applications. While the conventional PSDM schemes use either duty cycle control or phase/frequency control of the gate signal for switching devices, which achieve limited bitrate performances, this article proposes a novel PSDM scheme that combines the control of the three degrees of freedom (DoF) to further improve the bitrate. The scheme's feasibility is shown by examining the compatibility between the control of different DoFs from the perspective of communication. Then, a practical scheme is determined based on the analysis of the influence between signal carriers with different frequencies and the upper limit of M-ary modulation for each carrier. Finally, a 230 W experimental prototype, which achieves independence between power and communication control as well as a bitrate of 41.7 kb/s under the switching frequency of 100 kHz/83.3 kHz, demonstrates the correctness of the proposed scheme and the pertinent theoretical analysis.**

***Index Terms*—Combined three degrees of freedom (DoF) modulation, power and signal dual modulation (PSDM), power line communication (PLC), power system communication.**

I. Introduction

POWER electronics technology has become essential and has been widely applied to most electrical fields, such as renewable energy generation, microgrid systems, and electrical vehicles [1], [2]. Recently, the development of smart equipment and smart systems keeps raising the demand for information interaction between power electronics equipment [3], [4], making the equipment integrated with communication function a major research topic and a promising candidate for future applications.

To achieve communication, various methods, including field bus communication, wireless communication, and power line communication, have been applied [5], [6], [7]. However, for power electronics equipment, these methods have their respective limitations in system complexity, real-time performance, robustness, cost, and volume.

Fortunately, the study of power electronics technology elucidates that the power electronic converters are capable of transmitting information [8], [9], providing a new communication method known as power and signal dual modulation (PSDM). Compared with the mentioned conventional methods, PSDM does not require independent communication wiring or additional hardware for signal transmission, contributing to reduced system complexity, cost, and volume. Moreover, due to the deep integration of power and data, this method has good real-time performance and high robustness. Therefore, it is a suitable communication method for power electronics' applications.

PSDM schemes can be classified into two categories [10], which are PSDM by encoded switching carrier (PSDM-ESC) and PSDM by encoded control ripple (PSDM-ECR). PSDM-ESC uses switching ripples as the data carriers, and PSDM-ECR uses specially generated low-frequency data carriers. However, early schemes of both categories do not show a satisfying performance on communication speed. Since then, bitrate improvement has always been a main research in the PSDM field.

In PSDM-ESC schemes, frequency-shift keying (FSK) is achieved by controlling the gate signal frequency of a converter's switching components [11], [12], [13], [14], [15], [16], [17], which facilitates the implementation. Nevertheless, M-ary modulation is difficult to achieve, leading to a low bitrate. In order to improve the bitrate, phase control of the gate signal is used to achieve quadrature amplitude modulation (QAM) [18], [19] and differential phase-shift keying (DPSK) modulation [20], [21], [22]. However, QAM can only be implemented in interleaved topologies, limiting its application range, and DPSK modulation is influenced once multiple converters work at the same time. To address the issue of DSPK, frequency-hopping differential phase-shift key (FH-DPSK) modulation is proposed [8], [23], which combines the advantages of FSK and DPSK, and shows good overall performance in bitrate, noise immunity, and application convenience.

In PSDM-ECR schemes, the duty cycle is controlled to generate additional carriers with lower frequencies than the switching frequency, and data are modulated on the carriers,

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while the switching ripple carries no data. However, the maximum frequency of the additional carriers is less than one-fifth of the switching frequency [24], [25], [26], [27], [28], resulting in a low communication speed. Although orthogonal frequency division multiplexing (OFDM) has been applied to increase the bitrate [24], [25], it is still slower than the FH-DPSK schemes.

Considering that the maximum ratio of bitrate to switching frequency is 0.2 in previous FH-DPSK works, if better bitrate performance is preferred, a new modulation scheme should be developed. In light of the preceding discussion, PSDM schemes control the three degrees of freedom (DoF) of a gate signal—frequency, phase, and duty cycle—and only one or 2-DoF are controlled in one scheme. Thus, this article proposes a novel modulation scheme called combined 3-DoF modulation that applies the control of all 3-DoF for communication to further improve the bitrate. In experiments, the ratio of bitrate to switching frequency is increased to 0.417. The main contributions of this article are as follows.

1) A detailed discussion about the compatibility of the 3-DoF is presented, showing the feasibility of the new scheme and the direction to combine the control of the 3-DoF.
2) The influence between the signal carriers of different frequencies is analyzed, and the M-ary modulation upper limit for each carrier is determined.
3) A novel scheme is proposed, which achieves the independence of power control and communication control and outperforms FH-DPSK modulation in bitrate performance.

The rest of this article is organized as follows. Section II discusses the compatibility of the 3-DoF, providing basic conclusions about how to control them. Section III clarifies some practical problems and their solutions when applying 3-DoF for communication. Section IV conducts simulations and experiments to validate the proposed theories and the scheme's feasibility. Finally, Section V concludes this article.

II. Compatibility Between the Control of 3-DoF in Pulsewidth Modulation (PWM) for Communication

To increase the bitrate, a novel modulation scheme that controls all 3-DoF—frequency, phase, and duty cycle—is expected. Therefore, it is essential to discuss how the 3-DoF should be utilized in the new scheme. Based on the existing modulation schemes of PSDM-ESC and PSDM-ECR, the compatibility of the DoF is discussed, and the conclusions are drawn regarding their application. The following sections provide detailed contents.

A. Modulation Process of PSDM-ESC and PSDM-ECR

The modulation process of FH-DPSK, which is a typical modulation scheme for PSDM-ESC, is shown in Fig. 1(a). The carrier generator generates two PWM carriers with different frequencies, and carrier $f_s(\omega_1 t)$ is modulated using DPSK based on the baseband data. The communication switch $C(t)$ selects the modulated PWM carrier $e_{\mathrm{DPSK}}(t)$ when the converter sends data, and $f_s(\omega_0 t)$ when the converter does not. Fig. 1(b) depicts the quaternary FH-DPSK waveforms, where T_b is the symbol

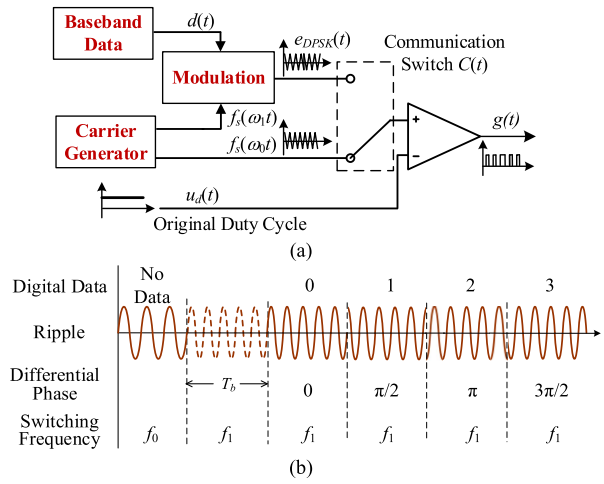

Fig. 1. (a) Modulation process of FH-DPSK. (b) Modulation waveforms of FH-DPSK.

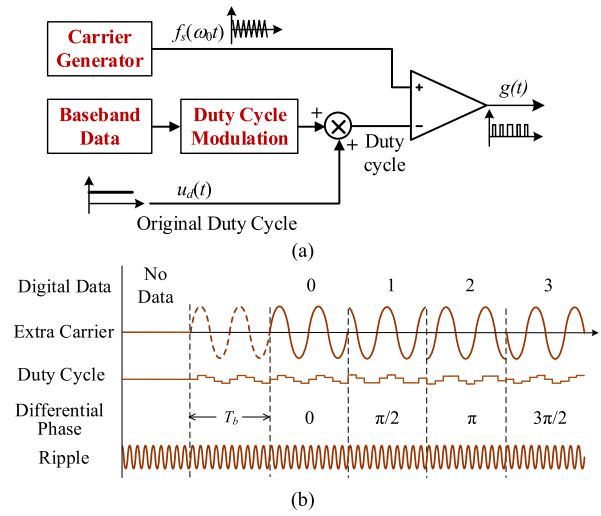

Fig. 2. (a) Modulation process of PSDM-ECR. (b) Modulation waveforms of PSDM-ECR.

length, the ripple frequency is dependent on whether data are being sent, and the ripple phase depends on digital data.

The PSDM-ECR modulation process is depicted in Fig. 2(a). The process of duty cycle modulation generates a modulated signal based on the baseband data. By adding the signal directly to the original duty cycle, the gate signal's duty cycle is controlled and carries data. Fig. 2(b) shows the 4DPSK modulated PSDM-ECR waveforms. The duty cycle waveform is the output of the aforementioned duty cycle modulation, and it varies every switching period to generate the expected additional carrier, while the switching ripple does not change in this scheme. The phase of the carrier is decided by digital data, and five switching periods are used to produce one carrier period in this figure.

B. Compatibility Between Frequency Control and Phase Control for PSDM

OFDM is a common way to achieve a high bitrate using the phase and frequency of the signal carrier [24], [25]. In terms

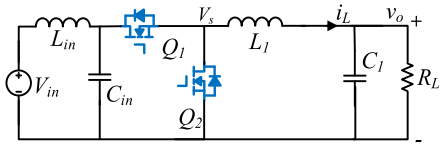

Fig. 3. Schematic of the buck converter.

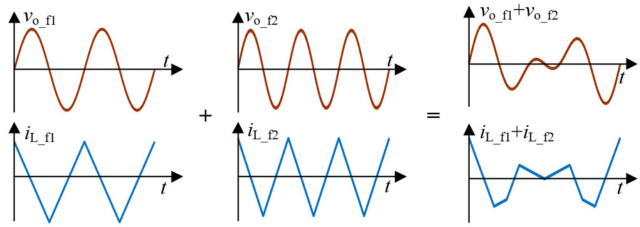

Fig. 4. Waveforms of OFDM.

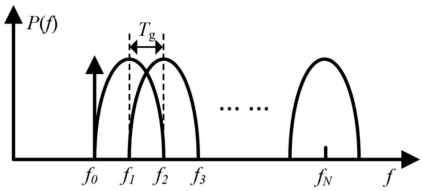

Fig. 5. Frequency spectrum of OFDM.

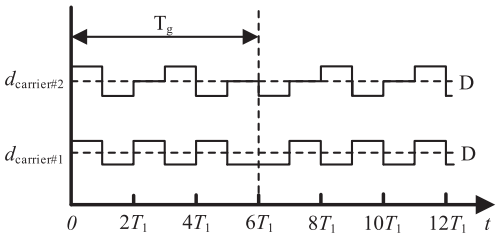

Fig. 6. Duty cycle waveforms of additional carriers.

of controlling the gate signal's frequency and phase, the signal carrier becomes the switching ripple. Take the buck converter in Fig. 3 as an example. Fig. 4 shows the C_1 voltage ripple and L_1 current at two distinct switching frequencies, denoted by v_{o_f1}, i_{L_f1}, v_{o_f2}, and i_{L_f2}, respectively. If the two frequencies are applied for OFDM, the voltage ripple is expected to equal the sum of v_{o_f1} and v_{o_f2}, thus bringing an L_1 current shown as $i_{L\_f1}+i_{L\_f2}$, which is impossible for a buck converter. Therefore, OFDM cannot be directly implemented in topologies, such as single buck converter for frequency and phase control of the gate signal.

Considering that two different frequencies are applied to distinguish the communication signal in [8] and [23], more frequencies can be used to achieve FSK together with FH-DPSK for bitrate increase. To avoid interference between different frequencies, the frequency f_0 for power conversion and the frequencies f_1–f_N for communication should be orthogonal within the demodulation window T_g. So, as shown in Fig. 5, a minimum bandwidth of $(N+1)/T_g$ is needed to achieve a bitrate of $\log_2 N/T_b + R_{b1}$, where T_b is the symbol length, and R_{b1} is the bitrate of FH-DPSK.

However, switching frequency is an important parameter for a converter, and a large N in FSK modulation for a significant bitrate improvement is unacceptable for converter design. As a result, only limited information can be directly modulated on the frequency, and the main contributions of the frequency control are distinguishing whether the ripple contains information and helping to shift the phase.

C. Compatibility Between Phase Control and Duty Cycle Control for PSDM

According to the Fourier series, the amplitude of the base frequency component of a switching device gate signal can be written as follows:

$$A_{rs} = \frac{2\sin(\pi D)}{\pi} \tag{1}$$

where D is the duty cycle. According to the equation, the amplitude can be controlled by the duty cycle. Thus, the duty cycle control and the phase control can be combined to achieve QAM if different amplitudes are used to represent different data. However, suppose the maximum duty cycle variation, which is defined as the modulation depth, is ΔD, then the amplitude becomes

$$A_r = A_{rs}\left(1 + \frac{\cos(\pi D)\,\pi D}{\sin(\pi D)}\right). \tag{2}$$

Equation (2) shows that the amplitude variation is too small to be detected when D is close to 0.5 or the value of ΔD is small. Besides, in order to keep the output power constant despite the duty cycle variation, specialized coding method should be developed. Therefore, this scheme is not applicable.

Producing additional carriers for PSDM [24], [25], [26], [27], [28] is another method of controlling the duty cycle. However, there are issues when combining this scheme directly with phase control. Due to the low carrier frequency, it is difficult to make a large promotion for the bitrate. Zhang et al. [24] employ an OFDM scheme and eight additional carriers are applied to achieve a bitrate close to that of the phase control scheme. In addition, in order to obtain a smooth phase shift, the transition process is necessary [23], which disrupts the long additional carrier period and influence the communication.

In order to implement both phase and duty cycle control, the additional carrier frequency has to be increased. The switching frequency should equal to an integral multiple of the additional carrier frequency so that the harmonic frequencies produced by modulation will not influence the communication. Moreover, according to Zhu et al. [26] and Han and Rogers [29], the additional carrier frequency should be above the closed-loop bandwidth in order to avoid the influence between the power control and the communication.

Fig. 6 depicts the ideal duty cycle signals, where T_1 is the switching period and $T_g = 6T_1$ is the demodulation window, D is the horizontal dashed line value that represents the duty cycle for power control, and $d_{\mathrm{carrier}\#1}$ and $d_{\mathrm{carrier}\#2}$ are the duty cycles producing two additional carriers with respective frequencies of half and one-third of the switching frequency. Take $d_{\mathrm{carrier}\#1}$ as an example, when D is ignored, $d_{\mathrm{carrier}\#1}$ becomes the signal in

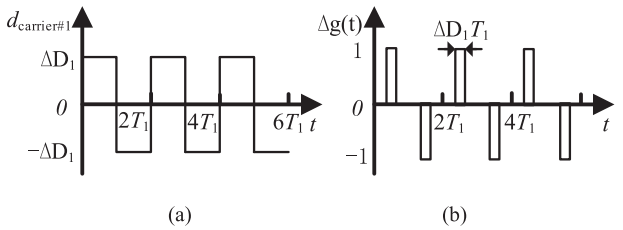

Fig. 7. Waveform of (a) duty cycle and (b) gate signal of carrier#1 when only considering duty cycle variation.

Fig. 7(a), and the corresponding gate signal is shown in Fig. 7(b), where ΔD_1 is the modulation depth. It is obvious that the gate signal has a period of $2T_1$ and its base frequency component is

$$\Delta g_{\text{base}}(t) = \frac{2\sin(\pi \Delta D_1)}{\pi} \sin\left(\frac{\pi}{T_1} t\right). \tag{3}$$

Moreover, a minus phase will be obtained if the signal within $[6T_1, 12T_1]$ is used. Based on the fact that the switching ripple can be considered as the gate signal filtered by the output filter of the converter, $\Delta g_{\text{base}}(t)$ can be detected from the switching ripple, so carrier#1 can be used for communication. The same conclusion can be obtained if $d_{\text{carrier}\#2}$ or carriers with other frequencies are used. Thus, additional carriers with a frequency greater than one-fifth of the switching frequency can also be applied in communication.

In the occasion in Fig. 6, additional carriers can share the same T_g with the switching ripple, allowing for a large improvement in bitrate. This is a duty cycle and phase-controlled OFDM scheme using both switching ripple and additional carriers.

III. Practical Modulation Scheme

A. Influence of Duty Cycle Control on Phase Control Under Different PWM Carriers

The gate signal of PWM control using sawtooth PWM carrier is shown in Fig. 8(a), where T_1 is the switching period and D is the duty cycle. Suppose that the corresponding angular frequency is ω_1, then the Fourier coefficient of the base frequency component is

$$\begin{aligned} \boldsymbol{A_{s1}} &= \frac{2}{T_1}\int_0^{T_1} g(t)\, e^{-j\omega_1 t} dt = \frac{2}{T_1}\int_0^{DT_1} e^{-j\omega_1 t} dt \\ &= \frac{2\sin(\pi D)}{\pi}\, e^{-j\pi D}. \end{aligned} \tag{4}$$

When carrier#1, as depicted in Fig. 6, is applied and the modulation depth is ΔD_1, the gate signal turns to the waveform, as shown in Fig. 8(b), and Fig. 8(c) shows the waveform when only the duty cycle variation is considered. Based on the figures, the period of the variation is $2T_1$, so the Fourier coefficient of the base frequency component of $\Delta g(t)$ is

$$\begin{aligned} &\boldsymbol{A_{s1,1}} \\ &= \frac{2}{2T_1}\left[\int_{DT_1}^{DT_1+D_1T_1} e^{-j\frac{\omega_1}{2}t} dt - \int_{T_1+DT_1-D_1T_1}^{T_1+DT_1} e^{-j\frac{\omega_1}{2}t} dt\right] \end{aligned}$$

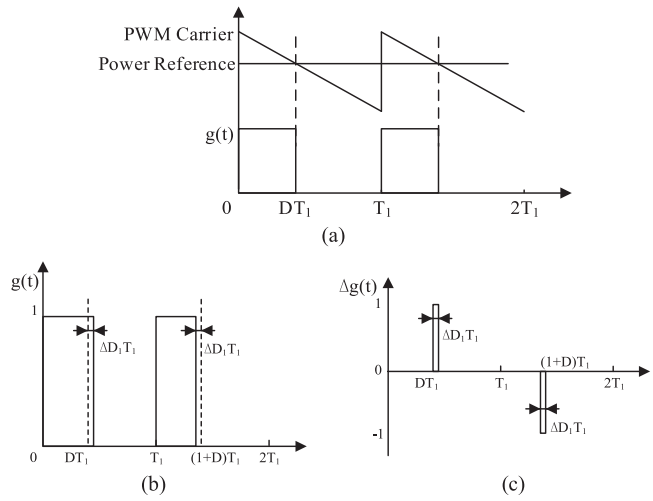

Fig. 8. Gate signal using (a) sawtooth PWM carrier when in conventional PWM, (b) applying additional carrier, and (c) applying additional carrier and only considering the duty cycle variation.

$$= \frac{2\sin(\pi D_1)}{\pi}\, e^{-j\pi D} \tag{5}$$

and the coefficient of the second harmonic is

$$\begin{aligned} &\boldsymbol{A_{s1,2}} \\ &= \frac{2}{2T_1}\left[\int_{DT_1}^{DT_1+D_1T_1} e^{-j\omega_1 t} dt - \int_{T_1+DT_1-D_1T_1}^{T_1+DT_1} e^{-j\omega_1 t} dt\right] \\ &= \frac{1-\cos(2\pi D_1)}{\pi}\, e^{-j2\pi(D+0.25)}. \end{aligned} \tag{6}$$

It is obvious that the second harmonic and the switching ripple have the same frequency, so the result of demodulation at frequency ω_1 is $\boldsymbol{A_{s1}}+\boldsymbol{A_{s1,2}}$. Therefore, according to (4) and (6), the second harmonic of carrier#1 brings a phase deviation to the switching ripple because $\boldsymbol{A_{s1}}$ and $\boldsymbol{A_{s1,2}}$ have different phases. Due to the fact that data are modulated on the switching ripple's phase, the deviation impacts communication and may result in an error code.

The gate signal of PWM control using triangular PWM carrier is shown in Fig. 9(a), and the Fourier coefficient of the base frequency is

$$\begin{aligned} \boldsymbol{A_{t1}} &= \frac{2}{T_1}\int_0^{T_1} g(t)\, e^{-j\omega_1 t} dt = \frac{2}{T_1}\int_{\frac{T_1}{2}(1-D)}^{\frac{T_1}{2}(1+D)} e^{-j\omega_1 t} dt \\ &= \frac{2\sin(\pi D)}{\pi}\, e^{-j\pi}. \end{aligned} \tag{7}$$

The gate signal after carrier#1 is applied, as shown in Fig. 9(b), and Fig. 9(c) shows the waveform when only considers the duty cycle variation. The Fourier coefficient of the base frequency component of $\Delta g(t)$ is

$$\begin{aligned} &\boldsymbol{A_{t1,1}} \\ &= \frac{2}{2T_1}\left[\int_{\frac{T_1}{2}(1-D-D_1)}^{\frac{T_1}{2}(1-D)} e^{-j\frac{\omega_1}{2}t} dt + \int_{\frac{T_1}{2}(1+D)}^{\frac{T_1}{2}(1+D+D_1)} e^{-j\frac{\omega_1}{2}t} dt\right. \end{aligned}$$

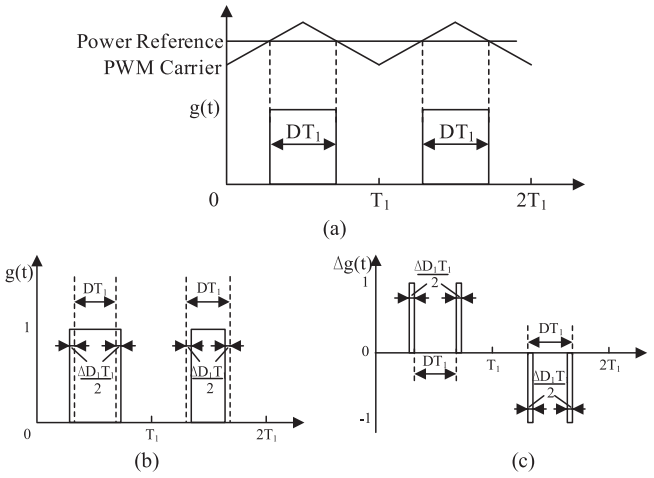

Fig. 9. Gate signal using (a) triangular PWM carrier when in conventional PWM, (b) applying additional carrier, and (c) applying additional carrier and only considering the duty cycle variation.

$$-\int_{\frac{T_1}{2}(3-D)}^{\frac{T_1}{2}(3-D+D_1)} e^{-j\frac{\omega_1}{2}t}dt-\int_{\frac{T_1}{2}(3+D-D_1)}^{\frac{T_1}{2}(3+D)} e^{-j\frac{\omega_1}{2}t}dt\Bigg] = \frac{4\cos\left(\frac{\pi}{2}D\right)\sin\left(\frac{\pi}{2}D_1\right)}{\pi}e^{-j\frac{\pi}{2}} \tag{8}$$

and the coefficient of the second harmonic is

$$\begin{aligned}\boldsymbol{A_{t1,2}} &= \frac{2}{2T_1}\left[\int_{\frac{T_1}{2}(1-D-D_1)}^{\frac{T_1}{2}(1-D)} e^{-j\omega_1 t}dt+\int_{\frac{T_1}{2}(1+D)}^{\frac{T_1}{2}(1+D+D_1)} e^{-j\omega_1 t}dt\right.\\ &\left.-\int_{\frac{T_1}{2}(3-D)}^{\frac{T_1}{2}(3-D+D_1)} e^{-j\omega_1 t}dt-\int_{\frac{T_1}{2}(3+D-D_1)}^{\frac{T_1}{2}(3+D)} e^{-j\omega_1 t}dt\right]\\ &= \frac{\sin(\pi D)\left[2\cos(\pi D_1)-1\right]}{\pi}e^{-j\pi}.\end{aligned} \tag{9}$$

According to (7) and (9), the second harmonic of carrier#1 and the switching ripple share the same phase. Thus, there is no phase deviation at frequency ω_1, and the communication using switching ripple is not influenced by additional carriers.

B. M-ary Modulation of Duty Cycle Control

Assume that the additional carrier with phase φ contains N switching periods, where N is an integer, and the corresponding modulation depth is ΔD_{N-1}. Then, within a period of the additional carrier, the duty cycle variation in each switching period is

$$d_n = D_{N-1}\cos\left(\frac{2n\pi}{N}+\varphi\right),\ n=0,1,2,\ldots,N-1. \tag{10}$$

When triangular PWM carrier is applied, the gate signal that only considers the duty cycle variation is shown in Fig. 10. Because the gate signal cannot have a negative pulse width, $\Delta g(t)$ has a negative amplitude instead during $[nT_1, (n+1)T_1]$, while the corresponding d_n is negative, and the two pulses are center-aligned incorporated within a range with a duration of

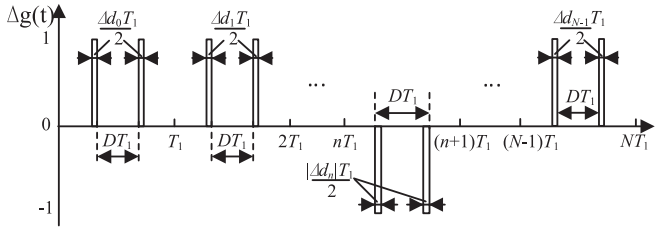

Fig. 10. Gate signal in each switching period when only considering duty cycle variation.

DT_1. Therefore, the coefficient of the base frequency component of the carrier is

$$\begin{aligned}\boldsymbol{A_{tN-1,1}} &= \frac{2}{NT_1}\sum_{n=0}^{N-1}\left[\int_{\frac{T_1}{2}(1+2n-D-d_n)}^{\frac{T_1}{2}(1+2n-D)} e^{-j\frac{\omega_1}{N}t}dt\right.\\ &\left.+\int_{\frac{T_1}{2}(1+2n+D)}^{\frac{T_1}{2}(1+2n+D+d_n)} e^{-j\frac{\omega_1}{N}t}dt\right]\\ &= \frac{2}{\pi}\sum_{n=0}^{N-1} e^{-j\frac{\pi}{N}(2n+1)}\left[\sin\frac{\pi(D+d_n)}{N}-\sin\frac{\pi D}{N}\right]\end{aligned} \tag{11}$$

where $\sin\frac{\pi D}{N}$ is a constant and $e^{-j\frac{\pi}{N}(2n+1)}$ represent N unit vectors with equal phase intervals. Thus, (12) can be obtained, and (13) can be conducted by (11) and (12)

$$\sum_{n=0}^{N-1} e^{-j\frac{\pi}{N}(2n+1)}\sin\frac{\pi D}{N} = 0 \tag{12}$$

$$\boldsymbol{A_{tN-1,1}} = \frac{2e^{-j\frac{\pi}{N}}}{\pi}\sum_{n=0}^{N-1}\left[e^{-j\frac{2n\pi}{N}}\sin\frac{\pi(D+d_n)}{N}\right]. \tag{13}$$

To simplify (13), (14) is obtained by using Taylor's formula and ignoring the terms higher than the first order

$$\sin\frac{\pi(D+d_n)}{N}\approx\sin\left(\frac{\pi D}{N}\right)+\cos\left(\frac{\pi D}{N}\right)\frac{\pi D_{N-1}}{N}\cos\left(\frac{2n\pi}{N}+\varphi\right). \tag{14}$$

Substitute (14) and (12) into (13), $\boldsymbol{A_{tN-11}}$ can be expressed as follows:

$$\boldsymbol{A_{tN-1,1}}\approx\frac{2D_{N-1}\cos\left(\frac{\pi D}{N}\right)e^{-j\frac{\pi}{N}}}{N}\sum_{n=0}^{N-1}\left[e^{-j\frac{2n\pi}{N}}\cos\left(\frac{2n\pi}{N}+\varphi\right)\right]. \tag{15}$$

Similar to (12), it can be easily obtained that

$$\sum_{n=0}^{N-1} e^{-j\left(\frac{4n\pi}{N}+\varphi\right)} = 0, N\geq 3. \tag{16}$$

Therefore, (15) can be written as

$$\boldsymbol{A_{tN-1,1}}\approx D_{N-1}\cos\left(\frac{\pi D}{N}\right)e^{j\left(\varphi-\frac{\pi}{N}\right)} \tag{17}$$

which shows that the phase φ can be extracted from the base frequency component of the additional carrier, implying that M-ary phase modulation can be applied when $N\geq 3$.

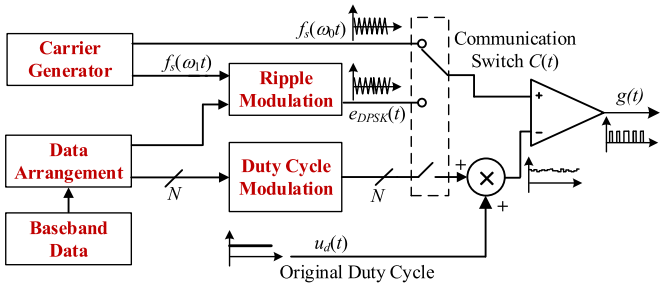

Fig. 11. Modulation process of combined 3-DoF modulation.

However, when $N = 2$, (16) turns to (18)

$$\sum_{n=0}^{N-1} e^{-j\left(\frac{4n\pi}{N}+\varphi\right)} = 2e^{-j\varphi} \tag{18}$$

so (17) is not satisfied, and (13) becomes

$$\boldsymbol{A_{t1,1}} \approx 2\cos\varphi D_1 \cos\left(\frac{\pi}{2}D\right) e^{-j\frac{\pi}{2}} \tag{19}$$

where φ appears in the amplitude of the coefficient, instead of the phase. Consequently, if phase detection is applied for communication, M-ary modulation is unable to be applied under the value of $N = 2$. In this case, only binary modulation is applicable.

C. Practical Modulation and Demodulation Scheme

Fig. 11 depicts the modulation scheme of the combined 3-DoF modulation in which the carrier generator generates two carriers with distinct angular frequencies ω_0 and ω_1. When the converter does not send data, the communication switch $C(t)$ selects $f_s(\omega_0 t)$ as the PWM carrier, and the whole process is identical to the conventional PWM control. When the converter sends data, $C(t)$ selects $e_{\mathrm{DPSK}}(t)$, which is the DPSK modulated signal using carrier $f_s(\omega_1)$ and the arranged data for ripple, to be the PWM carrier. The duty cycle modulation process generates duty cycle variation for N additional carriers based on the arranged data, and the final PWM reference is the sum of the original duty cycle and the duty cycle variation. Consequently, the gate signal can generate modulated ripple and additional carriers simultaneously.

Compared with the FH-DPSK scheme, which is with the best bitrate performance in previous works that can be applied in most of the ordinary converters, the proposed scheme uses the same way to modulate the phase, and frequency is not directly used for bitrate improvement either. Thus, the proposed scheme has the same bitrate performance when only considering the phase and the frequency. Moreover, it uses the duty cycle to improve the bitrate, and symbols modulated on the duty cycle share the same symbol length as those modulated on the phase. Therefore, the combined 3-DoF modulation scheme has an obviously better bitrate performance.

The demodulation process is shown in Fig. 12. The received signal $e(t)$ is first filtered by a bandpass filter according to the carrier frequency. Then, coherent demodulation processes are applied to extract the phase of each carrier, and digital data

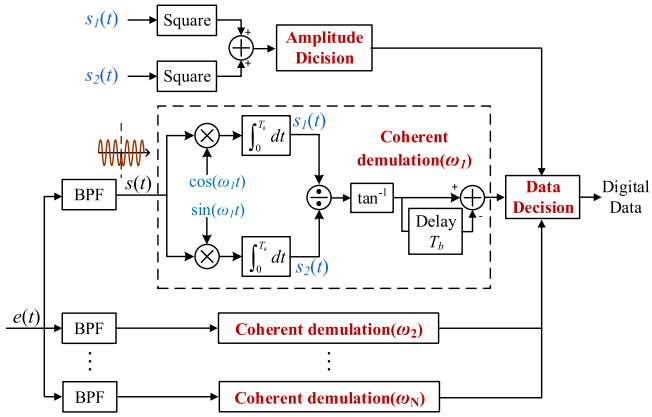

Fig. 12. Demodulation process of combined 3-DoF modulation.

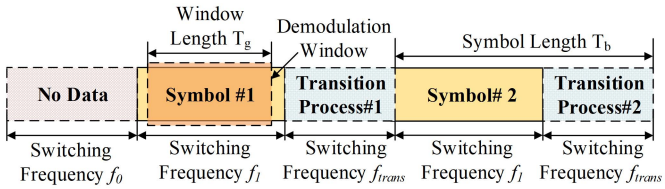

Fig. 13. Communication frame format.

are obtained by data decision. The figure shows N coherent demodulation processes, including one for the switching ripple and $N-1$ for the additional carriers.

In each coherent demodulation process, the input signal is multiplied by two sinusoidal signals with a $\pi/2$ phase difference, and their frequencies are the same as that of the input signal. The two products are then integrated within a demodulation window T_g, and the results are used to calculate the phase using inverse trigonometry. The phase difference between the current and the previous symbol can be easily calculated using subtraction. Besides, the integration results $s_1(t)$ and $s_2(t)$ are used to calculate ripple amplitude, which is judged by amplitude decision and tells the data decision process whether there is a converter sending data. The synchronization of demodulation is also achieved by the amplitude decision. The position of the demodulation window for the first symbol is supposed to have a maximum amplitude calculated by $s_1(t)$ and $s_2(t)$, and the following windows are obtained by delaying T_b.

The format of the communication frame is depicted in Fig. 13. When no data are being transmitted, the converter selects switching frequency f_0 and the duty cycle is determined solely by power control, producing no additional carrier. The frequency is shifted to f_1 when it comes to symbol#1 and the duty cycle variation is applied to produce additional carriers. To ensure the correctness of demodulation, the demodulation window should be included in this area. Then, it comes to the transition process, which has been discussed and explained in [23]. The frequency is shifted to f_{trans} for good phase-shift performance, and the duration of the process is determined by the phase difference of the two adjacent symbols.

As this scheme employs multiple frequencies, in order to prevent interference between them, demodulation window length

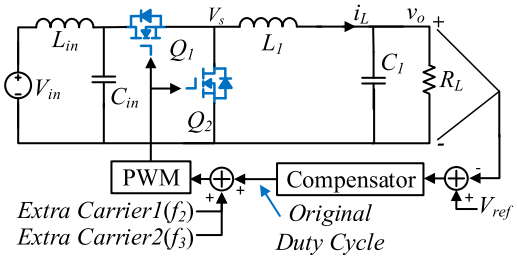

Fig. 14. Schematic of a buck converter using combined 3-DoF modulation.

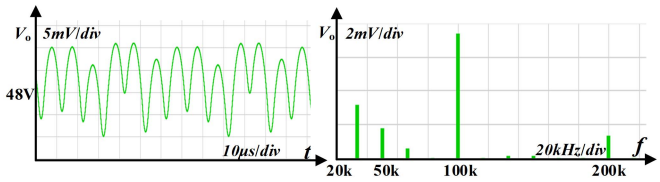

Fig. 15. Simulation output voltage of the buck converter.

T_g should satisfy (20) [8], [23], [24], where T_0, T_1, and T_n are the periods corresponding to f_0, f_1, and the nth additional carrier frequency

$$T_g = N_0, \quad T_0 = N_1, \quad T_1 = N_n\, T_n, \quad N_1, N_2, N_n \in N^*. \tag{20}$$

Additionally, (21) should be satisfied to guarantee that the demodulation window can be included within a symbol [23]

$$T_b - K_1 T_1 \geq T_g \tag{21}$$

where T_b is the symbol length, $K_1 T_1$ is the duration of the transition process, and K_1 is a positive integer.

The proposed combined 3-DoF scheme is applicable in converters that only use the duty cycle to control the power, while the frequency and the phase do not influence the power control, such as buck, boost, and buck–boost.

IV. Simulation and Experiment

The practical scheme for the experiment is shown as follows. Frequency control of the gate signal is applied for the transition process and distinguishing the communication signal. The 83.3 kHz and 100 kHz switching frequencies are for power conversion only and communication, respectively. Phase control is applied to modulate data on the ripple's phase, and duty cycle control is applied to generate additional carriers. Two additional carriers are applied in the experiment, and they are 2DPSK and 4DPSK modulated, respectively. The sampling frequency of the receiver is 1 MHz.

A. Simulation Results

The schematic of the simulation is shown in Fig. 14, and the closed-loop bandwidth is 4.5 kHz. The parameters are listed in Table I, where f_0 is the switching frequency for no data sending and f_1 is the switching ripple for data sending. The simulation result is shown in Fig. 15, where additional carriers with frequencies f_2 and f_3 are applied. The figure depicts the output voltage ripple and its frequency spectrum.

TABLE I
Experimental Parameters

Parameter	Value	Parameter	Value
V_{in}	200 V	f_2	50 kHz
V_o	48 V	f_3	33.3 kHz
L	300 μH	T_b	120 μs
C	100 μF	T_g	60 μs
R	10 Ω	M-ary(f_1)	4
C_{in}	100 μF	M-ary(f_2)	2
L_{in}	2 μH	M-ary(f_3)	4
f_0	83.3 kHz	Bitrate	41.7 kb/s
f_1	100 kHz	ΔD	0.02
MCU	TMS320F28377DZWT	Q_1,Q_2	IPW65R080CFD

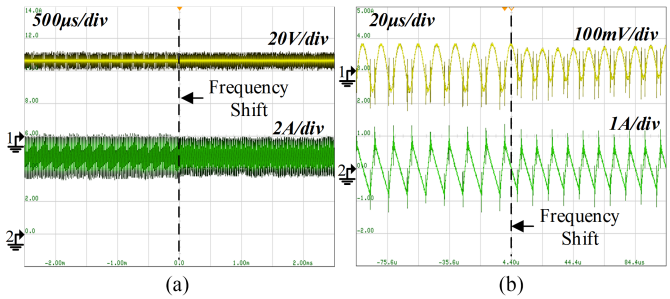

Fig. 16. Waveforms of frequency shift in (a) large time scale and (b) small time scale.

The spectrum clearly shows five peaks with the following frequencies: 33.3, 50, 66.7, 100, and 200 kHz. The two frequencies, i.e., 50 and 33.3 kHz, correspond to f_2 and f_3, indicating that the two frequencies can be detected from the ripple, so they are practicable as signal carriers. Their amplitudes can be easily increased by increasing the modulation depth ΔD. The 66.7 kHz component is the second harmonic of f_3. Because f_1, f_2, and f_3 are orthogonal, the harmonic does not influence the communication channel of the three frequencies. The 100 kHz component consists of the switching ripple with frequency f_1, the third harmonic of f_3, and the second harmonic of f_2. According to Section III-A, as long as the triangular PWM carrier is adopted, the communication channel of frequency f_1 will not be influenced. The 200 kHz component is considered as noise in this system and should be filtered.

B. Experimental Results

Fig. 16(a) shows the output voltage (CH1) and inductor current (CH2) waveforms of the converter when the switching frequency shifts from 83.3 to 100 kHz, and their dc values are 48 V and 4.8 A, respectively. Fig. 16(b) shows the zoomed-in waveforms of Fig. 16(a), and the peak-to-peak amplitudes of the ripples under 83.3 and 100 kHz are 154 mV, 1.71 A, 106 mV, and 1.46 A, respectively.

Fig. 17(a) and (b) depicts the waveforms when the converter is sending random data using FH-DPSK. The channels 1–5 denote the gate signal, output voltage ripple, transmitted digital

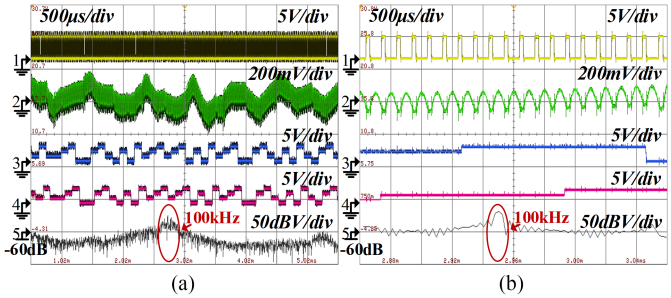

Fig. 17. Waveforms of FH-DPSK in (a) large time scale and (b) small time scale.

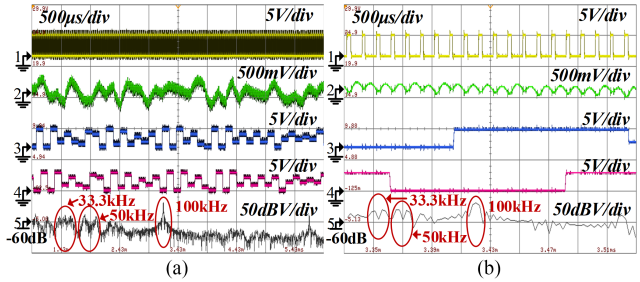

Fig. 18. Waveforms when only additional carriers are applied in (a) large time scale and (b) small time scale.

data, received digital data, and frequency spectrum of CH2, respectively. The digital data are received correctly and the 100 kHz component can be obviously observed in CH4. In this case, the bitrate is 16.7 kb/s.

Fig. 18(a) and (b) shows the waveforms when the converter is sending random data only using additional carriers, and the switching ripple is not digitally modulated. The channels 1–5 denote the gate signal, output voltage ripple, transmitted digital data, received digital data, and frequency spectrum of CH2, respectively. The carrier frequencies f_2 and f_3 and the modulation depth ΔD are listed in Table I. The frequency components of f_2 and f_3 can be observed in Fig. 18(a). However, due to their short symbol length and small modulation depth, the component of f_2 and f_3 cannot be clearly observed in Fig. 18(b). All the data are received correctly, demonstrating that the carriers with frequencies higher than one-fifth of the switching frequency can also be applied for communication, and additional carriers with different frequencies do not influence each other. In this case, the bitrate is 25 kb/s.

Fig. 19(a), (c), and (e) shows the waveforms of modulation using the proposed scheme while the converter is sending data, and the corresponding modulation depth is 0.008, 0.02, and 0.05, respectively. Fig. 19(b), (d), and (f) shows the same waveforms under a smaller time scale. The channels 1–5 denote the gate signal, output voltage ripple, transmitted digital data, received digital data, and frequency spectrum of CH2, respectively. Compared with the 100 kHz component in Fig. 18(a), the 100 kHz bandwidth in Fig. 19(a), (c), and (e) is broadened, showing that it has been digitally modulated. All the data are received correctly, implying that the ripple and additional carriers do not influence each other, proving the feasibility of the proposed scheme and

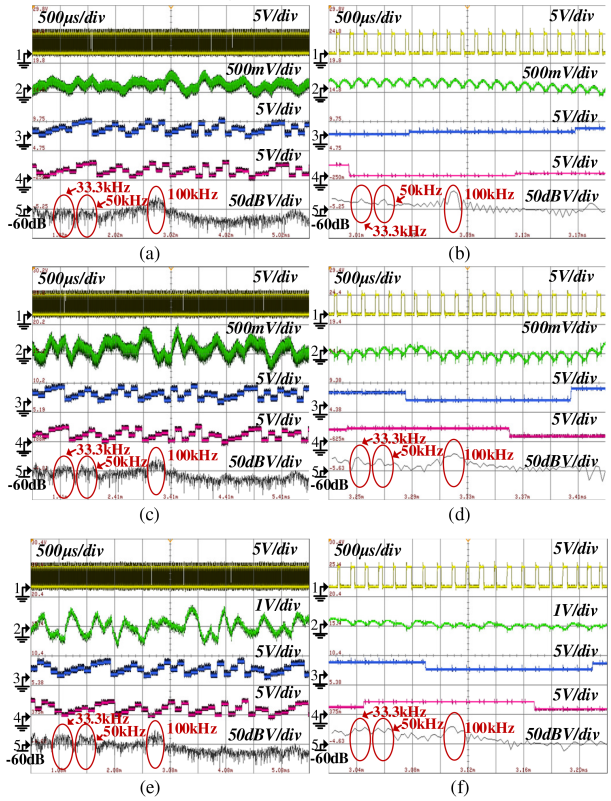

Fig. 19. Waveforms of combined 3-DoF modulation under the modulation depth of (a) 0.008 in large time scale and (b) 0.008 in small time scale, (c) 0.02 in large time scale and (d) 0.02 in small time scale, and (e) 0.05 in large time scale and (f) 0.05 in small time scale.

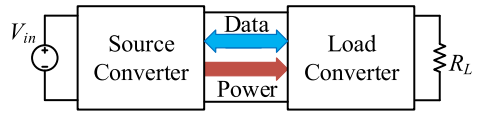

Fig. 20. Structure of multiple-converter experiment.

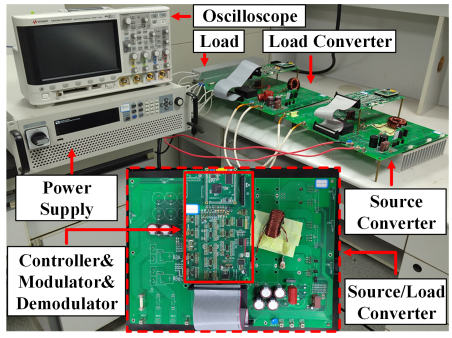

Fig. 21. Photograph of the experimental prototype.

showing good overall performance under different modulation depths. In this case, the bitrate is 41.7 kb/s.

When converters are connected, as shown in Fig. 20, the platform is shown in Fig. 21, and the performance of the proposed scheme is shown in Fig. 22. The components of 33.3, 50, 83.3, and 100 kHz can be obviously observed in

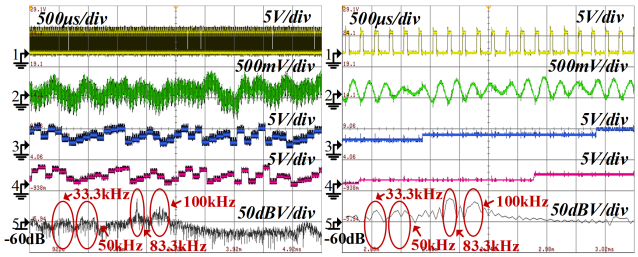

Fig. 22. Waveforms of combined 3-DoF modulation under multiple working converters (a) in large time scale and (b) in small time scale.

TABLE II
COMPARISON OF FH-DPSK AND COMBINED 3-DOF

Scheme / Parameter	Bitrate	Output Disturbance	Implementation
FH-DPSK	16.7 kb/s	small	simple
Combined 3-DoF	41.7 kb/s	large	complex

CH5. Bidirectional communication between the source and load converter is achieved, and all the data are received correctly; besides, the tested bit error rate is under 10^{-6}. In conclusion, converters not sending data do not influence communication in the proposed scheme, and the scheme is applicable in occasions with multiple working converters.

Based on the above experimental results, Table II presents the comparison between the FH-DPSK scheme and the combined 3-DoF scheme, where the two schemes are compared under the same experimental prototype and operating condition. It is obvious that the combined 3-DoF scheme has a higher bitrate; however, it also brings larger output disturbance and is harder for implementation.

V. CONCLUSION

This article proposes a novel combined 3-DoF modulation scheme that applies the control of frequency, phase, and duty cycle to increase the bitrate, achieving a better bitrate performance than FH-DPSK schemes. Moreover, the compatibility between the control of the 3-DoF for communication as well as the influence between different carriers are discussed. Simulations and experiments are conducted to prove the correctness of the relevant analysis, and the bitrate of 41.7 kb/s is achieved under the switching frequency of 83.3 kHz/100 kHz on a 230 W experimental platform.

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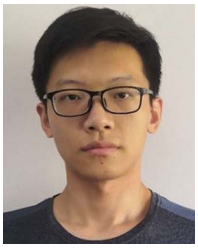

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