Letters

Power Decoupling Rectifier With Common-Ground Concept for Lighting Applications

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***Abstract*—The lightweight and the electrolytic capacitor-less are the development trends of microconverters for transportation lighting applications. Some solutions available to address the power fluctuations are caused by electrolytic capacitor-less. However, the leakage currents caused by nonisolated converters have been little studied. Given this, an improved transformerless single-phase rectifier based on the virtual dc-bus concept is proposed in this letter. This solution connects the negative of the LED array directly to the grid neutral, thus shorting the stray capacitance to the ground, suppressing leakage currents, and improving system reliability. In addition, the active pulsating power buffering solution is introduced with only one additional power switch due to the sharing of cells. Finally, the experimental results verify the correctness and superior performance of the proposed solution.**

***Index Terms*—Common-mode current, lighting applications, power decoupling, single-phase rectifier.**

I. Introduction

In RECENT years, due to the benefit of high transfer efficiency, single-phase power factor correction (SPPFC) rectifiers have gotten a lot of attention [1], [2]. Unfortunately, most SPPFC rectifiers still require hefty EMI modular and electrolytic capacitors (Ecaps). It is worth noting that Ecaps is also responsible for one-third of all circuit defects [3].

Considering this, many researchers focus on improving the topologies to achieve non-Ecaps by introducing active circuits. In [4] and [5], three-port converters based on flyback circuits are proposed with the third port used to cope with the power ripple and recover the leakage energy. The third port and the main circuit, however, are generally independent, resulting in significant component redundancy and higher production costs. In this regard, the typical H-bridge and the active buffer circuit (ABC) are cascaded to obtain a four-switch configuration by sharing one bridge arm [6], [7]. But, the bidirectional power flow in each switching cycle of the ABC makes it difficult to optimize the efficiency. Qi et al. [8] and de Araújo et al. [9] investigate unidirectional ABCs. Due to the scheme of energy-flow-path optimization (EFPO), the majority of the energy is transmitted straight to the load while the buffer tank only deals with pulsing power. In the ABCs, the energy processing connection is then further lowered. It is worth noting that the miniaturization of the microrectifier is the inevitable trend, so the transformer should be considered a redundant component and should be removed.

Unfortunately, the removal of line-frequency or high-frequency transformers will result in an electrical connection between the load and the grid. As a result, the common-mode leakage current caused by the change of common-mode voltage increases the total harmonic distortion (THD) of the grid current, system loss, and even threatens personal safety. Therefore, the reliability of these converters is poor. In this regard, the converters, with two bridge legs and four switches, are presented in [10] and [11] to satisfy the needs of ac/dc applications. This kind of topology has the characteristics that the negative of the load is grounded with the neutral point of the grid, obviating the requirement for an isolation transformer and eliminating common-mode current. The principle is to short circuit the stray capacitance directly. However, the problem of the inrush current limits its application, and power decoupling is not taken into account. As a result, a compact, high-efficiency, long-life, and nonisolated LED driver is urgently needed.

Given the above shortcomings, a revolutionary SPPFC rectifier with reduced leakage currents and power decoupling capabilities is proposed in this letter. Compared to similar works, the main advantage of this topology is the zero-leakage currents and

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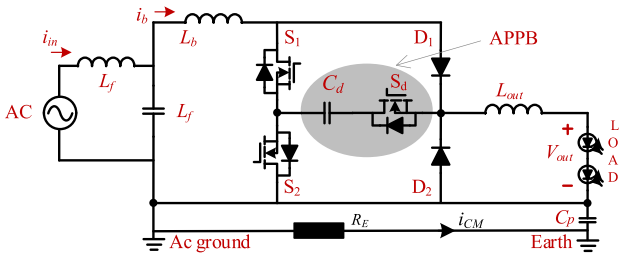

Fig. 1. Topology of the proposed SPPFC rectifier.

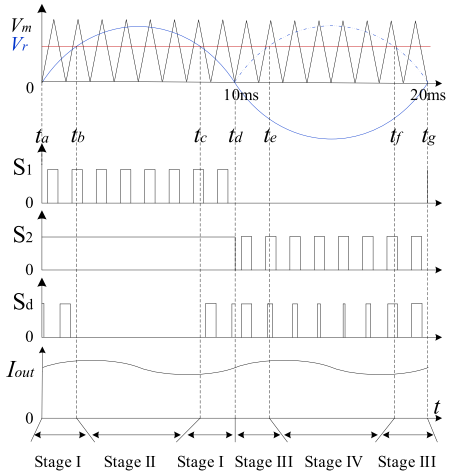

Fig. 2. Modulation method of the proposed SPPFC rectifier.

the near-zero double-frequency ripple in the absence of transformers and Ecaps. In short, the output terminal of the proposed rectifier is common-ground (CG) with the grid, so the leakage current could be eliminated. Furthermore, by introducing an extra switched network, a unidirectional APPB cell is produced without the inrush current, and the pulsating power is absorbed.

II. Proposed Topology

The proposed rectifier consists of a conventional boost circuit, a modified H-bridge, and a switch-capacitor cell (SCC), as shown in Fig. 1. A conventional boost circuit and a modified H-bridge (S_1–S_2, D_1–D_2) are employed to perform the PFC function and provide a power transmission path for SCC, respectively. The SCC (C_d, S_d) is used to absorb pulsating power and is regarded as APPB. The traditional boost converter and the modified H-bridge are integrated through time-sharing multiplexing the switches S_1–S_2 and the diode D_1.

A. Modulation Method

Fig. 2 shows the subregion based on the PWM method. According to the intersection between the reference wave V_r and the modulating wave V_m, the positive reference wave (stages I and II) and the negative reference wave (stages III and IV) both have two stages.

1) Positive Input Voltage $V_{in} > 0$ (t_a–t_d)*:* Stage I (t_a–t_b, t_c–t_d): The input power is less than the output power. Therefore, the power deficit at this stage needs to be provided by a decoupled capacitor to maintain the power balance of the system. This stage requires three modes to complete together, as shown in Fig. 3(a)–(c).

Stage II (t_b–t_c): The input power is greater than the output power, and the surplus power needs to be absorbed by the decoupled capacitor. Therefore, this stage requires two modes to complete together, as shown in Fig. 3(a), (b).

2) Negative Input Voltage $V_{in} < 0$ (t_d–t_g)*:* Stage III (t_d–t_e, t_f–t_g) and Stage IV (t_e–t_f): The completion of these two stages requires three modes, as shown in Fig. 3(d)–(f). The difference lies in the duty cycle of the switch S_d in the APPB. From Fig. 2, the switch S_d presents sinusoidal pulsewidth modulation (SPWM) to realize energy buffering operation.

B. Operating Principle

Fig. 3 shows the six operating modes of the proposed rectifier. The current path is indicated by the red arrows in the diagram. These models are discussed in detail as follows.

Mode 1: At the start of this mode, S_1 is ON. The ac source v_{in} charges the inductor L_b, and the inductor current i_b increases linearly. Meanwhile, the output current freewheels through the diode D_2, as shown in Fig. 3(a)

$$\frac{di_b}{dt}L_b = v_{in}, \quad \frac{dI_{out}}{dt}L_{out} = V_{out} \tag{1}$$

where the current flowing through L_{out} is I_{out}.

Mode 2: S_1 is turned OFF at the beginning of this mode. The inductor Lb is discharging to the SCC and the load, as shown in Fig. 3(b)

$$\frac{dV_C}{dt}C_d = i_b - I_{out} \tag{2}$$

where the voltage across the capacitor C_d is V_C.

Mode 3: S_2 is turned ON at the beginning of this mode. The APPB starts running and is discharging to the inductor L_{out} and the load, as presented in Fig. 3(c). The equation in this state is derived as

$$\frac{dI_{out}}{dt}L_{out} = V_C - V_{out}. \tag{3}$$

Mode 4: The voltage v_{in} charges the inductor L_b, and the inductor current increases linearly. Meanwhile, the APPB is discharging to the inductor L_{out} and the load, as shown in Fig. 3(d)

$$\frac{di_b}{dt}L_b = v_{in}, \quad \frac{dI_{out}}{dt}L_{out} = V_C - V_{out}. \tag{4}$$

Mode 5: S_2 is turned OFF at the beginning of this mode. The inductor Lb is fully discharging to the APPB. Meanwhile, the output current freewheels through the diode D_2, as presented in Fig. 3(e)

$$\frac{di_b}{dt}L_b = v_{in} - V_C, \quad \frac{dI_{out}}{dt}L_{out} = V_{out}. \tag{5}$$

Mode 6: The current only appears at the load and freewheels through the diode D_2.

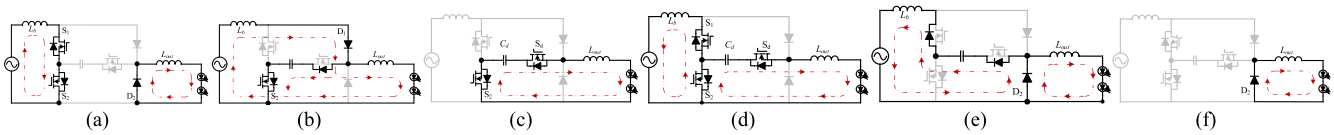

Fig. 3. Equivalent circuit of one switching period. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

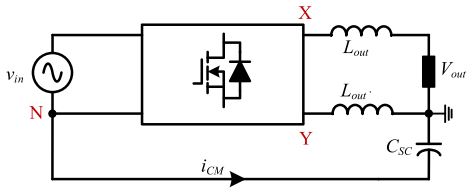

Fig. 4. Equivalent diagram of SPPFC rectifier with leakage current path.

III. Performance Analysis

A. Common-Mode Current Analysis

Fig. 4 shows a simple equivalent model of a conventional SPPFC rectifier with parasitic capacitance. As can be seen from Fig. 4, the common-mode voltage $V_{\rm CM}$ and the differential-mode voltage $V_{\rm DM}$ can be calculated by

$$V_{\rm CM} = \frac{V_{\rm XN} + V_{\rm YN}}{2}, \quad V_{\rm DM} = V_{\rm XN} - V_{\rm YN} \tag{6}$$

where $V_{\rm XN}$ is the voltage at both ends of X and N, and $V_{\rm YN}$ is the voltage at both ends of Y and N.

According to [5], $V_{\rm DM}$ also affects the leakage current, so the total mode voltage $V_{\rm TCM}$ can be expressed as

$$V_{\rm TCM} = \frac{V_{\rm XN} + V_{\rm YN}}{2} + \frac{V_{\rm XN} - V_{\rm YN}}{2} \frac{L'_{\rm out} - L_{\rm out}}{L_{\rm out} + L'_{\rm out}}. \tag{7}$$

From Fig. 1, we could know that $L'_{\rm out} = 0$. Therefore, (7) can be simplified to $V_{\rm TCM} = V_{\rm YN}$. Then, the common-mode current on the parasitic capacitor is

$$i_{\rm CM} = C_{\rm SC} \frac{dV_{\rm TCM}}{dt} \tag{8}$$

where $C_{\rm SC}$ is the stray capacitance.

According to (8), the leakage current is affected by the amplitude and frequency of the change of voltage $V_{\rm TCM}$. The proposed rectifier topology benefits from the CG structure, $V_{\rm YN} = 0$. Therefore, the new topology can eliminate the leakage current.

B. Power Decoupling Analysis

Since the operation is different between $v_{\rm in} > 0$ and $v_{\rm in} < 0$, there are two values for C_d. The relationship between the capacitance and the voltage ripple is

$$\Delta U = \frac{Q}{C_{de}} \tag{9}$$

where ΔU is the voltage ripple across the capacitor C_d, and Q is the amount of charge of the capacitor C_d.

From Fig. 3, we have

$$Q_1 < Q_{1'}. \tag{10}$$

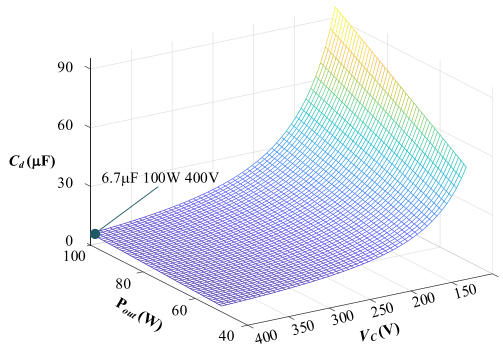

Fig. 5. Relation curve between $P_{\rm out}$, V_C, and C_d.

Hence, by combining (10) and (11), we have

$$\Delta U_1 < \Delta U_{1'} \tag{11}$$

where ΔU_1 and $\Delta U_{1'}$ represent the voltage ripples for $v_{\rm in} > 0$ and $v_{\rm in} < 0$, respectively.

According to (11), a larger capacitance is needed under $v_{\rm in} < 0$ to limit the voltage ripple within the allowable range. As a result, the selection of decoupled capacitor is based on the condition of $v_{\rm in} < 0$. Suppose PF $= 1$, the change of the C_d energy storage ΔE [3] can be expressed as

$$\Delta E = \int_{\pi/4}^{3\pi/4} \frac{P_{\rm in} - P_{\rm out}}{\omega} d\omega t = \frac{P_{\rm out}}{\omega} \tag{12}$$

where $P_{\rm out}$ is the output power, $P_{\rm in}$ is the input power, and ω is the grid angular frequency.

Since the energy stored in the capacitor is determined by its capacitance and voltage, the energy storage variation ΔE can be expressed as

$$\Delta E = \frac{1}{2} C_d (V_{C1}^2 - V_{C2}^2) = C_d \Delta V_C \Delta V_{C-\rm av} \tag{13}$$

where V_{C1}, V_{C2}, ΔV_C, and $\Delta V_{C-\rm av}$ are the maximum, minimum, ripple, and average values of the voltage V_C, respectively.

Combining (12) and (13), the equivalent capacitance can be expressed as

$$C_d = \frac{P_{\rm out}}{\omega \Delta V_C \times V_C}. \tag{14}$$

According to (14), when $P_{\rm out}$, ΔV_C, and V_C are fixed values, increasing ΔV_C can reduce the capacitance, and remove the electrolytic capacitors. Considering a 20% capacitance voltage ripple, Fig. 5 shows the change of decoupling capacitance from half-load to full load. Obviously, the maximum voltage of the decoupling capacitor and rated power must be determined before the decoupling capacitance is selected.

TABLE I
COMPARISON OF PROPOSED CONVERTER WITH OTHER RECENT WORKS

Refs.	Out power P_{out}	Number of			Rated voltage and rated current of		NCM	NIC	PD (W/cm²)	Maximum efficiency
		S	D	C	S Model	D Model				
[3]	80 W	4	3	1	600 V/1.9 A	400 V/5 A	√	√	1.01	97.1%
[5]	100 W	4	4	2	600 V/3.5 A	450 V/5 A	×	×	0.78	94.7%
[7]	100 W	2	5	2	600 V/20 A	650 V/6 A	×	×	≈1.33	No data
[8]	110 W	2	6	2	400 V/25 A	400 V/3 A	×	√	1.13	95.1%
[9]	43 W	2	7	7	–	–	×	√	0.33	93.2%
[10]	–	4	4	2	–	–	×	√	–	–
[11]	180 W	4	0	2	–	–	√	×	–	93.3%
[12]	150 W	10	6	8	–	–	×	×	≈2.86	92%
[13]	100 W	2	5	3	600 V/13 A	150 V/87 A	×	×	1.76	94%
Proposed	100 W	3	2	1	600 V/1.9 A	600 V/4 A	√	√	1.11	96.8%

Note: S is the switch, D is the diode, C is the capacitor, PD is the power density, NCM is the non-common current, and NIC is the noninrush current.

C. Comparative Analysis

Table I provided to summarize comparisons of the popular SPPFC non-Ecaps rectifiers and the proposed rectifier. The comparative items are the number of the switches, the diodes, and the capacitors. The performances such as the common-mode current, the inrush current, the power density, and the efficiency are also considered.

To be fair, the measured efficiency of all topologies is at the switching frequency of 25 kHz. As can be realized from Table I, the work in [3] is slightly higher than the proposed topology in the transmission efficiency. However, the proposed topology requires fewer semiconductor devices and can achieve higher power density. Liu et al. [10] utilize virtual *LC* technology to realize the power decoupling, which leads to complex control strategies and difficult mass production. Although the performance of the work in [11] is good, the current stress of switches is high. Compared with the work in [5], [7], [8], and [10], the proposed topology can achieve nearly zero common-mode current operation without an isolated transformer, so the reliability is higher. From Table I, the power density and the semiconductor selection perform well, which is due to the sharing of power devices with different functions and the inductors designed to participate in the operation of each mode.

Compared with the above schemes, ultrahigh-frequency is applied in [12], which benefits from the soft switching. The power density has been greatly improved. However, the overall number of semiconductor devices and magnetic components is higher than the proposed ones. In [13], the problems in [12] have been optimized, especially the number of switches has been drastically reduced. However, according to (8), a nonisolated converter with a switching frequency of 250 kHz results in a higher common-mode leakage current and endangers personal safety. Therefore, the proposed converter topology is more competitive.

IV. CONTROLLER DESIGN

The control method of output current and ripple current in this letter is shown in Fig. 6. The output current $i_{\rm out}$ passes through the detection resistance, and the average output current $I_{\rm out}$ is obtained by the low-pass filter. The detection signal is compared with the reference signal $I_{\rm out\text{-}ref}$. The error signal is

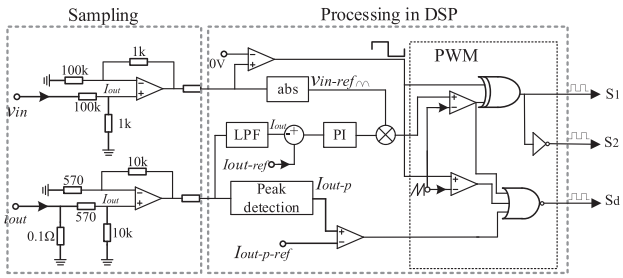

Fig. 6. Control block diagram for the proposed rectifier.

transmitted to the PI regulator. The detailed PI parameters are detailed in [14], which will not be described again in this letter. Subsequently, the output of the regulator is multiplied by $v_{\rm in\text{-}ref}$ to obtain the PFC tracking signal, which is transmitted to the PWM unit. Then, the required PWM driving signals are obtained through logic operation and transmitted to the switches S_1 and S_2. It is worth noting that $v_{\rm in\text{-}ref}$ is the electric signal after the input voltage takes the absolute value.

The output current ripple control is as follows. The peak output current $I_{\rm out\text{-}p}$ is obtained by peak current detection, and then, $I_{\rm out\text{-}p}$ is compared with the peak reference current $I_{\rm out\text{-}p\text{-}ref}$ to obtain the control signal of the output current ripple. $v_{\rm in\text{-}ref}$ gets a square-wave signal with the same frequency after zero detection to determine the working status of $S_{\rm d}$. After comparing the low-frequency square-wave signal, ripple current control signal, and sawtooth-wave, the driving signal is obtained through the logic gates and transmitted to the switch $S_{\rm d}$.

V. PERFORMANCE EVALUATIONS

To verify the performance of the proposed SPPFC rectifier, a 100 W prototype has been built in the lab, as shown in Fig. 7. The parameters are listed in Table II.

Fig. 8 depicts the measured waveforms of input current, input voltage, and the drive waveform of the switch S_1, whose waveforms are enlarged to the right in Fig. 8(a). It can be seen from Fig. 8(a) that 1) the inductor current is symmetrical within the positive and negative cycles of the grid frequency; 2) the current presents an SPWM signal and operates in discontinuous

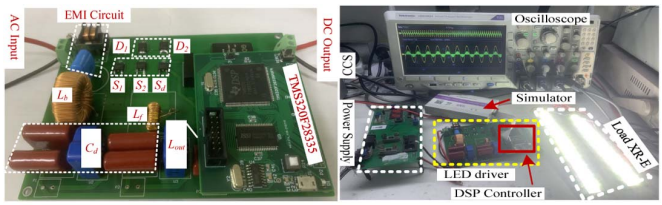

Fig. 7. Photo of (a) experimental prototype and (b) experiment platform.

TABLE II
COMPONENT PARAMETERS OF THE PROPOSED DRIVER

Parameters	Value	Parameters	Value
Input voltage v_{in}	220Vac	Filtering inductor L_{out}	500 μH
Rated power	100 W	PI	K_p = 0.2, K_i = 500
Switching frequency f_s	25 kHz	Input filter inductance L_f	3 μH/400 V
Decoupling capacitance C_d	4 ×2.2 μF/400 V	Input filter capacitance C_f	0.2 mF
Cree Cool white XR-E	45 Ω	Power switches S_1–S_2, S_d	FQD2N60C TM 600 V/1.9 A
PFC inductance L_b	100 μH	Diodes D_1–D_2	SVF4N60R D-TR

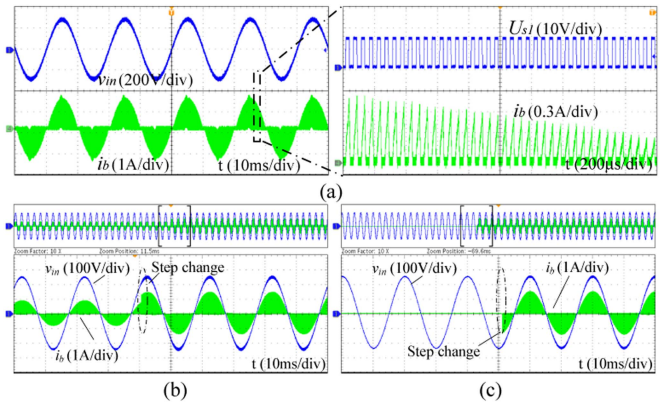

Fig. 8. Measured waveform of ac side. (a) Under steady-state. (b) Under dynamic 1. (c) Under dynamic 2.

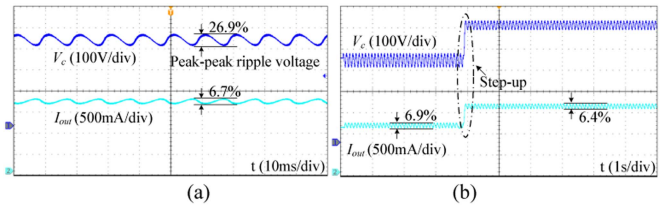

Fig. 9. Measured decoupled capacitor voltage. (a) Under steady-state. (b) Under dynamic-state.

conduction mode. As a result, the power factor is 0.989. The input current with robust dynamic performance and the noninrush current are observed in Fig. 8(b) and (c), respectively.

Fig. 9(a) and (b) depicts the measured decoupling voltage waveforms and the measured output current waveforms. From (14), it is clear that larger voltage ripples can effectively alleviate the dependence on the dc-link capacitance. The maximal ripple

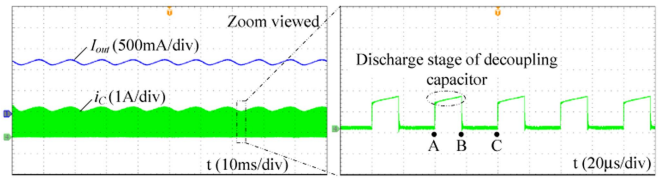

Fig. 10. Measured decoupled capacitor current.

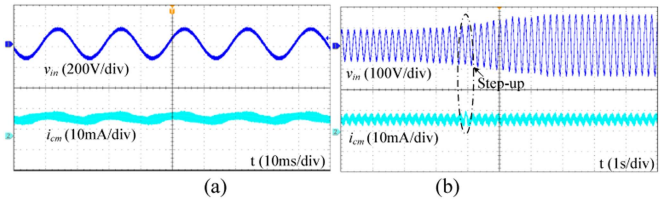

Fig. 11. Common-mode leakage current under (a) steady state and (b) dynamic state.

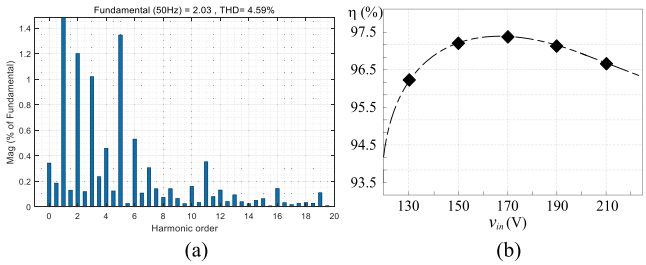

Fig. 12. Performance analysis. (a) Harmonic of input current $i_{\rm in}$. (b) Measured efficiency.

is 26.9% of the average voltage, which is the reason that the pulsating power is transferred to the decoupled capacitor. It can be noted that the ripple of the output current is less than 7% in both static and dynamic operations, so the APPB ripple does not affect the output current. It can also be seen from Fig. 9(b) that the brightness can be easily adjusted by changing the amplitude of the output current. Furthermore, as compared to the current ripple of 14.1% in [15], the performance of this letter is much improved because the decoupling capacitor is decoupled from the input side. In addition, due to the bootstrap effect of the decoupling capacitor in [15], the input current is less sinusoidal and the harmonic content is higher.

Fig. 10 shows the current of the decoupling capacitor i_C. The right side of Fig. 10 is an enlarged view. As can be seen from the enlarged view, the decoupling capacitor discharges the load from A to B, and the current increases slightly. From B to C, the switch S_d is turned OFF, and the inductor $L_{\rm out}$ provides energy for the load. The above process is consistent with the theoretical analysis.

To verify the effectiveness of suppressing CMC, a 90-nF parasitic capacitor is added to this prototype. Fig. 11 depicts the leakage current at various voltage levels. From Fig. 11, the leakage current is immune to the step-up voltage. And, when v_s = 90V, $i_{\rm CM}$ reaches 8.3 mA (rms value). As a result, the transformerless converter satisfies the stringent safety requirements of DIN VDE 0126-1-1 [9].

The grid current is analyzed using the fast Fourier transform, as shown in Fig. 12(a). The THD of the grid current i in is 4.59%, which compiles with the IEC-610003-2 standards. It is obvious from this finding that LED connectivity with the suggested LED driver is possible. Besides, the efficiency under rated power is shown in Fig. 12(b), where the output current and the output voltage are 1.6 A and 65 V, respectively. Finally, the proposed rectifier may achieve maximum efficiency of 96.8%.

VI. Conclusion

A novel SPPFC rectifier based on a virtual dc-bus is proposed in this letter. The CG feature completely removes leakage current, allowing the proposed topology to be used without a transformer. An integrated boost converter is used in such a way that the proposed rectifier can limit the SC precharge current while also minimizing the inrush current. Besides, only one additional power switch can obtain the power decoupling capability, which greatly simplifies the proposed structure. Finally, a 100-W experimental prototype is tested, and the measured results show a very good LED driving performance and a high degree of agreement with the analysis offered.

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