Parameters Influences Analysis and Optimization Design Method for Synchronous Transformer of Switched-Capacitor MMC-SST

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***Abstract*—In the switched-capacitor-based modular multilevel converter-solid state transformer scheme, the switched-capacitor circuit plays a key role in power transfer, electric isolation, voltage clamping, and low-frequency voltage ripple decoupling. However, the operational performances of switched-capacitor circuits are depended on the distribution parameters of synchronous transformers. To explore the parameter constraints, the mathematical model is established, the relationship between the active power transmission capacity and the transformer time constant is studied, the dynamic inrush current stress is also given. The analysis results show that the distribution resistance should be minimally designed to reduce the voltage clamping error, however, a large distribution resistance is good for suppressing the inrush current. Moreover, if the distribution resistance is large and the leakage inductance is small, the time constant is small, which benefits the power transfer. So, there are some contradictions in the transformer design, which needs to make a tradeoff. For coordinating the parameter optimization, the design criteria and influence factors of distribution parameters for the synchronous transformer are analyzed. Then the transformer optimization design flow considering distribution parameter constraints is proposed. Finally, the toroidal transformer prototype and the switched-capacitor experimental platform are developed to verify the correctness of the proposed scheme.**

***Index Terms*—Distribution parameters, modular multilevel converter-solid state transformer (MMC-SST), switched-capacitor circuit, synchronous transformer.**

NOMENCLATURE

SST	Solid State Transformer.
MMC	Modular Multilevel Converter.
SM	Submodule.
FB	Full Bridge.
LVdc	Low Voltage dc.
u_{SM}	SM capacitor voltage.
u_{LV}	LVdc voltage.
n	Transformer ratio.
S_1-S_4	FB switch devices.
g_1-g_4	FB driver signals.
u_{pri}	Transformer primary voltage.
u_{sec}	Transformer secondary voltage.
i_{T}	Transformer current.
L_{e}	Leakage inductance.
R_{e}	Distribution resistance.
ε_{v}	Voltage control error.
ε_{p}	Active power transfer ratio.
i_{T1}	Inrush current between SM capacitors.
i_{T2}	Inrush currents between SM capacitor and LVdc capacitor.
ΔV	Voltage deviation.
H	Magnetic field strength.
i_{SMx} (x = a,b,c)	SMx input current.
i_{FBx} (x = a,b,c)	FBx input current.
i_{HFac}	HFac output current.

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I. INTRODUCTION

WITH the significant emergence of photovoltaic, electric vehicles, energy storage systems, and other dc equipment, the traditional ac grid will face great changes and the construction of ac/dc hybrid grid has become a general trend gradually [1]. As the hub of ac/dc hybrid distribution system, solid state transformer (SST) has been a hot research direction both in industry and academia [2]. Compared with traditional power frequency transformers, which can only realize the power conversion and electrical isolation between ac–ac at the same frequency, SST integrates the power electronics semiconductor devices and high-frequency magnetic conversion technology [3], which can realize the conversion between various forms of power and voltage levels [4].

Modular multilevel converter (MMC) is a popular solution for medium- and high-voltage SSTs due to the inherent medium-voltage dc interface, modular design, and good harmonic performance [5]. However, a large number of low-frequency ripples are introduced on the submodule (SM) capacitors when there is power transfer between the medium voltage ac and dc port [6], and the large capacitance is required to absorb the low-frequency ripples, which causes a negative effect on the power density of the MMC-SST [7].

In order to reduce the SM capacitance for improving the power density of MMC-based systems, Teng et al. [8] proposed

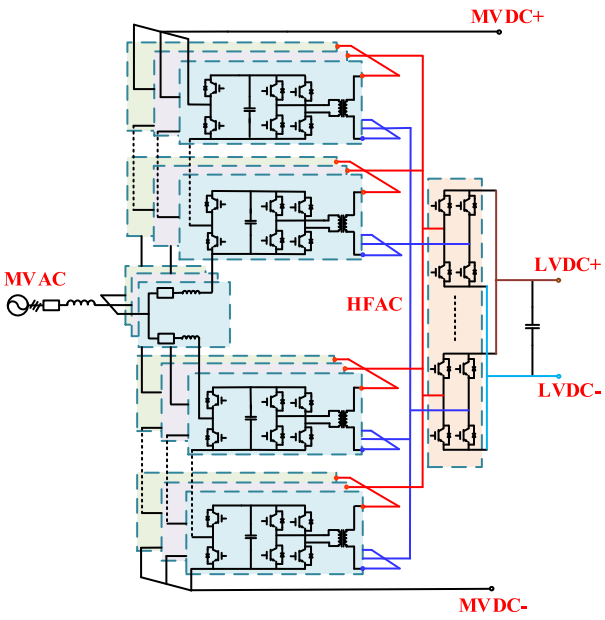


Fig. 1. Switched-capacitor conversion-based MMC-SST [9].

a miniaturization MMC structure of SMs parallel power coupling channel, which can realize a significant reduction of the capacitor volume and also the autonomous voltage equalization between the interconnected SMs. But the power coupling channel is only used to transmit ripple powers, resulting in low device utilization, and additional cost and loss. Based on the ripple powers coupling suppression idea, a switched-capacitor conversion-based MMC-SST topology is proposed in [9] as shown in Fig. 1. This topology is composed of a half-bridge MMC and a switched-capacitor interconnection circuit. The switched-capacitor interconnection circuit comprises a high-frequency ac (HFac) bus, synchronous transformers, and full-bridge (FB) modules driven by the same control signals. This structure has the following characteristics.

1) The SM capacitor voltage and low-voltage dc (LVdc) voltage are clamped by the HFac bus due to the switched-capacitor characteristic, which eliminates the voltage closed-loop control and saves the sensor resources.
2) The ripple powers present a symmetrical characteristic between three phases. Under synchronous control, the low-frequency ripple currents flowing into the SM capacitor originally will automatically flow into the HFac bus and cancel with others, which greatly improves the power density of SST.

Although the autonomous voltage clamping between SMs and ripple powers free transmission could be realized in [9], the switched-capacitor working performance is susceptible to the loop distribution parameters, which has not received much attention in previous studies. In the research and experiment, it is found that the distribution resistance of synchronous transformer and transmission line could bring steady-state error to the voltage clamping characteristic, while the leakage inductance parameter could reduce the power transfer efficiency of the switched-capacitor circuit. So it is necessary to make a further exploration of the influences between system performance and distribution parameters, which is an extension work of [9].

In the switched-capacitor conversion stage, the distribution parameters mainly exist in the high-frequency synchronous transformer, different from the high-frequency transformer design objectives of the dual active bridge [10] or series resonance converter [11] commonly used in the SST, which usually takes the transformer leakage inductance as the phase shifting inductor or resonance inductor for magnetic elements integration and reduce the parasitic resistance furthest to improve the conversion efficiency. In the switched-capacitor conversion process, the time constant defined as the ratio of leakage inductance to distribution resistance is expected as small as possible to improve the active power transfer capacity. Moreover, the distribution resistance should be designed compromised considering voltage clamping control and inrush current suppression. The design procedure of synchronous transformer is directly related to these distribution parameters, which play a critical role in the operation performance.

During the transformer design procedure, the choice of magnetic material is vital for different frequencies and power levels, a comparison between silicon steel sheets, amorphous and nanocrystalline alloy materials applied to medium- and high-frequency transformers is given in [12], results show that the nanocrystalline magnetic core is a preferred scheme in high power applications due to the high saturated magnetic flux density, curie temperature, and minimal core loss. Different core structures and winding arrangements could also affect the transformer distribution parameters [13], the toroidal core constituted by a closed geometry is suitable for the low leakage application [14], whereas the influence of frequency on leakage inductance in toroidal transformer has not been analyzed. The maximum magnetic potential is affected by the number of continuous winding layers, so the leakage inductance can be greatly reduced by cross-winding the primary and secondary windings [15]. In high-frequency applications, additional winding losses will be introduced by the proximity and skin effects, Litz wire and copper foil conductors are often used to reduce the winding losses [16]. Based on these, a high-frequency transformer design method based on multiobjective nondominant sorting genetic algorithm II fitted for the dual active bridge is proposed in [17], which takes the minimum difference between leakage inductance and phase shifting inductance as the optimized objective for improving the power density of dual active bridge. In [18], a 166 kW/20 kHz high-frequency transformer prototype is presented for the series resonant dc–dc converter, the excellent heat exchange can be realized through water-cooled technology and the parasitic resistance can be controlled to the minimum. But these design methods are not suitable for the synchronous transformer in switched-capacitor conversion.

In order to optimize the working performance of switched-capacitor interconnection circuit, this article proposed an optimization design method for a synchronous transformer based on the constraint analysis of distribution parameters. The main contributions of this article can be summarized as follows.

1) The distribution resistance in synchronous transformers can be utilized to improve the active power transfer ratio

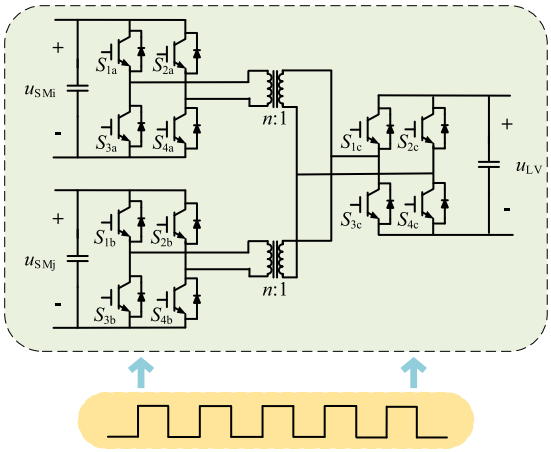


Fig. 2. Switched-capacitor simplified circuit.

and broaden the allowable voltage deviation range, but also bring the steady-state error to voltage clamping control.

2) The leakage inductance of synchronous transformers could cause the power backflow, thus reducing the active power transfer ratio and weakening the low-frequency ripple voltage decoupling characteristic.
3) The turn numbers, insulation distance, and winding arrangements are the main influencing factors to optimize distribution parameters during the synchronous transformer design procedure. An optimized design process to reduce leakage inductance and coordinate distribution resistance is considered for the switched-capacitor-based MMC-SST.

The rest of this article is organized as follows: the distribution parameter constraint is analyzed in the next section. In Section III, the distribution parameter optimization criteria and a synchronous transformer optimization design process fit for switched-capacitor conversion are presented. In Section IV, the synchronous transformer prototype based on the nanocrystalline toroidal core and a high-power switched-capacitor experimental platform that meets the application requirements are built for experimental verification. Finally, Section V concludes the article.

II. Distribution Parameter Constraint Analysis of High-Frequencies Transformer-Based Switched-Capacitor Circuit

A. Introduction of Switched-Capacitor Circuit

Since all the FBs connected to the HFac in Fig. 1 adopt the same control signals, the switched-capacitor simplified circuit shown in Fig. 2 can be discussed for easy understanding. Where $u_{SMi/j}$ and u_{LV} represent the $SM_{i/j}$ capacitor voltage and LVdc voltage, n is the transformer ratio, S_{1x}-S_{4x} (x = a, b, or c) are the switch devices. The FB switches on both sides of transformer are controlled by the synchronous signals, the energy could be transferred from high to low autonomously, so it behaves as a switched-capacitor circuit.

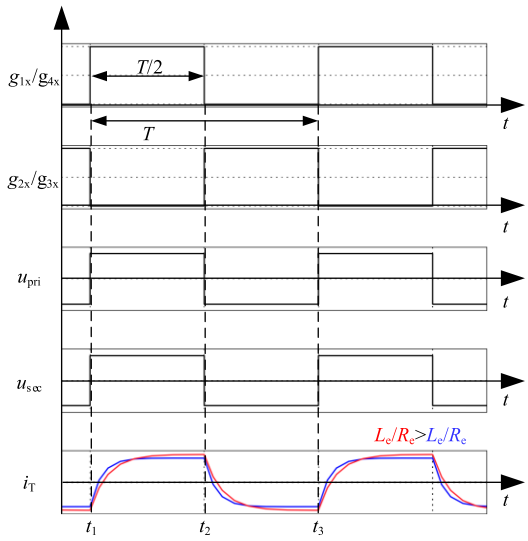


Fig. 3. Typical operating waveforms of the switched-capacitor circuit.

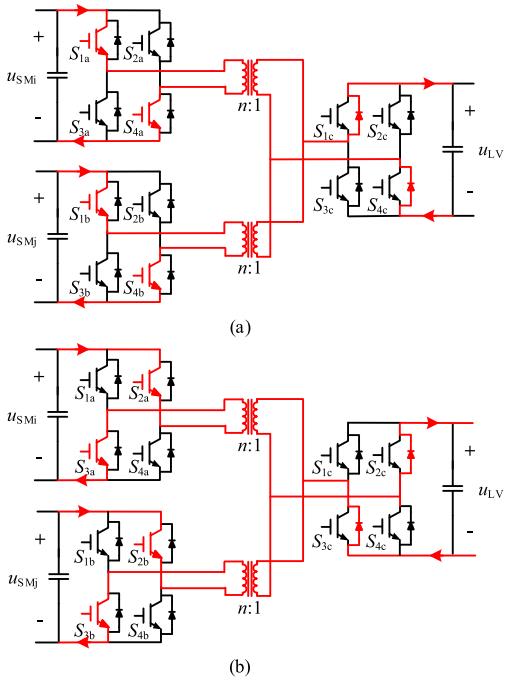


Fig. 4. Schematic diagram of energy transfer during a switching cycle. (a) Under stages t_1–t_2. (b) Under stages t_2–t_3.

The typical operating waveforms of the switched-capacitor circuit are shown in Fig. 3. Where g_{1x}-g_{4x} (x = a,b, or c) are the drive signals of switches, T is the switching cycle, u_{pri} and u_{sec} are the input and output voltage of the transformer, and i_T is the transformer current. There is no phase difference between the primary and secondary voltages due to the synchronous control and the transformer current presents an exponential functional tendency in each half of the switching cycle.

Take the energy transfer from SMs to the LVdc port as an example. When switches S_{1x}/S_{4x} are driven and S_{2x}/S_{3x} are blocked like the period t_1–t_2 of Fig. 3, the energy transfer process is shown in Fig. 4(a). It can be regarded as the capacitors of all

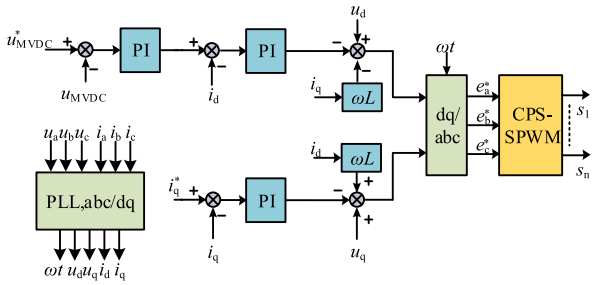


Fig. 5. MMC control diagram of the switched-capacitor-based MMC-SST.

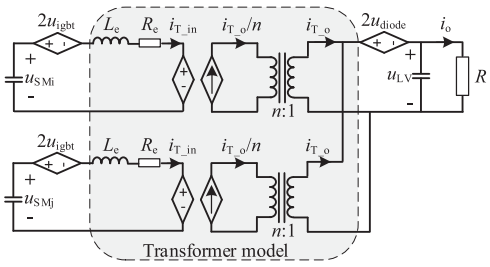


Fig. 6. Equivalent circuit model of switched-capacitor circuit.

SMs and LVdc port connected parallel through the transformers and HFac bus. When switches S_{2x}/S_{3x} are driven and S_{1x}/S_{4x} are blocked like the period t_2–t_3 of Fig. 3, the energy transfer process is shown in Fig. 4(b). Similarly, it can also be regarded as the capacitors of all SMs and LVdc port connected parallel through the transformers and HFac bus. Therefore, the voltage clamping characteristic could be realized by the switched-capacitor interconnected circuit.

As the basis of voltage clamping in switching capacitor interconnection circuit, the voltage of medium voltage dc bus should be stable firstly, which is controlled by the MMC stage as shown in Fig. 5. Then the SMs and LVdc voltages could be clamped by the medium voltage dc voltage indirectly. Besides the control scheme, another important factor is the distribution parameter of synchronous transformers, which could affect the precision of the voltage clamping and is discussed in the next section.

B. Impact of Transformer Distribution Parameters on Voltage Clamping

Based on the switching mode analysis, the equivalent circuit model of switched-capacitor circuit can be obtained, as shown in Fig. 6. Where u_{igbt} is the IGBT conduction voltage drop, u_{diode} is the diode conduction voltage drop, L_{e} is the transformer leakage inductance, R_{e} is the transformer distribution resistance, $i_{\mathrm{T\_in}}$ and $i_{\mathrm{T\_o}}$ are the input and output current of transformer, i_{o} is the load current, and R is the load resistance.

From Fig. 6, the mathematical model of the switched-capacitor circuit can be obtained

$$\begin{cases} u_{\mathrm{SMi/j}} = 2u_{\mathrm{igbt}} + R_{\mathrm{e}} i_{\mathrm{T\_in}} + L_{\mathrm{e}} \dfrac{di_{\mathrm{T\_in}}}{dt} + n\left(u_{\mathrm{LV}} + 2u_{\mathrm{diode}}\right) \\ i_{\mathrm{T\_in}} = \dfrac{i_{\mathrm{T\_o}}}{n} \\ i_{\mathrm{o}} = \dfrac{u_{\mathrm{LV}}}{R} \\ C_{\mathrm{LV}} \dfrac{du_{\mathrm{LV}}}{dt} = 2i_{\mathrm{T\_o}} - i_{\mathrm{o}} \end{cases} \tag{1}$$

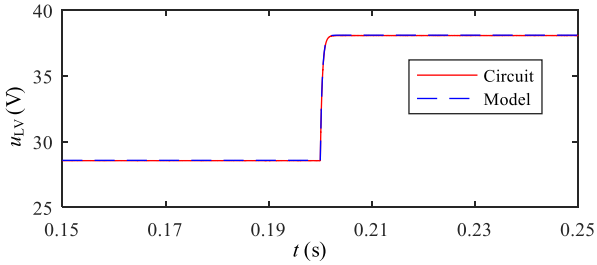


Fig. 7. Mathematical model and detailed switch model comparison result.

Applying the Laplace transformation to (1), the voltage gain transfer function can be derived as

$$\begin{aligned} G(s) &= \frac{u_{\mathrm{LV}}}{u_{\mathrm{SM}} - 2u_{\mathrm{igbt}} - 2nu_{\mathrm{diode}}} \\ &= \frac{2nR}{s^2 RL_{\mathrm{e}}C_{\mathrm{LV}} + s\left(RR_{\mathrm{e}}C_{\mathrm{LV}} + L_{\mathrm{e}}\right) + 2n^2R + R_{\mathrm{e}}}. \end{aligned} \tag{2}$$

In order to verify the accuracy of the developed mathematical model, the detailed switching circuit is built in PLECS for step disturbance comparison. As shown in Fig. 7, the high degree of similarity between the two step responses in the shape confirms the validity of the developed mathematical model.

The second-order standard transfer function can be obtained from (2)

$$G(s) = \frac{\omega_{\mathrm{n}}^2}{s^2 + 2\omega_{\mathrm{n}}\zeta s + \omega_{\mathrm{n}}^2} \times \frac{2nR}{2n^2R + R_{\mathrm{e}}} \tag{3}$$

where

$$\omega_{\mathrm{n}} = \sqrt{\frac{\left(2n^2R + R_{\mathrm{e}}\right)}{RL_{\mathrm{e}}C_{\mathrm{LV}}}}, \zeta = \frac{\left(RR_{\mathrm{e}}C_{\mathrm{LV}} + L_{\mathrm{e}}\right)}{\sqrt{4RL_{\mathrm{e}}C_{\mathrm{LV}}\left(2n^2R + R_{\mathrm{e}}\right)}} \tag{4}$$

According to (2) and (3), the step response steady-state solution of the switched-capacitor circuit can be obtained as

$$u_{\mathrm{LV}} = \frac{2nR}{2n^2R + R_{\mathrm{e}}}\left(u_{\mathrm{SM}} - 2u_{\mathrm{igbt}} - 2nu_{\mathrm{diode}}\right). \tag{5}$$

From (5), it can be seen that R_{e} has an influence on the voltage clamping characteristic of the switched-capacitor circuit. If the distribution resistance is zero ideally, the voltage relationship between the SM capacitor and LVdc port is only related to the transformer ratio and switches voltage drop, that is, $u_{\mathrm{LV}} = (u_{\mathrm{SM}}\text{-}2u_{\mathrm{igbt}}\text{-}2nu_{\mathrm{diode}})/n$. Then the voltage control error ε_{v} can be defined as

$$\varepsilon_{\mathrm{v}} = \frac{u_{\mathrm{LV\_ide}} - u_{\mathrm{LV\_act}}}{u_{\mathrm{LV\_ide}}} = 1 - \frac{2n^2R}{2n^2R + R_e} \tag{6}$$

where $u_{\mathrm{LV\text{-}ide}}$ and $u_{\mathrm{LV\text{-}act}}$ are the ideal value and actual value, respectively. The change trend of voltage control error with distribution resistance and load resistance can be drawn from (6). As shown in Fig. 8, the distribution resistance has a more serious impact on the voltage control error with the load resistance decreased. When the distribution resistance is the largest and the load resistance is the smallest, the output voltage disturbance reaches the maximum value. So, the distribution resistance should be constrained reasonably to avoid large control errors in rated conditions.

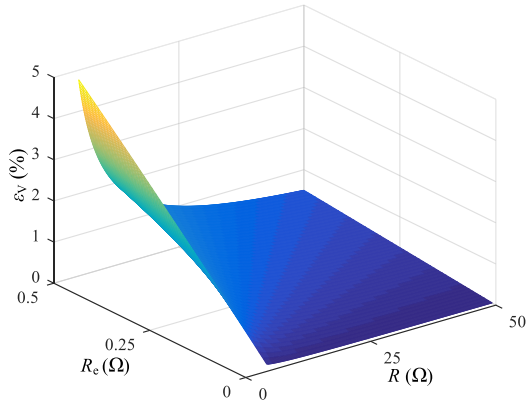


Fig. 8. Influence factors analysis of voltage clamping.

C. *Impact of* L_e/R_e *Defined Transformer Time Constant on Active Power Transfer Ratio*

During synchronous control operation of switched-capacitor circuit, the leakage inductance of synchronous transformers could cause a delay in the current response, resulting in the current phase is opposite to the square wave voltage phase, during which the forward transmitted power is negative and the power is returned to the input side, which can be defined as the backflow power [19]. In order to avoid the backflow power affecting the conversion efficiency, it is necessary to make a reasonable constraint on the leakage inductance.

The transformer current is symmetrical about the time axis during the switching cycle from Fig. 3. When the switches S_1/S_4 are turned ON and the switches S_2/S_3 are turned OFF, the loop description can be obtained according to Kirchhoff's voltage law

$$u_{\text{pri}} - nu_{\text{sec}} = R_{\text{e}} i_{\text{T}}(t) + L_{\text{e}} \frac{di_{\text{T}}(t)}{dt}. \tag{7}$$

The initial condition is

$$i_{\text{T}}(0) = -\frac{(u_{\text{pri}} - nu_{\text{sec}})}{R_{\text{e}}}. \tag{8}$$

Then the transformer current time-domain expression could be obtained from (7) and (8)

$$i_{\text{T}}(t) = \frac{(u_{\text{pri}} - nu_{\text{sec}})}{R_{\text{e}}} \cdot \left(1 - 2e^{-\frac{R_{\text{e}}}{L_{\text{e}}}t}\right). \tag{9}$$

According to (9), the transformer current is divided into the transient period and steady-state period in a half-switching cycle. The transient process is attenuated exponentially, and the attenuation time constant is L_e/R_e. In steady-state period, the leakage inductance is close to saturation, and only the distribution resistance consumes energy. The current zero crossing point can be obtained from (9)

$$t_{\text{c}} = \frac{kT}{2} + \frac{L_{\text{e}} \cdot \ln 2}{R_{\text{e}}} \, (k = 0, 1, 2 \ldots). \tag{10}$$

By combining (9) and (10), the average backflow power within a half-switching cycle can be obtained

$$\begin{aligned} P_{\text{bf}} &= \frac{2}{T} \int_0^{\frac{L_{\text{e}} \ln 2}{R_{\text{e}}}} i_{\text{T}}(t) u_{\text{pri}} dt \\ &= \frac{2u_{\text{pri}}^2 L_{\text{e}} - 2nu_{\text{sec}} u_{\text{pri}} L_{\text{e}}}{TR_{\text{e}}^2} (\ln 2 - 1). \end{aligned} \tag{11}$$

When L_e/R_e is larger, the backflow time is longer due to the attenuation speed being slower per half cycle, as the red current shown in Fig. 3. If the output power is stable, the power transmitted by synchronous transformer during the switching cycle is greater, then the transformer current peak will be larger, which would increase the loss of power devices and magnetic components and reduce the switched-capacitor conversion efficiency.

According to (9), the actual power transmitted by the switched-capacitor circuit in a half cycle is

$$\begin{aligned} P_{\text{act}} &= \frac{2}{T} \int_0^{\frac{T}{2}} i_{\text{T}}(t) u_{\text{pri}} dt \\ &= \frac{2u_{\text{pri}}^2 - 2nu_{\text{sec}} u_{\text{pri}}}{TR_{\text{e}}} \cdot \left[\frac{T}{2} - \frac{L_{\text{e}}}{R_e}\left(2 - 2e^{-\frac{R_{\text{e}} T}{L_{\text{e}} 2}}\right)\right]. \end{aligned} \tag{12}$$

If the leakage inductance is ignored, the ideal power transmitted in a half cycle can be defined as

$$P_{\text{ide}} = \frac{2}{T} \int_0^{\frac{T}{2}} i_{\text{T}} u_{\text{pri}} dt = \frac{u_{\text{pri}}^2 - nu_{\text{sec}} u_{\text{pri}}}{R_{\text{e}}}. \tag{13}$$

According to (12) and (13), the active power transfer ratio ε_{p} can be obtained

$$\varepsilon_{\text{p}} = \frac{P_{\text{act}}}{P_{\text{ide}}} = 1 - 2f \frac{L_{\text{e}}}{R_e}\left(2 - 2e^{-\frac{R_{\text{e}}}{2L_{\text{e}} f}}\right). \tag{14}$$

The changing trend of active power transfer ratio with distribution resistance, leakage inductance, and time constant can be drawn from (14), as shown in Fig. 9.

From Fig. 9(a), it can be seen that the active transfer ratio is not the optimal solution even though the leakage inductance is the minimum, which is also related to the distribution resistance. When the leakage inductance decreases while the distribution resistance increases, the active power transfer ratio gradually increases and reaches the peak point. In fact, the time constant is the most key factor affecting the active power transmission. Fig. 9(b) shows that the active power transfer ratio decreases gradually with increasing the time constant.

Besides the active power transferred to the LVdc port, the low-frequency ripple power also presents the same tendency. If the ripple current flow path to the HFac bus is restricted by the distribution parameters [9], the SM capacitor voltage ripples will increase due to the parallel structure. Furthermore, the arm circulating currents related to the SM capacitor voltage ripples cannot be eliminated completely [20]. Therefore, the large time constant could also weaken the low-frequency voltage ripple decoupling and circulating current natural elimination characteristics of the switched-capacitor-based MMC-SST.

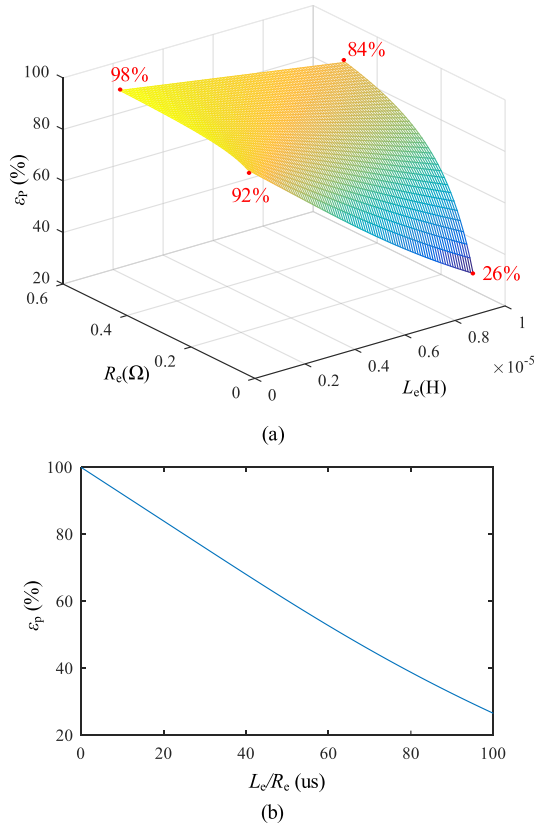


Fig. 9. Influence factors analysis of power transfer. (a) Active power transfer ratio versus distribution parameters. (b) Active power transfer ratio versus time constant.

In order to better control SM capacitor voltage ripples and circulating currents, and also to improve the switching capacitor conversion efficiency, it is necessary to reduce the time constant, that is, reduce the leakage inductance and coordinate the distribution resistance.

D. Impact of Transformer Distribution Parameters on Inrush Current

During steady state operation, the SM capacitor voltages are clamped with each other due to the switched-capacitor characteristic. There is little energy difference and inrush current between SM capacitors. But there are voltage differences between capacitors at the start-up moment due to the inconsistency of distribution parameters, which would introduce inrush currents. The inrush current analysis is crucial to evaluate the dynamic security of the switched-capacitor-based MMC-SST. When there is a voltage imbalance between SM capacitors or a voltage mismatch between the SM capacitors and the LVdc port, the switched-capacitor circuit will act quickly to force the voltage to balance or match. The corresponding charging circuits are shown in Fig. 10.

It is assumed that the transformer ratio n is 1, the loop expressions can be written respectively from Fig. 10

$$\begin{cases} \Delta V_1 = 2R_{\mathrm{e}} i_{\mathrm{T1}}(t) + 2L_{\mathrm{e}} \frac{di_{\mathrm{T1}}(t)}{dt} \\ \Delta V_2 = R_{\mathrm{e}} i_{\mathrm{T2}}(t) + L_{\mathrm{e}} \frac{di_{\mathrm{T2}}(t)}{dt} \end{cases} \tag{15}$$

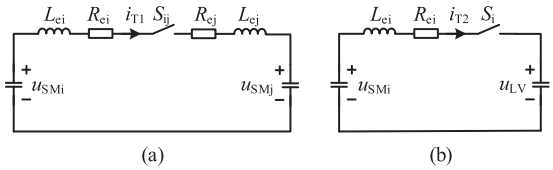


Fig. 10. Equivalent charging circuits of switched-capacitor. (a) Between SM capacitors. (b) Between the SM capacitor and the LVdc port.

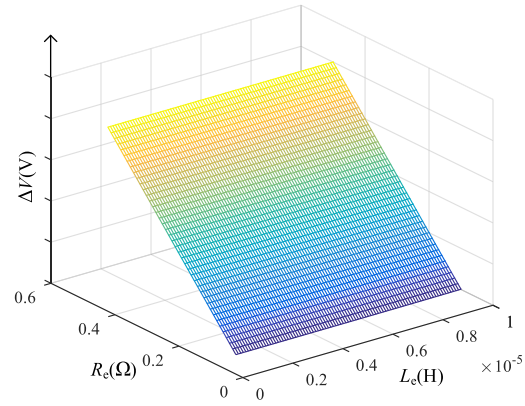


Fig. 11. Influence factors analysis of voltage deviation.

where ΔV_1 is the voltage deviation between SM capacitors, ΔV_2 is the voltage deviation between SM capacitor and LVdc port. i_{T1} and i_{T1} are the charging inrush currents, respectively. The inrush current peak can be solved from (15)

$$\begin{cases} i_{\mathrm{T1\_max}} = \frac{\Delta V_1}{2R_{\mathrm{e}}} \left(1 - \mathrm{e}^{-\frac{R_{\mathrm{e}}}{L_{\mathrm{e}} f}}\right) \\ i_{\mathrm{T2\_max}} = \frac{\Delta V_2}{R_{\mathrm{e}}} \left(1 - \mathrm{e}^{-\frac{R_{\mathrm{e}}}{L_{\mathrm{e}} f}}\right) \end{cases} . \tag{16}$$

In order to prevent the inrush current from damaging the switching devices and affecting the SST normal operation, it is necessary to ensure that the current peak does not exceed the rated collector current of the switching device, that is

$$\begin{cases} i_{\mathrm{T1\_max}} + i_{\mathrm{T}} \le I_{\mathrm{c1max}} \\ 6N_{\mathrm{SM}} \left(i_{\mathrm{T2\_max}} + i_{\mathrm{T}}\right) \le N_{\mathrm{FB}} I_{\mathrm{c2max}} \end{cases} \tag{17}$$

where N_{SM} is the number of arm SMs, N_{FB} is the number of FBs on LVdc side, I_{c1max} and I_{c2max} represent the IGBT-rated collector currents of primary side FB and secondary side FB.

According to (16) and (17), the voltage deviation should be met

$$\begin{cases} \Delta V_1 \le 2R_{\mathrm{e}} \left(I_{\mathrm{c1max}} - i_{\mathrm{T}}\right) \Big/ \left(1 - \mathrm{e}^{-\frac{R_{\mathrm{e}}}{L_{\mathrm{e}} f}}\right) \\ \Delta V_2 \le R_{\mathrm{e}} \left(\frac{N_{\mathrm{FB}} I_{\mathrm{c2max}}}{6N_{\mathrm{SM}}} - i_{\mathrm{T}}\right) \Big/ \left(1 - \mathrm{e}^{-\frac{R_{\mathrm{e}}}{L_{\mathrm{e}} f}}\right) \end{cases} . \tag{18}$$

The changing trend between voltage deviation and distribution parameters can be drawn from (18), as shown in Fig. 11. It can be seen that the leakage inductance has little effect on voltage deviation, but the distribution resistance has a great influence on the voltage deviation. With the distributed resistance increased, the allowable voltage deviation level could be improved due to the inrush current can be well suppressed according to (16)–(18).

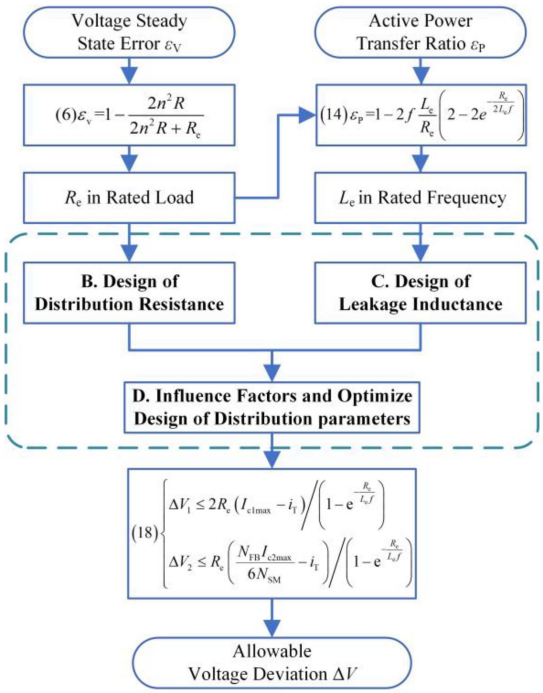


Fig. 12. Optimization design criteria for distribution parameters.

III. Optimized Design of Synchronous Transformers

A. Optimization Criteria for Distribution Parameters

According to the above analysis, there are some contradictions in distribution parameters optimization. The distribution resistance is supposed to be small from the point of voltage clamping. Besides, it is also expected to decrease the distribution resistance to reduce the power loss. However, the distribution resistance could be utilized to improve the active power transfer ratio and constrain inrush current caused by voltage mismatch. So a compromise distribution parameters optimization design criteria should be given, as shown in Fig. 12.

First, the allowable voltage steady-state error ε_v and the expected active power transfer ratio ε_p should be defined by the designer, then the maximum distribution resistance could be solved according to (6), which should meet the voltage steady-state error in rated operating conditions. After that, the appropriate leakage inductance could be found by substituting the distribution resistance and active transfer ratio into (14), then the distribution parameters can be used to guide synchronous transformer design, which will be introduced in the next sections. Finally, the maximum allowed voltage deviation can be deduced from (18) and the measured distribution parameters. The synchronous transformer design parameters are shown in Table I.

B. Distribution Resistance Evaluation and Winding Loss Analysis Calculation

The winding loss of synchronous transformer is affected by the transformer current and the winding ac resistance simultaneously, when the transformer current contains a wealth of harmonics, the total loss is equal to the sum of the winding loss caused by each harmonic, as shown in (19)

TABLE I
The Electrical Parameters of Synchronous Transformer

Parameters	Value
Power rating/ S	50kVA
Primary voltage/ u_{pri}	800V
Secondary voltage/ u_{sec}	800V
RMS current/ i_T	62.5A
Working frequency/ f	5kHz
Voltage steady-state error/ ε_v	1.5%
Active power transfer ratio/ ε_p	90%

$$P_w = \sum_{k=1}^{max} (i_{T\_k})^2 R_{ac}^k \tag{19}$$

where i_{T_k} is the RMS value of the k_{th} harmonic current and $R_{ac}{}^k$ is the k_{th} winding ac resistance.

The ac resistances of Litz wire can be calculated according to the Dowell model [21]

$$R_{ac}^k = R_{dc} \times F_k \tag{20}$$

where

$$\begin{cases} R_{dc} = \rho\frac{L}{S} \\ F_k = \sqrt{\eta}\Delta\left[\frac{\sinh 2\Delta + \sin 2\Delta}{\cosh 2\Delta - \cos 2\Delta} + \frac{2}{3}\left(z^2 - 1\right) \times \frac{\sinh\Delta - \sin\Delta}{\cosh\Delta + \cos\Delta}\right] \\ \Delta = \frac{d_{eq}}{\delta} \\ d_{eq} = d\sqrt{\frac{\pi}{4}} \\ \sqrt{\eta} = \frac{d}{p} \end{cases} \tag{21}$$

where R_{dc} is the dc resistance of Litz wire, ρ is the conductor resistivity, L is the conductor length, S is the conductor cross-sectional area, F_k is the ac/dc resistance ratio for the k_{th} harmonic, which is affected by the skin effect and proximity effect. Δ is the equivalent penetration rate, z is the number of continuous winding layers, δ is the skin depth, d is the Litz wire diameter, η is the porosity factor, and p is the distance of two adjacent conductor centers. When the main harmonic frequency is close to the sideband harmonic frequency, the ac/dc resistance ratio can be approximately equal [22].

According to [9], the input current of switched-capacitor circuit can be obtained as

$$i_{FB} = \underbrace{\frac{i_{LVdc}}{6nN_{SM}}}_{DC} + \underbrace{\left(\frac{I_{Mx}}{4} - \frac{mi_{MVdc}}{6}\right)\sin\omega t}_{FundamentalFrequencyAC} + \underbrace{\frac{mI_{Mx}}{8}\cos 2\omega t}_{DoubleFrequencyAC} \tag{22}$$

where i_{LVdc} is the current of LVdc port, i_{MVdc} is the current of medium voltage dc port, I_{Mx} (x = a, b, c) is the current amplitude of medium voltage ac port, ω is the fundamental angular frequency, m is the voltage modulation ratio. Substituting (22) into Appendix (A3) and (A12), the transformer current can be expressed as (23) shown at the bottom of the next page, where ω_c is the switching angular frequency of FB.

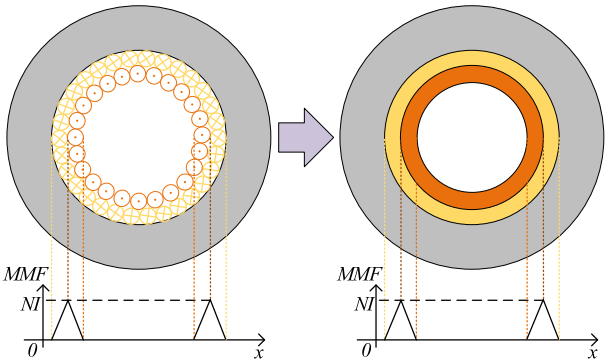


Fig. 13. Copper foil winding equivalent structure diagram.

C. Leakage Inductance Evaluation of Toroidal Transformer Considering Frequency Characteristic

During high-frequency magnetic conversion, the leakage flux existed in the insulation layers and windings, which stores energy but does not interact with other windings. This effect can be quantitatively described as leakage inductance. It is calculated as

$$L_{\mathrm{e}}=\frac{2W_{\mathrm{s}}}{I^2}=\frac{2}{I^2}\int_V\frac{H\cdot B}{2}dV=\frac{\mu_0}{I^2}\int_V|H|^2dV \tag{24}$$

where W_{s} is the leakage magnetic field energy, I is the current excitation, μ_0 is the vacuum permeability, H is the magnetic field strength, B is the magnetic induction intensity, V is the volume of the transformer. It can be seen that the leakage inductance is closely related to the magnetic field strength. When applying Ampere's circuital law to calculate the magnetic field strength inside the windings and insulation layers, the following basic assumptions need to be made [23].

1) The winding with the round cross-sectional wires is replaced by an equivalent copper foil structure, as shown in Fig. 13. Where N is the number of turns and MMF is the magnetic motive force.
2) Magnetizing current is eliminated. This ensures that the leakage field in the winding would be parallel to the core as well as complete compensation of ampere-turns is achieved.

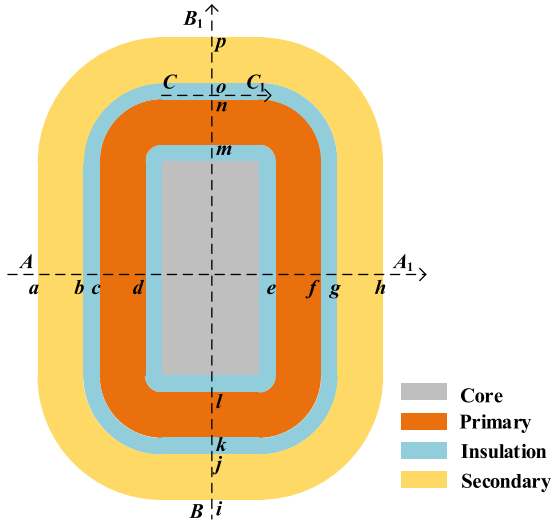


Fig. 14. 2D axisymmetric cross-sectional view of the toroidal core.

The axisymmetric cross-sectional view of the toroidal transformer is shown in Fig. 14, it contains the magnetic core, primary winding, insulation layers, and secondary winding.

The magnetic field strength distribution in Fig. 14 with different frequencies during a short-circuit test can be obtained.

The following conclusions can be summarized from Fig. 15.

1) In low-frequency conditions, the magnetic field strength of transversal to the windings rises linearly in one winding and decays linearly in the opposite winding. But in high-frequency conditions, the magnetic field strength of transversal to the windings shows a hyperbolic sinusoidal characteristic [24]. (AA_1 and BB_1).
2) The magnetic field strength distribution at the top and bottom is same (BB_1), and the magnetic field strength of the insulation layer is approximately proportional inversely to the radius (CC_1).

Then the toroidal transformer leakage inductance calculation could be divided into five regions: inner vertical region, outer vertical region, horizontal regions, inner rounded regions, and outer rounded regions, as shown in Fig. 16. According to the partitions, the total leakage inductance of the toroidal transformer can be obtained as

$$L_{\mathrm{e}}=L_{\mathrm{e1}}+L_{\mathrm{e2}}+2L_{\mathrm{e3}}+2L_{\mathrm{e4}}+2L_{\mathrm{e5}} \tag{25}$$

$$\begin{aligned} i_{\mathrm{T\_k}}(t)=&\underbrace{\frac{2i_{\mathrm{LVdc}}}{3n\pi N_{\mathrm{SM}}}\sum\nolimits_{k=1}^{\infty}\frac{\sin(2k-1)\omega_c t}{2k-1}}_{\text{Main Harmonic Currents}}\\ &+\underbrace{\frac{\sum_{k=1}^{\infty}\left(\frac{I_{\mathrm{Mx}}}{2(2k-1)\pi}-\frac{mi_{\mathrm{MVdc}}}{3(2k-1)\pi}\right)\sin\frac{(2k-1)\pi}{2}}{\sin\left[(2k-1)\omega_{\mathrm{c}}\pm\omega\right]t}}_{\text{Fundamental Frequency Sideband Harmonic Currents}}\\ &+\underbrace{\sum\nolimits_{k=1}^{\infty}\frac{mI_{\mathrm{Mx}}}{(2k-1)4\pi}\sin\frac{(2k-1)\pi}{2}\sin\left[(2k-1)\omega_{\mathrm{c}}\pm2\omega\right]t+\frac{\pi}{2}\Big)}_{\text{Double Frequency Sideband Harmonic Currents}} \end{aligned} \tag{23}$$

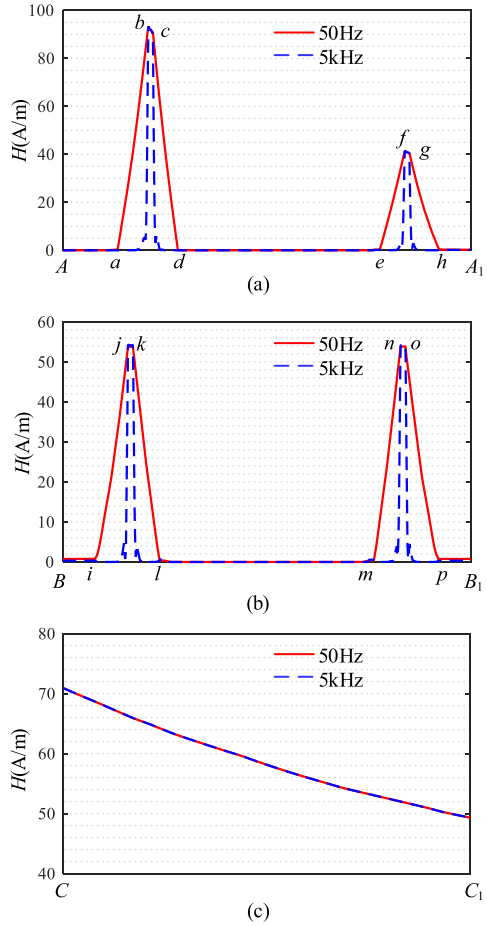


Fig. 15. Distribution of the magnetic-field strength in the toroidal transformer. (a) Radial distribution of the magnetic field on the vertical sections. (b) Magnetic-field strength on the horizontal sections. (c) Radial variation of the field at the insulation of the horizontal parts.

where L_{ei} (i is 1, 2, 3, 4, 5) indicates the leakage inductance corresponding to the i region, and each region can be divided into three major sections: primary winding, secondary winding, and insulation layers.

1) Vertical Regions: According to Ampere's circuit law, it can be found that the magnetic field strength at the insulation layers on the inner vertical region and outer vertical region are, respectively,

$$\begin{cases} H_b = \frac{NI}{2\pi R_2} \\ H_{bc}(x) = \frac{NI}{2\pi(R_2+x)} \\ H_c = \frac{NI}{2\pi R_3} \end{cases} \quad \begin{cases} H_f = \frac{NI}{2\pi R_6} \\ H_{fg}(x) = \frac{NI}{2\pi(R_6+x)} \\ H_g = \frac{NI}{2\pi R_7} \end{cases} . \tag{26}$$

According to [25], the magnetic field strength in the primary winding and the secondary winding under high frequency conditions can be solved

$$\begin{cases} H_{ab}(x) = \frac{H_b \sinh(\gamma x)}{\sinh(\gamma a)} \\ H_{cd}(x) = \frac{H_c \sinh[\gamma(b-x)]}{\sinh(\gamma b)} \\ H_{ef}(x) = \frac{H_f \sinh(\gamma x)}{\sinh(\gamma b)} \\ H_{gh}(x) = \frac{H_g \sinh[\gamma(a-x)]}{\sinh(\gamma a)} \end{cases} \tag{27}$$

where γ is the characteristic root of Helmholtz equation.

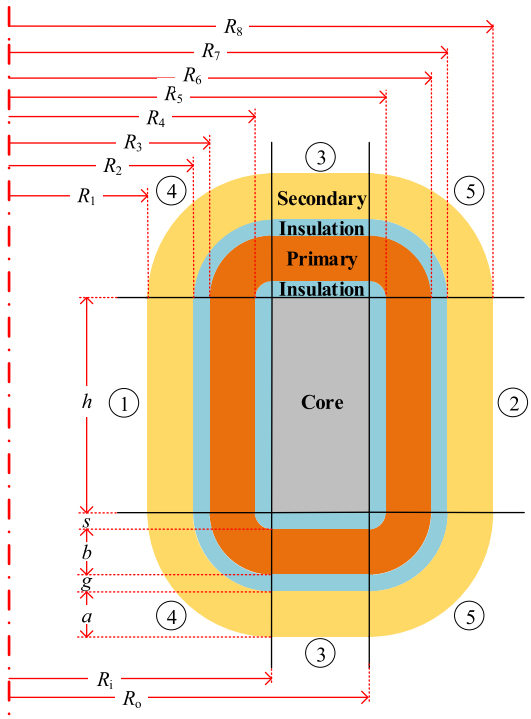


Fig. 16. Main geometric data of toroidal transformer.

Substituting (26) and (27) into (24), the inner vertical and outer vertical leakage inductances can be obtained

$$\begin{cases} L_{e1} = \frac{2\pi\mu_0 h}{I^2}[R_{m1}\int_0^a |H_{ab}(x)|^2 dx + R_{m2}\int_0^g |H_{bc}(x)|^2 dx \\ \quad + R_{m3}\int_0^b |H_{cd}(x)|^2 dx] \\ \quad = \frac{N^2\mu_0 h}{2\pi}\left[\left(\frac{R_{m1}}{R_2^2}\right) f(a) + \frac{gR_{m2}}{R_2 R_3} + \left(\frac{R_{m3}}{R_3^2}\right) f(b)\right] \\ L_{e2} = \frac{2\pi\mu_0 h}{I^2}[R_{m5}\int_0^b |H_{ef}(x)|^2 dx + R_{m6}\int_0^g |H_{fg}(x)|^2 dx \\ \quad + R_{m7}\int_0^a |H_{gh}(x)|^2 dx] \\ \quad = \frac{N^2\mu_0 h}{2\pi}\left[\left(\frac{R_{m5}}{R_6^2}\right) f(b) + \frac{gR_{m6}}{R_6 R_7} + \left(\frac{R_{m7}}{R_7^2}\right) f(a)\right] \end{cases} \tag{28}$$

where

$$\begin{cases} f(x) = \frac{\sinh(2\gamma x)-2\gamma x}{4\gamma \sinh^2(\gamma x)} \\ R_{m,j} = \frac{(R_j+R_{j+1})}{2} \end{cases} \tag{29}$$

where h is the core height, R_{m1}, R_{m2}, R_{m3}, R_{m5}, R_{m6}, and R_{m7} are the average radius of the primary winding, insulation layer, and secondary winding.

2) Horizontal Regions: Since the top and bottom horizontal regions have the same magnetic field distribution, as shown in Fig. 15(b), the magnetic field strength in the top region can be solved as an example. According to Ampere's circuit law, the magnetic field strength of the insulation layer is computed as follows:

$$H_{jk}(x) = \frac{NI}{2\pi x}. \tag{30}$$

Similarly, the magnetic field strength of windings can be solved

$$\begin{cases} H_{ij}(xy) = \frac{H_{jk}(x)\sinh(\gamma y)}{\sinh(\gamma a)} \\ H_{kl}(xy) = \frac{H_{jk}(x)\sinh[\gamma(b-y)]}{\sinh(\gamma b)} \end{cases}. \tag{31}$$

Substituting (30) and (31) into (24), the leakage inductance of the top horizontal region is obtained

$$\begin{aligned} L_{e3} &= \frac{2\pi\mu_0 R_{mh}}{I^2}\Big[\int_{R_i}^{R_o}\int_0^a |H_{ij}(xy)|^2 dydx \\ &\quad + \int_{R_i}^{R_o}\int_0^g |H_{jk}(x)|^2 dydx + \int_{R_i}^{R_o}\int_0^b |H_{mn}(xy)|^2 dydx\Big] \\ &= \frac{N^2\mu_0}{2\pi}\left(\frac{R_{mh}R_o - R_{mh}R_i}{R_i R_o}\right)[f(a) + g + f(b)] \end{aligned} \tag{32}$$

where

$$R_{mh} = \frac{(R_i + R_o)}{2} \tag{33}$$

where R_{mh} is the average radius of core.

3) Rounded Regions: The leakage calculation of the rounded regions can be converted to the polar coordinate system from the Cartesian coordinate system, which can be performed by integrating around the periphery denoted by φ (from 0 to $\pi/2$), (34) shown at the bottom of this page
where

$$\begin{cases} F(x) = \frac{\gamma x\sinh(2\gamma x) - \sin h^2(\gamma x) - \gamma^2 x^2}{4\gamma^2\sinh^2(\gamma x)} \\ F_1(x) = \frac{\sin h^2(\gamma x) - \gamma^2 x^2}{4\gamma^2\sinh^2(\gamma x)} \end{cases}. \tag{35}$$

In order to investigate the accuracy of the proposed calculation method, which considers the frequency variation characteristics, a finite element analysis (FEA) covering a wide range of frequencies has been performed, as shown in Fig. 17. The classical calculation method for toroidal transformers mentioned in [26] has also been compared. It can be seen that the classical calculation method produces a large error with the frequency increased, while the proposed method keeps high consistency with the FEA result in all frequency ranges. Therefore, the proposed method has great significance for the leakage inductance refined design of high-frequency toroidal transformers.

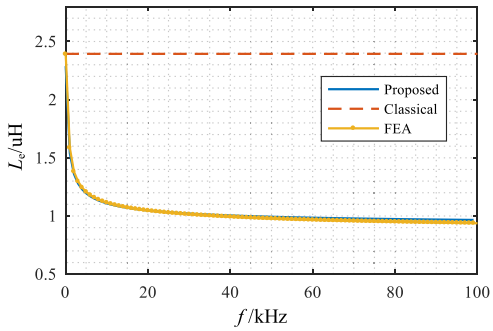


Fig. 17. Comparison results of different calculation methods.

D. Influence Factors and Optimization Design of Distributed Parameters

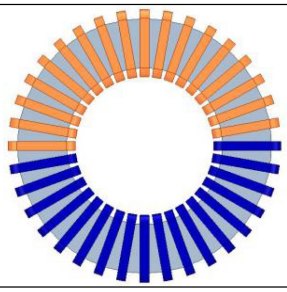
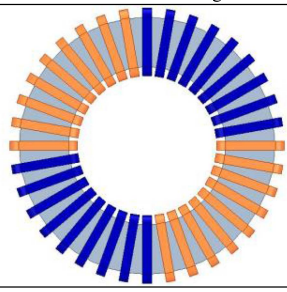
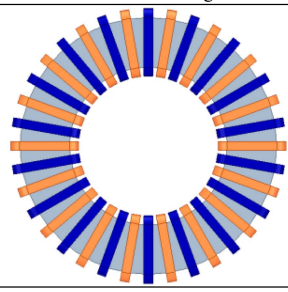
i) The distribution resistance R_e of the synchronous transformer is related to the conductor length L, cross-sectional area S, and ac/dc resistance ratio F_k according to (20) and (21). But the ac/dc resistance ratio is close to 1 under the designed working frequency and the minimum cross-sectional area is limited by physical conditions. So the number of turns N and the mean length per turn MLT are the dominant factors to adjust distributed resistance. The distribution resistance is directly related to the winding loss, which then affects the temperature rise of the synchronous transformer. Therefore, the temperature should be considered as a constraint condition to limit excessive distribution resistance.

ii) The leakage inductance L_e of the synchronous transformer is related to the number of turns N, insulation thickness g, core and winding dimensions according to (28), (32), and (34). Since the core and winding dimensions are decided by AP value and current density, the turn number N is coupling with resistance, so the insulation thickness g is the adjustable factor of leakage inductance. However, the minimum insulation thickness should be guaranteed to avoid insulation breakdown. Therefore, dielectric strength should be considered as another constraint condition to limit insulation thickness.

iii) The leakage inductance simulation tests are carried out for three different winding types, which are full discrete type, partial interleaving type, and full interleaving type, respectively, as shown in Table II. The full discrete structure means that the primary and secondary windings are wound on both sides of the core, the partial interleaving

$$\begin{cases} L_{e4} = \frac{2\pi\mu_0}{I^2}\left\{\int_0^{\pi/2}\left[\, R_{m1}\int_0^a |H_{ab}(x)|^2 xdx + R_{m2}\int_0^g |H_{bc}(x)|^2 xdx \right.\right. \\ \qquad \left.\left. + R_{m3}\int_0^b |H_{cd}(x)|^2 xdx\right] d\varphi\right\} \\ \qquad = \frac{N^2\mu_0}{4}\left[\left(\frac{R_{m1}}{R_2^2}\right)F(a) + R_{m2}\left(\ln\frac{R_3}{R_2} - \frac{g}{R_3}\right) + \left(\frac{R_{m3}}{R_3^2}\right)F_1(b)\right] \\ L_{e5} = \frac{2\pi\mu_0}{I^2}\left\{\int_0^{\pi/2}\left[\, R_{m5}\int_0^b |H_{ef}(x)|^2 xdx + R_{m6}\int_0^g |H_{fg}(x)|^2 xdx \right.\right. \\ \qquad \left.\left. + R_{m7}\int_0^a |H_{gh}(x)|^2 xdx\right] d\varphi\right\} \\ \qquad = \frac{N^2\mu_0}{4}\left[\left(\frac{R_{m5}}{R_6^2}\right)F(b) + R_{m6}\left(\ln\frac{R_7}{R_6} - \frac{g}{R_7}\right) + \left(\frac{R_{m7}}{R_7^2}\right)F_1(a)\right] \end{cases} \tag{34}$$

TABLE II
COMPARISON RESULTS OF DIFFERENT WINDING STRUCTURES

	Full Discrete	Partial Interleaving	Full Interleaving
Turns ratio 10:10 Frequency 5kHz			
Magnetizing Inductance	15.8mH	15.8mH	15.8mH
Leakage Inductance	48.6uH	27.9uH	3.2uH

structure indicates that the windings are symmetrically separated and each occupies 1/4 of the core, while the primary and secondary windings are cross-wound, and the full interleaving structure indicates that each turn of the secondary winding is close to the primary winding. According to the simulation results, three winding structures have the same magnetizing inductance, while the leakage inductance of the full discrete type is the largest, which has reached 48.6 uH, and the full interleaving type is only 3.2 uH. It can be concluded that the leakage inductance can be decreased by increasing the coupling degree between the primary and secondary windings.

In the synchronous transformers design procedure, distribution parameters R_e and L_e are considered as the optimization targets, thermal and insulation are considered as the constraints, the winding structure, turns, and insulation distance are considered as the optimizable parameters. According to the design requirements, the transformer optimization design flow suitable for switching capacitor-based MMC-SST can be obtained, as shown in Fig. 18. First, the system-level parameters such as rated capacity, primary secondary voltage current, and operating frequency should be entered. Then the AP design method is used to select the core, the Litz wire and insulation material are determined according to the current density and insulation level. Importantly, the winding structures, turn numbers, and insulation distances are regulated constantly until the distribution parameters meet the design requirements. During parameter selection, thermal and insulation should be evaluated based on Appendix (A13)–(A19) to ensure safe operation. Finally, the switched-capacitor conversion efficiency should also be tested.

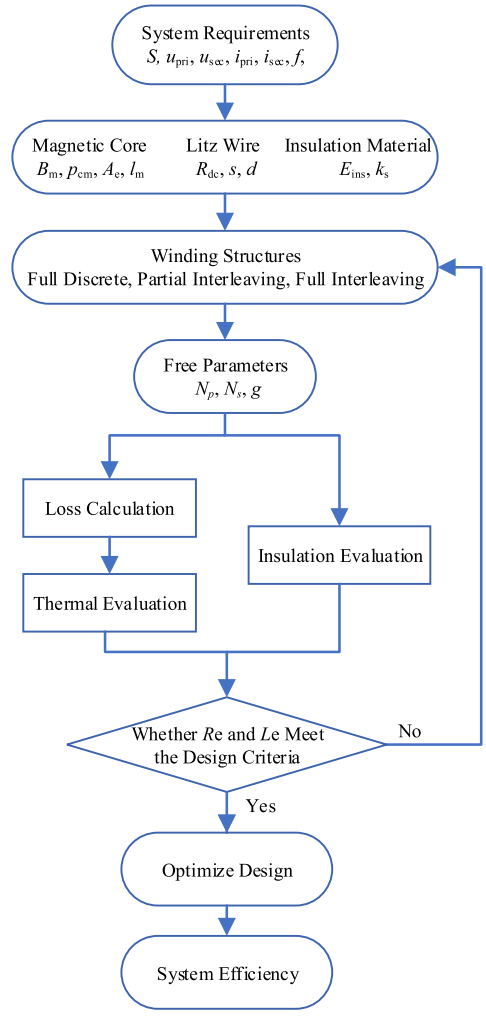


Fig. 18. Optimization design flow chart of synchronous transformers.

IV. DESIGN EXAMPLES AND PERFORMANCE TESTS

A. Prototype of Synchronous Transformer

According to the optimization design process in Fig. 18, the optimized design parameters can be obtained as shown in Table III. In order to better verify the effectiveness of the proposed design scheme, the traditional toroidal transformer is also designed based on [29], which only considers the basic transformer design constraints and the distribution parameter constraints are ignored. In the optimized design scheme, the full interleaving winding structure is selected to reduce leakage inductance, and the distribution resistance is slightly increased to improve the active power transfer ratio and reduce the inrush current. The synchronous transformer prototypes are shown in Fig. 19

TABLE III
OPTIMIZE DESIGN TRANSFORMER PARAMETERS

Type	Specification	
Scheme name	Proposed Design	Traditional Design
Core material	Nanocrystalline	
Core structure	Toroidal	
Core size	ID 85 mm/ OD 150mm/ H 40mm	
Turn insulation	Polyimide Film 0.1mm	
Core number	3	2
Core insulation	Nomex Paper 1mm	Nylon 2mm
Litz wire	0.1mm*1200*2	0.1mm*2200
Turn ratio	18:18	26:26
Equivalent resistance	106mΩ	84mΩ
Leakage inductance	1.95uH	5.2uH

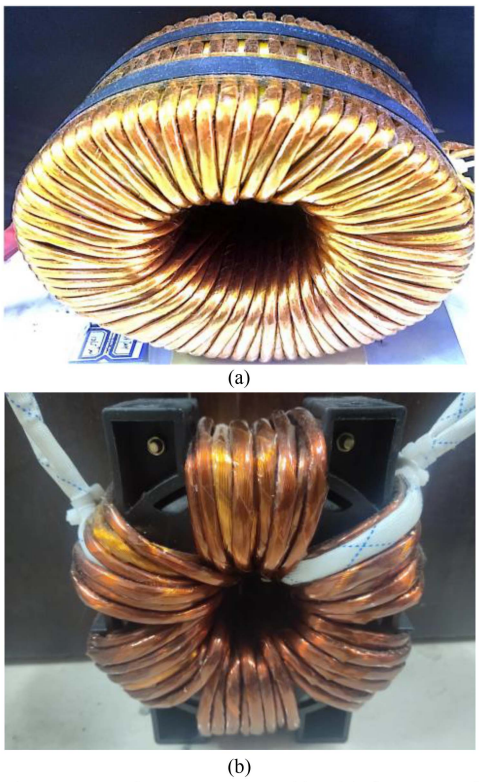


Fig. 19. Synchronous transformer prototype. (a) With the proposed design. (b) With the traditional design.

B. Performance Verification of Synchronous Transformer

In order to verify the effectiveness of the transformer design strategy, a high-power three-phase switched-capacitor test platform is built based on the parameters of Table IV. As shown in Fig. 20, the IGBT half-bridge module of Infineon FF100R12RT4 is selected as the primary FB and SM switches, and the IGBT half-bridge modules of Infineon FF300R12KE4 are selected as the secondary FB switches. The SMs and inductors are used to generate symmetrical ripple currents for verifying the fluctuating power transfer ability of the synchronous transformer.

TABLE IV
SWITCHED-CAPACITOR TEST PLATFORM PARAMETERS

Description	Values
Rated capacity/ S_N	3*50kVA
SM input voltage/ u_{IN}	500V
SM capacitor voltage/ u_{SM}	800V
LVdc voltage/ u_{LV}	800V
SM switching frequency/ f_{SM}	2kHz
FB switching frequency/ f_{FB}	5kHz

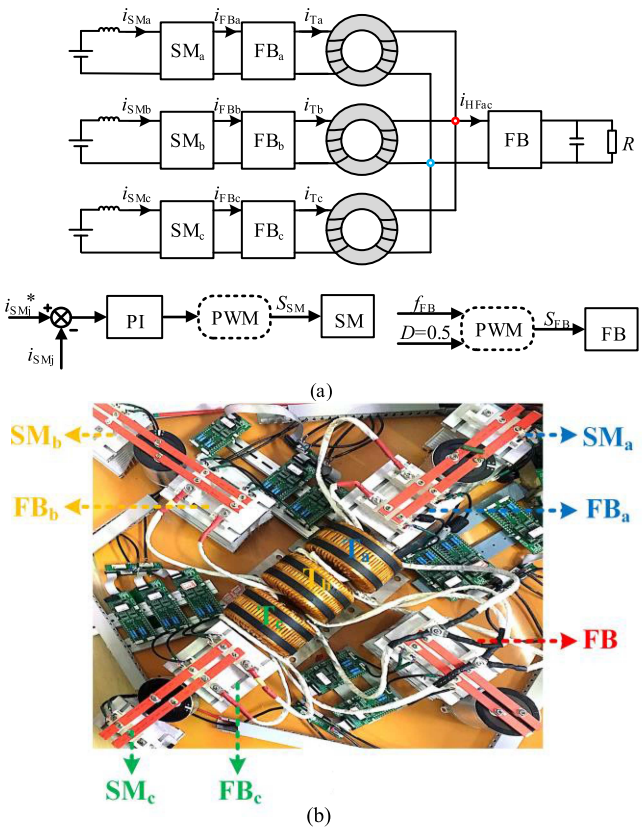


Fig. 20. Switched-capacitor circuit experiment platform. (a) Equivalent structure diagram. (b) Prototype.

Fig. 21 shows the steady-state operating waveforms under rated conditions. There is no phase difference between the primary and secondary transformer voltage in switched-capacitor conversion. From the transformer current in a half switching cycle, it can be seen that the steady state period is the dominating part in the proposed design transformer, whereas the transient period is in the traditional design due to the large time constant configuration. The active power transfer ratio of the proposed design transformer is 93%, which results in massive suppression of backflow power. Meanwhile, the steady-state voltage error is 1.5%, which is consistent with the theoretical analysis. Although the steady-state voltage error is 1.3% based on the traditional design scheme, the active power transfer ratio is only 78%, and the power transfer process is inhibited severely, which is inefficient for switched-capacitor conversion.

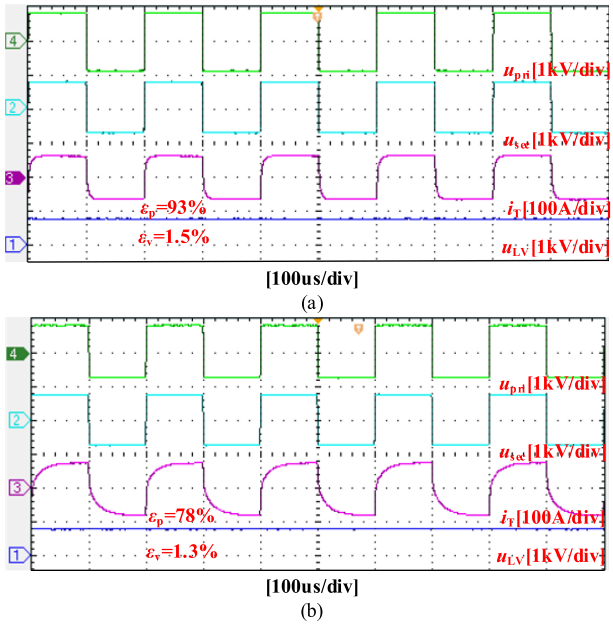


Fig. 21. Switched-capacitor circuit steady-state operating waveforms. (a) With the proposed design transformer. (b) With the traditional design transformer.

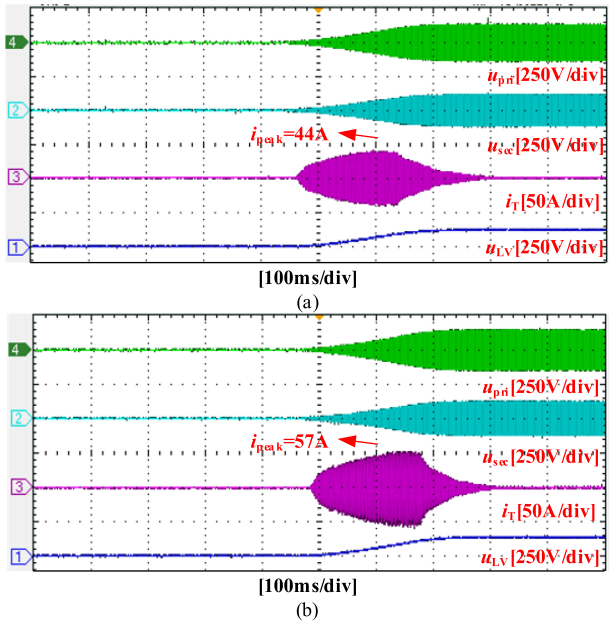


Fig. 22. Switched-capacitor circuit dynamic state operating waveforms. (a) With the proposed design transformer. (b) With the traditional design transformer.

Fig. 22 shows the dynamic state operating waveforms under the voltage mismatch condition. It is worth noting that the capacitors of switched-capacitor circuit should be pre-charged to the rated voltage before operation. And the voltage mismatch condition only occurs at the voltage disturbance moment. In this test, the no-load charging moment is used to observe the suppression of distribution resistance on the inrush current. It can be seen the charging inrush current peak is suppressed from 57 to 44 A due to the larger distribution resistance in the proposed design scheme, which can help to increase the allowable voltage

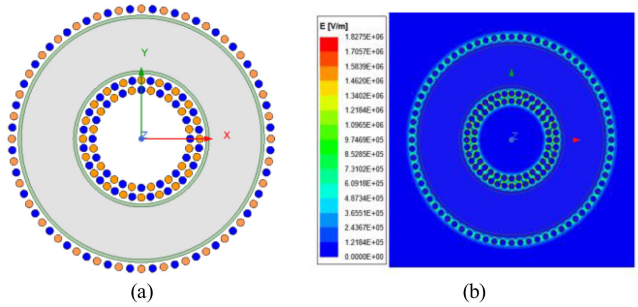


Fig. 23. FEM simulation results of the electric field in the transformer. (a) Simulation model. (b) Electric field intensity distribution.

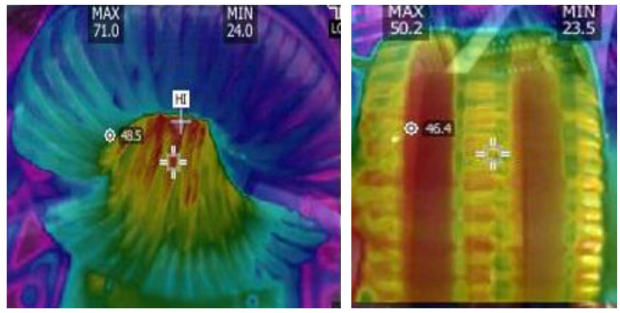


Fig. 24. Transformer temperature rise observation results. (a) Inside surface. (b) Outside surface.

deviation range with the same capacity switch devices. The dynamic security of the switched-capacitor-based MMC-SST could also be improved.

Fig. 23 shows the finite element method (FEM) simulation results of the electric field in the transformer. The windings are constituted by the full interleaving structure, as shown in Fig. 23(a). A long-term high-frequency voltage of 1.6 kV is used to evaluate core and turn insulation. It can be seen that the maximum electric field strength is within the range of the selected insulation materials that can withstand. During the experiment, there is no discharge phenomenon and leakage current on the surface of the transformer.

Fig. 24 shows the working temperature of the transformer under rated operating conditions. Since the effective heat exchange area of the inner surface is smaller than the outer surface, the inner layer is hotter. Although the distribution resistance is slightly increased compared with the traditional scheme, the highest temperature rise is well limited to the scope of 80 °C, as shown in Fig. 24.

Fig. 25 shows the steady-state operating waveform with ripple currents input. It can be seen that the primary high-frequency currents of the synchronous transformer present three-phase symmetrical characteristics, and the high-frequency sideband harmonic currents can be canceled on the secondary side, which verifies that the synchronous transformer optimization design could meet the fluctuating power coupling requirement in the switched-capacitor-based MMC-SST.

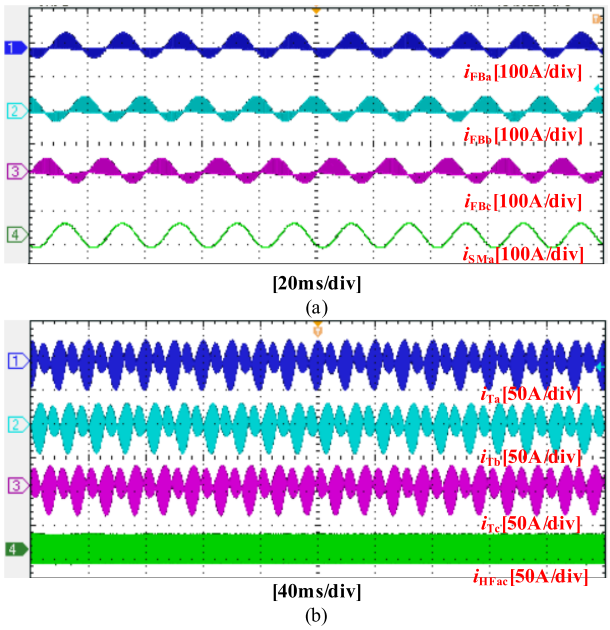


Fig. 25. Switched-capacitor circuit operating waveforms with ripple input. (a) Input currents of SM and FBs. (b) Synchronous transformer and HFac currents.

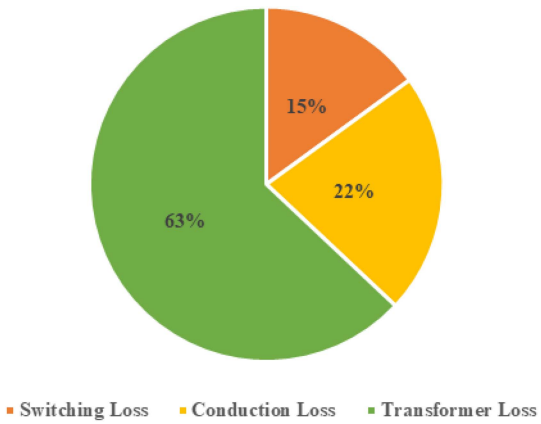


Fig. 26. Loss distribution diagram.

C. Loss Distribution and Efficiency Testing of Switched-Capacitor Circuit

In addition to the synchronous transformer loss, switching device loss is also an important factor affecting conversion efficiency, which can be calculated according to Appendix (A20) and (A21). Then the switched-capacitor circuit loss distribution can be obtained based on the theoretical calculation, as shown in Fig. 26. It can be seen that the transformer loss accounts for 63% of the converter total loss, the switching loss and conduction loss are 15% and 22% respectively.

Fig. 27 shows the operating efficiency curve of the switched-capacitor circuit under different operating conditions, which is fitted by the experimental results. It can be seen that the converter could keep high operating efficiency in the normal working range.

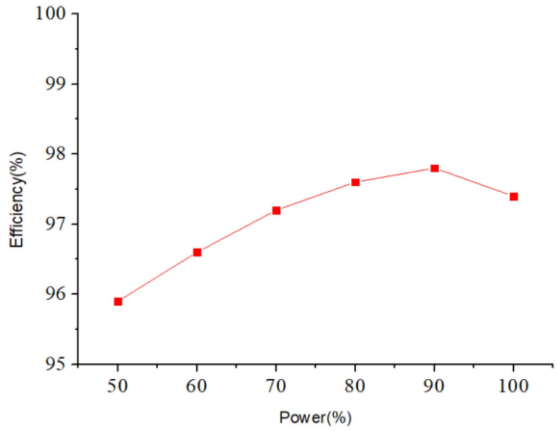


Fig. 27. Operating efficiency curve.

V. Conclusion

This article makes further research about the influences of distribution parameters on the switched-capacitor working performance. The distribution resistances can be utilized to improve the active power transmission ratio and broaden the allowable voltage deviation range, but also bring the steady-state error to voltage clamping control. The leakage inductance could cause the active power backflow, thus reducing the active power transfer ratio. Considering the voltage control error, active power transfer ratio, and inrush current suppression requirements, the compromise design criterion for the distribution parameters is obtained.

A synchronous transformer optimization design scheme that fits for the switched-capacitor conversion-based MMC-SST is also proposed. The turn numbers, insulation distance, and winding arrangements are the main influence factors to optimize distribution parameters. The Dowell model is used to evaluate the distribution resistance. The frequency-dependent leakage inductance expression of the toroidal transformer is derived according to the magnetic field energy method. The optimized synchronous transformer has good abilities for active power transfer and inrush current suppression, while the voltage control error is within a reasonable range.

Appendix

The synchronous transformer winding loss is closely related to the harmonic currents generated by the high-frequency modulation process. These high-frequency harmonic currents can be solved as follows.

A. When the Input Current of Switched-Capacitor Converter is DC

The transformer current can be expressed as

$$f(t) = \begin{cases} i_{\mathrm{dc}}, (0 < t \le T/2) \\ -i_{\mathrm{dc}}, (T/2 < t \le T) \end{cases} \tag{A1}$$

where i_{dc} represents the current amplitude, T represents the switching period. According to the Fourier Transform formula,

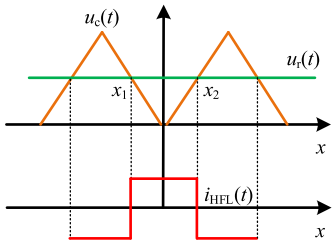


Fig. 28. Modulation process diagram.

the coefficients are

$$A_0 = \frac{1}{T}\int_0^T f(t)\,\mathrm{d}t = 0$$

$$a_k = \frac{2}{T}\int_0^T f(t)\cos(k\omega_c t)\,\mathrm{d}t = 0$$

$$b_k = \frac{2}{T}\int_0^T f(t)\sin(k\omega_c t)\,\mathrm{d}t = \begin{cases} \frac{4i_{dc}}{k\pi} & k = \text{odd} \\ 0 & k = \text{even} \end{cases} \tag{A2}$$

The transformer current in the frequency domain can be expressed as

$$f(t) = \frac{4i_{dc}}{\pi}\sum_{k=1}^{\infty}\frac{\sin(2k-1)\omega_c t}{2k-1} \tag{A3}$$

where ω_c is the switching angular frequency and k is the harmonic order. According to (A3), it can be seen that the dc input current is converted into switching frequency times and switching frequency odd times harmonic current through the high-frequency chopper.

B. When the Input Current of Switched-Capacitor Converter is AC

In this situation, the transformer current is affected by the input current frequency and switching frequency simultaneously. The modulation process of the switching capacitor circuit is shown in Fig. 28.

According to Fig. 28, the modulation signal $u_r(t)$ and carrier signal $u_c(t)$ can be defined respectively

$$u_r(t) = 0.5$$

$$u_c(t) = \begin{cases} \frac{x}{\pi}, x \in [0,\pi] \\ -\frac{x}{\pi}, x \in [-\pi,0] \end{cases}$$

$$x = \omega_c t \tag{A4}$$

where ω_c is the carrier angular frequency. The action time of switches in a carrier cycle can be obtained from (A4)

$$\begin{aligned} x_1 &= \pi/2, t \in [0,\pi] \\ x_2 &= -\pi/2, t \in [-\pi,0]. \end{aligned} \tag{A5}$$

The input current can be defined

$$\begin{cases} i_{ac} = A\sin y \\ y = \omega_0 t \end{cases} \tag{A6}$$

where A is the current amplitude, ω_0 is the current angular frequency. Then, the transformer current can be expressed as

$$f(t) = \begin{cases} i_{ac}, (x_2 < x \le x_1) \\ -i_{ac}, (-\pi < x \le x_2 || x_1 < x \le \pi) \end{cases}. \tag{A7}$$

According to the Double Fourier Transform formula, the coefficients can be deduced

Condition I: $m = 0$, $n = 0$

$$A_{00} + jB_{00} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(t)\,dxdy = 0. \tag{A8}$$

Condition II: $m = 0$, $n>0$

$$A_{0n} + jB_{0n} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(t)\,e^{jny}dxdy = 0. \tag{A9}$$

Condition III: $m>0$, $n = 0$

$$A_{m0} + jB_{m0} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(t)\,e^{jmx}dxdy = 0. \tag{A10}$$

Condition IV: $m>0$, $n\neq 0$

$$\begin{aligned} A_{mn} + jB_{mn} &= \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(t)\,e^{j(mx+ny)}dxdy \\ &= \begin{cases} j\frac{2A}{m\pi}\sin\frac{m\pi}{2} & m = \text{odd} \\ 0 & m = \text{even} \end{cases} \end{aligned} \tag{A11}$$

Then, the transformer current in the frequency domain can be expressed as

$$\begin{aligned} f(t) = &\sum_{m=1}^{\infty}\frac{2A}{(2m-1)\pi}\sin \\ &\times\frac{(2m-1)\pi}{2}\sin\left[(2m-1)\omega_c \pm \omega_0\right]t \end{aligned} \tag{A12}$$

where m is the carrier harmonic orders and n is the number input current harmonic orders. It can be seen that the ac input current is converted into switching frequency times and switching frequency odd times sideband harmonic current through the high-frequency chopper.

C. Core Loss Assessment

The core loss is calculated by the improved generalized Steinmetz equation (IGSE) in this article, which considers the rate of change of magnetic induction and the magnetization period, with a high calculation accuracy. The unit core loss can be expressed as [27]

$$P_c = \frac{1}{T}\int_0^T k_i\left|\frac{dB(t)}{dt}\right|^{\alpha}|\Delta B|^{\beta-\alpha}dt \tag{A13}$$

where

$$k_i = \frac{K}{(2\pi)^{\alpha-1}\int_0^{2\pi}|\cos\theta|^{\alpha}2^{\beta-\alpha}d\theta} \tag{A14}$$

where $\triangle B$ is the peak-to-peak of the magnetic induction, K, α, β are the SE coefficients. The magnetic induction waveform induced by 0.5 duty cycle voltage excitation is shown in Fig. 29.

In the case of Fig. 29, (A13) can be further expressed as

$$P_c = 2^{\alpha+\beta}k_i \cdot f^{\alpha}B_m^{\beta}. \tag{A15}$$

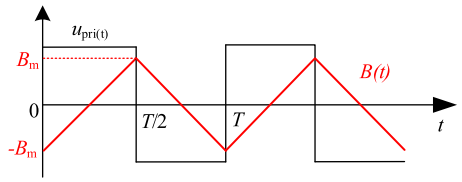


Fig. 29. Excitation voltage and magnetic induction waveform.

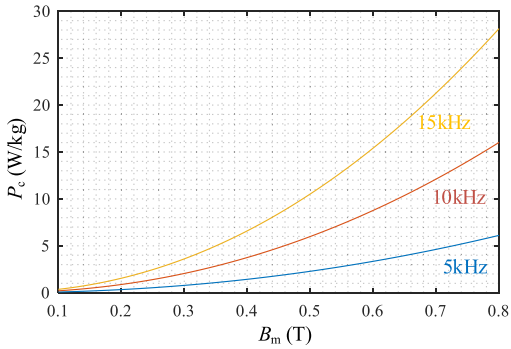


Fig. 30. Unit core loss curves at different frequencies.

When the coefficient α is at (03], (A14) could be equivalent to [28]

$$k_i = \frac{K}{2^{\beta+1}\pi^{\alpha-1}\left(0.2761 + \frac{1.7061}{\alpha+1.354}\right)}. \tag{A16}$$

According to the B_m-P_c values provided by the core manufacturer, the B_m-P_c curves under sinusoidal excitation with different frequencies could be fitted in the curve-fitting toolbox. Then the SE coefficients (K, α, β) can be obtained by quadratic linear regression from the sinusoidal excitation B_m-P_c curves and original SE. Finally, the unit core loss curves under square wave excitation with different frequencies could be obtained from (A15) and (A16), as shown in Fig. 30.

D. Insulation Distance and Temperature Calculation

Dry insulation is more suitable for the high power density system than oil-immersed insulation. According to [17], the required insulation level can be translated into the minimum distance between the insulating conductors, which is calculated as

$$g = \frac{V_{ins}}{k_s E_{ins}} \tag{A17}$$

where V_{ins} is the voltage level that needs to be insulated, E_{ins} is the electric field intensity of the insulating material, and k_s is the safety margin factor.

The synchronous transformer will be heated continuously during operation, resulting in a temperature increase, which would change the core electromagnetic parameters, damage the insulation materials, and affect the normal operation of dc–dc converter. It is necessary to strictly control the transformer temperature in a reasonable range, and the temperature rise can be approximated calculated as [29]

$$T_t = 450\left(\frac{P_t}{A_t}\right)^{0.826} \tag{A18}$$

where

$$A_t = K_{st}(A_e A_w)^{0.5} \tag{A19}$$

where P_t is the transformer total loss including core loss and winding loss. A_t is the transformer surface area, A_e is the transformer effective cross-sectional area, A_w is the transformer window area, K_{st} is the coefficient related to the core structure.

E. Loss Calculation of Switching Devices

The switching device loss can be divided into conduction loss and switching loss [30], [31]. The conduction loss is calculated as

$$\begin{cases} P_{CL,I} = v_{CE0} \cdot i_{AVG,I} + r_{ON} \cdot (i_{RMS,I})^2 \\ P_{CL,D} = v_{F0} \cdot i_{AVG,D} + r_{ON} \cdot (i_{RMS,D})^2 \end{cases} \tag{A20}$$

where v_{CE0} and v_{F0} are the threshold voltage drops of IGBTs and diodes, r_{ON} is slope resistance, $i_{AVG,\,X}$ and $i_{RMS,\,X}$ (X is I or D) represent the average currents and RMS currents flowing through the IGBTs and diodes.

The switching loss calculation can be expressed as

$$\begin{cases} P_{SW,I} = f_s \cdot i_{AVG,I} \cdot \frac{E_{on}(I_N)+E_{off}(I_N)}{I_N} \cdot \frac{V_{DC}}{V_B} \\ P_{SW,D} = f_s \cdot i_{AVG,D} \cdot \frac{E_{rec}(I_N)}{I_N} \cdot \frac{V_{DC}}{V_B} \end{cases} \tag{A21}$$

where f_s is the switching frequency, I_N is the rated current, E_{on}, E_{off}, and E_{rec} represent the switching energy, which is available from the IGBT data sheet, V_{DC} is the dc voltage used to measure the switching energy, and V_B is the blocking voltage.

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