Low-Cost and Compact Asymmetrical Unidirectional-Current Modular Multilevel Converters

Zhengxuan Li, *Graduate Student Member, IEEE*, Bojin Tang, Qiang Song, *Senior Member, IEEE*, Lifeng Gou, Biao Zhao, *Senior Member, IEEE*, Na Jia, and Fang Cai

***Abstract*—Although the modular multilevel converters (MMCs) that contain submodules (SMs) with negative voltage capability have various advantages, they usually demand many more semiconductors than the conventional half-bridge SM-based MMC (HB-MMC). This study proposes a unidirectional-current clamp-double submodule (UC-CDSM) by combining two unidirectional-current full-bridge SMs (UC-FBSMs) using a shared switching device. The sharing design enables the UC-CDSM-based MMC (UC-CD-MMC) to have 25% fewer switching devices compared with the UC-FBSM-based MMC. The quantity of switching devices is rather similar to that in a conventional HB-MMC while the UC-CD-MMC still retains the advantages, such as low capacitor usage, dc fault clearing capability, and wide-range dc voltage adjustability. Moreover, a unidirectional-current hybrid MMC composed of UC-CDSMs and UC-FBSMs (UC-HYB-MMC) is presented to further enlarge the adjustable range of dc voltage. Detailed comparisons indicate that the UC-CD- and UC-HYB-MMCs can reduce the valve costs by 32% and 25%, respectively, and volumes by 39% and 34%, respectively, compared with HB-MMCs. Simulation and experimental results verify the steady-state and dc-fault clearance of the proposed topologies, and that the capacitor voltages in the UC-FBSMs and UC-CDSMs are well maintained and balanced in the UC-HYB-MMC.**

***Index Terms*—Compactness, dc voltage adjustability, modular multilevel converter (MMC), submodule (SM) topology.**

I. Introduction

MODULAR multilevel converter (MMC) has become the most competitive solution to the voltage source converter-based high-voltage direct current (VSC-HVdc) transmission systems. The half-bridge submodule (HBSM), which can output zero and positive voltage levels, is the most widely used submodule (SM) to compose an MMC [1]. However, the development of VSC-HVdc also brings many new challenges to MMCs, such as how to reduce the converters' cost and volume [2], clear dc fault currents [3], [4], and adjust the dc voltage in a wide range [5], [6], [7], which are difficult to be implemented by a conventional HBSM-based MMC (HB-MMC).

Compared with HBSM, full-bridge submodule (FBSM) can output an additional negative voltage level [3]. The FBSM-based MMC (FB-MMC) and the hybrid MMC (HYB-MMC) composed of HBSMs and FBSMs were initially proposed to block the dc fault current. Further studies have noticed that the negative voltage states of FBSMs enable the FB-MMCs or HYB-MMCs to output adjustable dc voltages without affecting the ac voltage capability, which is highly important in some applications, such as active dc fault clearing [4], online converter switch-in and -out [5], and series multiterminal dc [6], [7], [8]. For example, the active dc fault clearing and online converter switch-in and -out have been implemented in the Kunliulong ultra-high voltage multiterminal dc project using HYB-MMCs [5].

Existing studies have reported that the negative voltage states of FBSMs can help to increase the modulation index, thereby significantly suppressing energy fluctuations in the converter arms and reducing the capacitor usage in MMCs [9], [10]. For instance, the dominant fundamental-frequency energy fluctuation can be significantly suppressed if the modulation index reaches a certain high value, such as 1.414 at unity power factor [9], [10], [11]. This is extremely essential to reduce the volume and cost of the valves, given that the SM capacitors require high capacitance to suppress the voltage ripples caused by arm energy fluctuations and may occupy more than 50% of the valves' volume [12], [13] and entail more than 30% of the cost.

Despite the various advantages brought by the negative voltage states of FBSMs, an FBSM utilizes twice the quantity of switching devices as an HBSM, inevitably bringing negative effects on the cost and volume. Although the capacitor usage can be reduced greatly by increasing the modulation index to an appropriate value, the extra semiconductors and SMs cancel the reduction effects on the valve cost and volume brought by the reduced capacitor usage [10]. Several variant topologies, such as five-level SMs [14], [15] and semi-FBSMs [16], [17], were proposed to reduce the quantity of switching devices while retaining the negative voltage state capabilities. However, the

Manuscript received 23 May 2022; revised 17 October 2022; accepted 25 November 2022. Date of publication 8 December 2022; date of current version 26 December 2022. This work was supported in part by the National Key R&D Program of China under Grant 2022YFB2405300 and in part by the National Natural Science Foundation of China under Grant 51977119. Recommended for publication by Associate Editor F. Dijkhuizen. *(Corresponding author: Qiang Song.)*

Zhengxuan Li, Qiang Song, Biao Zhao, and Fang Cai are with the Department of Electrical Engineering, Tsinghua University, Beijing 100084, China (e-mail: zx-li18@mails.tsinghua.edu.cn; songqiang@tsinghua.edu.cn; zhao-biao@tsinghua.edu.cn; caif22@tsinghua.org.cn).

Bojin Tang, Lifeng Gou, and Na Jia are with the China Three Gorges Corporation, Beijing 100036, China (e-mail: tang_bojin@ctg.com.cn; gou_lifeng@ctg.com.cn; jia_na@ctg.com.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3225861.

Digital Object Identifier 10.1109/TPEL.2022.3225861

MMCs based on these SM topologies still demand excessive additional switching devices in practice compared with the HB-MMC.

Considering that many converters transmit active power unidirectionally, such as renewable energy integration and hybrid HVdc using line commuted converters and MMCs, a unidirectional-current FBSM (UC-FBSM)-based MMC (UC-FB-MMC) was proposed to reduce the quantity of required switching devices while retaining the advantages of FB-MMC [18], [19]. The UC-FB-MMC can act as a unidirectional interface between the dc systems and the generations or loads. The basic idea of the UC-FB-MMC is that the arm currents are kept unidirectional by increasing the ac voltage to decrease the ac current, thereby removing two switching devices from each FBSM because the unidirectional arm currents never flow through them [19], [20]. However, the quantities of required SMs and semiconductors in a UC-FB-MMC are still approximately 40% more than those in a conventional HB-MMC to attain the increased ac voltage [19], limiting the reduction effects on the cost and volume.

The UC-FB-MMC inherits the advantages of FB-MMC, including dc fault clearing capability, low capacitor usage, and dc voltage adjustability, whose dc voltage can vary ranging from the positive to negative rated values. In fact, in many applications, the dc voltage range is not necessarily that wide, that is, the lower limit of the adjustable range is not necessarily to reach the negative rated value [4], [6], [7], [20], [21]. In these cases, the requirement for the negative voltage capability of the converter arms can be lower than the positive one. On this basis, this study proposes a new asymmetrical unidirectional-current clamp double submodule (UC-CDSM) by combining two UC-FBSMs using a shared switching device. The UC-CDSM-based MMC (UC-CD-MMC) can significantly reduce the quantities of SMs and semiconductors while still having the advantages, including dc fault clearing capability, low capacitor usage, and dc voltage adjustability. Furthermore, a hybrid MMC topology composed of the proposed UC-CDSM and the UC-FBSM (UC-HYB-MMC) is presented to extend the dc voltage range. The UC-HYB-MMC inherits the advantages of UC-CD-MMC and extends the dc voltage range by increasing its hybrid rate. In addition, a universal sorting and capacitor voltage balancing algorithm for UC-CD- and UC-HYB-MMCs is proposed. The UC-CD- and UC-HYB-MMCs are evaluated, which allows for quantitative comparisons of the valve costs and volumes between the existing and proposed MMC topologies and summarizes their advantages. Simulation and experimental results verify the feasibility of the proposed MMC topologies and control methods.

II. UC-CDSM AND UC-CD-MMC

A. Derivation of the Topology of UC-CDSM

Fig. 1 shows the topology of MMC. The arm currents must be unidirectional for implementing the UC-CDSMs. The essential means to create unidirectional arm currents is to increase the ac voltage. As shown in Fig. 2(a), the fundamental frequency components of the arm current can be reduced by increasing

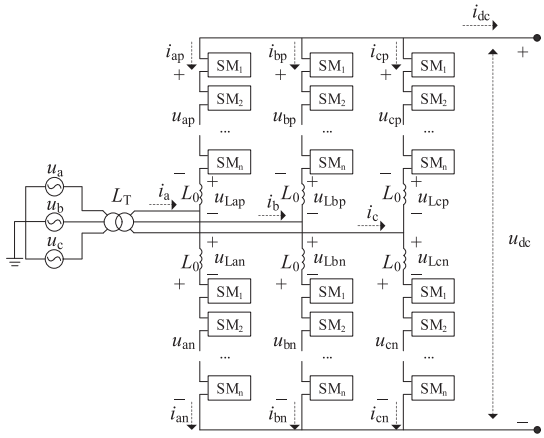


Fig. 1. Topology of MMC.

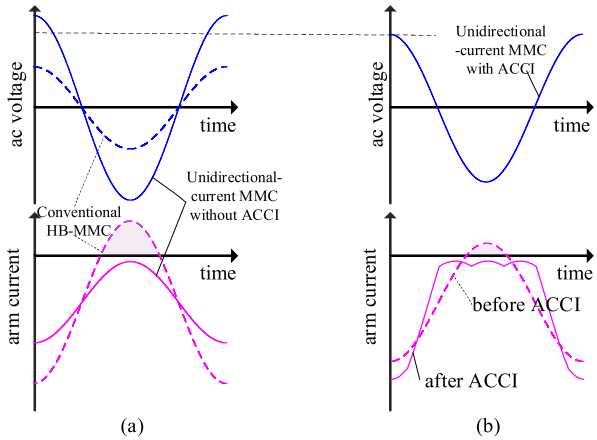


Fig. 2. Basic principle of creating unidirectional arm currents. (a) Unidirectional arm currents by only increasing the ac voltage. (b) Unidirectional arm currents by both increasing the ac voltage and ACCI, but the ac voltage is not increased so high as that in (a).

the ac voltage to a certain value. Thus, the dc component offset forces the arm currents to be unidirectional. However, the ac voltage must increase to such a high value that the minimum modulation index becomes higher than 2.0, which is not acceptable in practice [19]. As shown in Fig. 2(b), an active circulating current injection (ACCI) can be used to help the arm current be unidirectional, and thereby, the ac voltage requirement is reduced by 1/3 at most compared with that in Fig. 2(a) [19]. Furthermore, given that the ac voltage is reduced, the quantities of the SMs and semiconductors in the MMCs also decrease, thereby lowering the total power losses [19]. On the premise of unidirectional am current, two switching devices and two diodes can be eliminated from an FBSM because the unidirectional arm current never flows through them, thereby creating a unidirectional-current variant named as UC-FBSM [19]. Fig. 3(a) shows two UC-FBSMs connected in series.

The UC-FBSM is a simplified variant of FBSM and can save half the quantity of semiconductors compared with FBSM [18], [19]. Similar to FB-MMC, the UC-FBSM-based MMC (UC-FB-MMC) still retains the advantages, such as low capacitor usage, dc fault clearing capability, and wide-range dc voltage

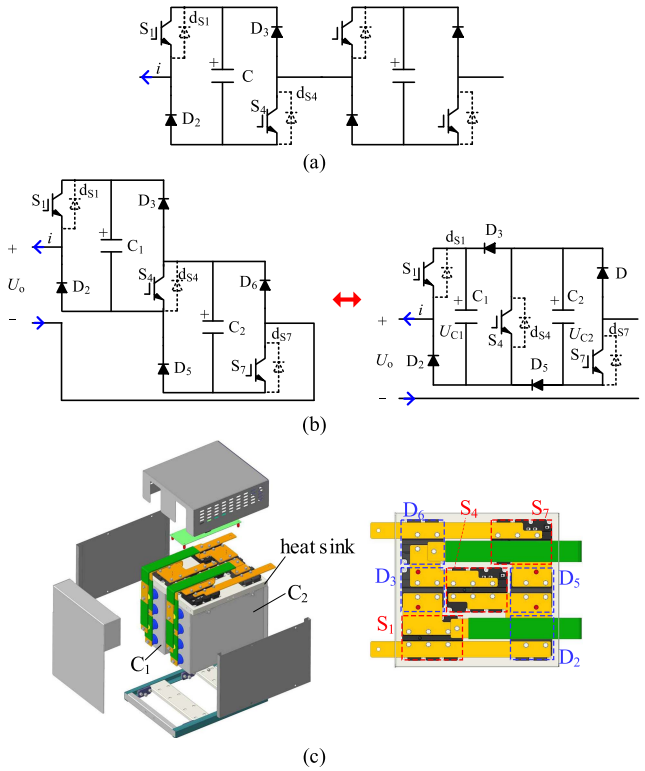


Fig. 3. (a) Two UC-FBSM. (b) Combination of two UC-FBSMs using a shared switching device (intuitive demonstration and rearrangement of semiconductors). (c) Structural design example of UC-CDSM.

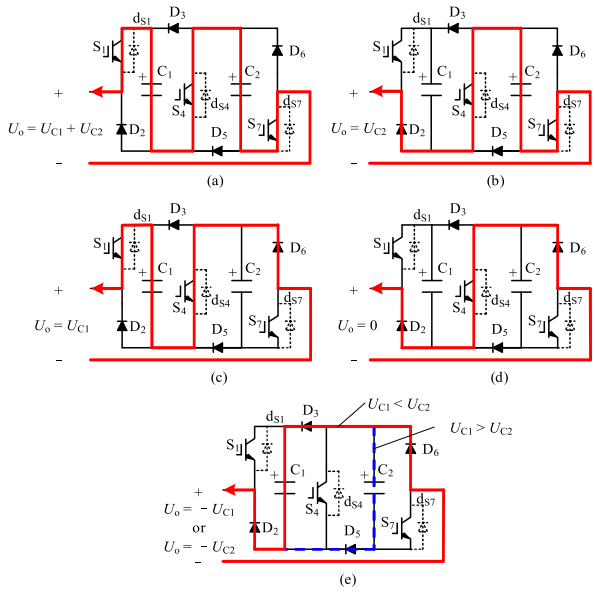


Fig. 4. Switch states, current paths, and output voltages of UC-CDSM. (a) $(S_1, S_4, S_7) = (1, 1, 1)$. (b) $(S_1, S_4, S_7) = (0, 1, 1)$. (c) $(S_1, S_4, S_7) = (1, 1, 0)$. (d) $(S_1, S_4, S_7) = (0, 1, 0)$. (e) $(S_1, S_4, S_7) = (0, 0, 0)$.

adjustability [22]. However, the UC-FB-MMC still requires approximately 40% more SMs and switching devices to attain the high ac voltage for unidirectional arm currents compared with a conventional HB-MMC [19]. Although the semiconductor usage, indicated by the total capacity of switching devices and diodes, is similar to that of HB-MMC because the UC-FB-MMC has decreased arm currents [19], the increased quantities of SMs and semiconductors still bring cost and volume problems.

To reduce the quantity of SMs and save the semiconductor usage while retaining the advantages of MMCs that utilize the negative states of SMs, this study proposes to combine two UC-FBSMs using a shared switching device and creates a new asymmetrical SM topology, as illustrated in Fig. 3(b). Evidently, the sharing design can reduce the quantity of switching devices by 25%. Inherently, this SM topology can also be understood as the unidirectional-current variant of the clamp double submodule (CDSM) reported in [3], which was originally proposed to block the fault current. Therefore, in this article, this SM topology is named as unidirectional-current CDSM (UC-CDSM). As illustrated in Fig. 3(b), a UC-CDSM mainly consists of three switching devices S_1, S_4, and S_7 and four independent diodes D_2, D_3, D_5, and D_6. The antiparallel diodes d_{S1}, d_{S4}, and d_{S7} are only used to provide current paths for precharging the capacitors from the ac side during start-up stages, and no current flows through them in normal operations. Therefore, if they are separately installed, the diodes with much lower current ratings can be selected. Given their necessity only if the MMC is charged from the ac side, the diodes are plotted with dotted lines.

Fig. 3(c) presents a structural design example of the UC-CDSM using the modular IGBTs and diodes, indicating the feasibility of the integration for the UC-CDSM.

Fig. 4 shows the switch states, current paths, and output voltages of the UC-CDSM. When the current on the negative direction flows through the UC-CDSM, the sum of the two capacitor voltages ($U_{C1} + U_{C2}$), the voltage of C_1 (U_{C1}), the voltage of C_2 (U_{C2}), zero voltage and the negative voltage ($-U_{C1}$ or $-U_{C2}$) can be output by controlling the pulse signals of the three switching devices. Therefore, when assuming that all the capacitor voltages are approximately the rated value U_{CN}, each UC-CDSM can output four levels: $2U_{CN}$, U_{CN}, 0, and $-U_{CN}$. The average quantity of switching devices used for outputting a positive voltage level is 1.5, even less than the HBSM.

Among all the voltage levels, the negative voltage level should be specially explained. As shown in Fig. 4(e), the UC-CDSM outputs the negative voltage level by switching off all the switching devices. Whether the voltage of C_1 or C_2 is output depends on the voltage relationship between the two capacitors rather than the pulse signals of switching devices. For instance, if U_{C1} is higher than U_{C2}, then D_3 is in the cut-off state, and the current flows through C_2 following the dashed line in Fig. 4(e), and the output voltage is $-U_{C2}$. If U_{C1} is lower than U_{C2}, then the output voltage is $-U_{C1}$. Although the controller cannot decide which capacitor to be inserted negatively, this automatic output mechanism helps to balance the voltages of the two capacitors because the one with the lower voltage has the chance to be inserted negatively and charged.

B. Characteristics of UC-CDSM-Based MMC (UC-CD-MMC)

1) Reduction in Quantities of SMs and Semiconductors: Fig. 5(a) shows the diagram of the arm voltage waveforms when

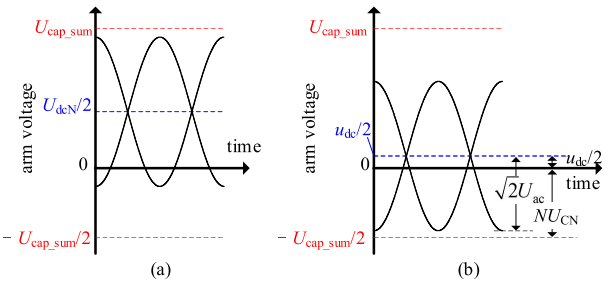


Fig. 5. Diagrams of arm voltages when the dc voltage is (a) rated value and (b) a reduced value.

the UC-CD-MMC operates under the rated dc voltage. Given that a UC-CDSM can output two positive and one negative voltage levels at most, the instantaneous arm voltages should be within the range of $[-U_{\rm cap\_sum}/2,\ U_{\rm cap\_sum}]$ to fulfill the linear modulation constraint, where $U_{\rm cap\_sum}$ is the summed capacitor voltages of each arm, defined as

$$U_{\rm cap\_sum} = N_{\rm cap}U_{\rm CN} = 2NU_{\rm CN} \tag{1}$$

where $N_{\rm cap}$ and N are the quantities of capacitors and UC-CDSMs in each arm, respectively. Therefore, once the rated capacitor voltage is determined, the quantity of series-connected UC-CDSMs should be designed to meet the requirement of linear modulation at any possible operating condition. As shown in Fig. 5(a), under the rated dc voltage, the linear modulation constraint for a given operating condition is mainly determined by the arm voltage peaks, which is expressed as

$$U_{\rm cap\_sum} - \frac{U_{\rm dcN}}{2} \geq \sqrt{2}U_{\rm ac} \tag{2}$$

where $U_{\rm ac}$ is the rms value of the ac voltage output under the given operating condition. Substituting (1) into (2) yields

$$N_{\rm cap} = 2N > \left(\frac{1}{2}m_{\rm ac} + \frac{1}{2}\right)\frac{U_{\rm dcN}}{U_{\rm CN}} \tag{3}$$

where $m_{\rm ac}$ is the modulation index under the given operating condition, defined as

$$m_{\rm ac} = \frac{\sqrt{2}U_{\rm ac}}{U_{\rm dcN}/2}. \tag{4}$$

Given that the value of $U_{\rm ac}$ varies with the operating conditions, the value of $m_{\rm ac}$ also varies with different operating conditions. The constraint on the quantity of UC-CDSMs defined in (3) should be fulfilled for all possible operating conditions within the designed operating range. Specifically, the quantity of SMs must be selected considering the maximum modulation index in the whole operating range, which is denoted as $m_{\rm ac(max)}$. For a conventional HB-MMC, the parameters must be designed to ensure that $m_{\rm ac(max)}$ does not exceed 1.0 when the third-order harmonic injection is not implemented. By comparison, the modulation index for the unidirectional-current MMCs must be increased to over 1.0 for unidirectional arm currents [19], which can be realized by utilizing the negative voltage states of the SMs.

In order to intuitively illustrate the reduction effects of the UC-CD-MMC on the quantities of SMs and switching devices, a case of 1000 MW/640 kV MMC is used as an example. Its detailed design targets can be referred to in Table I in Section V. In this example, the rated capacitor voltage is designed as 1.6 kV, and the quantity of SMs per arm of an HB-MMC is commonly designed as 400. For the unidirectional-current MMCs, the maximum modulation index $m_{\rm ac(max)}$ may reach 1.81 [19]. Thus, the quantities of SMs in the UC-FB-MMC should be designed no lower than 562, which is about 1.4 times that in a conventional HB-MMC. By comparison, since each UC-CDSM is equivalent to two UC-FBSMs, the UC-CD-MMC only uses 281 SMs per arm, which is 30% fewer than that in HB-MMC. Although this reduction is caused by the combination of two UC-FBSMs, it is still meaningful in real applications because the costs and volumes of accessory components related to the quantity of SMs, such as structural components, electronic interface units, and heat sinks, can be reduced.

A more important advantage of the UC-CD-MMC is the reduced quantity of switching devices. Given that a UC-CDSM is obtained by combining two UC-FBSMs using a shared switching device, the total quantity of switching devices in a UC-CD-MMC can be substantively reduced. In this example, the quantities of switching devices per arm in HB-MMC, UC-FB-MMC, and UC-CD-MMC are 800, 1124, and 843, respectively. The quantity of switching devices in a UC-CD-MMC is 25% fewer than that in a UC-FB-MMC and is similar to that in an HB-MMC. Considering the decreased arm current ratings due to the increased ac voltage, the UC-CD-MMC has even lower semiconductor usage than the conventional HB-MMC while still having significant advantages, such as lower capacitor usage, dc fault clearing capability, and wide-range dc voltage adjustability. Detailed comparisons of various MMC topologies are illustrated in Section V.

2) Reduction in Energy Storage Requirement: The capacitor usage is commonly evaluated by the energy storage requirement per MVA [23]. Existing literature has revealed that an increase in the modulation index by utilizing negative voltage states of SMs can significantly suppress the energy fluctuations in the converter arms, thereby reducing the energy storage requirement [9], [10].

The requirement of increasing the ac voltage for creating unidirectional arm currents just coincides with the requirement of increasing the modulation index for reducing the energy storage requirement. The increased ac voltage enables the UC-CD-MMC to have an increased modulation index, thereby having a much lower energy storage requirement. As will be evaluated in detail in Section V, the UC-CD-MMC can reduce the energy storage requirement by over 50% compared with the conventional HB-MMC [22], thereby reducing the valve volume and cost. Detailed comparisons of various MMC topologies are also illustrated in Section V.

3) DC Fault Clearing Capability: As explained in the previous section, the UC-CDSM can also be understood as a variant of CDSM, having dc fault clearing capability by blocking all the switching devices [3]. Fig. 6 shows an example of a fault current path after blocking the converter, where u_x and u_y are

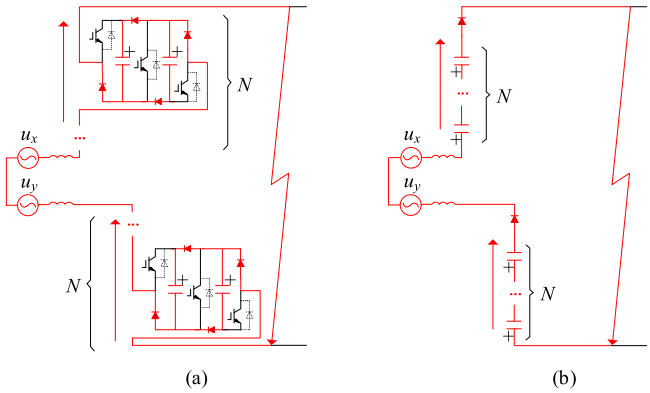


Fig. 6. Current paths during fault clearance by blocking UC-CD-MMC. (a) Fault current path. (b) Equivalent circuit.

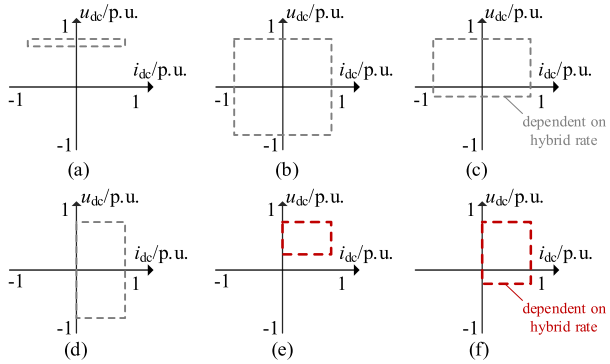


Fig. 7. Comparison of dc ranges of different MMC topologies. (a) HB-MMC. (b) FB-MMC. (c) HYB-MMC. (d) UC-FB-MMC. (e) UC-CD-MMC. (f) UC-HYB-MMC.

the phase voltages of the power grid. The UC-CDSMs are automatically inserted negatively into the converter arms to absorb fault energies and block the fault current.

4) Wide-Range DC Voltage Adjustability: The MMCs based on the SMs that have negative voltage capabilities, such as FB-MMC, HYB-MMC, and UC-FB-MMC, can adjust the dc voltage in a wide range without affecting the ac voltage capability. This feature enables these MMCs to fit many special applications, as mentioned in Section I [4], [5], [6], [7], [8], and [24]. Given that the UC-CDSM can also output negative voltage level, the UC-CD-MMC also inherits the advantage of adjustable dc voltage. However, as shown in Fig. 4, the UC-CDSM is an asymmetrical topology, whose negative voltage capability is only half of the positive one, bringing a limit to the range of the adjustable dc voltage.

As illustrated in Fig. 5(a), there is still much room between the arm voltage valleys and the lower limit $-U_{\mathrm{cap\_sum}}/2$ when outputting the rated dc voltage. Therefore, as illustrated in Fig. 5(b), the dc components of the upper and lower arm voltages can simultaneously move downward. Therefore, the dc voltage of a UC-CD-MMC can vary in a wide range without affecting the ac voltage capability. According to Fig. 5(b), the constraint for the value of the dc voltage u_{dc} is that the arm voltage valleys are no lower than the lower limit $-U_{\mathrm{cap\_sum}}/2$, expressed as

$$\frac{u_{\mathrm{dc}}}{2}+\frac{U_{\mathrm{cap\_sum}}}{2}\geq\sqrt{2}U_{\mathrm{ac}}. \tag{5}$$

According to (5), the constraint on the per-unit value of the dc voltage can be obtained by normalizing (5) with the rated dc voltage U_{dcN}, expressed as

$$u_{\mathrm{dc}}^{*}\geq\frac{2\sqrt{2}U_{\mathrm{ac}}-U_{\mathrm{cap\_sum}}}{U_{\mathrm{dcN}}}=m_{\mathrm{ac}}-\frac{U_{\mathrm{cap\_sum}}}{U_{\mathrm{dcN}}}. \tag{6}$$

Supposing that the quantity of capacitors in each arm is selected as the minimum value that fulfills (3), then

$$U_{\mathrm{cap\_sum}}=N_{\mathrm{cap}}U_{\mathrm{CN}}=\left(\frac{1}{2}m_{\mathrm{ac(max)}}+\frac{1}{2}\right)U_{\mathrm{dcN}}. \tag{7}$$

Substituting (7) into (6) yields

$$u_{\mathrm{dc}}^{*}\geq m_{\mathrm{ac}}-\frac{1}{2}m_{\mathrm{ac(max)}}-\frac{1}{2}. \tag{8}$$

Given that the modulation index m_{ac} varies with different operating conditions, the right-hand side of (8) also varies with different operating conditions. Therefore, using U^{*}_{dcmin0} to denote the minimum value that the dc voltage can reach no matter what operating condition the MMC operates at, the value of U^{*}_{dcmin0} must be the maximum value of the right-hand side of (8) (i.e., $m_{\mathrm{ac}}=m_{\mathrm{ac(max)}}$), which is expressed as

$$U_{\mathrm{dcmin0}}^{*}=\frac{1}{2}m_{\mathrm{ac(max)}}-\frac{1}{2}. \tag{9}$$

Still using the abovementioned example of $m_{\mathrm{ac(max)}}=1.81$, the minimum value of the dc voltage is approximately 0.4 per unit (p.u.) Specifically, without affecting the ac voltage output, the dc voltage can only vary in the range of [0.4 p.u., 1.0 p.u.] in this example.

Fig. 7 compares the dc voltage and current ranges of various MMC topologies. Fig. 7(a)–(c) shows the typical dc voltage and current ranges of bidirectional-current MMC topologies, including HB-, FB-, and HYB-MMCs, whose dc currents are bidirectional. The dc voltage of HB-MMC is only within a narrow range around the rated value. The employment of FBSM enables the FB-MMC to have a dc voltage range of [−1.0 p.u., 1.0 p.u.]. In the HYB-MMC composed of both FBSMs and HBSMs, the dc voltage range is dependent on the ratio of the FBSMs in each arm. For example, when the ratio of FBSMs in each arm is 50%, the HYB-MMC has a theoretical dc voltage range of [0, 1.0 p.u.].

Fig. 7(d) and (e) shows the typical dc voltage and current ranges of unidirectional-current MMC topologies, including UC-FB- and UC-CD-MMCs, whose dc currents are unidirectional. The UC-FB-MMC has the same dc voltage range as the FB-MMC, while the dc current must be unidirectional. By comparison, the dc voltage adjustable range of the UC-CD-MMC becomes narrower since the UC-CDSM is an asymmetrical topology, whose negative voltage capability is sacrificed for fewer switching devices. However, the adjustable range of the dc

voltage shown in Fig. 7(e) is still sufficient to fit some applications, such as HVdc with reduced dc voltage in extreme weather, even if it cannot reach zero. As will be analyzed in Section V, among the MMC topologies with adjustable dc voltages, the UC-CD-MMC has the fewest switching devices, which is greatly advantageous to reduce the cost and volume.

Compared with other MMC topologies, another disadvantage of UC-CD-MMC is that the power is unidirectional and the UC-CD-MMC can only operate as a rectifier because both the dc current and voltage are unidirectional. However, the reduced volume and cost, the dc fault clearing capability, and the dc voltage adjustability still make the UC-CD-MMC attractive in many dc applications, such as renewable energy integration and long-distance overhead line-based HVdc. In the applications that require the MMC to possess sort of power reversal capability for inverting, the UC-HYB-MMC to be proposed in Section III can be adopted. The UC-HYB-MMC can reverse the power direction from rectifying to inverting by changing the polarity of dc voltages, as shown in Fig. 7(f). For other applications, inverters in HVdc for example, the existing UC-FB-MMC can be selected, and the UC-CD-MMC can operate as a rectifier in coordination with the UC-FB-MMC.

III. Unidirectional-Current Hybrid MMC

A. Principle of Unidirectional-Current Hybrid MMC

As introduced in Section I, many special applications require MMCs to adjust the dc voltage to zero or even to a negative value [4], [5], [6], [7], [8], [24]. The UC-CDSM is an asymmetrical topology, sacrificing the negative voltage capability for fewer switching devices and resulting in a limited adjustable dc voltage range of UC-CD-MMC. To overcome this disadvantage, this study proposes a unidirectional-current hybrid MMC (UC-HYB-MMC) composed of UC-CDSMs and UC-FBSMs.

The existing UC-FBSM shown in Fig. 3(a) can symmetrically output voltage levels of 1, 0, and -1. The basic idea of a UC-HYB-MMC is to replace some UC-CDSMs in each arm with UC-FBSMs, thereby enhancing the negative voltage capability of the converter arm. To remain the positive voltage capability as $U_{\mathrm{cap\_sum}}$, each UC-CDSM should be replaced by two UC-FBSMs, expanding the negative voltage capability by $-U_{\mathrm{CN}}$. Using N_{F} to denote the quantity of UC-FBSMs in a converter arm in the UC-HYB-MMC (N_{F} must be even, and $N_{\mathrm{F}}/2$ UC-CDSMs are replaced by N_{F} UC-FBSMs), a hybrid rate indicating the contribution of UC-FBSMs to the positive voltage capability of the converter arm is defined as

$$k_{\mathrm{F}} = \frac{N_{\mathrm{F}}}{N_{\mathrm{cap}}} = \frac{N_{\mathrm{F}}}{2N}. \tag{10}$$

With the replacement, the positive voltage capability of the converter arm remains unchanged, whereas the negative capability is extended, and the arm voltage can vary within the range of $[-(1+k_{\mathrm{F}})U_{\mathrm{cap\_sum}}/2,\ U_{\mathrm{cap\_sum}}]$. Similar to (5), if the negative limit of the arm voltage is extended to $-(1+k_{\mathrm{F}})U_{\mathrm{cap\_sum}}/2$, the constraint for the dc voltage is expressed as

$$\frac{u_{\mathrm{dc}}}{2} + (1+k_{\mathrm{F}})\frac{U_{\mathrm{cap\_sum}}}{2} \geq \sqrt{2}U_{\mathrm{ac}}. \tag{11}$$

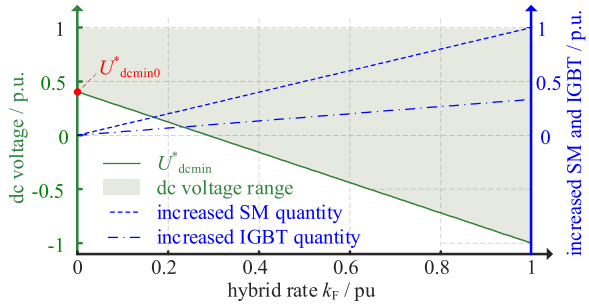


Fig. 8. Effects of hybrid rate k_{F} on dc voltage range enlargement in the case study, and increase in SM and switching device quantities.

Substituting (7) into (11) and normalizing (11) by the rated dc voltage yield

$$u^*_{\mathrm{dc}} \geq m_{\mathrm{ac}} - \frac{1+k_{\mathrm{F}}}{2} \times \left(m_{\mathrm{ac(max)}} + 1\right). \tag{12}$$

Given that the modulation index m_{ac} varies with different operating conditions, the right-hand side of (12) is also related to the operating condition. Therefore, using U^*_{dcmin} to denote the minimum value that the dc voltage of UC-HYB-MMC can reach no matter what operating condition the UC-HYB-MMC operates at, the value of U^*_{dcmin} must be the maximum value of the right-hand side of (12) (i.e., $m_{\mathrm{ac}} = m_{\mathrm{ac(max)}}$), which is expressed as

$$\begin{aligned} U^*_{\mathrm{dcmin}} &= m_{\mathrm{ac(max)}} - \frac{1+k_{\mathrm{F}}}{2} \times \left(m_{\mathrm{ac(max)}} + 1\right) \\ &= U^*_{\mathrm{dcmin0}} - \frac{k_{\mathrm{F}}}{2}\left(m_{\mathrm{ac(max)}} + 1\right) \end{aligned} \tag{13}$$

where U^*_{dcmin0} is the minimum reachable dc voltage of UC-CD-MMC presented in Section II. Equation (13) indicates that by increasing the hybrid rate k_{F}, the reachable minimum dc voltage decreases, thereby extending the dc voltage range. An extreme case is that the UC-HYB-MMC is essentially a UC-CD-MMC when $k_{\mathrm{F}} = 0$, and another extreme case is that the UC-HYB-MMC totally becomes a UC-FB-MMC when $k_{\mathrm{F}} = 1$, which can output full-range dc voltages. Still taking $m_{\mathrm{ac(max)}} = 1.81$ as an example, Fig. 8 plots the relationships between dc voltage ranges and k_{F} in this example. With the increase in k_{F}, the dc voltage range is enlarged.

Clearly, the replacement of UC-CDSMs by the UC-FBSMs brings side effects that the quantities of the SM and switching devices will increase. Compared with UC-CD-MMC, a UC-HYB-MMC utilizes k_{F} times more SMs and $k_{\mathrm{F}}/3$ times more switching devices. Fig. 8 also plots the increased SM and switching device quantities with the increase in the hybrid rate k_{F}. Therefore, in order to minimize the cost and volume, the hybrid rate can be selected as low as possible under the premise that the adjustable dc voltage range can meet the design requirement. For example, under $m_{\mathrm{ac(max)}} = 1.81$, the hybrid rate can be designed as 29% in this case study to obtain an adjustable range of $[0,\ U_{\mathrm{dcN}}]$.

B. Characteristics of UC-HYB-MMC

Given that the UC-HYB-MMC is developed on the basis of the UC-CD-MMC, the UC-HYB-MMC also has the characteristics of reduced volume and cost and dc fault-clearing capability. Compared with the UC-CD-MMC, the UC-HYB-MMC can have a wider adjustable dc voltage range by increasing the hybrid rate k_{F}, enabling the UC-HYB-MMC to fit more application scenarios, such as online switch-in and -out [5] and series multiterminal HVdc [6], [7], [8]. By increasing k_{F}, the UC-HYB-MMC can further output negative dc voltages for active clearance of dc faults [4]. The advantage of the active clearance is that the energy stored in the long-distance lines can be transferred into the ac system rather than absorbed by the SM capacitors, thereby alleviating overvoltage on SMs. The enlargement of dc voltage range is certainly at a cost of increases in the quantities of SMs and switching devices.

IV. Universal Sorting and Capacitor Voltage Balancing Algorithm of UC-CD- and UC-HYB-MMCs

When the UC-CDSM outputs positive or zero voltage levels, it is equivalent to two independent UC-FBSMs that are connected in series. Therefore, the conventional sorting and capacitor voltage balancing algorithm can be directly implemented, that is, inserting the capacitors with the highest voltages.

When the arm outputs negative voltages, the sorting and capacitor voltage balancing algorithm should have been to insert the capacitors with the lowest voltages negatively. However, as analyzed in Section II, whether the voltage of C_1 or C_2 is negatively inserted depends on the voltage relationship between them rather than the on or off states of the switching devices: only the capacitor with the lower voltage has the chance to be negatively inserted. Therefore, the higher capacitor voltage in each UC-CDSM must not be involved in the sorting algorithm. To cope with this problem, this study proposes a preprocessing algorithm that improves the conventional sorting algorithm to fit the UC-HYB-MMC. Given that the UC-CD-MMC is a special case of UC-HYB-MMC, whose hybrid rate $k_{\mathrm{F}} = 0$, the proposed algorithm is also suitable for UC-CD-MMC.

As described in the previous sections, there are $(N_{\mathrm{cap}} - N_{\mathrm{F}})/2$ UC-CDSMs and N_{F} UC-FBSMs in a converter arm. Therefore, since each UC-CDSM has two capacitors and each UC-FBSM has one, there are $(N_{\mathrm{cap}} - N_{\mathrm{F}})$ capacitors in UC-CDSMs and N_{F} capacitors in UC-FBSMs. Fig. 9 shows the entire sorting and capacitor voltage balancing algorithm, where n is the quantity of capacitors to be inserted. The entire algorithm is divided into the preprocessing and the conventional sorting algorithms. If the converter arm is about to output a positive voltage, the preprocessing algorithm does nothing and the capacitor voltages are directly sent into the conventional sorting algorithm. The n capacitors with the highest voltages are inserted positively and discharged. By comparison, if the converter arm is about to output a negative voltage (i.e., $n < 0$), then the two capacitor voltages in each UC-CDSM are first compared, and then, the higher voltage is added by a very large value, so that they are kept on the top highest places when all the capacitor voltages are sorted. Notably, the added value is not strictly restricted and

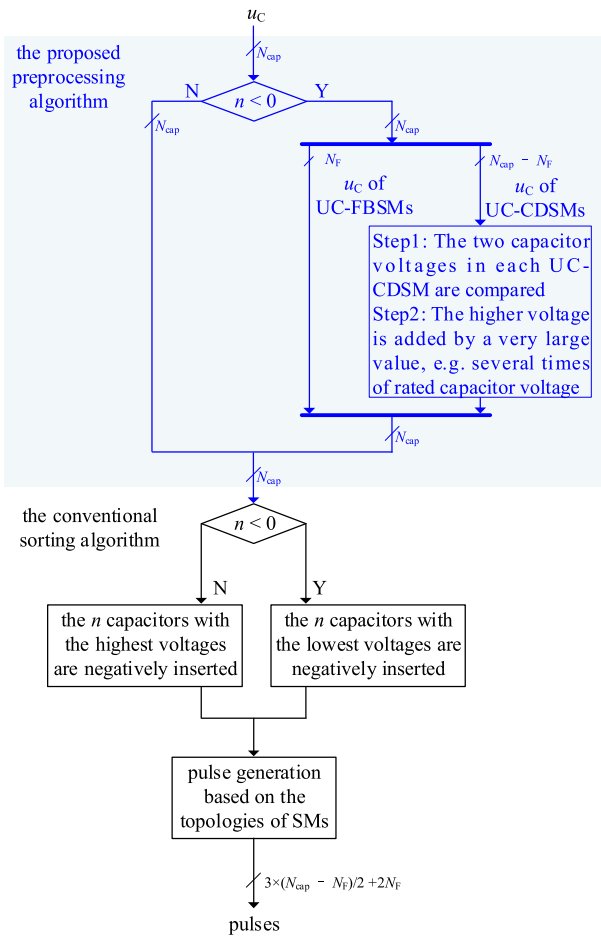


Fig. 9. Block diagram of improved sorting and selection algorithm of the UC-HYB-MMC.

specified. In practice, the added value can be selected meeting the requirement that the revised capacitor voltage (the higher one in the two capacitor voltages in each UC-CDSM) will go to the top highest places when sorted. For example, the value can be selected as several times of the rated capacitor voltage. Then, the processed capacitor voltages are sent to the conventional sorting algorithm, where the higher voltages in each UC-CDSM cannot be selected because the algorithm chooses the capacitors with the lowest voltages to charge. With the proposed preprocessing algorithm, the conventional sorting algorithm is improved and can be implemented in the UC-HYB-MMCs and UC-CD-MMCs.

V. Design Example and Characteristic Comparison

As analyzed in Sections II and III, the proposed UC-CD- and UC-HYB-MMCs have advantages over other MMC topologies. Generally, the existing SM topologies are divided into two categories: the ones without and with negative voltage capabilities. Compared with the MMCs based on the SM topologies without negative voltage capabilities, the proposed UC-CD- and UC-HYB-MMCs can reduce capacitor usages by increasing the modulation index and can widely adjust the dc voltage. Compared with the MMCs based on the SM topologies with

TABLE I
COMPARISONS OF DESIGN, COST, AND VOLUME AMONG VARIOUS MMC TOPOLOGIES

Categories	Bidirectional-current MMC topologies		Unidirectional-current MMC topologies*		
Topologies	HB-MMC	HYB-MMC	UC-FB-MMC	UC-CD-MMC	UC-HYB-MMC
Rated active power/MW			1000		
Reactive power capability/Mvar			±500		
Rated dc voltage/kV			640		
Rated ac voltage/kV	192	192	348	348	348
Max. modulation index $m_{ac(max)}$ /p.u.	1.0	1.0	1.81	1.81	1.81
Rated ac current /A	1941	1941	1071	1071	1071
Rated arm current /A	1102	1102	782	782	782
V/*I* ratings of IGBTs and diodes	3300 V / 1500 A	3300 V / 1500 A	3300 V / 1200 A	3300 V / 1200 A	3300 V / 1200 A
Quantities of SMs**	400 HBSM	200 HBSMs+ 200 FBSM	562 UC-FBSM	281 UC-CDSM	200 UC-CDSM+ 162 UC-FBSM
Hybrid rate/p.u.	-	0.5	-	-	0.29
Quantities of IGBTs/diodes	4,800 / 4,800	7,200 / 7,200	6,744 / 6,744	5,058 / 6,744	5,544 / 6,744
Semiconductor usage S_{sem} /MVA	23,760	35,640	26,706	21,365	22,904
SM capacitance/mF	12.57	12.57	3.82	3.82	3.82
Energy storage requirement E_{MMC}/kJ/MVA	34.54	34.54	14.76	14.76	14.76
DC voltage range/kV	640	[0, 640]	[–640, 640]	[256, 640]	[0, 640]
Cost/p.u.	1.00	1.2	0.93	0.68	0.75
Volume/p.u.	1.00	1.15	0.78	0.61	0.66

* Reactive power capabilities of the unidirectional-current MMCs are proportional to the transmitted active powers. At rated active power 1000 MW, the reactive power is designed as 500 Mvar in the case study. ACCI is considered when calculating the rated arm current of unidirectional-current MMCs.
** Quantities of HBSMs and FBSMs in HYB-MMC, and quantities of UC-CDSMs and UC-FBSMs in UC-HYB-MMC are based on a minimum adjustable dc voltage of 0, that is, the adjustable dc voltage range is [0, U_{dcN}].

negative voltage capabilities, the proposed MMC topologies use much fewer switching devices and SMs. Therefore, the proposed MMC topologies have reduced valve costs and volumes as well as power losses.

This section first presents quantitative evaluations and comparisons of the costs and volumes of various MMC topologies, and then the power losses of them are presented and compared.

The MMC topologies compared are divided into two categories: the bidirectional-current MMC topologies, including HB- and HYB-MMCs, and the unidirectional-current MMC topologies, including UC-FB-, UC-CD-, and UC-HYB-MMCs. Table I lists the main design targets. The rated active and reactive powers are 1000 MW and ±500 Mvar, respectively, and the rated dc voltage is designed as 640 kV. The arm inductance is designed as 0.2 p.u., and the transformer leakage inductance is 0.1 p.u. Table I also lists the main parameters of various MMCs according to their respective design methodologies. Compared with the bidirectional-current MMC topologies, the unidirectional-current MMCs have higher rated ac voltages to create unidirectional arm currents, thereby having lower rated ac and arm currents. According to the main parameters and the expected operating ranges, the maximum modulation indices $m_{\mathrm{ac(max)}}$ of the unidirectional-current MMC topologies are 1.81.

A. Evaluations and Comparisons of Costs and Volumes

The costs and volumes of the MMC valves are evaluated by mainly considering the usages of semiconductors, SM capacitors, and other accessary components. The insulated gate bipolar transistors (IGBTs) are taken as examples of the switching devices in the evaluation of the semiconductor usages.

In the aspects of semiconductors, including IGBTs and diodes, the voltage rating of 3300 V is selected in this case study, and the rated capacitor voltage is designed as 1600 V. For the conventional HB- and FB-MMCs, considering the rated arm currents, the IGBTs and diodes with current rating of 1500 A are selected. For the unidirectional-current MMCs, such as UC-FB-, UC-CD-, and UC-HYB-MMCs, the IGBTs with current rating of 1200 A are selected given their lower rated arm currents due to the increased rated ac voltages. Notably, although S_4 in the UC-CDSM has longer conduction time than S_1 and S_7, and generates more power losses and heat, it is still reasonable to select the same current ratings for the three switching devices because the peak currents they switch on or off are the same. The diodes in the unidirectional-current MMCs are divided into independent and precharging diodes. For the independent diodes, the ones with current rating of 1200 A are selected. By comparison, the precharging diodes are ignored in the evaluation and comparison because of their most low current ratings. Therefore, considering the different current ratings of IGBTs and diodes, a semiconductor usage related to the total capacities of IGBTs and diodes is defined in this study as

$$S_{\mathrm{sem}} = \eta \times K_{\mathrm{IGBT}} V_{\mathrm{CES}} I_{\mathrm{C}} + (1-\eta) \times K_{\mathrm{diode}} V_{\mathrm{RRM}} I_{\mathrm{F}} \quad (14)$$

where K_{IGBT} and K_{diode} are the total quantities of IGBTs and diodes in an MMC, respectively, V_{CES} and I_{C} are the voltage and current ratings of IGBTs, respectively, V_{RRM} and I_{F} are the voltage and current ratings of diodes, respectively, and η and $(1-\eta)$ denote the weight coefficients of IGBTs and diodes in the total semiconductor usage, respectively.

In the aspects of SM capacitors, the energy storage requirement per MVA in an MMC is commonly used to evaluate the

total capacitor usage in an MMC [23], which is defined as

$$E_{\mathrm{MMC}} = \frac{6 \times N_{\mathrm{cap}} \times \frac{1}{2} C_{\mathrm{SM}} U_{\mathrm{CN}}^2}{S_{\mathrm{N}}} \tag{15}$$

where C_{SM} is the SM capacitance, N_{cap} is the quantity of capacitors per arm, and S_{N} is the rated capacity of the MMC. Given that the interaction between the arm voltage and current causes energy fluctuations in the SM capacitors and further causes the voltage ripples, the values of C_{SM} for each MMC topology are designed on the basis that the maximum voltage ripples are limited within 10%. Therefore, the values of C_{SM} in each MMC topology can be obtained by first analyzing the arm voltages and currents, calculating the energy fluctuation in the capacitor, and then finding the minimum requirement for C_{SM} [25], [26], expressed as

$$C_{\mathrm{SM}} = \frac{2}{(\varepsilon_{\mathrm{lim}} + 1)^2 - 1} \times \frac{\hat{E}_{\mathrm{Cmax}}}{U_{\mathrm{CN}}^2} \tag{16}$$

where $\varepsilon_{\mathrm{lim}}$ denotes the upper limit of the permissible voltage ripple rate, and $\hat{E}_{\mathrm{Cmax}}$ denotes the maximum amplitude of the fluctuating energy in the SM capacitors.

Other accessory components of the MMC valves include structural components, electronic interface units, and heat sinks. In this study, the cost and volume of all these components are considered to be proportional to the quantity of SMs per arm.

In order to make a quantitative comparison, the cost and volume of different MMC solutions are normalized with respect to the values applicable to the conventional HB-MMC. The values of the cost and volume of the HB-MMC are set to 1.0 p.u. The per-unit cost and volume can be calculated as

$$C_{(\mathrm{MMC\_Type})} = \alpha_{\mathrm{C}} \frac{S_{\mathrm{sem(MMC\_Type)}}}{S_{\mathrm{sem(HB-MMC)}}} + \beta_{\mathrm{C}} \frac{E_{\mathrm{MMC(MMC\_Type)}}}{E_{\mathrm{MMC(HB-MMC)}}} + \gamma_{\mathrm{C}} \frac{N_{(\mathrm{MMC\_Type})}}{N_{(\mathrm{HB-MMC})}} \tag{17}$$

$$V_{(\mathrm{MMC\_Type})} = \alpha_{\mathrm{V}} \frac{S_{\mathrm{sem(MMC\_Type)}}}{S_{\mathrm{sem(HB-MMC)}}} + \beta_{\mathrm{V}} \frac{E_{\mathrm{MMC(MMC\_Type)}}}{E_{\mathrm{MMC(HB-MMC)}}} + \gamma_{\mathrm{V}} \frac{N_{(\mathrm{MMC\_Type})}}{N_{(\mathrm{HB-MMC})}} \tag{18}$$

where the subscript "MMC_Type" indicates a certain topology of MMC, including HYB-MMC, UC-FB-MMC, UC-CD-MMC, and UC-HYB-MMC. α_{C}, β_{C}, and γ_{C} denote the weight coefficients that the semiconductors, capacitors, and accessory components account for the total cost, respectively, and α_{V}, β_{V}, and γ_{V} denote the weight coefficients that the semiconductors, capacitors, and accessory components account for the total volume, respectively. The following relationship should be met:

$$\alpha_{\mathrm{C}} + \beta_{\mathrm{C}} + \gamma_{\mathrm{C}} = \alpha_{\mathrm{V}} + \beta_{\mathrm{V}} + \gamma_{\mathrm{V}} = 100\%. \tag{19}$$

The values of η, α_{C}, β_{C}, γ_{C}, α_{V}, β_{V}, and γ_{V} may vary in different dc projects because the voltage and power levels, SM structure designs, and market prices of the devices may change. In this case study, the weight coefficients are obtained based on the empirical data according to the parameters of the case study and are set as $\eta = 80\%$, $\alpha_{\mathrm{C}} = 40\%$, $\beta_{\mathrm{C}} = 37.5\%$, and $\gamma_{\mathrm{C}} = 22.5\%$, and $\alpha_{\mathrm{V}} = 30\%$, $\beta_{\mathrm{V}} = 55\%$, and $\gamma_{\mathrm{V}} = 15\%$.

As given in Table I, compared with the conventional HB-MMC and HYB-MMC with bidirectional arm currents, the unidirectional-current MMCs must increase the rated ac voltages to ensure unidirectional arm currents. However, increasing the rated ac voltage is double edged. The positive effect is that it helps to suppress the energy fluctuations in the converter arms by increasing the modulation index, which has an optimal value of 1.414 at the unity power factor [9], thereby greatly reducing the energy storage requirement. As given in Table I, the energy storage requirement can be decreased from 34.54 to 14.76 kJ/MVA by employing the unidirectional-current MMCs, thereby contributing greatly to reducing the costs and volumes of MMCs. By contrast, the negative effect of increasing the rated ac voltage is that the required quantities of SMs and IGBTs are increased. As given in Table I, the existing UC-FB-MMC technique [19] requires 562 SMs and 6744 IGBTs, increased by approximately 40% compared with the HB-MMC. Although the semiconductor usages defined in (14) are similar in the HB- and UC-FB-MMCs because the rated arm current of the UC-FB-MMC decreases with the increase in the ac voltage, the increased quantities of SMs and IGBTs still offset the reduction in the valve cost and volume.

The proposed UC-CD-MMC can overcome the negative effects brought by the increased ac voltage. Compared with the existing UC-FB-MMC [19], the proposed UC-CD-MMC can reduce the quantities of SMs and IGBTs by 50% and 25%, respectively. Therefore, the UC-CD-MMC has similar quantity of IGBTs to the HB-MMC, and the semiconductor usage is further lower given the decreased rated arm current, as illustrated in Table I. Given that the energy storage requirement, semiconductor usage, and quantity of SMs in the UC-CD-MMC are all lower than those in the HB-MMC, the cost the volume can be reasonably reduced by using UC-CD-MMC. As listed in Table I, the cost and volume of the UC-CD-MMC solution are 0.68 and 0.61 p.u., respectively, which are the lowest in the studied solutions.

As analyzed in Sections II and III, the main limit of the UC-CD-MMC is the limited adjustable dc voltage range. For example, the adjustable dc voltage range of the UC-CD-MMC is [256 kV, 640 kV], which limits its application in the scenarios that require the dc voltage being able to decrease to zero or even a negative value. In these application scenarios, the proposed UC-HYB-MMC combining the UC-CDSMs and UC-FBSMs can be employed to extend the dc voltage range. As analyzed in Section III, the required quantities of IGBTs and SMs increase with the increase in the hybrid rate k_{F}. Therefore, the hybrid rate can be designed as small as possible under the premise that the expected adjustable dc voltage range is fulfilled. In this case study, the hybrid rate is designed as 29% to obtain an adjustable range of [0, 640 kV]. Thus, the quantity of SMs in each arm is increased from 281 to 362, and the total quantity of IGBTs is increased from 5058 to 5544 compared with the UC-CD-MMC. However, the quantities of required SMs and IGBTs in the proposed UC-HYB-MMC are still much fewer compared with the existing topologies with dc voltage adjustability, such as

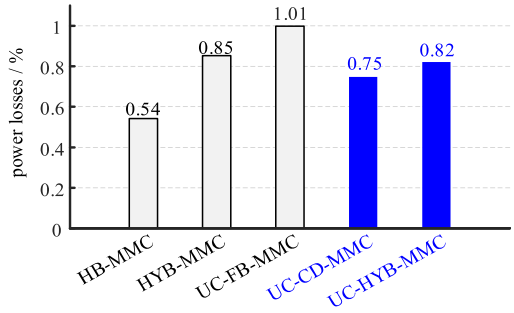


Fig. 10. Comparison of the power losses of different topologies of MMCs. Light bars represent the existing topologies, and dark bars represent the proposed topologies.

TABLE II
POWER LOSS DISTRIBUTION AMONG SEMICONDUCTORS IN UC-CD- AND UC-HYB-MMCS

UC-CD-MMC	UC-CDSM						
	S_1	S_4	S_7	D_2	D_3	D_5	D_6
	5%	36%	5%	24%	3%	3%	24%
UC-HYB-MMC	UC-CDSM						
	S_1	S_4	S_7	D_2	D_3	D_5	D_6
	3%	24%	3%	15%	2%	2%	15%
	UC-FBSM						
	S_1	S_4		D_2		D_3	
	12%	12%		6%		6%	

HYB-MMC and UC-FB-MMC, resulting in a much lower cost and volume. In fact, even if compared with the conventional HB-MMC, the UC-HYB-MMC only uses 15% more IGBTs, but the valve cost and volume are much lower due to the greatly reduced energy storage requirement and quantity of SMs. As given in Table I, the cost and volume of the UC-HYB-MMC are 0.75 and 0.66 p.u., respectively, which are only slightly higher than that of the UC-CD-MMC and are much lower than other MMC solutions.

Although the case studies in Table I are based on the high-voltage MMCs, the proposed UC-CD- and UC-HYB-MMCs can also reduce the valve costs and volumes in the middle-voltage applications because of their relatively low semiconductor usages, low energy storage requirements, and few SMs. Therefore, the proposed UC-CD- and UC-HYB-MMCs are also attractive to middle-voltage applications.

B. Loss Evaluation

The losses of different MMC topologies when transmitting the rated active and reactive powers are calculated using the discrete power loss model [27]. The conduction losses are calculated on the basis of the voltage drops and current flows, and the switching losses are calculated on the basis of the switching energies at each time point in the discrete model. Many modulation methods can be used, such as the nearest level modulation (NLM), phase shift modulation [28], and tolerance band modulation [29]. Given that the NLM is relatively simple to cope with hundreds of voltage levels, it is used when calculating the power losses in this study. Fig. 10 shows the evaluation results of the losses. The conventional HB-MMC certainly has the lowest loss because it has the simplest topology and the fewest switching devices. Other MMC topologies, which are improved to provide more optimal characteristics, such as lower energy storage requirements, dc voltage adjustability, and dc fault blocking capability, have higher losses mainly due to more semiconductor devices. However, the proposed UC-CD-MMC and UC-HYB-MMC have lower power losses due to the reduced quantities of switching devices compared with the HYB-MMC and UC-FB-MMC. As shown in Fig. 10, the power losses of the UC-CD-MMC and the UC-HYB-MMC are 0.75% and 0.82%, respectively, which are only higher than that of the HB-MMC and are still acceptable in real applications. Table II presents the power loss distribution among the semiconductors in the UC-CD- and UC-HYB-MMCs. S_4, D_2, and D_6 in the UC-CDSMs have much higher losses than other semiconductors, and thus, their heat sinks must be carefully designed to avoid possible damage caused by overheating.

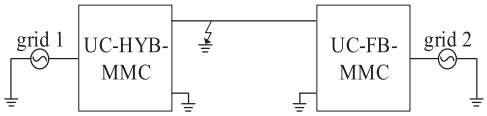


Fig. 11. Diagram of simulation model.

TABLE III
PARAMETERS OF SIMULATIONS

Terms	Values
Rated active power/MW	1000
Rated reactive power/Mvar	±500
Rated dc voltage/kV	640
Rated dc current/kA	1.5625
Rated ac voltage/kV	348
Rated SM voltage/kV	1.6
Quantities of UC-CDSMs per arm	200
Quantities of UC-FBSMs per arm	162
SM capacitance/mF	3.82

VI. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

The UC-CD-MMC is considered to be a special case of UC-HYB-MMC. Therefore, a simulation model of the UC-HYB-MMC was built in MATLAB/Simulink, as shown in Fig. 11, to verify the feasibility of the proposed MMC topologies and control schemes. The equivalent models of the MMCs were built by using a technique similar to those in [30] and [31]. A UC-HYB-MMC, controlling the dc voltage, and a UC-FB-MMC, controlling the dc current, were connected with two separate power grids. The parameters of the UC-CD-MMC are shown in Table III. The start-up process, active power rising and reactive power stepping-up, and dc fault clearing were simulated.

The start-up process is divided into uncontrollable and controllable charging stages. The uncontrollable charging stage of the UC-HYB-MMC is the same as the conventional HB- and FB-MMCs, so the waveforms are not demonstrated in this study. Fig. 12 shows the waveforms of the UC-HYB-MMC during the

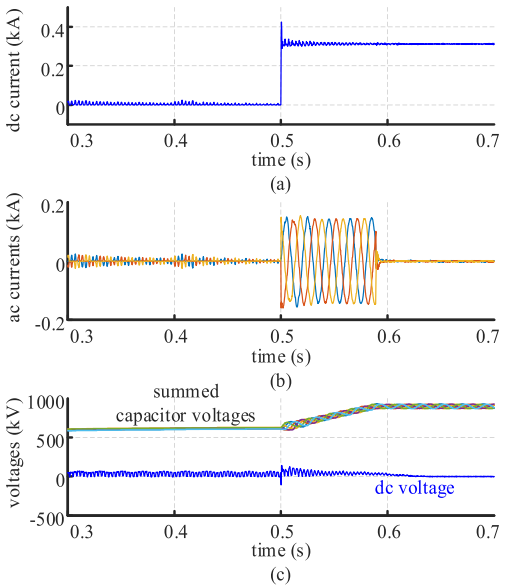


Fig. 12. Simulation results during controllable charging of UC-HYB-MMC. (a) DC current. (b) AC current. (c) Summed capacitor voltages and dc voltage.

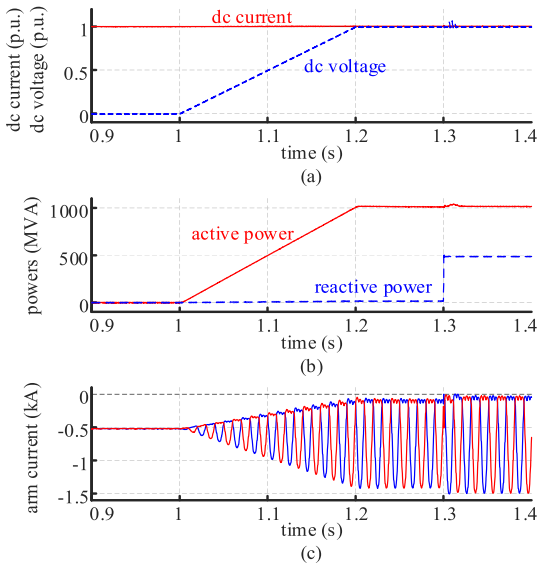


Fig. 13. Simulation results during active power rising and reactive power step. (a) DC current and voltage. (b) Active and reactive powers. (c) Arm currents.

controllable charging stage, before which the summed capacitor voltage was already around 600 kV (approximately 0.67 p.u.). At 0.5 s, the system was deblocked. The dc current was controlled to 0.2 p.u. (approximately 300 A), as shown in Fig. 12(a). As shown in Fig. 12(c), the dc voltage was around zero, so there was no power transmission between the two MMCs. The capacitor voltages increased in the controllable charging stage until they reached the rated value, 899 kV (1.6 kV per capacitor).

Fig. 13 shows the waveforms during active power rising and reactive power stepping-up. The system retains a rated dc current, as shown in Fig. 13(a). The UC-HYB-MMC increased the dc voltage with a slope from 1 to 1.2 s. As shown in Fig. 13(b), the active power increased following the dc voltage. The reactive

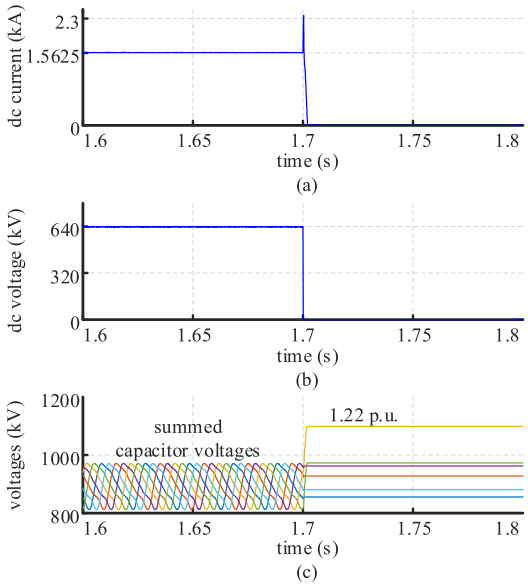


Fig. 14. Simulation results during dc fault clearance. (a) DC current. (b) DC voltage. (c) Summed capacitor voltages.

TABLE IV
PARAMETERS OF EXPERIMENTS

Terms	Values
Rated active power/W	2000
Rated dc voltage/V	250
Rated ac voltage/V	137
Rated SM voltage/V	84
Quantities of UC-CDSMs per arm	1
Quantities of UC-FBSMs per arm	2
SM capacitance/mF	1.17

power stepped up at 1.3 s. During the entire process, the arm currents were always negatively unidirectional, as shown in Fig. 13(c).

Fig. 14 shows the simulation results during active clearance of dc fault. The rated capacitor voltages were 1.6 kV, and thus, the rated summed capacitor voltages were 899 kV. Before 1.7 s, the MMC was operating normally. A dc short-circuit fault at 1.7 s was created in the simulation. The dc current suddenly increased, and the dc voltage fell to zero, as shown in Fig. 14(a) and (b), respectively. When the fault was detected, the MMC was blocked. Fig. 14(c) shows that the summed capacitor voltages increased to absorb the fault energy, and the fault was cleared. In real projects, the fault energy must be carefully calculated based on the specific projects, and the SM capacitance must be carefully designed to avoid overvoltage.

B. Experimental Results

A 250 V/2000 W experimental platform was built to verify the feasibility of the proposed MMC topologies and control schemes using hardware. Fig. 15(a) and (b) shows the photograph and diagram of the experimental platform, respectively. Two UC-FBSMs and one UC-CDSM are present in each arm of the UC-HYB-MMC. Table IV lists other parameters of the UC-HYB-MMC.

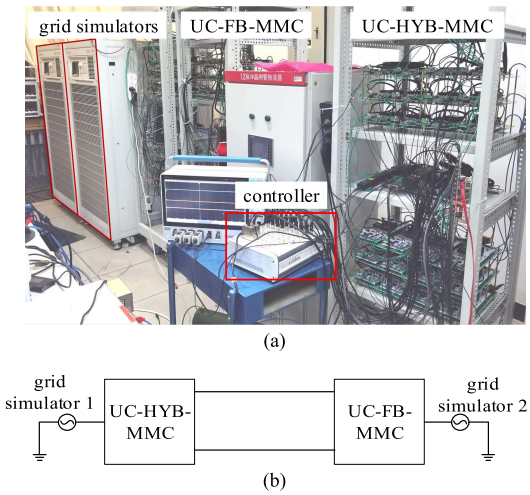


Fig. 15. (a) Photograph and (b) diagram of the experimental platform.

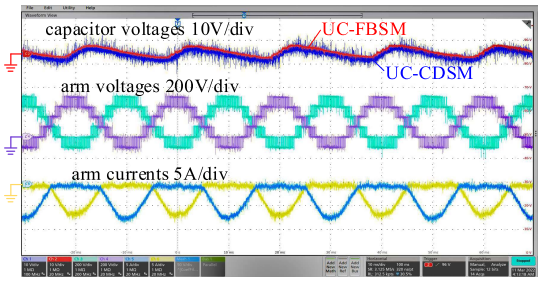


Fig. 16. Steady-state experimental results of UC-HYB-MMC.

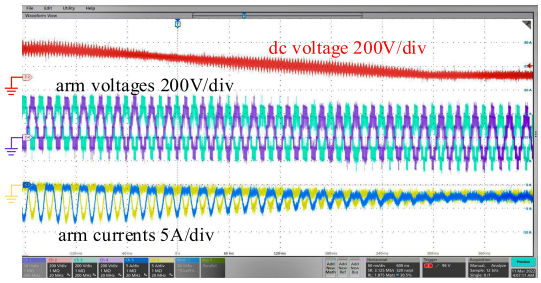


Fig. 17. Experimental results of UC-HYB-MMC during dc voltage decreasing.

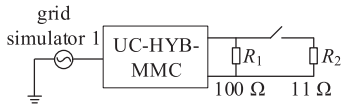


Fig. 18 Experimental circuit of dc-side short-circuit fault clearance.

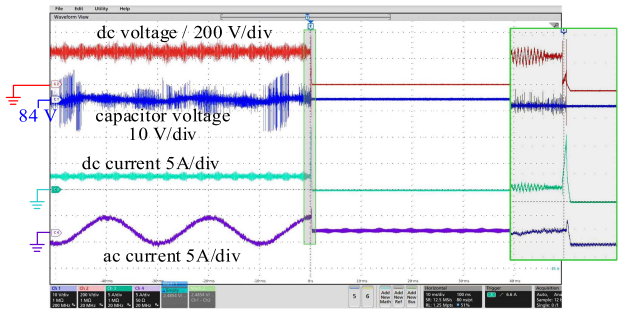


Fig. 19. Experimental results of UC-HYB-MMC during dc fault clearance.

Fig. 16 shows the experimental results in steady states. The capacitor voltages of a UC-FBSM and a UC-CDSM were overlaid on the top of the screenshot. Given that both the UC-FBSM and UC-CDSM can output negative voltage levels, no evident voltage divergence was observed between them. The proposed sorting and capacitor voltage balancing algorithm enabled them to have similar capacitor voltage waveforms. The arm voltages were presented in the middle of the oscilloscope screenshot. There were both positive and negative voltage sections. The proposed sorting and capacitor voltage balancing algorithm decided which capacitors to be inserted. The arm currents were put at the bottom of the screenshot. The arm currents were kept negatively unidirectional, creating a prerequisite for the UC-CDSM to output the negative voltage level.

Fig. 17 shows the experimental results during dc voltage decreasing. The dc voltage decreased from 250 to 0 V, as shown on the top of Fig. 17. As shown in the middle of Fig. 17, the dc components of the arm voltages decreased correspondingly. The converter arms output three negative voltage levels at most. During the entire process of dc voltage decreasing, the arm currents were always kept negatively unidirectional.

An experimental platform was built to verify the dc fault clearing capability of the UC-HYB-MMC. Fig. 18 shows the diagram and Table IV tabulates the parameters. The UC-HYB-MMC was operating with R_1 on the dc side, which has a resistance of 100 Ω (3.2 p.u.). The resistor R_2, which has a resistance of 11 Ω (0.35 p.u.), was switched into the circuit to simulate a short circuit fault. Fig. 19 shows the experimental result. As soon as the MMC had detected that the dc current exceeded the preset value, 12 A (1.5 p.u.), the MMC was quickly blocked to clear the dc fault. The dc current quickly decreased to 0, indicating that the fault was cleared.

VII. Conclusion

The proposed asymmetrical UC-CDSM, developed by combining two UC-FBSMs using a shared switching device, only uses three switching devices to output voltage levels of 2, 1, 0, and −1. The quantities of SMs and switching devices of the UC-CD-MMC can be significantly reduced, and the UC-CD-MMC still has various advantages brought by utilizing the negative voltage states of UC-CDSM, such as low capacitor usage, dc fault clearing capability, and wide-range dc voltage adjustability.

Although the UC-CD-MMC can adjust the dc voltage in a wide range, a lower limit that is slightly higher than zero exists because of the asymmetrical voltage output of UC-CDSM. This study further presents a UC-HYB-MMC composed of UC-CDSMs and UC-FBSMs to enhance the negative voltage capability of the converter arms, thereby extending the dc voltage adjustable range. Increasing the hybrid rate can enlarge the range of the dc voltage, but causes increases in the SM and semiconductor quantities. The hybrid rate can be designed by considering the tradeoff between the expected dc voltage range and the quantities of SM and switching devices.

The proposed UC-CD-MMC can be understood as a special case of the UC-HYB-MMC, whose hybrid rate is 0. A universal sorting and capacitor voltage balancing algorithm is proposed for the UC-CD- and UC-HYB-MMCs. A preprocessing algorithm is added to the conventional sorting algorithm, which helps to select the capacitors in the UC-CDSMs and balance the capacitor voltages in different SM topologies.

Detailed evaluations and comparisons are conducted on the designs and valve costs and volumes between various typical MMC topologies and the proposed UC-CD- and UC-HYB-MMCs. The results indicate that the proposed UC-CD- and UC-HYB-MMCs can reduce the valve cost by approximately 32% and 25%, respectively, and volume by approximately 39% and 34%, respectively, compared with the conventional HB-MMC. The feasibility of the proposed UC-CD- and UC-HYB-MMCs, and the control scheme are verified by the simulation and experimental results. The experimental results also indicate that no evident divergence is observed between the capacitor voltages of UC-FBSMs and UC-CDSMs.

REFERENCES

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Power Tech. Conf. Proc.*, 2003, pp. 1–6.

[2] C. Zhao, K. Luan, H. Zhang, Z. Li, P. Wang, and Y. Li, "Enhancement of ZSVI by circulating current injection for full-bridge MMC with low energy storage requirements," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4075–4085, Dec. 2020, doi: 10.1109/JESTPE.2019.2927690.

[3] R. Marquardt, "Modular multilevel converter: An universal concept for HVDC-networks and extended DC-bus-applications," in *Proc. Int. Power Electron. Conf.*, 2010, pp. 502–507, doi: 10.1109/IPEC.2010.5544594.

[4] Q. Song, S. Xu, Y. Zhou, Y. Gim, Z. Li, and Z. Deng, "Active fault-clearing on long-distance overhead lines using a hybrid modular multilevel converter," in *Proc. IEEE 28th Int. Symp. Ind. Electron.*, 2019, pp. 2033–2038, doi: 10.1109/ISIE.2019.8781312.

[5] H. Rao et al., "Key technologies of ultra-high voltage hybrid LCC-VSC MTDC systems," *CSEE J. Power Energy Syst.*, vol. 5, no. 3, pp. 365–373, 2019, doi: 10.17775/CSEEJPES.2019.01140.

[6] G. Guo et al., "Series-connected-based offshore wind farms with full-bridge modular multilevel converter as grid- and generator-side converters," *IEEE Trans. Ind. Electron.*, vol. 67, no. 4, pp. 2798–2809, Apr. 2020, doi: 10.1109/TIE.2019.2912777.

[7] Z. Li, Q. Song, R. Zeng, B. Zhao, J. Meng, and Z. Deng, "A DC grid access solution based on series-connected distributed full-bridge submodule-based MMCs," in *Proc. IEEE 28th Int. Symp. Ind. Electron.*, 2019, pp. 697–701, doi: 10.1109/ISIE.2019.8781208.

[8] G. Guo et al., "HB and FB MMC based onshore converter in series-connected offshore wind farm," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2646–2658, Mar. 2020, doi: 10.1109/TPEL.2019.2929689.

[9] Y. Lyu, C. Li, Y.-H. Hsieh, F. C. Lee, Q. Li, and R. Xu, "Capacitor voltage ripple reduction with state trajectory analysis for modular multilevel converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 1829–1836, doi: 10.1109/APEC.2017.7930947.

[10] Q. Song, W. Yang, B. Zhao, S. Xu, H. Rao, and Z. Zhu, "Energy storage requirement reduction using negative voltage states of a full-bridge modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5243–5255, Jun. 2019, doi: 10.1109/tpel.2018.2869464.

[11] W. Lin, D. Jovcic, S. Nguefeu, and H. Saad, "Full-bridge MMC converter optimal design to HVDC operational requirements," *IEEE Trans. Power Del.*, vol. 31, no. 3, pp. 1342–1350, Jun. 2016, doi: 10.1109/TPWRD.2015.2475130.

[12] Y. Tang, M. Chen, and L. Ran, "A compact MMC submodule structure with reduced capacitor size using the stacked switched capacitor architecture," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6920–6936, Oct. 2016, doi: 10.1109/TPEL.2015.2511189.

[13] C. Zhao, Z. Wang, Z. Li, P. Wang, and Y. Li, "Characteristics analysis of capacitor voltage ripples and dimensioning of full-bridge MMC with zero sequence voltage injection," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 2106–2115, Sep. 2019, doi: 10.1109/JESTPE.2018.2878411.

[14] A. Nami, L. Wang, F. Dijkhuizen, and A. Shukla, "Five level cross connected cell for cascaded converters," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, 2013, pp. 1–9, doi: 10.1109/EPE.2013.6631941.

[15] G. P. Adam, I. Abdelsalam, J. E. Fletcher, G. M. Burt, D. Holliday, and S. J. Finney, "New efficient submodule for a modular multilevel converter in multiterminal HVDC networks," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4258–4278, Jun. 2017, doi: 10.1109/TPEL.2016.2603180.

[16] S. Heinig et al., "Implications of capacitor voltage imbalance on the operation of the semi-full-bridge submodule," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9520–9535, Oct. 2019, doi: 10.1109/TPEL.2018.2890622.

[17] K. Ilves, L. Bessegato, L. Harnefors, S. Norrga, and H. Nee, "Semi-full-bridge submodule for modular multilevel converters," in *Proc. 9th Int. Conf. Power Electron. ECCE Asia*, 2015, pp. 1067–1074, doi: 10.1109/ICPE.2015.7167913.

[18] X. Yu, Y. Wei, and Q. Jiang, "New submodule circuits for modular multilevel current source converters with DC fault ride through capability," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 1468–1474, doi: 10.1109/APEC.2016.7468062.

[19] W. Yang, Q. Song, S. Xu, H. Rao, and W. Liu, "An MMC topology based on unidirectional current H-bridge submodule with active circulating current injection," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3870–3883, May 2018, doi: 10.1109/tpel.2017.2722011.

[20] L. Hou, S. Zhang, Y. Wei, X. Li, and Q. Jiang, "A hybrid-arm modular multilevel converters topology with DC low voltage operation and fault ride-through capability for unidirectional HVDC bulk power transmission," *IEEE Trans. Power Del.*, vol. 35, no. 6, pp. 2812–2820, Dec. 2020, doi: 10.1109/TPWRD.2020.3005710.

[21] B. Li, S. Shi, D. Xu, and W. Wang, "Control and analysis of the modular multilevel DC de-icer with STATCOM functionality," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5465–5476, Sep. 2016, doi: 10.1109/TIE.2016.2554564.

[22] W. Yang, Q. Song, and B. Zhao, "Energy storage requirement and low capacitance operation of unidirectional current H-bridge modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 11748–11759, Dec. 2019, doi: 10.1109/TPEL.2019.2910456.

[23] K. Ilves, S. Norrga, L. Harnefors, and H.-P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 77–88, Jan. 2014, doi: 10.1109/TPEL.2013.2254129.

[24] M. Lu, J. Hu, R. Zeng, W. Li, and L. Lin, "Imbalance mechanism and balanced control of capacitor voltage for a hybrid modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5686–5696, Jul. 2018, doi: 10.1109/TPEL.2017.2743780.

[25] Z. Li, Q. Song, S. Xu, B. Zhao, Z. Yu, and R. Zeng, "Analysis and optimization of energy variations in MMCs with variable DC voltages," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14562–14574, Dec. 2022, doi: 10.1109/TPEL.2022.3186875.

[26] Z. Li et al., "Reduction in submodule capacitance in FB- and HYB-MMCs with variable DC voltages," *IEEE Trans. Ind. Electron.*, early access, Aug. 24, 2022, doi: 10.1109/TIE.2022.3199914.

[27] J. Li, X. Zhao, Q. Song, H. Rao, S. Xu, and M. Chen, "Loss calculation method and loss characteristic analysis of MMC-based VSC-HVDC system," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2013, pp. 1–6, doi: 10.1109/ISIE.2013.6563615.

[28] K. Ilves, L. Harnefors, S. Norrga, and H.-P. Nee, "Analysis and operation of modular multilevel converters with phase-shifted carrier PWM," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 268–283, Jan. 2015, doi: 10.1109/TPEL.2014.2321049.

[29] A. Hassanpoor, L. Ängquist, S. Norrga, K. Ilves, and H.-P. Nee, "Tolerance band modulation methods for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 311–326, Jan. 2015, doi: 10.1109/TPEL.2014.2305114.

[30] W. Li and J. Bélanger, "An equivalent circuit method for modelling and simulation of modular multilevel converters in real-time HIL test bench," *IEEE Trans. Power Del.*, vol. 31, no. 5, pp. 2401–2409, Oct. 2016, doi: 10.1109/TPWRD.2016.2541461.

[31] W. Li, "Real-time simulation of CDSM modular multilevel converter for HIL test applications," in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc.*, 2016, pp. 2372–2377, doi: 10.1109/IECON.2016.7793028.

Zhengxuan Li (Graduate Student Member, IEEE) was born in Beijing, China, in 1995. He received the B.S. degree in electrical engineering from North China Electric Power University, Beijing, in 2018. He is currently working toward the Ph.D. degree in electrical engineering with Tsinghua University, Beijing.

His current research interests include modular multilevel converter, and wind power and VSC-HVdc transmission systems.

Bojin Tang received the M.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2006.

He is currently with the Institute of Science and Technology, China Three Gorges Corporation, Beijing. He has long been engaged in on-site management of large-scale hydropower projects, technical management, and technological innovation of large-scale new energy projects. He is currently in charge of projects, such as the research and engineering application of key technologies, for grid connection of 10 million kilowatts of new energy, and the key technologies for a new generation of offshore wind power flexible dc transmission based on IGCT.

Qiang Song (Senior Member, IEEE) was born in Changchun, China, in 1975. He received the B.E.E. and Ph.D. degrees in electrical engineering from Tsinghua University, Beijing, China, in 1998 and 2003, respectively.

From 2003 to 2008, he was a Lecturer with the Department of Electrical Engineering, Tsinghua University. Since 2008, he has been an Associate Professor with the Department of Electrical Engineering, Tsinghua University. His research interests include high-power electronic interfaces for utility system, flexible ac transmission system, VSC-HVdc system, and custom power quality.

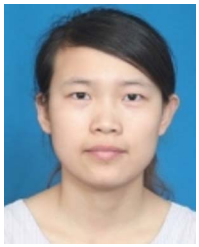
Lifeng Gou received the M.S. and Ph.D. degrees in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2015 and 2021, respectively.

He is currently with the Institute of Science and Technology, China Three Gorges Corporation, Beijing. His current research interests include electric drives and multilevel converters.

Biao Zhao (Senior Member, IEEE) was born in Hubei, China, in 1987. He received the B.S. degree from the Department of Electrical Engineering, Dalian University of Technology, Dalian, China, in 2009, and the Ph.D. degree from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 2014, both in electrical engineering.

He is currently an Associate Professor with the Department of Electrical Engineering, Tsinghua University, Beijing. His research interests include high-power converters, high-power semiconductor devices, and flexible dc transmission and distribution systems.

Dr. Zhao is a Senior Member of the Chinese Society for Electrical Engineering and the Chinese Electro-Technical Society.



Na Jia received the M.S. degree in electrical engineering from China University of Mining and Technology, Xuzhou, China, in 2008.

She is currently a Senior Engineer with the Institute of Science and Technology, China Three Gorges Corporation, Beijing, China. She has engaged in HVdc, ac/dc hybrid microgrid, and integrated energy. She is now promoting the research on offshore wind power.

Fang Cai He was born in Liaoning, China, in 1982. He is currently working toward the Eng.D. degree in electrical engineering with Tsinghua University, Beijing, China.

He is currently a Senior Engineer with Huairou Laboratory, Beijing. His current research interests include IGCT, dc circuit breaker, dc transformer, modular multilevel converter, wind power, and VSC-HVdc transmission systems.