Fractional-Order-Based Low-Order Harmonic Current Suppression Method Considering Asymmetrical Capacitor Parameters

Jingyu Zhang, Liangzong He, *Member, IEEE*, and Zhile Lin

***Abstract*—The problem of the second harmonic current (SHC) on the dc bus side of the single-phase inverter system has attracted widespread attention. The active power decoupling method based on dual capacitors can suppress SHC effectively. However, the asymmetrical capacitor parameters will deteriorate the SHC suppression performance and lead to the first-order harmonic current. To eliminate these low-order harmonic currents, this article proposes a SHC suppression method based on the fractional-order capacitor (FOC), where no power supply is employed and little loss is incurred. The capacitance and the order of the proposed FOC can, both, be adjusted. The principle and operating mode of the FOC are analyzed, and the control strategy of adjustment is given. The method can realize the SHC suppression with the advantages of a simple control strategy, hot-swappable, and high flexibility. Most importantly, the method can effectively suppress the first-order harmonic current caused by the asymmetrical parameters of the capacitors. Finally, an 800 W prototype based on the proposed method is built, and the simulation and experimental results both verify the effectiveness of the proposed method.**

***Index Terms*—Asymmetrical capacitor parameters, fractional-order capacitor (FOC), second harmonic current (SHC), single-phase inverter system.**

I. Introduction

In THE single-phase inverter system, the second harmonic current (SHC) appears on the dc side. Such current will increase the conduction loss [1], [2], reduce the efficiency of the power supply and shorten the life of the power supply [3], [4], [5], and influence the realization of maximum power point tracking [6].

In recent years, active power decoupling methods have been widely used in SHC suppression [7], [8], [9], [10], [11]. Where the dual capacitor-based method is the most promising [12], [13], [14], [15], [16], [17], [18], [19], [20]. However, to get a good SHC suppression performance, the two capacitors should be consistent with the theoretical parameter values. Unfortunately, there are no two identical capacitors in practice. Even if the initial values of the two capacitors are equal, the parameters may be shifted due to heat generation or aging. Capacitor parameters offset will reduce the absorption capability of secondary pulsating power. In addition, primary power will be generated in the harmonic suppression circuit, so that an additional first-order harmonic current will be introduced into the dc side [12]. The existence of the equivalent series resistance (ESR) of the capacitors may cause the power loss to reduce the performance of the SHC suppression.

Therefore, an improved scheme with the grid current feedback is proposed to reduce the low-order harmonic current caused by asymmetrical parameters of the capacitor [12]. But, it is limited to differential inverters only. An input current feedback method and a waveform control method are proposed for SHC suppression when the capacitance changes [13], [14]. Unfortunately, they should have the same capacitance values all the time. A rule-based controller can eliminate the effect of parameter asymmetry by optimizing control parameters [15]. By adding a closed-loop of the capacitor voltage reference based on the residual ripple voltage, the active power filter obtains the power regulation capability [16]. A variable capacitor is proposed to adapt to different capacitance requirements [17]. But methods in [15] and [16] can only compensate for the influence of capacitance. Moreover, a method in [17] can only adjust the capacitance to a smaller value. In [18], the power decoupling is realized by adding a decoupling control loop that modifies the voltages across the two-inverter arms with a compensation voltage. But, it increases the voltage stress of the switches. Tang et al. [19] proposed a dual voltage control strategy to compensate for the reference voltage in the harmonic suppression circuit, which improves the robustness of parameter deviation. However, the compensation margin is relatively small. The method of averaging the capacitor voltage distributes the effect of the parameters equally between the two capacitors, but can not eliminate the effect [20].

The abovementioned methods can solve the problem caused by asymmetrical capacitor parameters and the SHC can be well suppressed. However, the methods have several critical issues: 1) The capacitance and resistance cannot be adjusted

Manuscript received 5 July 2022; revised 28 September 2022; accepted 29 October 2022. Date of publication 8 November 2022; date of current version 26 December 2022. This work was supported in part by the National Natural Science Foundation of China under Grant 62071406 and in part by the Natural Science Foundation of Guangdong Province General under Grant 2021A1515011710. Recommended for publication by Associate Editor F. Freijedo. *(Corresponding author: Liangzong He.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3219880.

Digital Object Identifier 10.1109/TPEL.2022.3219880

synchronously. 2) Small adjustment margin. 3) Only on special application occasions.

Aiming at the abovementioned issues, this article proposes an SHC suppression method based on a fractional-order capacitor (FOC) for the symmetrical half-bridge structure. By constructing the FOC, the equivalent capacitance and ESRs of the two capacitors in the symmetrical half-bridge could be compensated to keep equal to each other. Even if the actual parameters of the capacitors are asymmetrical, the symmetrical half-bridge can still well suppress the SHC and the first-order harmonic current. The method is simple in theoretical calculation and easy to be implemented. And, it is suitable for SHC suppression occasions that require symmetrical capacitance parameters. The rest of this article is organized as follows. The principle of SHC suppression and the influence of asymmetrical capacitor parameters are presented in Section II. Section III introduces the concept and theoretical calculation of FOC construction. Section IV presents the principle of the SHC suppression circuit with FOC. Section V gives the parameter selection and shows the simulation and experimental results. Finally, Section VI concludes this article.

II. Principle of SHC Suppression and Influence of Asymmetrical Capacitor Parameter

A. Principle of SHC Suppression Based on Symmetric Half-bridge

In a single-phase inverter system, the output voltage u_o and current i_o can be written as

$$\begin{cases} u_o = U_o \sin \omega t \\ i_o = I_o \sin(\omega t + \theta). \end{cases} \tag{1}$$

And, the output power of the inverter is

$$p_o = p_{\rm dc} + p_{\rm 2nd} = \frac{U_o I_o}{2}\left[\cos\theta - \cos(2\omega t + \theta)\right] \tag{2}$$

where $p_{\rm dc}$ and $p_{\rm 2nd}$ represent the dc component and component twice the fundamental frequency, respectively. U_o and I_o represent the amplitude of the output voltage and current, respectively. θ is the phase of the output current and ω is the angular frequency. When the secondary pulsating power is fed back to the dc side, the bus current $I_{\rm bus}$ will contain SHC. Then, the current $I_{\rm bus}$ can be written as

$$I_{\rm bus} = I_{\rm dc} + I_{\rm 2nd} = \frac{U_o I_o \cos\theta}{2U_{\rm bus}} - \frac{U_o I_o \cos(2\omega t + \theta)}{2U_{\rm bus}} \tag{3}$$

where $I_{\rm dc}, I_{\rm 2nd}$, and $U_{\rm bus}$ represent the dc component current, the SHC and the voltage of the dc bus, respectively. The symmetrical half-bridge structure is shown in Fig. 1, which can be used to suppress the SHC. It is composed of switches S_a and S_b, capacitors C_1 and C_2, and inductor L_r. When the amplitude of the instantaneous power p_h in the symmetrical half-bridge circuit is equal to the secondary pulsating power $p_{\rm 2nd}$ and the phases are complementary, the SHC can be completely suppressed. From (2), $p_{\rm 2nd}$ can be written as

$$p_{\rm 2nd} = -\frac{U_o I_o}{2}\cos(2\omega t + \theta). \tag{4}$$

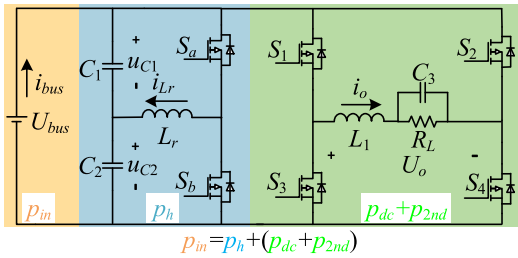

Fig. 1. Symmetrical half-bridge harmonic suppression circuit.

Ignoring the conduction loss and switching loss in the circuit, the instantaneous power of all energy storage elements in the symmetrical half-bridge circuit is

$$p_h = u_{C1}\cdot C_1\frac{du_{C1}}{dt} + u_{C2}\cdot C_2\frac{du_{C2}}{dt} + i_{Lr}\cdot L_r\frac{di_{Lr}}{dt} \tag{5}$$

where u_{C1} and u_{C2} represent the voltages of C_1 and C_2, respectively. i_{Lr} is the current of inductor L_r.

From [20], when $C_1 = C_2 = C$, the instantaneous voltage of u_{C1} and u_{C2} can be written as

$$\begin{cases} u_{C1} = \frac{U_{\rm bus}}{2} + u_h \\ u_{C2} = \frac{U_{\rm bus}}{2} - u_h \end{cases} \tag{6}$$

where $u_h = U_h \sin(\omega t + \beta)$. U_h and β represent the amplitude and phase of u_h, respectively. And, the relationship of U_h and β is satisfied as follows:

$$\begin{cases} U_h = \sqrt{\frac{U_o I_o}{2\omega C}} \\ \beta = \frac{\pi}{4} + \frac{\theta}{2}. \end{cases} \tag{7}$$

Consequently, the bus current $I_{\rm bus}$ only contains dc components, and the SHC is eliminated. When the load impedance angle θ changes in (-π, π], the modulation phase β changes correspondingly.

B. Influence of Asymmetrical Capacitor Parameters

Through the analysis in Section II, u_h is easily obtained from (7). But it requires equal capacitance of C_1 and C_2 with no ESR. However, in practice, the maximum tolerance for capacitance may reach up to $\pm$20% [12], [19]. As a result, the actual p_h will have a deviation from the theoretical value. In this case, the SHC cannot be well suppressed. And ESR also brings adverse effects on harmonic suppression. The specific analysis is as follows.

Considering that the ESRs of C_1 and C_2 are, respectively, R_1 and R_2, the voltages of the capacitors u_1 and u_2 can be written as

$$\begin{cases} u_1 = \frac{U_{\rm bus}}{2} + u_h \\ u_2 = \frac{U_{\rm bus}}{2} - u_h. \end{cases} \tag{8}$$

Then, the capacitive and resistive components of the u_{C1} yields

$$\begin{cases} u_{C1} = \frac{\frac{1}{j\omega C_1}}{R_1 + \frac{1}{j\omega C_1}} u_1 \\ u_{R1} = \frac{R_1}{R_1 + \frac{1}{j\omega C_1}} u_1. \end{cases} \tag{9}$$

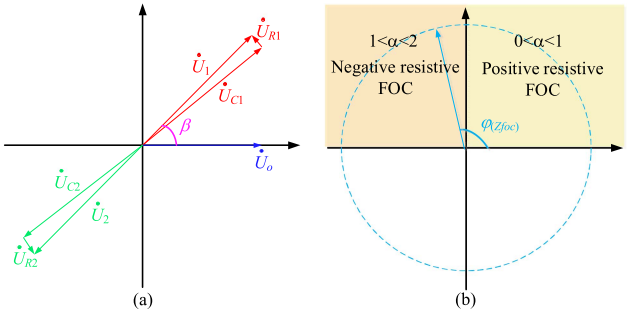

Fig. 2. (a) Phasor diagram of the voltages on C_1 and C_2. (b) Impedance-phase diagram of FOC.

Similarly, u_2 can also be written in the same form as (9). The phasor diagram of the voltages on C_1 and C_2 is shown in Fig. 2. Considering the ESRs, the instantaneous power of all energy storage elements in the symmetrical half-bridge branch can be derived as

$$p_h = u_{C1} \cdot C_1 \frac{du_{C1}}{dt} + \frac{u_{R1}^2}{R_1} + u_{C2} \cdot C_2 \frac{du_{C2}}{dt} + \frac{u_{R2}^2}{R_2} + i_{Lr} \cdot L_r \frac{di_{Lr}}{dt}. \tag{10}$$

Substituting (8) and (9) into (10), p_h can be expressed as

$$p_h = \frac{\omega U_h^2}{2} \left[\frac{C_1 \cos(2\omega t + 2\beta - \phi_1)}{(1 + j\omega R_1 C_1)^2} + \frac{C_2 \cos(2\omega t + 2\beta - \phi_2)}{(1 + j\omega R_2 C_2)^2} \right] + \frac{\omega U_{\text{bus}} U_h}{2} \left[\frac{C_1 \sin(\omega t + \beta - \phi_3)}{(1 + j\omega R_1 C_1)^2} - \frac{C_2 \sin(\omega t + \beta - \phi_4)}{(1 + j\omega R_2 C_2)^2} \right] + p_{\text{dc-loss}} \tag{11}$$

where $\tan\phi_1 = 1/\omega R_1 C_1$, $\tan\phi_2 = 1/\omega R_2 C_2$, $\tan\phi_3 = 2/\omega R_2 C_2$, and $\tan\phi_4 = 2/\omega R_2 C_2$, respectively. The rest of the analysis in this article is carried out under the assumption that R_1 and C_1 remain unchanged while R_2 and C_2 are changed. The first item in (11) represents the instantaneous power of the capacitors to absorb the $p_{2\text{nd}}$ and the power loss caused by the ESRs, respectively. When the capacitance deviates, p_h will be less than $p_{2\text{nd}}$. As a result, the SHC cannot be well suppressed. The second item represents the first-order instantaneous power. When the parameters of the two capacitors are the same ($C_1 = C_2$ and $R_1 = R_2$), they become zero. Conversely, the first-order instantaneous power cannot be canceled, resulting in first-order harmonic current on the dc bus. The last item $p_{\text{dc-loss}}$ represents the dc power loss of the ESRs. Therefore, the asymmetrical ESRs and capacitance will cause the first-order harmonic current on the dc side and reduce the maximum absorption capacity of the secondary pulsating power.

To overcome the issues caused by asymmetrical capacitor parameters, this article employs a FOC to compensate for this deviation. Hence, (7) is still applicable as the capacitor reference voltage when the parameters are asymmetrical. In theory, the SHC suppression performance with the FOC will be the same as the symmetrical parameters. Particularly, the first-order harmonic current will no longer appear on the dc bus.

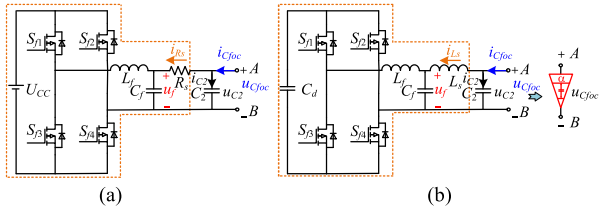

Fig. 3. FOC circuits. (a) Traditional FOC circuit. (b) Improved FOC circuit.

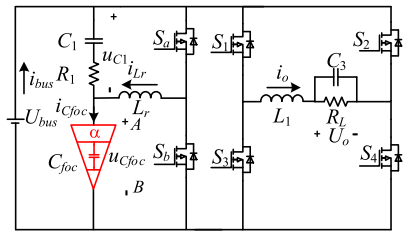

Fig. 4. SHC suppression circuit with FOC.

III. Concept and Theoretical Calculation of FOC

A. Concept of FOC

Fractional calculus has been used in power electronics to build a fractional-order circuit to improve the performance of the systems [21], [22], [23].

The voltage-current relationship of the first-order capacitor can be expressed as

$$i_C = C \frac{du_C(t)}{dt}. \tag{12}$$

And when the order is α, the voltage-current relationship of the capacitor is

$$i_C = C_\alpha \frac{d^\alpha u_C(t)}{dt^\alpha} \tag{13}$$

where α is the order and d^α/dt^α is termed the fractional-order derivative operator. C_α is the equivalent capacitance. Extending the traditional capacitor impedance expression to fractional order, the impedance expression of the FOC can be written as

$$Z = \frac{1}{\omega^\alpha C_\alpha} \cos(0.5\pi\alpha) - j \frac{1}{\omega^\alpha C_\alpha} \sin(0.5\pi\alpha) \tag{14}$$

where ω is the operating angular frequency of FOC. When α or ω changes, the equivalent capacitance and ESR may be changed accordingly. The impedance vector diagram of FOC is shown in Fig. 3. When α is $0<\alpha<2$, FOC can be grouped into positive or negative resistive FOC.

The traditional fractional-order capacitor circuit is shown in Fig. 4(a). The input port AB can be equivalent to a voltage source u_{Cfoc}. The impedance of port AB can be adjusted by regulating

the voltage u_f to achieve fractional impedance characteristics. And u_f is controlled by a voltage single closed-loop to adjust the compensated current i_{Rf}. The impedance of port AB can be adjusted by regulating the voltage u_f to achieve fractional impedance characteristics. So, port AB can be equivalent to FOC, which can be viewed as C_2 connected in parallel with a current source i_{Rf}. However, the structure has two critical issues: 1) Resistor R_f causes additional power loss. 2) An applied voltage source is required to achieve negative resistance characteristics.

Replacing the resistor with an inductor can avoid introducing power loss and using a capacitor as the energy source can solve the problem of the voltage source. Especially for symmetrical half-bridge structures, u_{C2} is controlled by S_a and S_b and contains both dc and ac components. The ac components can be used for power decoupling, while the dc component can be used for charging the energy storage capacitor. The improved FOC circuit proposed in this article is shown in Fig. 4(b). C_{foc} consists of an inverter and the C_2 in the symmetrical half-bridge. Like the traditional structure, the inverter can be viewed as a current source i_{Ls} and port AB can be equivalent to FOC. C_d is the storage capacitor for the inverter and u_f is the output voltage of the inverter. L_f, C_f, and L_s are the filter inductor, filter capacitor, and the inductor for voltage matching, respectively. i_{Ls} and i_{Cfoc} are the compensated current and port current of FOC, respectively. i_{C2} is the actual current of C_2. And u_{Cfoc} is the port voltage of C_{foc}, which is the same as u_{C2}. The improved FOC does not introduce extra loss and requires no additional voltage source to realize negative characteristics.

B. Equivalent the Same Parameters as C_1

From the analysis in Section II, u_{C1} and u_{C2} have the same amplitudes, and their phases are complementary (180° out of phase). When the parameters of C_2 are the same as C_1, the currents i_{C1} and i_{C2} should also have the same amplitudes and 180° out of phase. By adjusting the amplitude of i_{Cfoc} and i_{C1} to be the same, the same parameters of C_{foc} and C_1 can be achieved.

Transforming (14) through Euler's formula, the desired current of FOC can be expressed as

$$i_{Cfoc} = (j\omega)^{\alpha} C_{\alpha} u_{Cfoc} = -i_{C1}. \tag{15}$$

The current of capacitor C_2 can be written as

$$i_{C2} = j\omega C_2 u_{Cfoc}. \tag{16}$$

Then, the current compensated by fractional part can be derived as

$$i_{Ls} = i_{Cfoc} - i_{C2}. \tag{17}$$

The output voltage u_f of the inverter should be the sum of the port voltage of FOC and voltage on L_s. It yields

$$u_f = u_{Cfoc} + u_{Ls} = u_{Cfoc} - (i_{C1} + i_{C2})\, j\omega L_s. \tag{18}$$

Therefore, keeping $u_{Cfoc}(u_{C2})$ unchanged, u_{Cfoc} and i_{Cfoc} can exhibit fractional-order impedance characteristics by regulating the amplitude and phase of u_f. The C_{foc} can be equivalent to a C_α connected in series with an R_α. By controlling C_{foc} to have the same impedance characteristics as C_1, the problem caused by the asymmetrical parameters can be solved. The symmetrical half-bridge SHC suppression circuit with FOC is shown in Fig. 5.

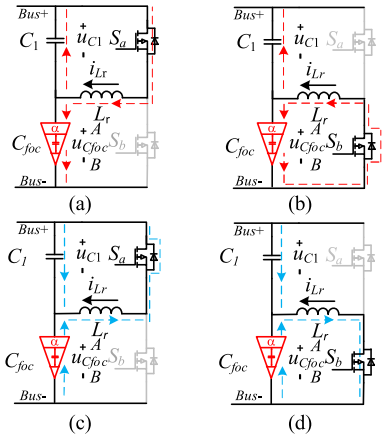

Fig. 5. Operation modes of harmonic suppression circuit with FOC. (a) Mode I, i_{Lr}>0. (b) Mode II, i_{Lr}>0. (c) Mode I, i_{Lr}<0. (d) Mode II, i_{Lr}<0.

C. Maintain the DC Bias Value of C_d

When FOC is activated, to absorb the secondary pulsation power completely, the energy provided by FOC in one line voltage period can be written as

$$Q_{Cfoc} = C_1 \Delta u_{Cfoc} = 2C_1 U_h \tag{19}$$

where Δu_{Cfoc} is the variation of u_{Cfoc} for line voltage. When FOC is inactivated, the energy provided by C_2 in one line voltage period can be written as

$$Q_{C2} = C_2 \Delta u_{C2} = 2C_2 U_h \tag{20}$$

where Δu_{C2} is the variation of u_{C2} for line voltage. The energy difference ΔQ is

$$\Delta Q = 2\Delta C U_h \tag{21}$$

where ΔC is the tolerance between C_2 and C_1. To maintain U_{Cd}, The energy variation of C_d in a line voltage period should be equal to ΔQ. It yields

$$C_d \Delta U_{Cd} = \Delta C U_h \tag{22}$$

where ΔU_{Cd} is the amplitude of the ripple on C_d. By reasonable values of C_d and ripple requirements, FOC can simultaneously equivalent the same parameters as C_1 and maintain the dc bias value of C_d.

IV. Principle of SHC Suppression Circuit With FOC

A. SHC Suppression Mechanism of the Symmetrical Half-Bridge Circuit With FOC

From the abovementioned analysis, by regulating C_α and R_α as the parameters of C_1, the first-order component in (11) can be eliminated. Therefore, it can be regarded as the case of the symmetrical parameter to perform power decoupling calculation.

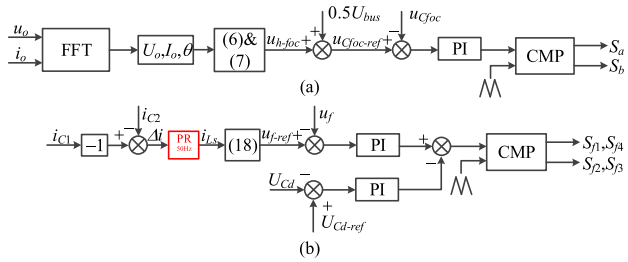

Fig. 6. System control block diagram. (a) Control block diagram of SHC suppression. (b) Parallel double closed-loop control block diagram of FOC.

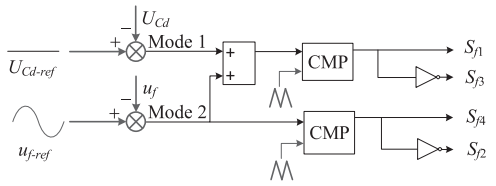

Fig. 7. The control logic of fractional-order part inverter.

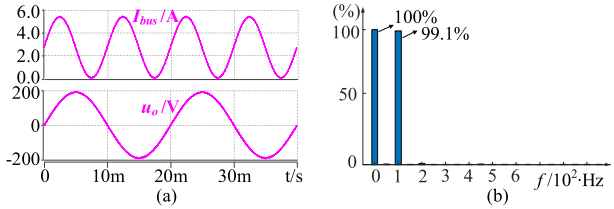

Fig. 8. Simulation results when the SHC suppression circuit is inactivated. (a) Key waveforms. (b) Fourier analysis of $I_{\rm bus}$.

Like the symmetrical parameters, when the p_h is equal to the $p_{2\rm nd}$ in amplitude and opposite in phase, the SHC can be completely suppressed and has no first-order harmonic current. Consequently, the bus current $I_{\rm bus}$ only contains dc components. Furthermore, the FOC part does not affect the modulation of u_{Cfoc}, which is determined by the output power and the load impedance angle θ. When the secondary pulsating power changes, u_{Cfoc} also changes to suppress the SHC. By regulating the amplitude and phase of u_f, impedance matching can still be achieved.

Since the inverter output in the fractional-order part contains secondary power, there is voltage fluctuation on the capacitor C_d. The amplitude of voltage fluctuation depends on the compensated power. The more serious the parameter deviation is, the greater the fluctuation is. But, it does not influence the SHC suppression or the characteristics of FOC.

B. Modal Analysis of the Symmetrical Half-Bridge Circuit With FOC

During a switching operation period, the symmetric half-bridge circuit with FOC can be divided into two operating modes, as shown in Fig. 6.

Mode I: S_a is turned ON and S_b is turned OFF. When $i_{Lr}>0$, as shown in Fig. 6(a), the dc bus charges L_r and C_{foc} through S_a. As a result, i_{Lr} increases in the positive direction, and u_{Cfoc} rises. When $i_{Lr}<0$, as shown in Fig. 6(c), L_r and C_{foc} feedback energy to the dc bus through the body diode of S_a. As a result, i_{Lr} decreases in the negative direction, and u_{Cfoc} drops.

Mode II: S_a is turned OFF and S_b is turned ON. When $i_{Lr}>0$, as shown in Fig. 6(b), L_r charges C_{foc} through the body diode of S_b, As a result, i_{Lr} decreases in the positive direction, and u_{Cfoc} rises. When $i_{Lr}<0$, as shown in Fig. 6(d), C_{foc} charges L_r through S_b. As a result, i_{Lr} increases in the negative direction, and u_{Cfoc} drops.

C. Control Strategy of the Symmetrical Half-Bridge Circuit With FOC

The control block diagram of the symmetrical half-bridge circuit with FOC is shown in Fig. 7. The control block diagram of SHC suppression is shown in Fig. 7(a). By sampling output voltage u_o and current i_o and Fourier analysis, U_o, I_o, and θ can be obtained. According to (6) and (7), the reference voltage $u_{Cfoc\text{-}ref}$ can be calculated. The PI compensator is used to follow $u_{Cfoc\text{-}ref}$. In one switching operation period, the driving signals of S_a and S_b are complementary.

The FOC part is based on the original voltage single closed-loop control, adding a parallel voltage closed loop. The parallel double closed-loop control block diagram of FOC, as shown in Fig. 7(b), aims to stabilize the voltage U_{Cd} of capacitor C_d and make the C_{foc} have the same characteristics as C_1. From (15), the reference current $i_{Cfoc\text{-}ref}$ can be easily obtained by flipping the sampled i_{C1} (multiply it by -1). Making a difference between i_{C1} and i_{C2}, the difference current Δi can be obtained. The proportional resonator with a bandwidth of 10 Hz is used to extract the fundamental component (50 Hz) to obtain the compensated current i_{Ls}. According to (18), the reference output voltage $u_{f\text{-}ref}$ of the inverter in the fractional-order part can be calculated. Then, $u_{f\text{-}ref}$ is compared with u_f. And, the error signal is sent to the PI compensator to generate the switch control signal.

To realize the abovementioned two control targets simultaneously, the converter of the fractional-order part operates in two modes. Mode 1 is the charging mode. The capacitor C_d is charged through S_{f1}, S_{f3} and the body diode of S_{f4} as a boost circuit to stabilize the voltage U_{Cd}. Mode 2 is the FOC mode. It works as an inverter to provide compensation for current i_{Ls}. Fig. 8 shows its control principle. In Mode 1, the reference voltage is a dc voltage of $U_{Cd\text{-}ref}$ for S_{f1} and S_{f3}, while in Mode 2 is the voltage of $u_{f\text{-}ref}$, which is a sine wave for all switches. In a switching operation period, both modes exist simultaneously to ensure the energy balance in the C_d.

V. Simulation and Experimental Results

A. Parameter Selection

From the analysis in Section III, C_1 and C_2 in the symmetrical half-bridge circuit both have dc components. And the larger the amplitude of the ac components U_h is, the more secondary pulsation power can be absorbed by the circuit. But, the increase of U_h is limited by the dc bus voltage.

TABLE I
PARAMETERS OF SIMULATION AND EXPERIMENT

Parameters/ Specification	Value	Parameters/ Specification	Value
U_{bus}	300V	L_r	120μH
U_{Cd}	300V	L_s	330μH
U_o	200V	L_1/L_f	2.5mH
R_L	25Ω	C_3/C_f	4.7μF
f_w	50Hz	C_d	330μF
f_k	10kHz	R_s	0.5Ω
Case	**Capacitance of C_1/C_2**		**ESRs of C_1/C_2**
Case A	220μF/220μF		0.432Ω/0.392Ω
Case B	220μF/220μF		0.432Ω/0.892Ω
Case C	220μF/187μF		0.432Ω/0.920Ω

When the capacitance of C_1 and C_2 are equal, U_h reaches the maximum amplitude

$$U_h \leq \frac{1}{2}U_{\text{bus}}. \tag{23}$$

Therefore, when U_h is equal to half of the dc bus voltage, it reaches the maximum secondary pulsation power absorption capacity, which can be written as

$$\omega C U_h^2 = \frac{U_o I_o}{2} = p_{2\text{nd}}. \tag{24}$$

Then, the minimum capacitance of C_1 and C_2 can be given from (7) as

$$C_{\min} = \frac{2U_o I_o}{\omega U_{\text{bus}}^2}. \tag{25}$$

To reduce the influence of the resonance between L_r and C_2, the resonance frequency should be 19 times larger than the line frequency. And according to the ripple index of GB/T 14549 93, each content of the first 19 harmonics can not exceed 4%. So the maximum inductance of L_r yields

$$L_{r-\max} = \frac{1}{(38\pi f_w)^2 C_2} \tag{26}$$

where f_w is the operating frequency of the inverter. For the inverter in the fractional-order part, the capacitance of C_d can be given from (22) as

$$C_d \geq \Delta C \frac{U_h}{\Delta U_{Cd}}. \tag{27}$$

The voltage of C_d should be higher than the magnitude of its output voltage u_f, so the minimum value of U_{Cd} should satisfy

$$U_{Cd-\min} > (u_{Ls} + u_{Cfoc})_{\max}. \tag{28}$$

To prove the feasibility of the proposed method, simulations and experiments are performed. The parameters of simulation and experiment are shown in Table I. f_k is the switching frequency of all switches.

B. Simulation Results

Fig. 9 shows the bus current I_{bus} and the output voltage u_o when the SHC suppression circuit is inactivated. From the Fourier analysis of I_{bus}, the SHC content is 99.1% relative to the dc component and there is no first-order harmonic current.

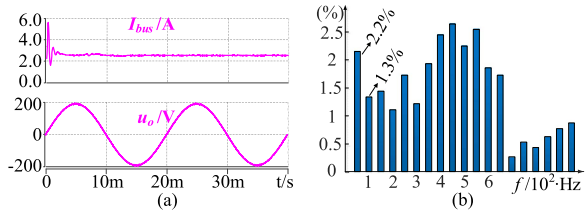

Fig. 9. Simulation results when the SHC suppression circuit is activated under case A parameter. (a) Key waveforms. (b) Fourier analysis of I_{bus}.

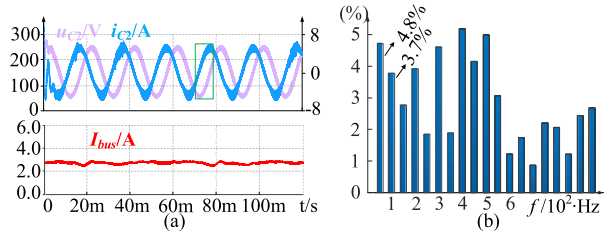

Fig. 10. Simulation results when FOC is not employed under case B parameter. (a) Key waveforms. (b) Fourier analysis of I_{bus}.

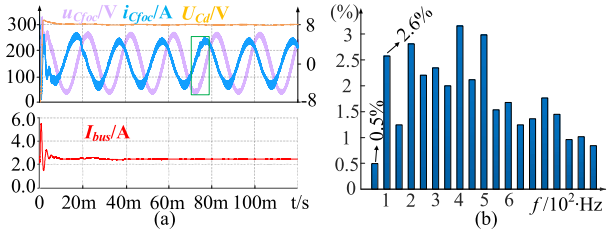

Fig. 11. Simulation results when FOC is employed under case B parameter. (a) Key waveforms. (b) Fourier analysis of I_{bus}.

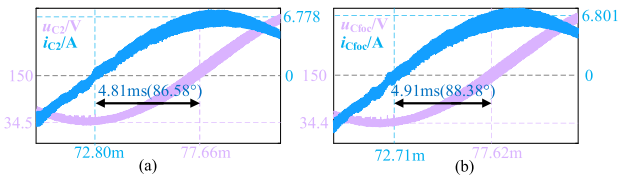

Fig. 12. Zoomed-in simulation phase relationship of u_{C2}, i_{C2} and u_{Cfoc}, i_{Cfoc}. (a) Simulation phase relationship of u_{C2}, i_{C2}. (b) Simulation phase relationship of u_{Cfoc}, i_{Cfoc}.

The simulation results under the case A parameter are shown in Fig. 10 when the SHC suppression circuit is activated. The SHC is reduced to (2.2%), but an additional first-order harmonic current (1.3%) appears, due to the slight parameter difference between C_1 and C_2.

To make the effect of asymmetrical ESRs relatively obvious, R_s of 0.5 Ω is introduced. The simulation results under the case B parameter are shown in Fig. 11 when the FOC is not employed. The SHC is reduced from 99.1% to 3.7%, and the first-order harmonic current in I_{bus} increases to 4.8%. The simulation results under the case B parameter are shown in Fig. 12 when the FOC is employed. The SHC is reduced from 99.1% to 2.6%, and the first-order harmonic current is reduced to 0.5% relative

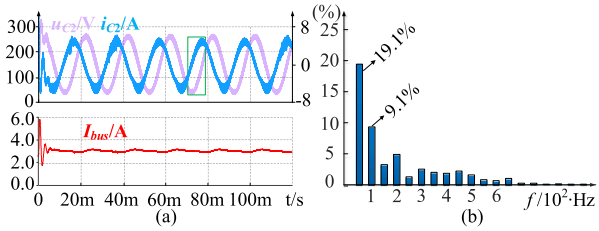

Fig. 13. Simulation results when FOC is not employed under case C parameter. (a) Key waveforms. (b) Fourier analysis of $I_{\rm bus}$.

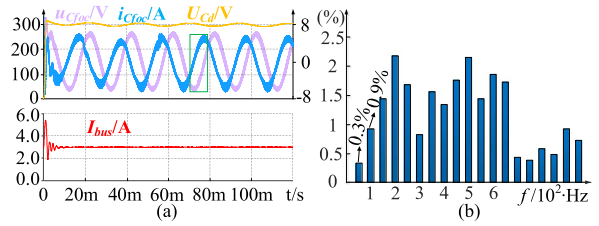

Fig. 14. Simulation results when FOC is employed under case C parameter. (a) Key waveforms. (b) Fourier analysis of $I_{\rm bus}$.

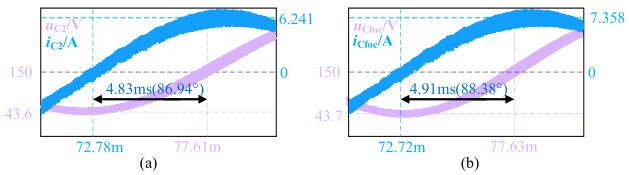

Fig. 15. Zoomed-in simulation phase relationship of u_{C2}, i_{C2} and u_{Cfoc}, i_{Cfoc}. (a) Simulation phase relationship of u_{C2}, i_{C2}. (b) Simulation phase relationship of u_{Cfoc}, i_{Cfoc}.

to the dc component. The voltage of C_d is about 300 V and there is just a little fluctuation on U_{Cd} because the effect of asymmetrical ESRs is light, and the power to be compensated is relatively small. Fig. 13 is an enlarged view of the green mark in Figs. 11 and 12, which represents the phase relationship between the voltages and currents on the capacitors. The phase difference between the voltage and current of C_2 (connected in series with R_s) is about 86.58°, while the C_{foc} is about 88.38°, which is the same as the expected value (the impedance angle of C_1, 88.37°).

Case C parameter is used to verify that the FOC proposed in this article can adjust both capacitance and ESR. The simulation results under the case C parameter are shown in Fig. 14 when the FOC is not employed. The bus current $I_{\rm bus}$ fluctuates obviously. From the Fourier analysis results, $I_{\rm bus}$ not only contains 19.1% of the first-order harmonic current but also has 9.1% of the SHC. The simulation results under the case C parameter are shown in Fig. 15 when FOC is employed. The SHC is reduced to 0.9%, and the first-order harmonic current is reduced to 0.3% relative to the dc component. The voltage of energy storage capacitor C_d is about 300 V and there are large fluctuations on U_{Cd} because the power that needs to be compensated for the asymmetrical capacitance is relatively more. Fig. 16 is an enlarged view of the green mark in Figs. 14 and 15 to represent the phase relationship between the voltages and currents on the capacitors. The phase

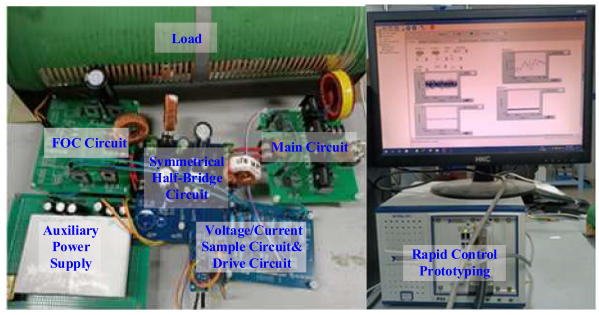

Fig. 16. Experimental prototype.

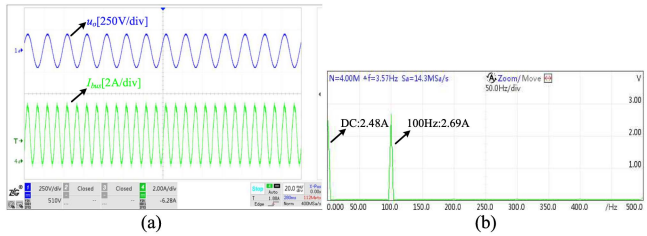

Fig. 17. Experimental results when SHC suppression circuit is inactivated under case A parameter. (a) Key waveforms. (b) Fourier analysis of $I_{\rm bus}$.

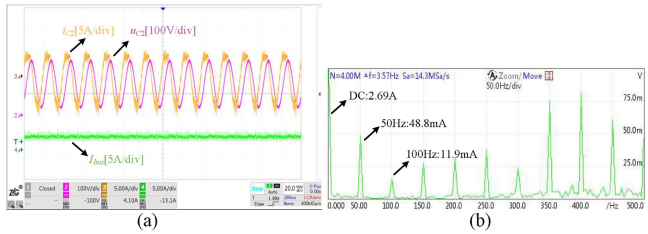

Fig. 18. Experimental results when SHC suppression circuit is activated under case A parameter. (a) Key waveforms. (b) Fourier analysis of $I_{\rm bus}$.

difference between the voltage and current of C_2 (connected in series with R_s) is about 86.94°, while the C_{foc} is about 88.38°, which is the same as the expected value (the impedance angle of C_1, 88.37°).

C. Experimental Results

The experiment parameters are the same as the simulation shown in Table I. And, the experimental prototype is shown in Fig. 17. The experimental results under the case A parameter are shown in Fig. 18 when the SHC suppression circuit is inactivated. There is 108.47% of SHC relative to the dc component and no first-order harmonic current. The SHC content exceeding 100% is due to the parasitic inductance of the resistive load used in the experiment. The experimental results under the case A parameter are shown in Fig. 19 when the SHC suppression circuit is activated. The SHC is reduced from 91.29% to 0.44%. And there is only 1.81% of the first-order harmonic current. The results meet the requirements of harmonic suppression IEEE-519 ($\leq$4%).

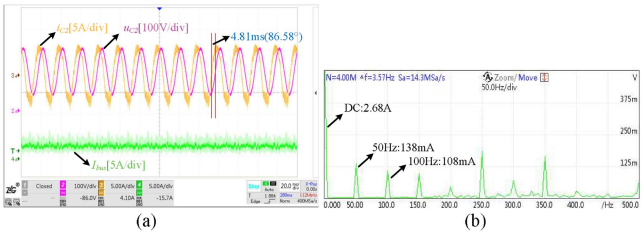

Fig. 19. Experimental results when FOC is not employed under case B parameter. (a) Key waveforms. (b) Fourier analysis of I_{bus}.

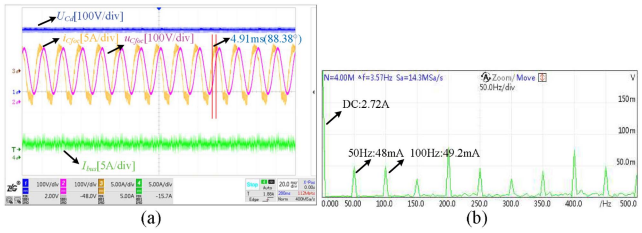

Fig. 20. Experimental results when FOC is employed under case B parameter. (a) Key waveforms. (b) Fourier analysis of I_{bus}.

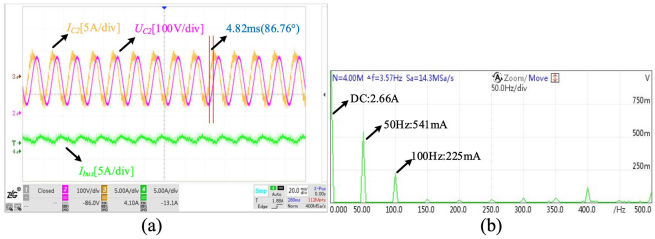

Fig. 21. Experimental results when FOC is not employed under case C parameter. (a) Key waveforms. (b) Fourier analysis of I_{bus}.

The experimental results under the case B parameter are shown in Fig. 20 when FOC is not employed. Compared to case A, the SHC increases to 4.03% and the first-order harmonic current increases to 5.15% relative to the dc component. The phase difference between the voltage and current of C_2 (connected in series with R_s) is 86.58°. The abovementioned experimental results show that as the deviation of the ESRs increases, the harmonic current suppression effect will become worse, increasing the residual SHC and causing the first-order harmonic current. The experimental results under the case B parameter are shown in Fig. 21 when FOC is employed. The SHC is reduced to 1.76% and the first-order harmonic current is reduced to 1.84% relative to the dc component. The first-order harmonic current and SHC have been significantly reduced, which is almost equivalent to that of symmetrical parameters. The voltage of C_d is about 300 V and there is a little fluctuation on U_{Cd}. The phase difference between u_{Cfoc} and i_{Cfoc} is about 88.38°, which is the same as the expected value (the impedance angle of C_1, 88.37°).

The experimental results under the case C parameter are shown in Fig. 22 when FOC is not employed. I_{bus} fluctuates obviously. The SHC is 8.46%, and the first-order harmonic

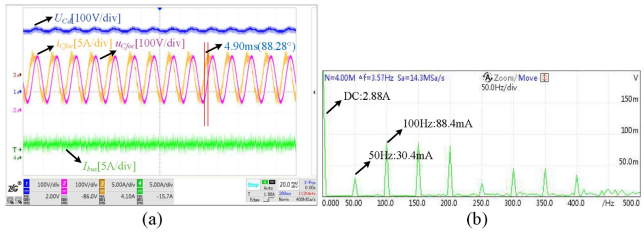

Fig. 22. Experimental results when FOC is employed under case C parameter. (a) Key waveforms. (b) Fourier analysis of I_{bus}.

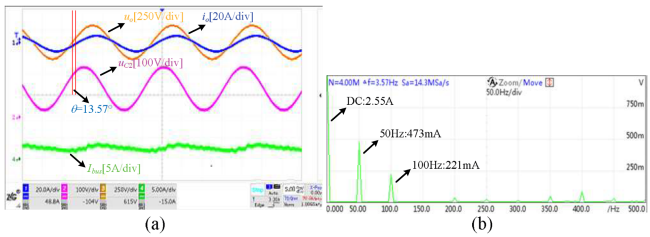

Fig. 23. Experimental results when FOC is not employed under case C parameter. (a) Key waveforms. (b) Fourier analysis of I_{bus}.

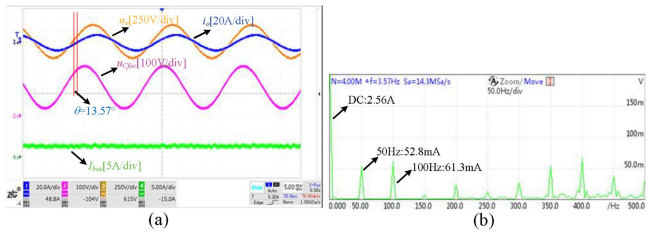

Fig. 24. Experimental results when FOC is employed under case C parameter. (a) Key waveforms. (b) Fourier analysis of I_{bus}.

current is 20.34%, which can no longer meet the requirements of harmonic suppression. The phase difference between the voltage and current of C_2 (connected in series with R_s) is 86.88°. The experimental results under the case C parameter are shown in Fig. 23 when FOC is employed. The first-order harmonic current content is reduced to 0.5%, and the SHC is reduced to 1.68%. The voltage of C_d is about 300 V and there are obvious fluctuations in U_{Cd}. And the phase difference between u_{Cfoc} and i_{Cfoc} is about 88.28°, which is the same as the expected value (the impedance angle of C_1, 88.37°).

To verify the feasibility of the proposed method at different ac power factors, a resistive-inductive (RL) load (a 25 Ω resistor series with a 19 mH inductor) is employed. The experimental results under the case C parameter are shown in Fig. 24 when FOC is not employed. The power factor angle θ is about 13.57°. The SHC content is 8.63% and the first-order harmonic current content is 18.55% relative to the dc component. The experimental results under the case C parameter are shown in Fig. 24 when FOC is employed. The power factor angle θ is about 13.57°. The SHC content is 2.39% and the first-order harmonic current content is 2.06% relative to the dc component.

TABLE II
PERFORMANCE COMPARISON OF HARMONIC CURRENT SUPPRESSION

Paper	Power level/output voltage	Capacitance compensation	ESR compensation	Compensation margin	Switching Frequency	1st harmonic	2nd harmonic
[10]	1kW/156V	N	N	N	19.2kHz	/	<3.8%
[12]	2.2kW/230V	Y	N	12μF/60μF	10kHz	0.49%	<1%
[14]	20W/40V	Y	N	6μF/60μF	20kHz	4.8%	3.4%
Proposed	800W/200V	Y	Y	33 μF/220μF 0.488Ω/0.432Ω	10kHz	0.5%	1.68%

The abovementioned experimental results verify that FOC can compensate both the capacitance and ESR to solve the problem caused by asymmetrical parameters. And, the proposed method is suitable for loads with different ac power factors.

Table II shows the performance comparison of parameter deviation between the proposed method and other power decoupling methods. The "compensation margin" means the maximum compensation ability defined as the ratio of the maximum offset capacitance/ESR to the theoretical value. In [10], a traditional symmetrical half-bridge circuit is employed to suppress the SHC. This method can suppress the second harmonic effectively, but it does not consider the possible effect of capacitor asymmetry parameters in practice. In [12], an improved power decoupling scheme considering the mismatch in storage capacitance is proposed. It can suppress the SHC and first-order harmonic current when the capacitance are asymmetrical. However, this method can only compensate for a middle deviation of capacitance (about 12 μF/60 μF) and be used for differential inverters. In [14], an input current feedback method is proposed, which is not affected by the capacitance tolerances. But, its compensation is relatively small, only 10% of the maximum capacitance (about 6 μF/60 μF). In this article, when the parameters of the capacitor are changed, FOC can compensate for both capacitance and ESR by a relatively large compensation (at least 33 μF/220 μF and 0.488 Ω/0.432 Ω). In addition, this method does not depend on the specific topology. In other applications, the capacitance and resistance also can be adjusted only by reconstructing the target capacitor into a FOC to solve the problem of asymmetrical parameters.

VI. CONCLUSION

Aiming at the dual-capacitor SHC suppression method, this article analyzes the influence on harmonic suppression when the capacitance and parasitic resistances of the capacitors are asymmetrical. And then, a fractional-order capacitor with adjustable capacitance and resistance to solve the problem caused by asymmetrical capacitor parameters is proposed. When the actual capacitor parameters are asymmetrical, the simulation and experimental results verify that the proposed method compensates for the capacitor parameters by adjusting the impedance characteristics of FOC. While effectively suppressing the SHC, no additional first-order harmonic current is introduced to the dc side. And since the FOC is completely composed of nondissipative components, in theory, no additional power loss will be incurred.

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