Fixed Switching Frequency Hybrid Modulation With ZVS for Single-Phase Inverter

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***Abstract*—Soft switching technology is an effective way to reduce the switching loss of the single-phase inverter to improve efficiency. Because of the ease of implementing soft switching, inverter works in boundary conduction mode (BCM) is widely used. On the contrary, BCM causes wide variation in switching frequency and large inductor current ripple. In this article, a fixed switching frequency hybrid modulation method for the inverter is proposed, which can achieve zero-voltage switching without changing the switching frequency and reduce the peak value of inductor current. The modulation achieves good tracking of the output current with different loads by switching mode between the triangular mode and the trapezoidal mode accurately. For implementing modulation, the operation states of the inverter with different conditions are analyzed in detail, the number of operation states is deduced and the state machine about mode switching is summarized. In addition, a single-phase inverter prototype is designed to verify the feasibility and effectiveness of the proposed modulation. Compared with BCM, the efficiency of the inverter at both light load and full load is increased.**

***Index Terms*—Fixed switching frequency, hybrid modulation, single-phase inverter, zero-voltage switching (ZVS).**

I. Introduction

SINGLE-PHASE inverter is one of the most common dc/ac converters, which are widely used in power amplifiers, motor drives, photovoltaic inverters, and so on [1], [2], [3]. Due to the development of wide band-gap semiconductors, the upper limit of switching frequency has been increased, enabling inverters to have lower costs and higher power density [4]. However, for nonisolated converters, such as buck converter and full-bridge converter, affected by the filter inductor and output current, part of power switches cannot transfer the charge on the parasitic capacitor during the dead time, which are in a hard-switching state. As the switching frequency increases, the switching loss also increases, resulting in a serious drop in efficiency. In order to reduce switching loss, many single-phase inverter soft-switching topologies and modulation methods have been proposed by researchers [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27].

In terms of topology, in most soft-switching topologies of inverter, resonant circuit and auxiliary power switches are always playing important roles in circuits, which are used to create the zero-voltage or zero-current conditions for power switches [5], [6], [7], [8], [9], [10], [11], [12]. Compared with additional auxiliary power switches, resonant circuit composed by passive components has less driving circuit, less degree of freedom, and less control complexity of the inverter. Among them, a full bridge converter with the auxiliary LC resonant circuit is proposed creatively in [13], as shown in Fig. 1(b). The converter can spontaneously separate the fundamental frequency current and the high frequency current in the filter inductor through the resonant circuit. The loop for the fundamental frequency current i_{ff} and the high frequency current i_{hf} are shown in Fig. 1(c) and (d). The i_c is the reverse current required to achieve zero-voltage

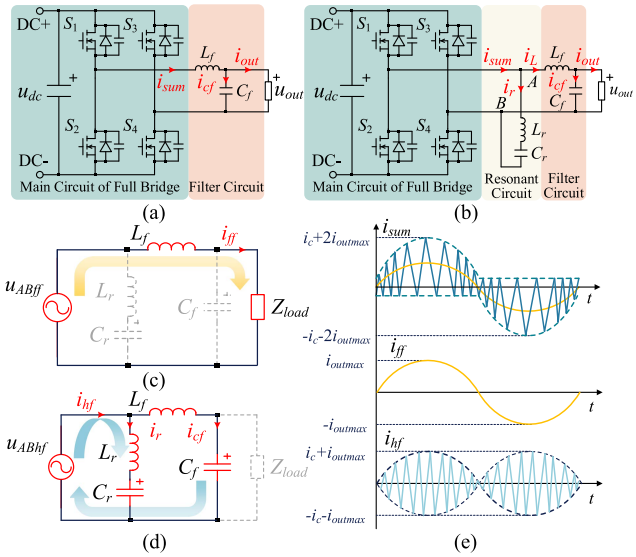

Fig. 1. (a) Topology of conventional full-bridge inverter. (b) Topology of full-bridge inverter with auxiliary resonant circuit. (c) Loop of fundamental frequency current. (d) Loop of high frequency current. (e) Current waveforms of i_{sum}, i_{ff}, and i_{hf}.

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switching (ZVS). The resonant capacitor C_r prevents the passage of fundamental frequency current. By a suitable design, i_{hf} flows mainly through the resonant inductor L_r, reducing the current stress on L_f. Compared with the conventional full-bridge converter, the peak value and loss of the filter inductor current are reduced significantly, which allows the converter to obtain higher efficiency [13], [14]. On the other hand, the size of the filter inductor L_f can be reduced significantly, and both the resonant inductor and filter inductor can be optimized separately. Therefore, the addition of resonant circuits does not significantly affect the power density of the converter [13], [14], [15]. Another advantage is that the original modulation methods, such as SPWM and BCM, can still be used without additional control and vice versa. In summary, the full bridge converter with the auxiliary LC resonant circuit is selected as the main circuit topology in this article.

In terms of modulation, the boundary conduction mode (BCM) has been widely studied because of its simplicity and ease of implementation [16], [17], [18], [19], [20], [21], including critical conduction mode (CRM) and triangular current mode (TCM). In BCM, the inductor current is large enough to change the polarity of the current in each switching cycle to achieve the ZVS of the power switches. Compared with CRM that requires the dc bus voltage to be higher than twice the maximum output voltage, TCM does not have strict requirements for dc voltage [22]. In BCM, the switching frequency changes in a wide range within a fundamental frequency period [13], which increases the difficulty of passive components. Although ZVS technology avoids the turn-ON loss of the power switches, the turn-OFF loss still exists, which is mainly determined by the drain-source current at the turn-OFF moment and the switching energy [23], [24]. When the average value of the inductor current is around zero, the switching frequency is very high, which causes high turn-OFF loss [25]. In order to reduce the range of switching frequency, many modulation methods have been proposed by scholars to optimize that, such as changing the operating current threshold or using different modulations according to the instantaneous value of the output current [25], [26], [27], [28], [29]. At the same time, affected by the inductor current ripple, the peak value of the inductor current is about twice the maximum value of the output current. Therefore, the conduction loss of the elements, the core loss of the inductor, and the turn-OFF loss are further increased. In this article, a fixed switching frequency hybrid modulation (FSFHM) with ZVS is proposed. As the output current changes, the inverter will switch between triangular mode and trapezoidal mode to reduce the range of switching frequency and reduce the peak value of the inductor current.

The rest of this article is arranged as follows. In Section II, the working principle of triangular mode and trapezoidal mode is introduced, and the influence of different load characteristics on inductor current is analyzed in detail. In addition, the switching process between different modes is described in detail. In Section III, the sequence of different modes in a fundamental frequency period is analyzed. The switching conditions of different modes and the number of modes in a fundamental frequency period with different loads are derived. The arrangement

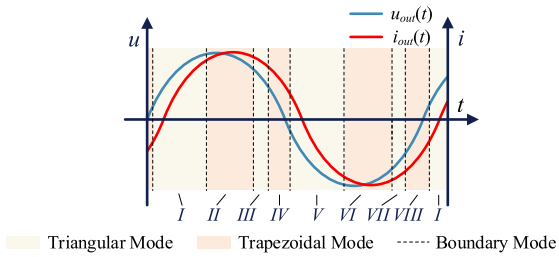


Fig. 2. Operation mode of the inverter in a fundamental frequency.

characteristics of different modes are summarized. The state machine is proposed to control the inverter to work in the appropriate mode. In Section IV, the control scheme of the FSFHM and the flow chart of software are introduced. Finally, a single-phase ZVS inverter prototype is designed. The experiment proves the feasibility and correctness of the proposed modulation method.

II. FSFHM With ZVS

In the conventional BCM, the inverter works in unipolar or bipolar modulation. When the inductor current reaches the upper or lower limit of the reference value, the switching state of the inverter will change. Affected by the output voltage and output current, the switching frequency of the inverter in BCM is variable. Different from the modulation method in the BCM that only uses the instantaneous value of the inductor current to determine the switching state. The fix switching frequency hybrid modulation calculates the duty of different levels by the instantaneous value of the output voltage and output current.

The FSFHM has two main modes, triangular mode and trapezoidal mode. Depending on the instantaneous value of output voltage and output current, different modes are used along the fundamental frequency cycle. As the boundary of triangular mode and trapezoidal mode, boundary mode plays an important role in switching mode. In a fundamental frequency cycle, as the output current changes, the inverter's operation mode is shown in Fig. 2. The default load is resistive-inductance load.

A. Triangular Mode

In the triangular mode, the full-bridge converter only outputs two levels in a switching cycle. When the output voltage is positive, the full-bridge inverter outputs the positive level and the zero level. Otherwise, the inverter outputs the negative level and the zero level.

In order to achieve ZVS, i_{sum} needs to change to the action current threshold $-i_c$ or i_c within each switching cycle, the current waveform of the i_{sum} is shown in Fig. 3.

Taking into account the symmetry of the sine wave, the default output voltage is positive in the analysis in this section. The analysis of the negative half-cycle can be deduced by analogy.

As shown in Fig. 3, in the triangular positive mode, the inverter first outputs the positive level, and the current i_{sum} starts to rise from zero. When the hold time of the positive level reaches t_1, the inverter outputs the zero level. Because the output voltage is

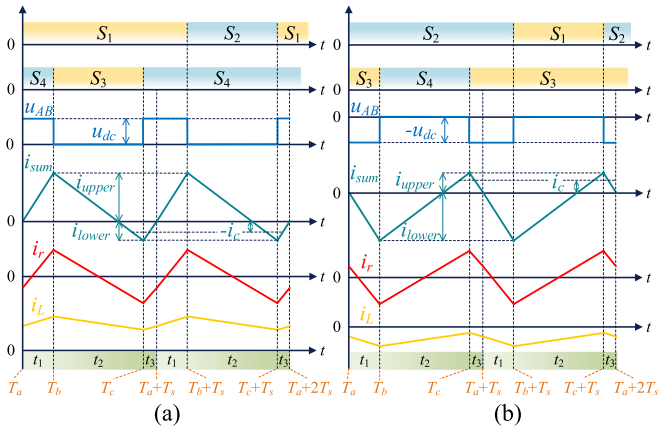


Fig. 3. Key waveforms of inverter in triangular mode. (a) Voltage and current waveforms in triangular positive mode. (b) Voltage and current waveforms in triangular negative mode.

positive, the current i_{sum} begins to fall. And after the hold time of zero level reaches t_2, the inverter outputs the positive level again until the end of the switching cycle.

According to the volt-second balance and average inductor current, the time t_1 and t_3 of positive level and the time t_2 of zero level can be expressed as follows:

$$\begin{cases} (u_{dc} - u_{out}(t)) \times (t_1 + t_3) - u_{out}(t)t_2 = 0 \\ \frac{1}{T_s}\int_{t_0}^{t_0+T_s} i_{sum}(t)dt = i_{out}(t) \end{cases} \tag{1}$$

where T_s is switching period. The voltages of the filter capacitor and the resonant capacitor are almost the same. And the impedance of both is negligible at the switching frequency. So the slope of the current $i_{sum}(t)$ can be expressed as follows:

$$\begin{cases} k_{isum}(t) = \frac{u_{AB}(t) - u_{out}(t)}{L_{eq}} \\ i_{sum}(t) = \int_{t_0}^{t_0+T_s} k_{isum}(t)dt \end{cases} \tag{2}$$

where L_{eq} is the equivalent inductor, equal to L_rL_f /(L_r+L_f). Since the switching frequency of the inverter is much higher than the fundamental frequency, it can be considered that the output voltage $u_{out}(t)$ does not change within one switching cycle. Substituting (2) into (1) can solve for the time of each level. And t_1, t_2, and t_3 can be expressed as follows:

$$\begin{cases} t_1 = \frac{u_{out}(t)}{2u_{dc}}T_s + \frac{L_{eq}i_{out}(t)}{u_{dc} - u_{out}(t)} \\ t_2 = \frac{u_{dc} - u_{out}(t)}{u_{dc}}T_s \\ t_3 = \frac{u_{out}(t)}{2u_{dc}}T_s - \frac{L_{eq}i_{out}(t)}{u_{dc} - u_{out}(t)} \end{cases} . \tag{3}$$

i_{upper} and i_{lower} in Fig. 3 represent the upper and lower of i_{sum} in a switching cycle. In triangular positive mode, i_{upper} and i_{lower} increase with the increase of $i_{out}(t)$. When i_{lower} rises to the action threshold current $-i_c$ or i_{upper} drops to i_c, the triangular positive mode is in the limit state.

The intervals t_1, t_2, and t_3 in triangular negative mode can be derived similarly.

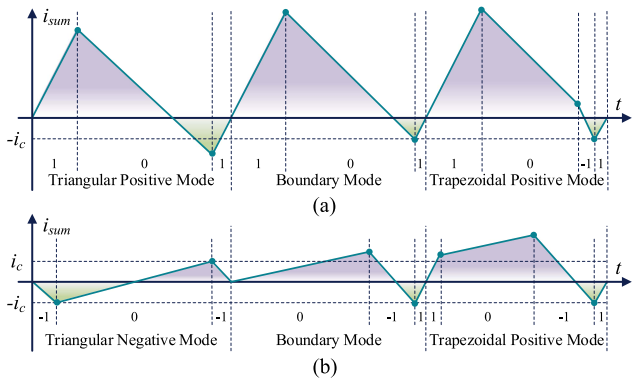


Fig. 4. Key waveforms of inverter in trapezoidal mode. (a) Trapezoidal positive mode when $u_{out}(t)$ is positive. (b) Trapezoidal positive mode when $u_{out}(t)$ is negative. (c) Trapezoidal negative mode when $u_{out}(t)$ is negative. (d) Trapezoidal negative mode when $u_{out}(t)$ is positive.

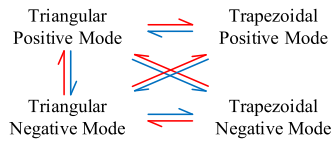


Fig. 5. Switching path of the operation mode.

B. Trapezoidal Mode

In the trapezoidal mode, the full-bridge converter outputs the positive level, the zero level, and the negative level. Affected by the instantaneous value of the output voltage and output current, the trapezoidal mode has a total of four voltage and current waveforms shown in Fig. 4.

Different from the triangle mode, the switching sequence of the trapezoidal mode is determined by the positive and negative of the output current. When the output current is positive, the inverter works in the trapezoidal positive mode, which outputs the positive level, the zero level, the negative level, and the positive level in sequence. The switching sequence when the output current is negative can be similarly deduced.

In the trapezoidal positive mode, the inverter first outputs the positive level, and the current i_{sum} starts to rise from zero. When the hold time of the positive level reaches t_1, the inverter outputs the zero level. Affected by the output voltage, the current i_{sum} has two possible changing trends in the zero level, namely rising and falling. After the hold time of zero level reaches t_2, the inverter outputs the negative and the current i_{sum} falls. When the hold time of the negative level reaches t_3, the current i_{sum} falls to the lower limit $-i_c$ at the same moment. At last, the inverter outputs the positive level again until the end of the switching cycle.

As can be seen in Fig. 4, in the trapezoidal positive mode, the addition of the negative level reduces the time for i_{sum} to drop to $-i_c$. The increase in the area of the positive trapezoid increases the average value of i_{sum}. At the same time, compared with changing the zero level in the triangular positive mode to the negative level directly, the zero level in the trapezoidal positive mode reduces the peak-to-peak value of the i_{sum}. By adjusting

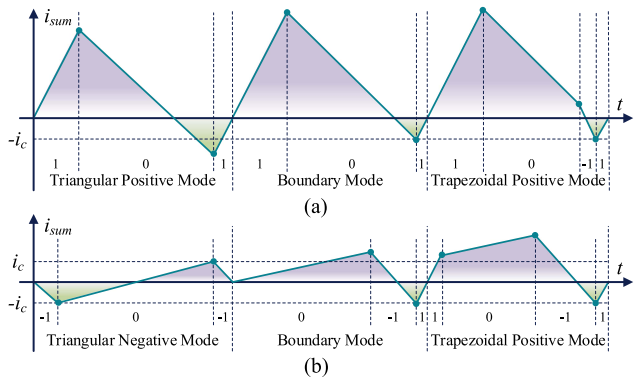


Fig. 6. Current waveforms during the switching process of operation mode. (a) Process of switching from the triangular positive mode to the trapezoidal positive mode. (b) Process of switching from the triangular negative mode to the trapezoidal positive mode.

the time of zero level and negative level, the switching frequency can be changed to realize fixed switching frequency modulation.

Similar to the previous analysis, the current i_{sum} and each interval t_1, t_2, t_3, and t_4 in trapezoidal positive mode can be expressed as follows:

$$\begin{cases} t_1 = \frac{u_{dc}+u_{out}(t)}{2u_{dc}} T_a - \frac{1}{2} t_2 \\ t_2 = \sqrt{\frac{u_{dc}^2-u_{out}^2(t)}{u_{dc}^2} T_a^2 - \frac{4L_{eq} i_{out}(t)}{u_{dc}} T_s - \frac{4L_{eq}^2 i_c^2}{u_{dc}^2-u_{out}^2(t)}} \\ t_3 = \frac{u_{dc}-u_{out}(t)}{2u_{dc}} T_a - \frac{1}{2} t_2 + \frac{L_{eq} i_c}{u_{dc}+u_{out}(t)} \\ t_4 = \frac{L_{eq} i_c}{u_{dc}-u_{out}(t)} \\ T_a = T_s - \frac{2L_{eq} u_{dc} i_c}{u_{dc}^2-u_{out}^2(t)} \end{cases} . \quad (4)$$

According to (4), as the output current i_{out} increases, the interval t_2 decreases. When t_2 reduces to zero, the inverter output current reaches its maximum with ZVS.

In trapezoidal negative mode, it is necessary to replace the positive level and the negative level with each other. The specific interval calculation is similar to (4).

C. Boundary Modes

As the current $i_{\mathrm{sum}}(t)$ changes, the operating mode of the inverter also changes. The switching path between different modes is shown in Fig. 5. When the inverter switches from one mode to another, the boundary mode will appear between the two modes. As the limit state of each mode, the boundary mode plays an important role in the process of smooth switching between different modes. According to the previous analysis, the circuit has four operation modes. And the trapezoidal positive mode and the trapezoidal negative mode cannot switch to each other directly, which is explained in Section III. The switching process of any two modes is reversible. So there are five switching processes in the boundary mode. At the same time, considering that the switching process from the triangular mode to the trapezoidal mode is similar. The following analyzes the switching process with the trapezoidal positive mode as the final mode.

The process of switching from the triangular positive mode to the trapezoidal positive mode is shown in Fig. 6(a). As the output current i_{out} increases, the lower limit of i_{sum} also increases. When the lower limit of i_{sum} reaches $-i_c$, the triangular positive mode reaches the limit state. In the next switching cycle, the output voltage of the inverter changes from two levels to three levels. The negative level is inserted between the zero level and the positive level. In this switching process, the boundary mode can also be considered as the trapezoidal positive mode with the negative level duty cycle is zero.

When the output voltage is negative and the output current changes from negative to positive, the inverter switches from triangular negative mode to trapezoidal positive mode. The specific process is shown in Fig. 6(b). In the last switching cycle of the triangular negative mode, the current waveform of the i_{sum} changes symmetrically, and the output current i_{out} is almost zero. Because the two triangles enclosed by the current and time axis have the same area, changing the order of the two triangles does not affect the average value of the i_{sum}. In the next switching cycle, the duty cycle of the first negative level of the triangular negative mode reduces to zero. In order to maintain the output current without sudden change, the duty cycle of the second negative level has been increased. At the end of the switching cycle, the positive level is added to make i_{sum} rise to zero. The boundary mode can also be considered as the trapezoidal negative mode with the positive level duty cycle is zero.

The switch from the triangular positive mode to the triangular negative mode only exists in the resistive load. When the output voltage and output current are zero at the same time, the zero level duty cycle is close to 1. And the slope of the current i_{sum} at the zero level is almost zero. This is the same as the waveform of the general SPWM modulation method at zero crossing.

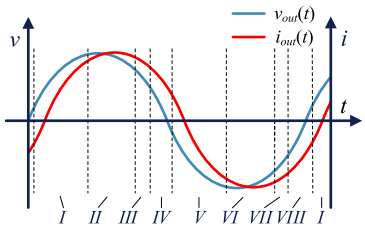
It can be seen from Fig. 6 that sometimes the current of MOSFETS in the boundary mode cannot reach the action current. This situation always happens when the output current crosses zero. In this situation, the inductor ripple current and the switching loss are small. On the other hand, it can be approximately considered that the MOSFETS realize zero-current switching.

III. Implemented Modulation

After confirming the switch states of each mode, it is necessary to arrange each mode reasonably. This section takes a fundamental frequency cycle as an example. The operation states of the inverter with different conditions are analyzed in detail. The relationship between the circuit parameters and the number of operation states is deduced. The state machine about mode switching is summarized to guide the subsequent control system design.

A. Operation State

When the load is resistive-inductive, the inverter has eight operation states at most in a fundamental frequency cycle, as shown in Fig. 7. When the output voltage is zero as the starting point of the fundamental frequency cycle. The operation states are analyzed as follows.



Triangular Positive Mode: *I & III* Trapezoidal Positive Mode: *II & IV*
Triangular Negative Mode: *V & VII* Trapezoidal Negative Mode: *VI & VIII*

Fig. 7. Operation modes of the inverter in a fundamental frequency with resistive-inductive load ($R = 20\ \Omega$, $L = 2.4$ mH, $f_{out} = 200$ Hz).

State *I*: During this state, the inverter works in triangular positive mode. The output voltage of the inverter is positive and the output current is from negative to positive. Limited by the output voltage, the triangular negative mode cannot be used. Because the output current is small, the inverter does not work in trapezoidal mode.

State *II*: During this state, the increase in output current makes the inverter switch to the trapezoidal positive mode. The output voltage and output current of the inverter are both positive.

State *III*: During this state, the inverter return to the triangular positive mode like state *I*.

State *IV*: As the output voltage decreases, the slope of the i_{sum} at zero level becomes smaller. This causes the inverter to enter the trapezoidal positive phase mode even though the current is also decreasing. At the end of this state, the output voltage is negative, the output current is positive and the current value is large. So the inverter does not enter other modes due to the change in output voltage.

Because of the symmetry of the sine wave, the analysis of states *V–VIII* is similar to that of states *I–IV*. This article does not discuss it in detail. When the load is a resistive load or a resistive-capacitive load, the operation state of the inverter can also be determined by a similar method.

B. Details of States

The operation state of the inverter with resistive-inductive load is deduced earlier. In fact, with the change of load parameters, there are at least two operation states of the inverter and eight at most.

According to the analysis of the boundary mode in Section II, the inverter starts the new mode because the current mode cannot meet the ZVS condition, which can be expressed as $t_1 \leq 0$ or $t_3 \leq 0$ in (4). Considering that the output current amplitude is much larger than the action current i_c. To simplify the analysis, assuming that $i_c = 0$, the switching conditions in the positive half-cycle can be expressed as follows:

$$\begin{cases} \frac{u_{dc}+u_{out}(t)}{2u_{dc}}T_s \leq \frac{1}{2}\sqrt{\frac{u_{dc}^2-u_{out}^2(t)}{u_{dc}^2}T_s^2 - \frac{4L_{eq}i_{out}(t)}{u_{dc}}T_s} \\ \frac{u_{dc}-u_{out}(t)}{2u_{dc}}T_s \leq \frac{1}{2}\sqrt{\frac{u_{dc}^2-u_{out}^2(t)}{u_{dc}^2}T_s^2 - \frac{4L_{eq}i_{out}(t)}{u_{dc}}T_s} \end{cases}. \quad (5)$$

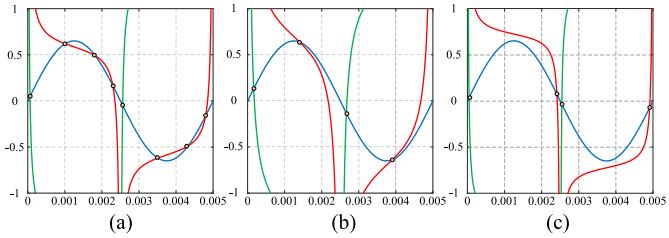


Fig. 8. Curves and intersections with different conditions. (a) $\varphi = 15°$, $L_{eq}/Z_{load}T_s = 0.21$. (b) $\varphi = 45°$, $L_{eq}/Z_{load}T_s = 0.21$. (c) $\varphi = 15°$, $L_{eq}/Z_{load}T_s = 0.14$.

After simplifying (5), the inequality can be rewritten as follows:

$$\begin{cases} m\sin\omega t \leq -1 - \frac{2L_{eq}}{Z_{load}T_s}(\cos\varphi - \cot\omega t\sin\varphi) \\ m\sin\omega t \leq 1 - \frac{2L_{eq}}{Z_{load}T_s}(\cos\varphi - \cot\omega t\sin\varphi) \end{cases} \quad (6)$$

where m represents the degree of modulation, which is the ratio of the output voltage amplitude to the dc voltage. ω is the output angular frequency. Z_{load} is the impedance of the load, and φ represents the impedance angle. Therefore, the moment of mode switching is the moment when the equation is established in (6). Combined with the switching conditions of the negative half-cycle, all switching moments t_{switch} can be expressed as follows:

$$\begin{cases} f_1(t) = m\sin\omega t \\ f_2(t) = sign(\omega t)\left[1 - \frac{2L_{eq}}{Z_{load}T_s}(\cos\varphi - \cot\omega t\sin\varphi)\right] \\ f_3(t) = -sign(\omega t)\left[1 + \frac{2L_{eq}}{Z_{load}T_s}(\cos\varphi - \cot\omega t\sin\varphi)\right] \\ t_{switch} = \{t|\, f_1(t) = f_2(t) \vee f_1(t) = f_3(t)\} \end{cases}. \quad (7)$$

Therefore, the t_{switch} can always be determined by the intersection of the modulating wave and the other two curves. According to (7), f_1 (blue curve) is only affected by the degree of modulation. f_2 (red curve) and f_3 (black curve) are affected by the impedance angle φ and parameter $L_{eq}/Z_{load}T_s$. Three curves can be drawn as shown in Fig. 8. It can be seen from Fig. 8 that with the condition that the degree of modulation is constant, the number of operation modes of the inverter in a fundamental frequency cycle changes with the change of the impedance angle φ and parameter $L_{eq}/Z_{load}T_s$.

To better describe the relationship among the different parameters, the quantitative relationship among the impedance angle, parameter $L_{eq}/Z_{load}T_s$ and the number of state is shown in Fig. 9. As shown in Fig. 9, with resistive loads, the number of states can only be 2 or 6. Under resistive-inductive loads or resistive-capacitive loads, the number of states is 4 or 8. As the phase difference between the output voltage and output current increases, the duration of states *II* and *IV* in Section III-A becomes longer. And the duration of state *III* becomes shorter until it reaches zero. It is worth mentioning that the disappearance of state *III* connects the two states adjacent to it. The original three states become one state. It is the direct reason that affects the number of states. Similar to the impedance angle, the parameter

TABLE I
SEQUENTIAL CHANGES OF THE OPERATION STATES IN A FUNDAMENTAL FREQUENCY CYCLE WITH DIFFERENT LOADS

	Trapezoidal positive mode (1)	Triangular positive mode (2)	Trapezoidal positive mode (3)	Triangular positive mode (4)	Trapezoidal positive mode (5)	Trapezoidal negative mode (6)	Triangular negative mode (7)	Trapezoidal negative mode (8)	Triangular negative mode (9)	Trapezoidal negative mode (10)
$\varphi>0$	×	√	√ *or* ×	√ *or* ×	√	×	√	√ *or* ×	√ *or* ×	√
$\varphi=0$	×	√	√ *or* ×	√	×	×	√	√ *or* ×	√	×
$\varphi<0$	√	√ *or* ×	√ *or* ×	√	×	√	√ *or* ×	√ *or* ×	√	×

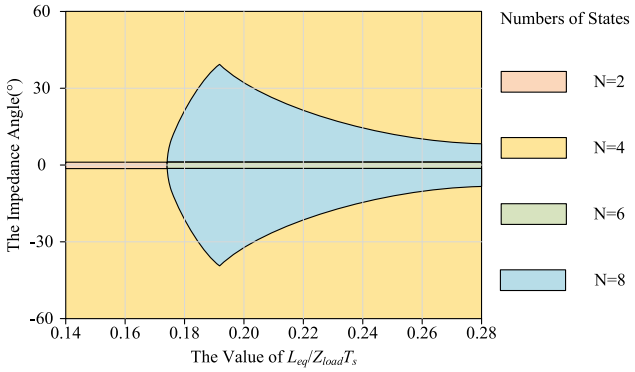


Fig. 9. Relationship among the number of operation states, the impedance angle, and the value of the parameter.

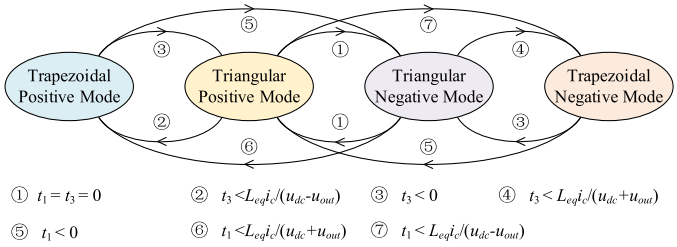


Fig. 10. State machine of the FSFHM.

$L_{eq}/Z_{load}T_s$ affects the duration of states *I–III*. When state *II* disappears, the number of states will also change.

According to the above-mentioned analysis, the sequential changes of the operation states in one fundamental frequency cycle, starting from the output voltage of zero, are shown in Table I. Some of the operation states will not occur due to the parameters of the inverter. For example, under the resistive-capacitive load, i.e., $\varphi>0$, the first operation state of the inverter must be the triangular positive mode. The two uncertain operation states in the negative half-cycle are also recorded in Table I.

C. State Machine

In addition to the number and the order of states, the duty of different states is also very important to the inverter. However, the amount of calculation to accurately calculate the duty of each state is large in FSFHM. From the previous analysis, it can be known that in any switching cycle, there is only one operation mode that can achieve ZVS without affecting the output waveforms. For the parallel controller, four modes can be calculated together. The result of suitable mode can make t_1, t_2, and t_3 all greater than zero. For serial controllers, the calculation of the four modes greatly increases the burden on the controller. The state machine can simplify the calculation of the controller.

Similar to the analysis in Section II of the boundary mode, when the current mode is difficult to follow the output current, the inverter switches to another mode. No matter in triangle mode or trapezoidal mode, the zero level time t_2 is always larger than zero. Unless the circuit has reached the maximum output current, which cannot be solved by switching modes. When the positive level time or the negative level time drops below the threshold, the inverter switches operation mode. The specific state machine is shown in Fig. 10.

IV. CONTROLLER IMPLEMENTATION AND PARAMETERS DESIGN

A. Controller Implementation

Both the voltage loop and the current loop of the inverter adopt *PI* control to achieve good tracking of the reference waveform. Different from the variable switching frequency modulation, because of the fixed switching frequency, the current sampling link does not need to be very sensitive to capture the zero-crossing time of the current i_{sum}. Through controlling the sampling time of the ADC, the voltage and current values at the beginning of the switching cycle can always be collected. The current value of the i_{sum} at this moment reflects its deviation from zero, which affects the average current of filter inductor in the switching cycle. The state machine and the duty of each level have been introduced in Sections II and III. After obtaining the mode and duty, the logic circuit cooperates with the timer to output different levels at a suitable time. Finally, the pulses sent by the controller are amplified by the drive circuit to realize the control of the power circuit. The specific control scheme is shown in Fig. 11.

In terms of filter design of the sampling circuit, all of dc voltage, output voltage and output current use a low-pass filter (LPF) to filter out the switching ripple. The design of the filters' cut-off frequency needs to consider the existence of the double-frequency ripple in the dc bus of the single-phase inverter. For the sampling circuit of i_{sum}, the method through *Rogowski* coil or predictive control has been introduced in detail in [25] and [30]. The current sampling circuit in this article is shown in Fig. 12. Combined with the main frequencies of the current in the i_{sum}, the LPF and the band-pass filter can be used to achieve noise suppression and effective current sampling.

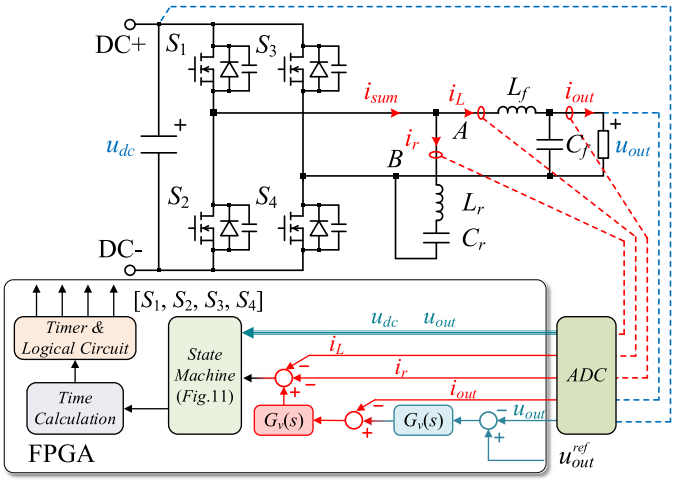


Fig. 11. Control scheme of the inverter in FSFHM.

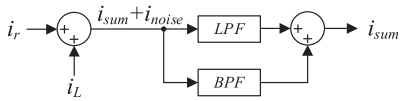


Fig. 12. Schematic diagram of current sampling circuit.

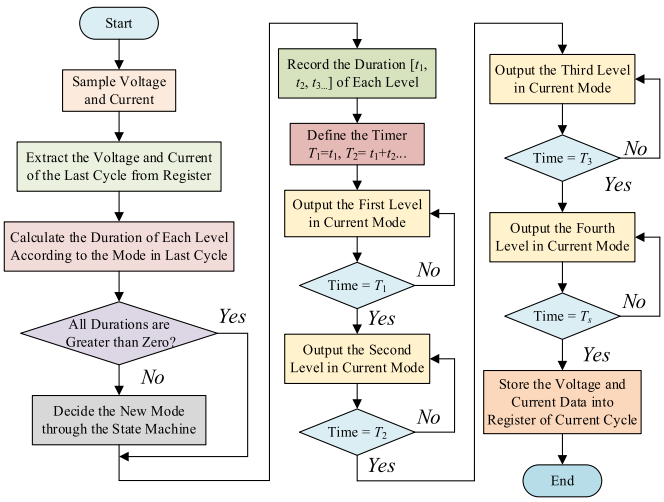


Fig. 13. Flow chart of the proposed FSFHM.

In the switching cycle, the flow chart of the controller is shown in Fig. 13. The controller needs the voltage and current values at the beginning of the switching cycle to calculate the duty. But the ADC needs conversion time, which affects the driving signal transmission. Therefore, the control system uses the sampling value of the previous cycle during calculation. The sampling value of the current cycle is stored in the register after the ADC conversion is completed, waiting for the next cycle to use. The controller first defaults that the operation mode of the circuit remains unchanged in adjacent cycles, and judges the calculation result. If the calculation results are suitable and valid data, no further processing is done. Instead, the controller switches to the new mode according to the state machine and

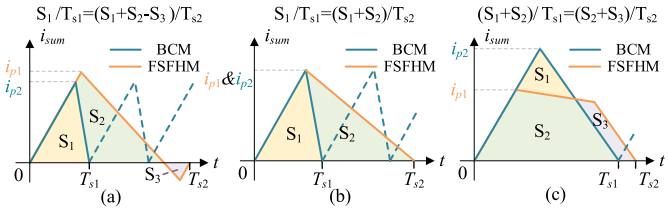


Fig. 14. (a) Current waveforms of i_{sum} in BCM and triangular positive mode. (b) Current waveforms of i_{sum} in BCM and boundary mode. (c) Current waveforms of i_{sum} in BCM and trapezoidal positive mode.

recalculates. Finally, different levels are output in turn according to the calculation results.

B. Comparison of Current Stress

In terms of stress, the voltage of the power switches remains unchanged at u_{dc}. On the contrary, the current stress of the power switches changes. The current waveforms of i_{sum} in different operating modes are shown in Fig. 14. To simplify the analysis, the action current i_c is temporarily ignored and the output voltage and output current are assumed to be positive. i_{p1}, i_{p2} are the peak currents of i_{sum} in FSFHM and BCM.

To fix the switching frequency, the peak current of i_{sum} in triangular mode is larger than that in BCM, which increases the conduction loss of the power switches at low output current. According to the average current model, the peak current of i_{sum} in boundary mode equals to that in BCM. At high output current, inverter works in trapezoidal mode. Compared with BCM, the addition of the zero level in FSFHM maintains the switching frequency and reduces the peak current. The duration of the zero level can be approximated based on (4) as follows:

$$t_2 \approx \sqrt{\frac{u_{dc}^2 - u_{out}^2(t)}{u_{dc}^2 f_{sw}^2}\left(1 - \frac{f_{sw}}{f_{BCM}}\right)} \tag{8}$$

where f_{sw} and f_{BCM} are the switching frequencies of FSFHM and BCM, respectively. From (1), it can be seen the zero level exists when the f_{sw} is lower than the minimum of the f_{BCM}. In the other words, when f_{sw} is lower than f_{BCM}, the peak current of FSFHM is always less than that of BCM. According to the energy equation of the inductor $E(t) = LI^2(t)/2$, the lower peak current reduces the maximum magnetic energy of the inductor. So the size and loss of the core can also be reduced. In summary, the FSFHM increases the current RMS of the power switches as influenced by the triangular mode. On the other hand, the peak current of the power switches decrease, which affects both the volume of the inductor and the core loss. Because the filter inductor passes almost only the fundamental frequency current. According to KCL, the current RMS of the power switch also rises.

C. Parameters Design

In order to achieve ZVS over the entire fundamental frequency cycle, inequality (9) should hold. When the duration of the zero level in trapezoidal mode is 0, the two sides of the inequality are

exactly equal.

$$\frac{2L_{eq}i_{out\max}}{u_{dc}-u_{out\max}}+\frac{2L_{eq}i_{out\max}}{u_{dc}+u_{out\max}}\le\frac{1}{f_{sw}}. \tag{9}$$

At the determined switching frequency, the equivalent inductor L_{eq} in the inverter can be expressed as follows:

$$L_{eq}\le\frac{u_{dc}^2-u_{out\max}^2}{4u_{dc}i_{out\max}f_{sw}}. \tag{10}$$

Assuming that the inductance of the filter inductor is k times that of the resonant inductor, each of the two inductors can be expressed as follows:

$$\begin{cases}L_f=(k+1)L_{eq}\\ L_r=(k+1)L_{eq}/k\end{cases}. \tag{11}$$

Ideally, k should be a large enough positive number to achieve complete separation of the fundamental frequency current and high frequency current. In practical application, the filter circuit can take on part of the high frequency current, which is absorbed by the filter capacitor. On the other hand, the peak current also affects the volume of the resonant inductor. As a tradeoff, the high frequency current ripple of the inductor current is generally limited to within 40% of the rated current of the filter inductor [13], which can be expressed as follows:

$$\Delta i_{Lf}\le\frac{2i_{out\max}}{k+1}\le 40\%i_{out\max}. \tag{12}$$

After simplifying (12), we can obtain k should greater than 4. Considering the margin, this article takes k equal to 6. The inductance of filter inductor and resonant inductor can also be determined. In order to filter out high frequency harmonics, the cut-off frequency of the output filter is designed as follows [31]:

$$10f_{out\max}\le f_{cutoff}\le f_{sw}/2 \tag{13}$$

where $f_{out\max}$ is the maximum output frequency. According to (13), the range of values of the filter capacitor can be expressed as follows:

$$\frac{1}{(\pi f_{sw})^2L_f}\le C_f\le\frac{1}{(20\pi f_{out\max})^2L_f}. \tag{14}$$

For resonant capacitor, the fundamental frequency current through them is limited to 1% of the output current for a good blocking of the fundamental frequency current.

$$C_r\le\frac{i_{out\max}}{200\pi f_{out\max}u_{out\max}}. \tag{15}$$

Meanwhile, the voltage of the resonant capacitor should not vary excessively to prevent it from affecting the current of the resonant inductor, with the design equation derived in [13].

$$C_r\ge\frac{5i_{out\max}}{4\pi^2f_{sw}^2L_ri_c}. \tag{16}$$

V. Experiment

To verify the correctness and feasibility of the proposed modulation method, an experimental prototype has been built, as shown in Fig. 15. The specific parameters are shown in Table II. The core of the resonant inductor is made of ferrite (PC90 PQ5050) with better high frequency characteristics. The core of the filter inductor is made of Fe-Si magnetic ring (NPF184060) with better magnetic saturation capability. The power switch is SiC MOSFET CAB011M12FM3, and the controller is EP4CE10E22C8 from Altera.

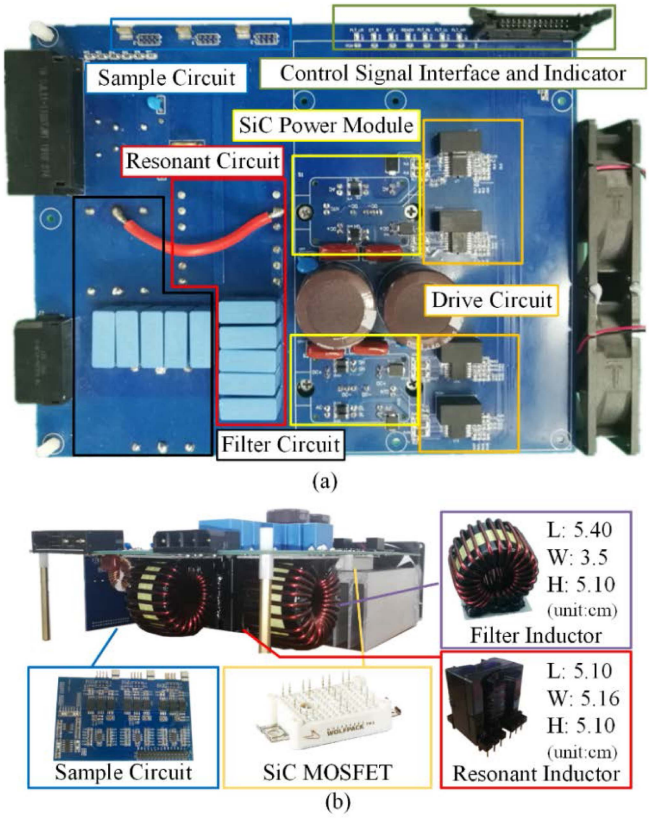


Fig. 15. Experimental prototype, showing the main blocks.

TABLE II
Parameters of the Experimental Prototype

Parameter	Value
Input voltage u_{dc}	600 V
Raged output power P_o	3000 W
Switching frequency f_{sw}	100 kHz
Output frequency f_{out}	50–500 Hz
Resonant ductor L_r	50 μH
Resonant capacitor C_r	1.1 μF
Filter inductor L_f	300 μH
Filter capacitor C_f	1.1 μF
Dead time	200 ns

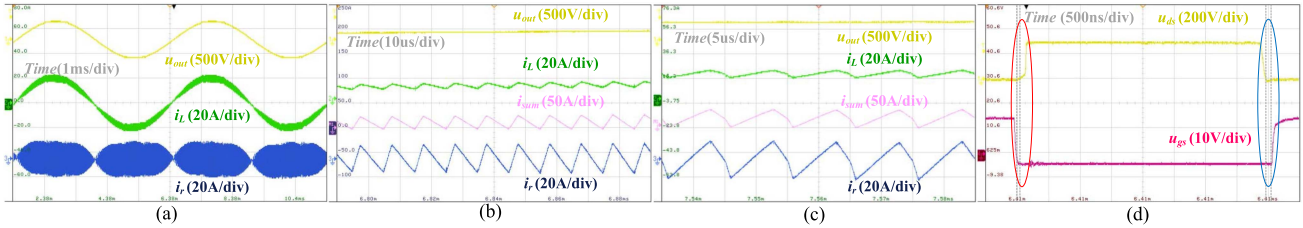


Fig. 16. Key waveforms of the inverter under resistive loads (20 Ω, 200 Hz). (a) Output voltage, filter inductor current, and resonant inductor current waveforms. (b) Voltage and current waveforms in triangular mode. (c) Voltage and current waveforms in trapezoidal mode. (d) Drain-source and gate-source voltage waveforms of the power switch.

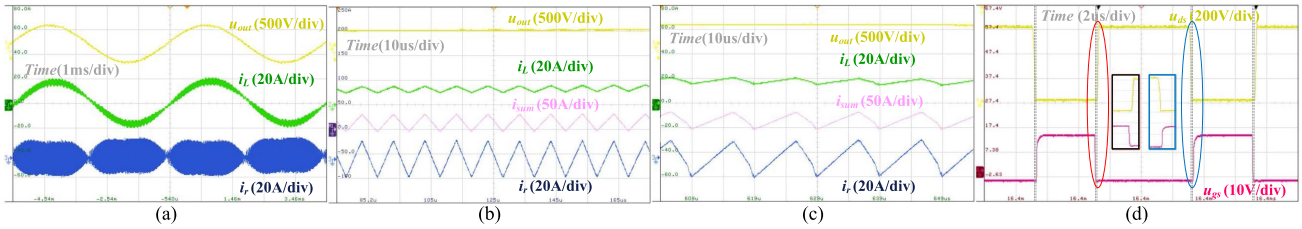


Fig. 17. Key waveforms of the inverter under resistive-inductive load (20 Ω+4.8 mH, 200 Hz). (a) Output voltage, filter inductor current, and resonant inductor current waveforms. (b) Voltage and current waveforms in triangular mode. (c) Voltage and current waveforms in trapezoidal mode. (d) Drain-source and gate-source voltage waveforms of the power switch.

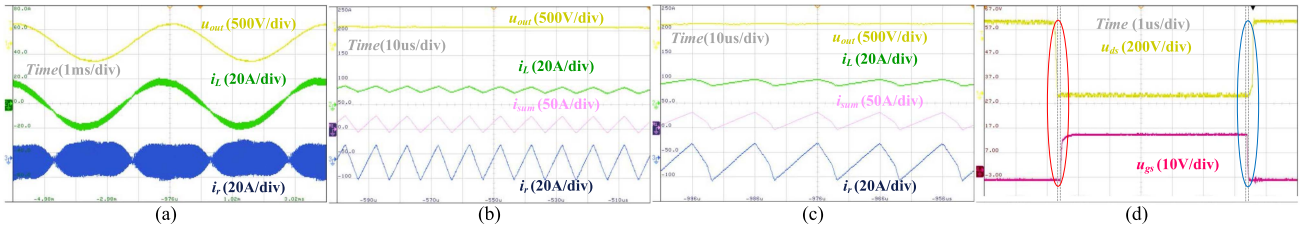


Fig. 18. Key waveforms of the inverter under resistive-capacitive load (20 Ω+145 μF, 200 Hz). (a) Output voltage, filter inductor current, and resonant inductor current waveforms. (b) Voltage and current waveforms in triangular mode. (c) Voltage and current waveforms in trapezoidal mode. (d) Drain-source and gate-source voltage waveforms of the power switch.

The waveforms of the inverter output voltage, resonant inductor current, and filter inductor current under different loads are shown in Figs. 16–18. It can be seen that the resonant inductor takes up most of the high frequency current ripple regardless of the load. The high frequency current ripple through the filter inductor is less, which improves the quality of the output current waveform. As can be seen from among output voltage waveforms in Figs. 16(a), 17(a), and 18(a), the switching process between different operating modes is smooth. The output voltage waveform has no significant distortion due to mode switching. The voltage and current waveforms of the inverter at the switching frequency are shown in Fig. 16(b) and (c), etc. i_{sum} is the sum of i_r and i_L. The inverter switches between triangular mode and trapezoidal mode with different operating conditions. In triangular mode, the inverter outputs two levels. In trapezoidal mode, the inverter outputs three levels. In each mode, i_{sum} can always cross zero in each switching cycle, enabling the switch to achieve ZVS.

As can be seen from Figs. 16(d), 17(d), and 18(d), in addition to the current of i_{sum}, it can also be seen from the drain-source voltage u_{ds} and gate-source voltage u_{gs} that the power switch achieves ZVS. The resonant current is not affected by the load and takes up most of the switching frequency current. Therefore, the u_{gs} and u_{ds} of the power switch are always similar under different loads.

Figs. 19 and 20 show the voltage and current waveforms of the inverter at different modulation degrees and output frequencies in turn. From Figs. 19 and 20, the inverter can output good voltage waveforms at different modulation degrees and output frequencies. It is worth mentioning that, similar to SPWM, as the output frequency increases, the carrier ratio keeps decreasing and the waveform quality of the output voltage decreases.

In the dynamic response experiments, Fig. 21 shows the key waveforms of voltage and current when the output voltage changes suddenly, and Fig. 22 shows the key waveforms of voltage and current when the load changes suddenly. In the case of sudden changes in output voltage, the resonant inductor current is affected first and changes rapidly because the impedance of the resonant circuit is smaller. And then with the voltage and current loop, modulation degree is raised and the output voltage tracks to the new reference. In order to achieve soft switching, the inverter goes from the triangular mode to the trapezoidal mode. Due to

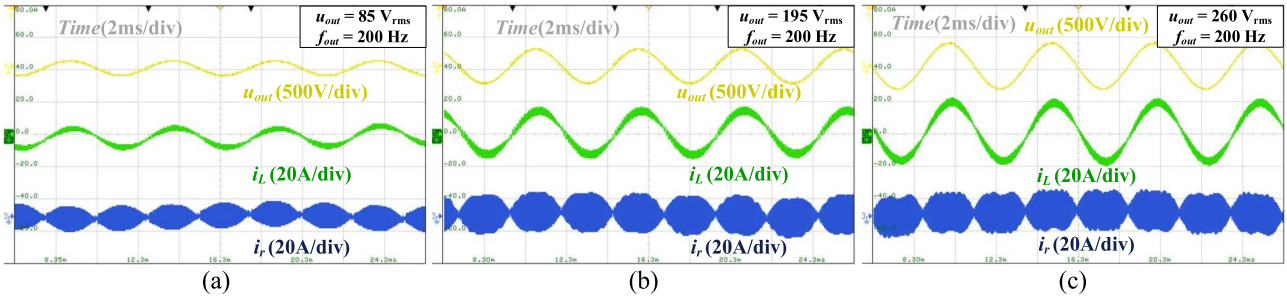


Fig. 19. Key waveforms of the inverter at different modulation degree with resistive-inductive load (20 Ω+4.8 mH, 200 Hz). (a) Output power: 330 W+95 Var. (b) Output power: 1730 W+500 Var. (c) Output power: 2970 W+850 Var.

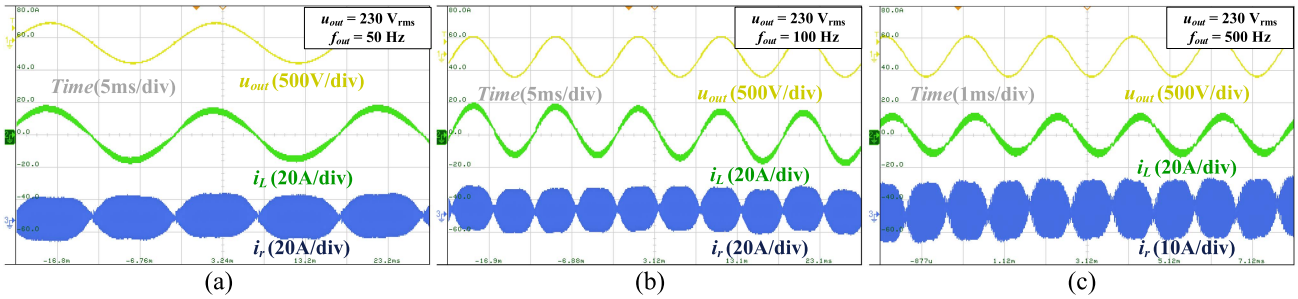


Fig. 20. Key waveforms of the inverter at different output frequencies with resistive-inductive load (20 Ω+4.8 mH). (a) Output frequency: 50 Hz. (b) Output frequency: 100 Hz. (c) Output frequency: 500 Hz.

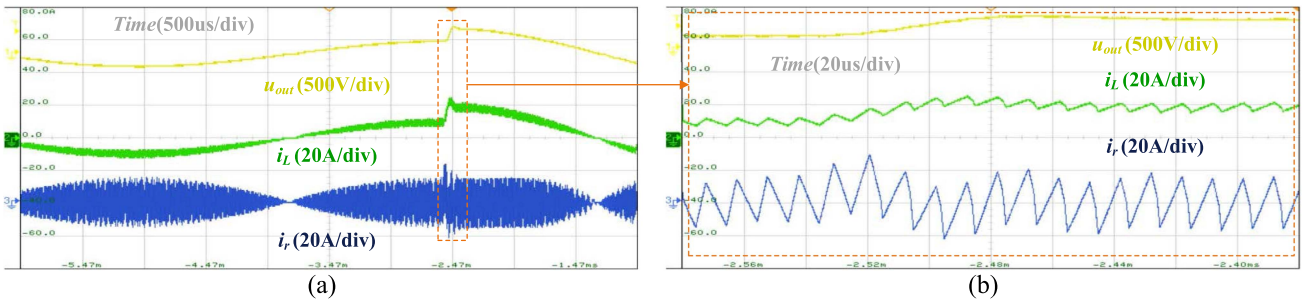


Fig. 21. Key waveforms of voltage and current when the output voltage changes suddenly (200–400 V_{peak}).

the rapid change in duty cycle, the resonant inductor current fluctuates and gradually stabilizes. And when the load changes suddenly, the modulation degree does not change at the first time. Therefore, the resonant inductor current does not change, and the filter inductor has a tendency to rise, but it changes slowly. The voltage of the filter capacitor has a voltage dip. With the voltage outer loop, the modulation degree is raised and the inverter enters the trapezoidal mode. The output voltage is recovered and tracked to the reference value. The filter and resonant current are also gradually stabilized with the current inner loop.

Table III shows the switching frequency, switching loss, inductor current peak value, and THD of output current with different topologies and modulation methods. The load is resistive-inductive load (40 Ω+4.8 mH, 200 Hz). It can be seen from the comparison that the modulation method proposed in this article greatly reduces the range of switching frequency and reduces the turn-OFF loss of the MOSFETS. The FSFHM can also reduce the

TABLE III
TEST RESULTS OF DIFFERENT TOPOLOGIES AND MODULATIONS

Topology	Full bridge		Full bridge with resonant circuit			
Modulation	SPWM		BCM		FSFHM	
Switching frequency	100 kHz		100-300 kHz		100 kHz	
RMS of power switch current i_{ds}	5.90 A		7.01 A		7.84 A	
Switching loss	27.10 W		13.18 W		12.46 W	
Peak value of Inductor current	L_f	12.59A	L_r	17.01 A	L_r	16.48 A
			L_f	13.96 A	L_f	13.45 A
THD	0.70 %		1.31 %		0.94 %	

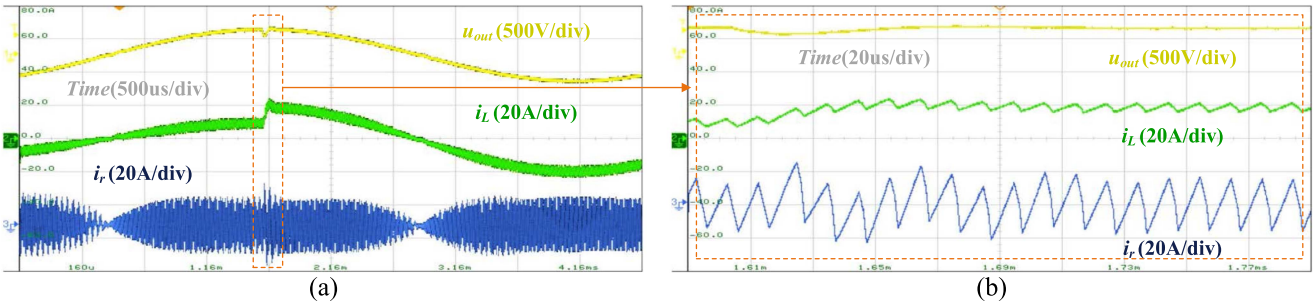


Fig. 22. Key waveforms of voltage and current when the load changes suddenly (40–20 Ω).

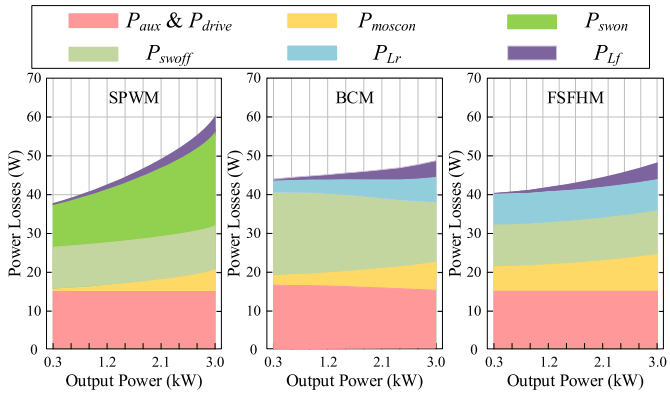


Fig. 23. Loss distribution under different topologies and modulation methods.

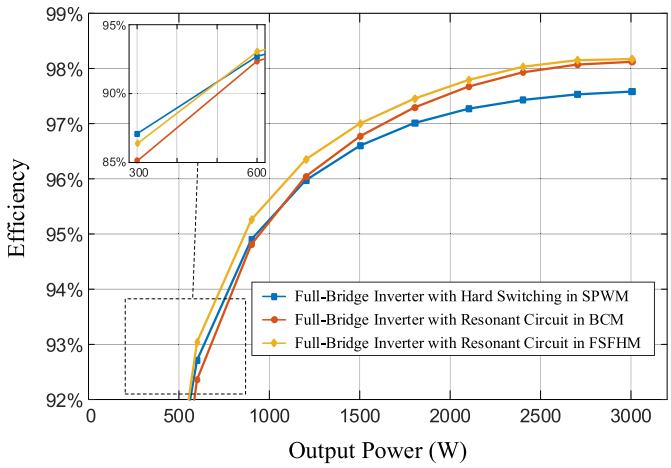


Fig. 24. Measured efficiency curve of the FSFHM inverter and a comparison to SPWM and BCM schemes.

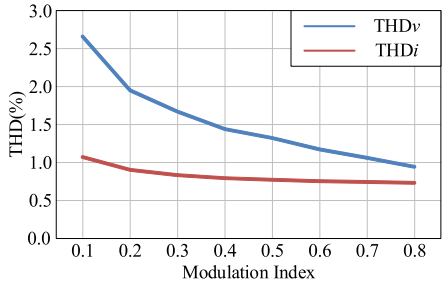


Fig. 25. THD curves of inverter in FSFHM with resistive-inductive load (40 Ω+4.8 mH, 200 Hz).

peak current of resonant inductor, but increases the conduction loss of the power switches. The result is consistent with the previous analysis.

Figs. 23 and 24 show the loss distribution curves and efficiency curves of the full-bridge inverter with different topologies and modulation methods, respectively. At the rated voltage and light load, the output current of the inverter is small. The total loss of the SPWM inverter with hard-switched is smaller because of the smaller conduction loss. The inverter in BCM has some current ripple in resonant inductor, but its RMS value is not high. The BCM has the high average switching frequency and the turn-OFF loss P_{swoff} mainly affects the total loss. The inverter in FSFHM has the loop current in the resonant circuit at the rated output voltage. The resonant inductor loss P_{Lr} and conduction loss P_{moscon} reduce the efficiency of the inverter. At this stage, the hard-switching SPWM has higher efficiency. The efficiency of FSFHM and BCM is lower due to loop current and turn-OFF losses, respectively. As the output current rises, the percentage of conduction loss and filter inductor loss of the SPWM inverter with hard-switched remains small, while the turn-ON loss P_{swon} gradually increases. The switching frequency and turn-OFF loss P_{swoff} of the inverter in BCM gradually decreases, and the conduction loss P_{moscon} and resonant inductor loss P_{Lr} of the inverter increases. Because the switching frequency is fixed, the resonant inductor loss P_{Lr} and turn-OFF loss P_{swoff} of the inverter in FSFHM are almost independent of the output current, and the conduction loss P_{moscon} has increased. At this stage, the advantages of soft-switching modulation gradually emerge. The efficiency of both FSFHM and BCM increases significantly and the total loss of both modulation increases slightly. Under heavy load, the SPWM inverter with hard-switched has higher losses at heavy load because the turn-ON loss P_{swon} increase more rapidly. The total loss of the inverter in FSFHM is slightly smaller than that of the inverter in BCM due to the smaller turn-OFF loss and core loss. Meanwhile, the efficiency difference between the two soft-switching modulation methods decreases as the power increases.

In terms of output voltage and output current waveforms quality, the THD of output voltage and output current tends to decrease with the increase of modulation degree as shown in Fig. 25.

VI. Conclusion

This article proposes the FSFHM method with ZVS to reduce the range of switching frequency and the peak value of inductor current. The correctness and feasibility of the proposed modulation method have been verified by the experimental prototype. The modulation method proposed in this article can also be used without the resonant circuit independently to improve the efficiency of the inverter. On the other hand, whether it is to reduce the switching frequency range or ZVS, it is realized by increasing the RMS of the current of the MOSFETS and the inductors. So it is necessary to combine the working conditions in the design and selection of components to make the inverter achieve the best cost, efficiency, and power density.

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