Decomposed Nearest Level PWM Method With Reduced Switching Frequency for MMC

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***Abstract*—For modular multilevel converters in medium-voltage applications, the nearest level pulse width modulation (NL-PWM), which combines the nearest level modulation (NLM) with pulse width modulation (PWM), has the advantage of better harmonic characteristics over conventional NLM. However, the introduction of high-frequency PWM also results in a significant increase in switching frequency. To solve this issue, a decomposed NL-PWM method is proposed in this article. By properly allocating the rising edge and falling edge of PWM to two different SMs, the capacitor voltage differences can be decreased more efficiently. On this basis, the allocation priority of different switching transitions is quantitatively analyzed, and then a new voltage-balancing strategy involving five switching modes is proposed. Moreover, to achieve a good tradeoff between voltage-balancing effect and switching loss, the relationship between voltage threshold and switching frequency under the proposed method is also derived. Finally, the comparative simulation and experimental results demonstrate the superiority of the proposed method in different aspects of performance.**

***Index Terms*—Decomposed nearest level pulse width modulation (NL-PWM), modular multilevel converter (MMC), reduced switching frequency, voltage balancing.**

I. Introduction

RECENTLY, the modular multilevel converter (MMC) is developing rapidly and gaining popularity in medium- or high-voltage applications due to its advantages of high efficiency, superior output waveforms, and fault-tolerant capability [1], [2], [3], etc. To fully exert these advantages, the control strategy of MMC is especially crucial in which the modulation method is the key to determining final performance. When the number of submodules (SMs) in MMC is relatively small, the non-negligible staircase approximation error of conventional nearest level modulation (NLM) will result in poor quality of output waveforms; thus, the multicarrier pulse width modulation (PWM) is more preferable.

Among various configurations of multicarrier PWM, carrier phase-shifted PWM (CPS-PWM) and phase disposition PWM (PD-PWM) are most commonly discussed in the literature and proven feasible in actual projects [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14]. These methods can offer low harmonic distortion if SM capacitor voltages are well-balanced, but still have limitations in some aspects. In the conventional CPS-PWM [4], hierarchical control is adopted and the relatively low weight of individual balancing control loop results in a slow response of voltage balancing. In [6], the driving pulses generated by CPS-PWM were reassigned to SMs based on their contributions to capacitor charge transfer in each carrier period. Since the change of modulation signals during a carrier period is ignored, the pulse reallocation may be inappropriate. Besides, the average switching frequency is increased due to the step change of driving signals at the moment of pulse reallocation. The pulse reallocation methods have also been adopted in PD-PWM [8], [9], and similarly the requirements for voltage balancing and switching frequency are hard to satisfy simultaneously. In addition, for multicarrier PWM, once any SM is in failure and isolated, the periods, phase-shifted angles, or amplitudes of carriers need to be regulated accordingly [12], [13], [14], which increases the complexity of implementation.

Meanwhile, in order to expand the applicability of NLM in MMC, several improvements were put forward in [15], [16], [17], [18], [19], [20], [21], [22], [23], [24]. These researches provide more choices of modulation for MMC with a small number of SMs, especially considering the limitations of multicarrier PWM. By defining a new rounding function and staggering switching actions in upper and lower arms, the level number of output voltage under NLM can be increased from $N+1$ (where N is the number of SMs per arm) to $2\ N+1$ without increasing switching frequency [15]. On this basis, small offsets were added to the voltage references in [16], thus reducing the output harmonics as well as restraining capacitor voltage fluctuations. Focusing on the optimization of circulating current, the small offset was replaced by a small second-order harmonic control term in [17]. When selecting proper sampling frequency and inserted term, the second-order harmonic of circulating current can almost be eliminated.

By adopting the aforementioned level-increased NLM methods, control performance of MMC can be obviously enhanced, especially when the number of SMs is small. However, compared to CPS-PWM, the deficiency of NLM in waveform quality is still non-negligible due to the limitation of modulation accuracy. Thus, the nearest level PWM (NL-PWM), which combines NLM with PWM, is presented and discussed in [19], [20], [21], [22]. To some extent, the NL-PWM is equivalent to PD-PWM with specific carrier frequency (equal to control frequency) and

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flexible reallocation of switching pulses. After introducing high-frequency PWM, the low-order harmonics of output waveforms are almost eliminated, but meanwhile the switching frequency and switching losses are greatly increased. To avoid unnecessary switching actions, a five-segment switching sequence was designed in [21], but the control performance relies highly on the parameter accuracy. In [22], by replacing the triangle carrier with rising or falling sawtooth, the switching frequency of NL-PWM can be obviously decreased, but more harmonics are inevitably caused by irregular sawtooth.

Therefore, although NL-PWM can achieve even lower output harmonics than that under CPS-PWM [20], the unresolved issue of high switching frequency restricts its application to a great extent. Referring to NLM [25], [26], [27], [28], [29], the switching frequency of NL-PWM can also be reduced by modifying the voltage-balancing strategy. One typical way is to set a voltage threshold that determines the additional switching transitions. Taking [27] as an example, if the maximum voltage difference among SM capacitors exceeds the threshold, the switching times are equal to the variation of inserted SM number; otherwise, all the SMs should be inserted or bypassed in the order of voltage sorting. However, except the SMs with the highest and lowest voltages, the voltage differences among the other SMs may be small and the associated switching transitions are unnecessary for voltage balancing. Another way is to arrange fixed or adjustable number of SMs to switch in different control cycles. However, it is primarily suited to high-voltage applications. Besides, since there exist at least three switching modes in NL-PWM, the NLM-based strategies cannot be simply used for NL-PWM.

In this article, a decomposed NL-PWM method is proposed for MMC. Unlike the conventional NL-PWM, the rising edge and falling edge of PWM can be assigned to two SMs, and totally five switching modes are involved. Through such fully utilization of PWM, the voltage differences of SM capacitors can be decreased more efficiently. Furthermore, an improved NL-PWM-based voltage-balancing strategy is proposed. In each control period, SMs are paired up according to the voltage relationship and previous switching states. Except for essential switching transitions, the paired SMs exchange the switching states only if the corresponding voltage difference exceeds the preset threshold. The allocation priority of essential PWM-up and PWM-down, essential insertion/bypass, and additional state exchange is based on quantitative analysis of the voltage-balancing effect contributed by different types of switching transitions. Consequently, the switching frequency can be significantly reduced under the prerequisite of guaranteeing effective voltage balancing. Besides, the relationship between voltage threshold and switching frequency under the proposed method is derived to provide a guideline for determining voltage threshold. Both the simulation and experimental results demonstrate the validity and superiority of the proposed method.

II. Conventional NL-PWM

A. Basic Principle

Fig. 1(a) shows one phase of MMC in which the upper and lower arms are both formed by N series-connected SMs and a

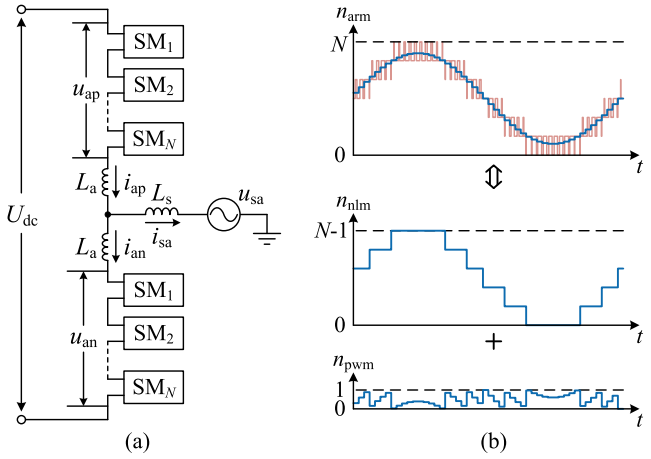

Fig. 1. (a) One phase of MMC. (b) Principle of conventional NL-PWM.

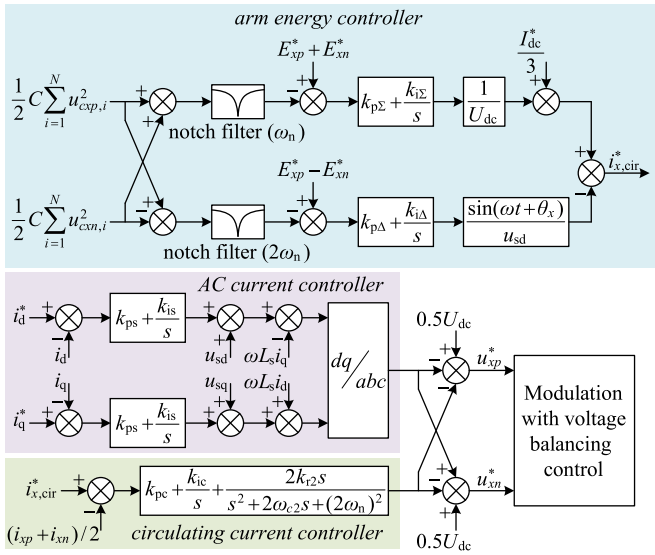

Fig. 2. Comprehensive control strategy of MMC.

buffer inductor. For any arm, the required insertion index $n_{\rm arm}$ is equal to the required arm voltage ($u_{x\rm p}$ or $u_{x\rm n}$, $x = a, b, c$) divided by the average capacitor voltage. The acquisition of $u_{x\rm p}$ or $u_{x\rm n}$ is shown in Fig. 2. In most cases, $n_{\rm arm}$ is not an integer, and therefore low-frequency staircase modulation and high-frequency PWM are combined to achieve the equivalent insertion in the conventional NL-PWM. As shown in Fig. 1(b), $n_{\rm nlm}$ SMs operate in inserted mode and one SM operates in PWM mode with duty cycle of $d_{\rm pwm}$, where $n_{\rm nlm}$ and $d_{\rm pwm}$ are obtained by

$$\begin{cases} n_{\rm nlm} = {\rm floor}(n_{\rm arm}) \\ d_{\rm pwm} = n_{\rm arm} - {\rm floor}(n_{\rm arm}) \end{cases} \tag{1}$$

where the function floor(x) returns the largest integer less than or equal to x.

Similar to NLM-based methods, voltage balancing of SM capacitors can be easily implemented in the conventional NL-PWM. The N SMs in each arm are first sorted in ascending (if the arm current $i_{\rm arm} \geq 0$) or descending order (if $i_{\rm arm} < 0$) of their capacitor voltages. Then, the first $n_{\rm nlm}$ SMs will be

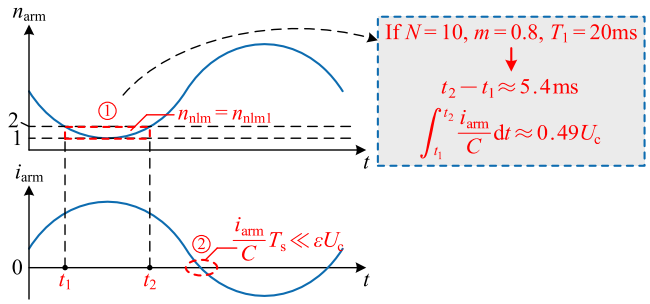

Fig. 3. Typical issues of conventional NL-PWM.

inserted, the $(n_{nlm}+1)$th SM will operate in PWM mode, and the other SMs will be bypassed. The frequent reallocation of three switching modes ensures small voltage difference, but results in high switching frequency and subsequently switching losses that are undesirable. Thus, to mitigate the increase of switching frequency, the voltage sorting is activated only when $n_{nlm} \neq n_{nlm1}$ (where n_{nlm1} is equal to n_{nlm} of last control period) in [20].

B. Characteristic Analysis

For the convenience of quantitative analysis, the power factor $\cos\varphi$, modulation index m, and the ripple ratio of capacitor voltages ε are set as 0.9, 0.8, and 0.1, respectively, here. Then, referring to [30], the expression of SM capacitance can be obtained as

$$C = \frac{S}{3\omega m N \varepsilon U_c^2}\left[1-\left(\frac{m\cos\varphi}{2}\right)^2\right]^{1.5} = \frac{I_{dc}}{92.85 U_c} \tag{2}$$

where S, U_c, and I_{dc} denote the capacity, rated SM voltage, and dc-side rated current of MMC, respectively, and ω is the angular frequency, which is equal to 100π assuming the grid standard frequency is 50 Hz.

Using the abovementioned parameter configuration, the voltage-balancing strategy in the conventional NL-PWM leads to the following two different consequences.

1) *When $n_{nlm} = n_{nlm1}$:* All the SMs maintain the previous switching modes (i.e., inserted mode, bypassed mode, or PWM mode). If N is relatively small (e.g., $N = 10$), this situation may last for several milliseconds during which the capacitors of inserted SMs are charged/discharged too much, and thus resulting in the major imbalance of capacitor voltages. As shown in Fig. 3, when $N = 10$, n_{nlm} remains unchanged during $t_1 \sim t_2$. Combining with (2), the maximum capacitor voltage variation of inserted SMs during this period is approximately $0.5U_c$. Such significant voltage imbalance threatens the stable operation of MMC seriously.
2) *When $n_{nlm} \neq n_{nlm1}$:* All the SMs participate in the allocation of three switching modes. Even if the voltage differences among some SMs are very small, their switching modes may also change. Especially when the arm current is close to zero, the capacitor voltage variations caused by switching transitions can be neglected (see Fig. 3). Similar to conventional NLM, this results in the increased switching frequency and subsequently undesirable losses.

Therefore, the switching frequency and voltage-balancing effect under the conventional NL-PWM are not satisfactory. If the sorted list is updated more frequently, the voltage imbalance can be avoided to some extent while higher switching frequency is required. To reveal the essence of the problem, the switching transitions are divided into three types in this article: 1) essential NLM part; 2) essential PWM part; and 3) additional part. The essential NLM part is caused by the variation of n_{nlm}, and the number of this part in a control period is equal to $|n_{nlm} - n_{nlm1}|$. The essential PWM part is caused by the rising edge and falling edge of PWM, and the number of this part in a control period is always equal to 2, unless $d_{pwm} = 0$. Except for these two parts, all the other switching transitions are classified as the additional part. Obviously, the key of modifying NL-PWM is to reduce the additional part with no or little sacrifice of voltage-balancing effect. To achieve this target, all the switching transitions need to be better utilized for voltage balancing.

III. Decomposed NL-PWM

A. Acquisition of New Switching Modes

Combining with Fig. 1(b), the number of essential NLM part and essential PWM part in a fundamental period (denoted by T_1) can be expressed as

$$N_{nlm} = 2\left[\text{floor}\left(\frac{1+m}{2}N\right) - \text{floor}\left(\frac{1-m}{2}N\right)\right] \tag{3}$$

$$N_{pwm} = 2\,T_1/T_s \tag{4}$$

where m and T_s denote the modulation index and sampling period, respectively. If $N = 20$, $m = 0.8$, $T_1 = 20$ms, and $T_s = 0.2$ms, N_{nlm} and N_{pwm} can be calculated as 32 and 200. When N is smaller, the ratio of N_{pwm} and N_{nlm} will be larger. This indicates the PWM part should play a crucial role in voltage balancing if pursuing reduced switching frequency in medium-voltage applications.

For conventional NL-PWM, one SM is selected to operate in PWM mode if $d_{pwm} \neq 0$. As shown in Fig. 4(a), the capacitor voltage variation caused by PWM, Δu_{pwm}, is $d_{pwm} i_{arm} T_s / C$ (where i_{arm} and C denote the arm current and SM capacitance, respectively). That is, if considering only the role of PWM, the maximum decrease of ΔU_{max} (denoting the maximum voltage difference of SM capacitors) is $|d_{pwm} i_{arm} T_s / C|$.

Actually, the realization of PWM can be more flexible, and thus a decomposed NL-PWM method is proposed in this article. As shown in Fig. 4(b), the rising edge and falling edge of PWM are assigned to a bypassed SM and an inserted SM; thus, two new switching modes are generated: 1) PWM-up mode; and 2) PWM-down mode. Compared with the original states (i.e., no switching transitions), charging time of the two SMs is, respectively, increased and decreased if $i_{arm} > 0$. Specifically, the voltage variations caused by PWM-up and PWM-down (denoted by Δu_{up} and Δu_{dn}, respectively) are $(d_{pwm}+1) i_{arm} T_s / 2\,C$

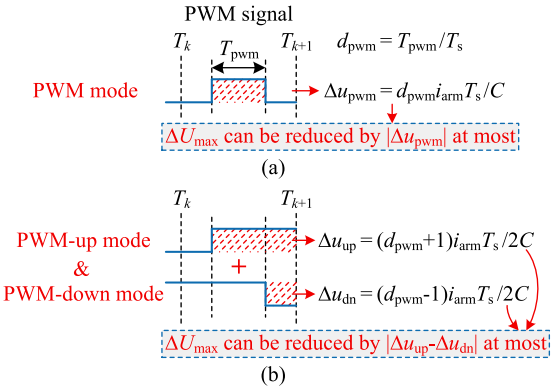

Fig. 4. Different ways to generate PWM signal. (a) Conventional NL-PWM. (b) Decomposed NL-PWM.

and $(d_{\text{pwm}}-1)i_{\text{arm}}T_{\text{s}}/2\,C$, respectively. Thus, the maximum decrease of $\Delta U_{\max}$ is $|\Delta u_{\text{dn}}-\Delta u_{\text{up}}|$, i.e., $|i_{\text{arm}}T_{\text{s}}/C|$. This indicates that the decomposition of PWM helps to balance capacitor voltages more efficiently. Furthermore, lower switching frequency can be achieved, which will be elaborated in the following section.

B. Improved Voltage-Balancing Strategy for Decomposed NL-PWM

According to the abovementioned analysis, the introduction of PWM-up mode and PWM-down mode can greatly enhance the voltage-balancing effect contributed by the essential PWM part. But, this conclusion is based on the assumption that the switching modes are properly allocated to SMs. Therefore, to maximize the advantages of decomposed NL-PWM, an improved voltage-balancing strategy involving new switching modes is proposed in this section.

For the MMC in medium-voltage applications, the performance degradation caused by control delay is not evident in general. If considering the control delay in the analysis, the initial switching states described during the control period $T_k \sim T_{k+1}$ may correspond to the actual switching states at T_{k+1}. This results in poor readability and possible ambiguity when describing some variables. Therefore, similar to most of the literature, the control delay is ignored here for simplicity and clarity.

The proposed strategy will be elaborated according to the specific procedure, which is given as follows.

1) SM Sorting and Pairing: As mentioned in Section II, the additional part of switching transitions never changes the total number of inserted SMs. Therefore, the additional part is always characterized by exchanging switching states (inserted/bypassed) of SMs, whether the state exchange is active or passive. Combining this with the previous description, the correspondence among the initial switching states, switching modes, and types of switching transitions under decomposed NL-PWM can be summarized, as shown in Fig. 5.

To match the paired transitions in essential PWM part or additional part, SMs are first sorted and paired off, as shown in Fig. 6. When $i_{\text{arm}} \geq 0$, the sorting priority of previously bypassed SMs is higher, otherwise the opposite. For SMs

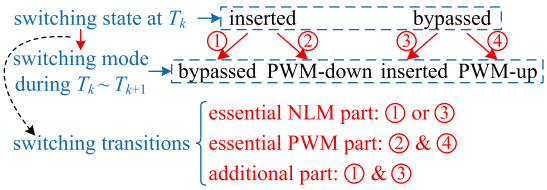

Fig. 5. Correspondence among the initial switching states, switching modes, and types of switching transitions under decomposed NL-PWM.

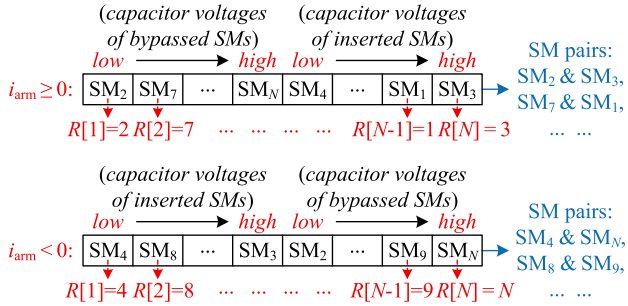

Fig. 6. Principle of SM sorting and pairing.

with the same initial switching state, they are always sorted in ascending order of capacitor voltages. Then, based on the sorted list $R[1] \sim R[N]$, SMs with different initial switching states (inserted/bypassed) are paired off, i.e., $\text{SM}_{R[1]}$ and $\text{SM}_{R[N]}$, $\text{SM}_{R[2]}$ and $\text{SM}_{R[N-1]}$, ... Apparently, the number of SM pairs is equal to $\min\{n_{\text{nlm1}}, N-n_{\text{nlm1}}\}$ and the voltage differences satisfy a relation $u_{R[N]}-u_{R[1]} > u_{R[N-1]}-u_{R[2]} > \cdots$ (where u_i denotes the capacitor voltage of SM_i, $i=1,2,\ldots,N$). Thanks to the parallel computing capability of field programmable gate array (FPGA) and bitonic sorting algorithm [31], the sorting and pairing process in each control period can be implemented within hundreds or even tens of nanoseconds [$\log_2 N\cdot(\log_2 N+1)/2$ clock cycles], which indicates the computational burden of this stage is light.

2) Priority Evaluation of Switching Transitions: For each SM pair, if the switching states remain unchanged in this control period, the relative voltage variation $|i_{\text{arm}}T_{\text{s}}/C|$ over this period may enlarge the voltage difference. Consequently, the voltage difference may exceed the allowable limit U_{th}. Such case can be avoided if one or more switching transitions are allocated to the corresponding SM pair. For the SM pair selected to operate in PWM-up and PWM-down modes, the voltage difference can be reduced by $|i_{\text{arm}}T_{\text{s}}/C|$ at most, which has been analyzed in Section III-A. For the other types of switching transitions, the similar conclusion can be obtained, as shown in Fig. 7. Thus, when the additional switching transitions are required, they should be allocated to the SM pairs with relatively large voltage difference (i.e., the SM pair $\text{SM}_{R[1]}$ and $\text{SM}_{R[N]}$ has the highest priority).

The voltage-balancing effects contributed by essential insertion/bypass and essential PWM-up and PWM-down seem the same ($|i_{\text{arm}}T_{\text{s}}/C|$) in the current period, but actually there exists distinct difference. Assuming that no switching transitions occur on the relevant SMs afterward, voltage difference of the SM pair selected for PWM-up and PWM-down can be further

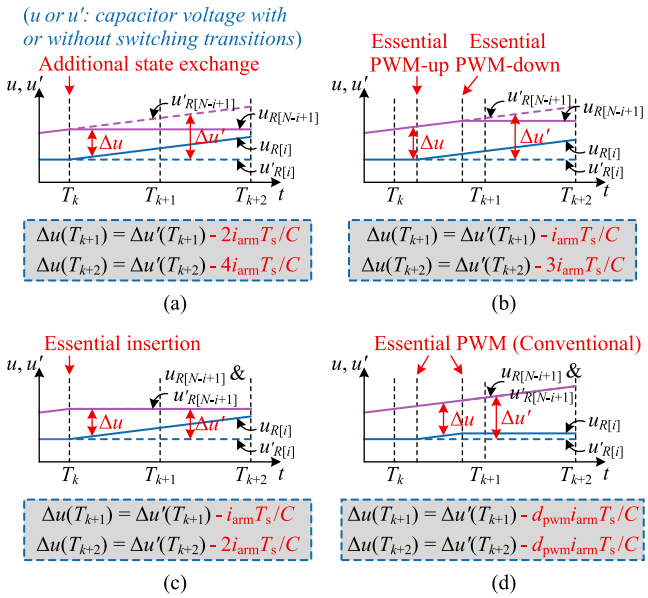

Fig. 7. Voltage-balancing effect contributed by the following terms. (a) Additional state exchange. (b) Essential PWM-up and PWM-down. (c) Essential insertion. (d) Essential PWM (in conventional NL-PWM) when $i_{\text{arm}} \geq 0$.

decreased, while the essential insertion/bypass results in the identical switching state of the SM pair [see Fig. 7(b) and (c)]. Thus, the allocation priority of essential NLM and PWM parts can be obtained.

3) Specific Implementation of Switching Transitions: Since the essential NLM and PWM parts can be easily obtained by n_{nlm}, d_{pwm}, and n_{nlm1}, the next key step is to determine the number of additional state exchange. Assuming the maximum voltage difference $\Delta U_{\max}$ is restricted within the preset threshold U_{th} and the switching states of all SMs during $T_k \sim T_{k+1}$ remain unchanged, $\Delta U_{\max}$ at T_{k+1} should satisfy

$$\Delta U_{\max} \leq U_{\text{th}} + |i_{\text{arm}} T_{\text{s}}/C| \tag{5}$$

where the variation of i_{arm} within several consecutive control periods is ignored. Generally, U_{th} is chosen around $0.5\varepsilon U_{\text{c}}$ and always larger than $|i_{\text{arm}} T_{\text{s}}/C|$ [27]. Combining with Fig. 7, the voltage difference of each SM pair at T_{k+1} can be restricted within U_{th} by any type of switching transitions under decomposed NL-PWM. In contrast, if adopting the conventional PWM mode, the voltage difference may still exceed U_{th} ($\Delta U_{\max} - |d_{\text{pwm}} i_{\text{arm}} T_{\text{s}}/C| > U_{\text{th}}$) and additional switching transitions are necessary for voltage balancing. For such cases, two additional switching transitions can be avoided by the decomposition of PWM. This is one of the reasons that switching frequency can be reduced with the proposed method (the paired operation of additional switching transitions is another major reason).

Besides, due to the nonpaired operation of essential insertion/bypass, the voltage difference between two SMs not in pair also needs to be considered. For example, if one additional state exchange, one essential PWM-up and PWM-down, and one essential insertion are, respectively, allocated to $\text{SM}_{R[1]}$ and $\text{SM}_{R[N]}$, $\text{SM}_{R[2]}$ and $\text{SM}_{R[N-1]}$, and $\text{SM}_{R[3]}$ at T_k, the SM pair with the largest voltage difference at T_{k+1} is probably $\text{SM}_{R[4]}$ and $\text{SM}_{R[N-2]}$ (where $R[4]$ and $R[N-2]$ correspond to the sorting list at T_k). Therefore, the following two cases should be considered for determining additional switching transitions.

a) *Step 1:* Determine the minimum k satisfying $u_{R[N-k]} - u_{R[k+1]} \leq U_{\text{th}} - |i_{\text{arm}} T_{\text{s}}/C|$ $(0 \leq k < N_{\text{p}}$, where N_{p} denotes the number of SM pair, equal to $\min\{n_{\text{nlm}}, n_{\text{nlm1}}, N - n_{\text{nlm}}, N - n_{\text{nlm1}}\})$. If there is no analytical solution, k will be taken as N_{p}. To avoid excessive computation overhead, the binary search method can be adopted here. Then, calculate the number of essential insertion/bypass (denoted by a), the number of essential PWM-up and PWM-down (denoted by b) and the sum of the two, which can be expressed as

$$\begin{aligned} \lambda &= a + b \\ &= |n_{\text{nlm}} - n_{\text{nlm1}}| + \text{ceil}(d_{\text{pwm}}) \end{aligned} \tag{6}$$

where the function $\text{ceil}(x)$ returns the smallest integer more than x.

b) *Step 2:* If $a = 0$, the number of additional state exchange c is equal to $k - \lambda$ $(k > \lambda)$ or 0 $(k \leq \lambda)$; otherwise, c is given by

$$c = \begin{cases} \max\{k - \lambda, 0\}, & \text{if } u_{R[N-k+a]} - u_{R[k+1]} \leq U'_{\text{th}} \\ \max\{k - \lambda + 1, 0\}, & \text{if } u_{R[N-k+a]} - u_{R[k+1]} > U'_{\text{th}} \end{cases} \tag{7}$$

where $U'_{\text{th}} = U_{\text{th}} - |i_{\text{arm}} T_{\text{s}}/C|$ and $i_{\text{arm}} \cdot (n_{\text{nlm}} - n_{\text{nlm1}})$ is assumed as a positive value.

After obtaining a, b, and c, the three types of switching transitions will be allocated to SMs according to the priority. For example, assuming that $N = 20$, $n_{\text{nlm}} = 9$, $d_{\text{pwm}} = 0.2$, $n_{\text{nlm1}} = 8$, $i_{\text{arm}} > 0$, $k = 3$, and $u_{R[N-2]} - u_{R[4]} > U'_{\text{th}}$, two additional state exchanges are required, which are allocated to $\text{SM}_{R[1]}$ and $\text{SM}_{R[N]}$ and $\text{SM}_{R[2]}$ and $\text{SM}_{R[N-1]}$. Besides, $\text{SM}_{R[3]}$ and $\text{SM}_{R[N-2]}$ operate in PWM-up and PWM-down modes, respectively; one essential insertion is allocated to $\text{SM}_{R[4]}$. In this way, the voltage difference between any two SMs in pair is effectively restricted within U_{th}. The whole procedure of the proposed strategy is shown in Fig. 8.

4) Consideration of Special Cases: Since the decomposition of PWM requires at least one bypassed SM and one inserted SM, there exist some special cases. When $n_{\text{nlm1}} = 0, N$ or $n_{\text{nlm}} = 0$, the rising edge and falling edge of PWM cannot be assigned to two SMs [see Fig. 4(b)]. Instead, the conventional PWM mode [see Fig. 4(a)], as the fifth switching mode in the proposed strategy, will be assigned to one selected SM. In such cases, since there is no SM pair, the additional state exchange is also unavailable. Thus, the allocation of switching modes is much simpler, as shown in Fig. 8.

It should also be noted that capacitor voltage of a previously inserted SM may be lower than that of a previously bypassed SM when $i_{\text{arm}} > 0$. If the similar situation occurs, the decomposition of essential PWM is not conducive to voltage balancing. Instead, the conventional PWM mode will be adopted (special case II shown in Fig. 8).

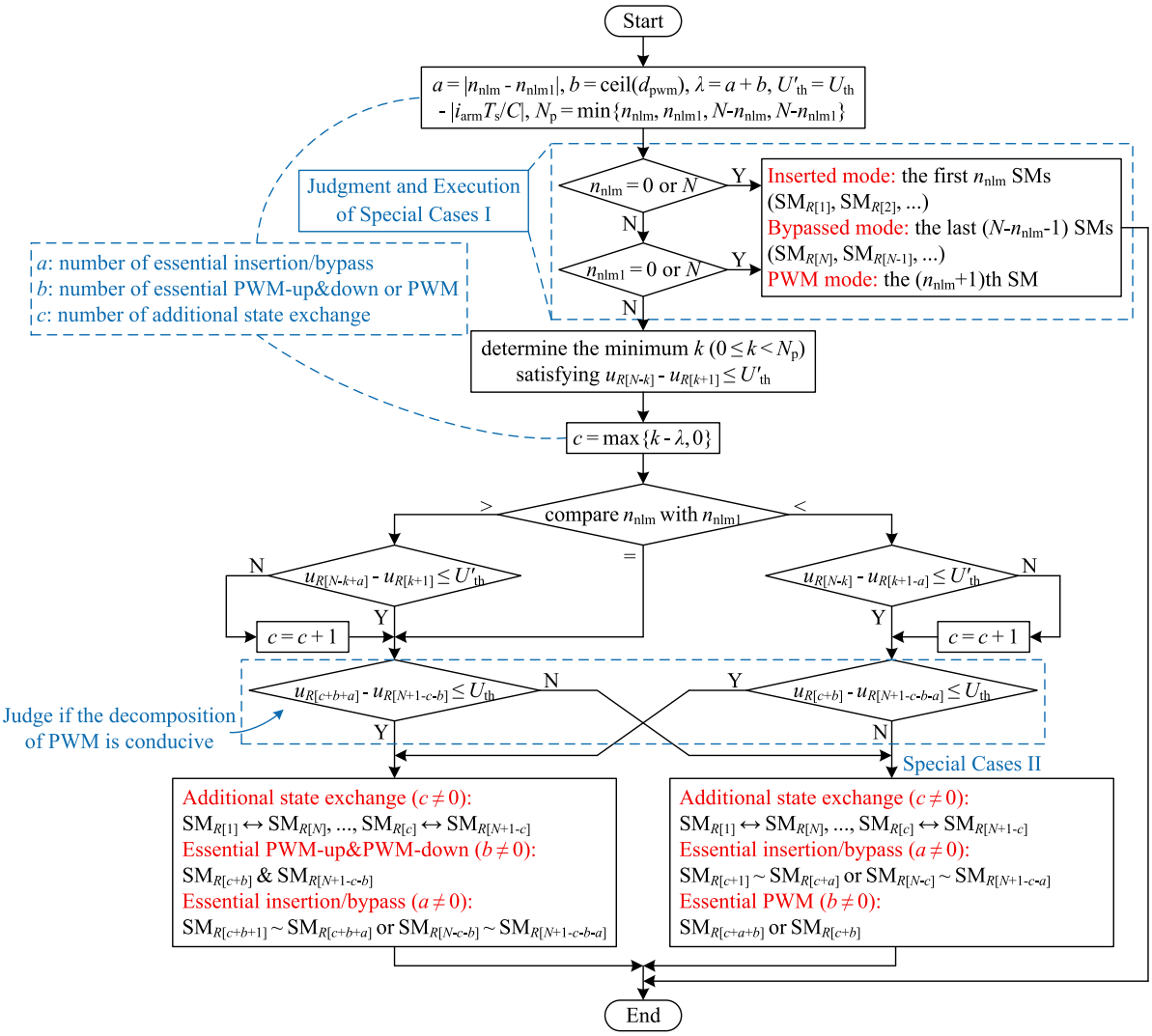

Fig. 8. Improved voltage-balancing strategy for decomposed NL-PWM (when the arm current is positive).

According to the abovementioned description, voltage differences can be restricted more efficiently by the paired operations (essential PWM-up and PWM-down and additional state exchange). Thus, under the same $\Delta U_{\max}$, the number of additional switching transitions can be effectively reduced, resulting in lower average switching frequency. Besides, the consideration of two special cases guarantees the completeness of the proposed strategy.

C. Relationship Between Voltage Threshold and Switching Frequency

Under the proposed method, the average switching frequency increases with the decrease of voltage threshold. To achieve a good tradeoff between these two aspects under different conditions, the quantitative relationship is analyzed in this section.

Assuming all the capacitor voltages remain identical at T_k, SMs inserted (bypassed) at T_k should take priority to be bypassed (inserted) to benefit voltage balancing. The local maximum voltage difference $\Delta U_{\max,k}$ will appear when all the SMs inserted at T_k have been bypassed or all the SMs bypassed at T_k have been inserted. To obtain the earliest moment corresponding to $\Delta U_{\max,k}$, two counters are adopted based on the following principles.

1) The initial values of counts 1 and 2 are equal to the number of inserted SMs and bypassed SMs at T_k, respectively.
2) Count 1 is decremented by 1 if the switching states of an SM pair are exchanged (only the essential PWM is considered here) or $n_{\text{nlm}} - n_{\text{nlm1}} = -1$; count 2 is incremented by 1 if the switching states of an SM pair are exchanged or $n_{\text{nlm}} - n_{\text{nlm1}} = 1$.
3) When count 1 reaches 0 or count 2 reaches N, both counters are stopped and the corresponding moment is T_{kE}.

Then, $\Delta U_{\max,k}$ can be calculated as

$$\Delta U_{\max,k} \approx \int_{T_k}^{T_{kE}} \frac{i_{\text{arm}}}{C} \mathrm{d}t. \tag{8}$$

By calculating and comparing $\Delta U_{\max,k}$ under different T_k, the global maximum voltage difference $\Delta U_{\max}$ can be roughly obtained. When the preset voltage threshold U_{th} is no lower than

TABLE I
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameter	Simulation	Experimental
Rated output power, P_{n}	2.4 MW	2.25 kW
DC-link voltage, U_{dc}	20 kV	480 V
AC phase voltage (RMS), U_{s}	5.66 kV	135 V
Number of SMs per arm, N	20	6
Arm inductance, L_{arm}	10 mH	3 mH
AC inductance, L_{s}	10 mH	3 mH
SM capacitance, C	1.4 mF	2 mF
Sampling frequency, f_{s}	5 kHz	5 kHz
Carrier frequency of CPS-PWM, f_{tri}	312.5 Hz	833.3 Hz

$\Delta U_{\max}$, no additional switching transitions are required and the average switching frequency can be calculated as

$$f_{\mathrm{sw}} = \left(N_{\mathrm{nlm}} + N_{\mathrm{pwm}}\right)/2NT_1 = mf_1 + f_{\mathrm{s}}/N. \tag{9}$$

For lower U_{th}, additional switching transitions have to be generated. After adding one additional state exchange, $\Delta U_{\max,k}$ will decrease by about $2T_{\mathrm{s}}i_{\mathrm{arm}}/C$. If $\Delta U_{\max,k}$ still exceeds U_{th}, more additional switching transitions are required until the comparison result changes. In this way, the number of additional switching transitions corresponding to different T_k is roughly obtained. Thus, the relationship between U_{th} and f_{sw} under the proposed method can be outlined without simulation and experiment.

IV. SIMULATION STUDIES

In order to compare the proposed decomposed NL-PWM with several typical NLM-based, NL-PWM-based, and CPS-PWM-based methods, a three-phase MMC system is simulated in MATLAB/Simulink. All the simulation studies are based on the same control architecture shown in Fig. 2 and the main simulation parameters are listed in Table I.

A. Comparison With NLM-Based and NL-PWM-Based Methods

Fig. 9 shows the steady-state performance of MMC under three different methods: 1) reduced switching frequency NLM [27]; 2) conventional NL-PWM [20]; and 3) proposed decomposed NL-PWM. Especially, the conventional NL-PWM with two different voltage-balancing strategies are both simulated. By incrementing the counter variable when changes occur in switching states in programs, the average switching frequencies f_{sw} corresponding to Fig. 9(a)–(d) can be obtained, which are about 300, 610, 1400, and 310 Hz, respectively. Referring to the loss characteristics presented in [32], the proportions of switching loss under these methods are about 0.2%, 0.4%, 1.0%, and 0.2%, respectively. Combining with (3) and (4), the switching frequency of 310 Hz under the proposed method can be divided into 40 Hz for essential NLM part ($N_{\mathrm{nlm}}/2NT_1$), 250 Hz for essential PWM part ($N_{\mathrm{pwm}}/2NT_1$), and 20 Hz for additional exchange of switching states. Substituting the simulation parameters into (8), the additional switching times during a fundamental period are about 27, which is close to the actual value. In addition to the total harmonic distortion (THD), the harmonic spectrums of output current and circulating current are also provided to reflect the low-frequency characteristics, as shown in Fig. 10. Compared with reduced switching frequency NLM, voltage-balancing effect or switching frequency under the proposed method is similar, but the much better harmonic characteristics of output current and circulating current indicate the significance of replacing NLM by decomposed NL-PWM. Besides, since the capacitor voltage variation during the current control period was not considered in [27], the maximum voltage

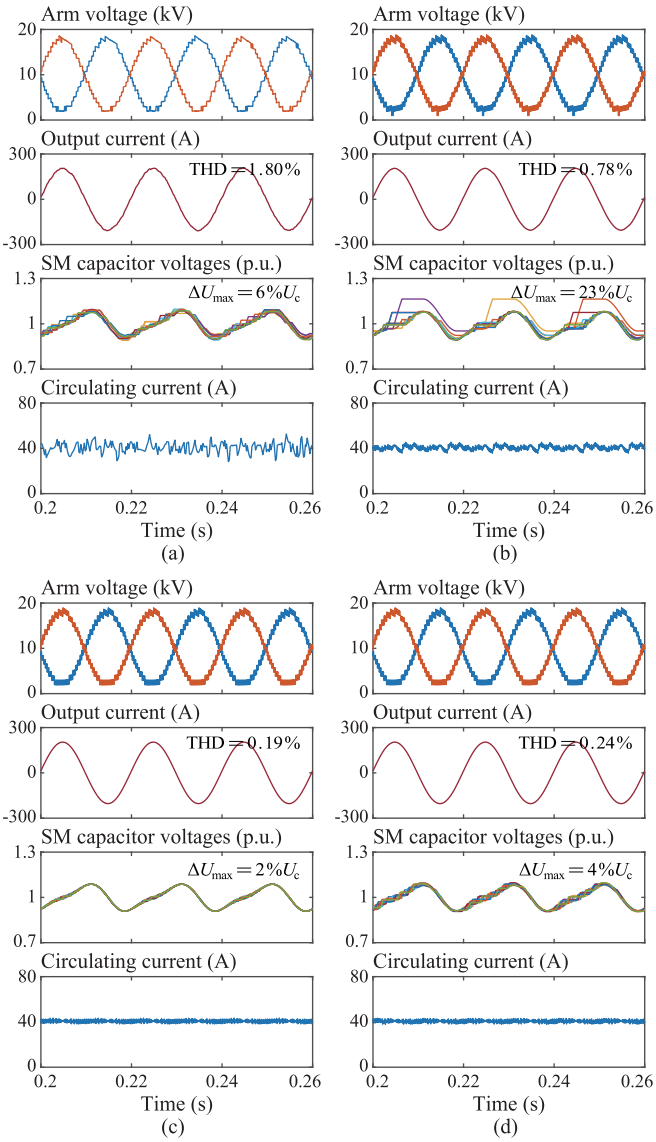

Fig. 9. Simulation waveforms of MMC under the following terms. (a) Reduced switching frequency NLM ($U_{\mathrm{th}} = 4\%U_{\mathrm{c}}$). (b) Conventional NL-PWM with optimization of switching frequency. (c) Conventional NL-PWM without optimization of switching frequency. (d) Proposed decomposed NL-PWM ($U_{\mathrm{th}} = 4\%U_{\mathrm{c}}$).

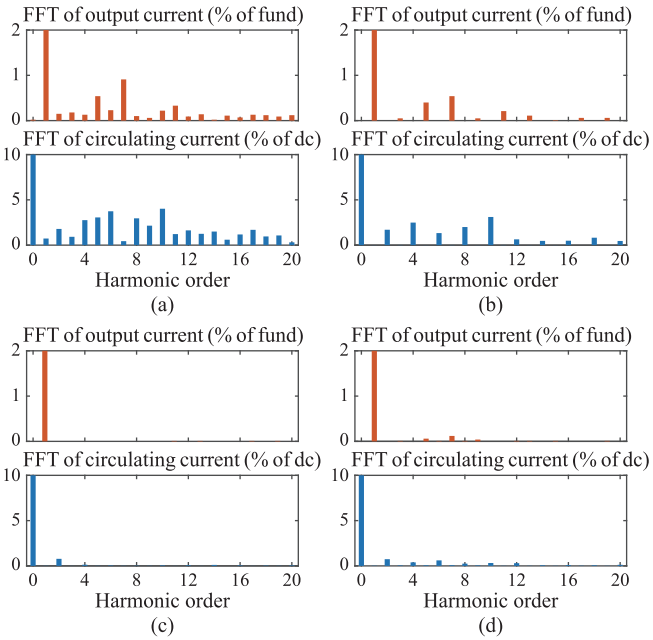

Fig. 10. (a)–(d) Harmonic spectrums of output current and circulating current corresponding to Fig. 9.

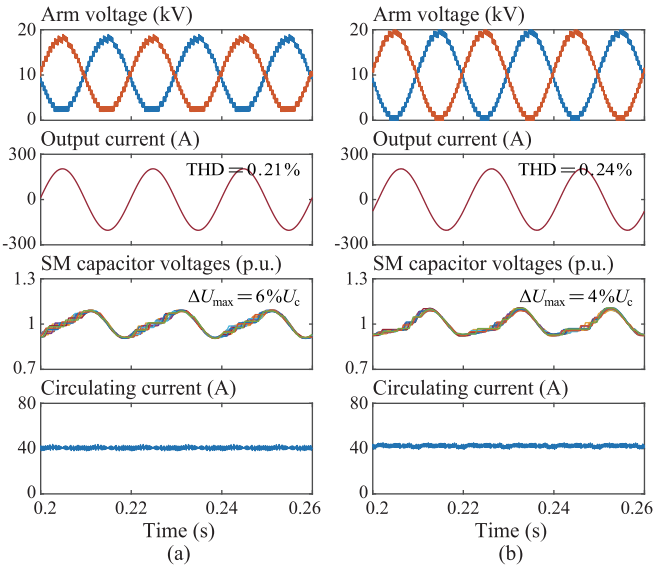

Fig. 11. Simulation waveforms of MMC under proposed decomposed NL-PWM with different parameters. (a) $m = 0.8$, $\cos\varphi = 1.0$, and $U_{\text{th}} = 6\%U_{\text{c}}$. (b) $m = 0.9$, $\cos\varphi = 0.9$ (inductance), and $U_{\text{th}} = 4\%U_{\text{c}}$.

difference $\Delta U_{\max}$ is larger than the preset U_{th}, as shown in Fig. 9(a).

As for the conventional NL-PWM method, if switching frequency is optimized as in [20], the simulation result coincides with the theoretical analysis in Section II-B. On the one hand, since voltage sorting is unactivated when $n_{\text{nlm}} = n_{\text{nlm1}}$, the continuous charging or discharging results in the major imbalance of capacitor voltages ($\Delta U_{\max} = 23\%U_{\text{c}}$). On the other hand, since some unnecessary switching transitions are generated when $n_{\text{nlm}} \neq n_{\text{nlm1}}$, the average switching frequency is still unsatisfactory (about 320 Hz for additional exchange of switching states). To avoid such significant voltage imbalance, the case of no switching optimization is also considered, as shown in Fig. 9(c). Although the current harmonics and voltage-balancing effect seem quite excellent, the switching frequency of up to 1400 Hz indicates that it is inapplicable for actual system.

In contrast, the proposed voltage-balancing strategy involving five switching modes can accurately restrict $\Delta U_{\max}$ within the preset U_{th} and the small voltage difference is beneficial for precise modulation, which results in low current harmonics. Based on the decomposition of PWM and paired operation, the proposed method cannot be simply regarded as a new tradeoff among harmonic, switching frequency, and voltage-balancing effect. To further validate the effectiveness of the proposed method and correctness of theoretical analysis, another two case studies are carried out, as shown in Fig. 11. The result indicates that higher voltage threshold, higher modulation index, or lower power factor has little impact on the control performance of MMC. Besides, the switching frequency under the voltage threshold of $6\%U_{\text{c}}$ is about 290 Hz, which is even lower than that under reduced switching frequency NLM.

For the other NLM-based methods that are not simulated here, the switching frequency in medium-voltage MMC is not further optimized in essence. That is, if $\Delta U_{\max}$ remains identical, the converter efficiency cannot be evidently promoted (even possibly demoted) on the basis of that under the proposed method. However, the harmonic characteristics under decomposed NL-PWM are significantly better. Therefore, among the NLM-based and NL-PWM-based methods, the proposed decomposed NL-PWM method possesses the distinct advantages in comprehensive performance.

B. Comparison With CPS-PWM-Based Method

The harmonic analysis of MMC under CPS-PWM and NL-PWM was carried out in [5] and [20]. Since the decomposition of PWM does not change the total output voltage, the harmonic characteristics of the basic NL-PWM also apply to the decomposed NL-PWM. According to the existing analytical conclusions, the phase voltages under NL-PWM contain odd carrier frequency harmonics and sideband harmonics near carrier frequency where the harmonic of ω_{c} (denoting the angular frequency of carriers) is the most prominent harmonic component. Since all the odd carrier frequency harmonics are cancelled in line voltages, the THD is very low even for MMC with very few SMs. However, for CPS-PWM, there exist larger sideband harmonics caused by the multicarrier modulation in line voltages.

The abovementioned conclusions are based on the assumption that all the capacitor voltages remain balanced and constant. Actually, influenced by large voltage difference, the output current and circulating current in [20] contain more harmonics compared to the proposed method. Similarly, since voltage balancing in conventional CPS-PWM depends on the individual balancing control loop, the synthesis of phase-shifted PWM with different pulse width is not as ideal as the theoretical calculation.

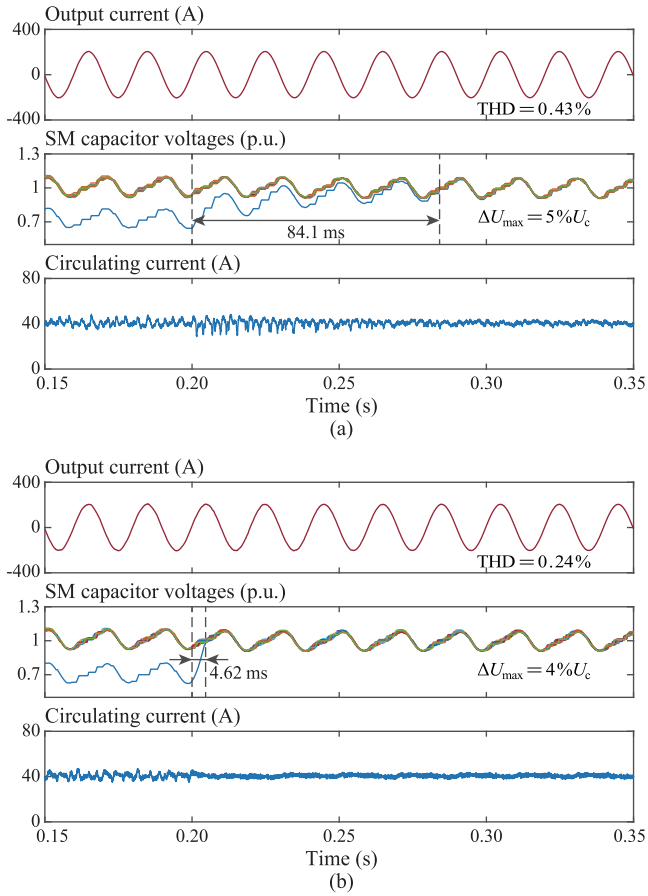

Fig. 12. Simulation waveforms of MMC during dynamic process under the following terms. (a) Conventional CPS-PWM. (b) Proposed decomposed NL-PWM.

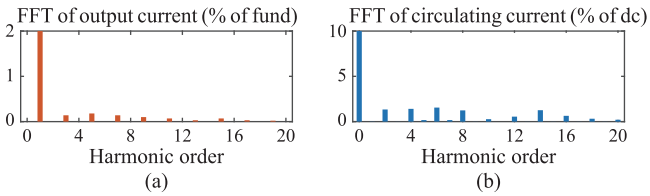

Fig. 13. (a) and (b) Harmonic spectrums of output current and circulating current under conventional CPS-PWM.

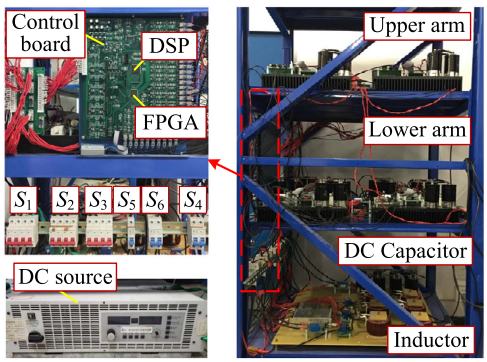

Fig. 14. Photograph of the laboratory prototype.

To verify the approximate correctness of harmonic analysis, the steady-state and dynamic performance under conventional CPS-PWM [4] and proposed decomposed NL-PWM are simulated, as shown in Figs. 12 and 13. The voltage reference of SM_1 is artificially set as $0.7U_c$ before 0.2 s and regulated to U_c at 0.2 s. It can be seen that the dynamic balancing process is much shorter under decomposed NL-PWM ($4.62 \ll 84.1$ ms) and more current harmonics are produced in the conventional CPS-PWM ($0.43\% > 0.24\%$). The carrier frequency of CPS-PWM is set as 312.5 Hz, but the actual switching frequency is around 380 Hz due to the step change of modulation signals at the beginning of each control period. Besides, once any SM is in failure and isolated, the periods, phase-shifted angles, or amplitudes of all the carriers in CPS-PWM need to be regulated accordingly [12], [13], [14], while the carrier in decomposed NL-PWM is constant in all cases. This leads to a distinct difference in the complexity of implementation. Although the dynamic performance of voltage balancing under CPS-PWM has been improved a lot in the existing literature, the abovementioned inherent limitations cannot be well-addressed. When these factors are considered, the proposed method has obvious superiority to CPS-PWM.

V. Experimental Verification

A scaled-down laboratory prototype of a single-phase MMC with six SMs per arm is developed to confirm the proposed scheme. The photograph of the experimental setup is shown in Fig. 14, with the key parameters listed in Table I. All the data acquisition, data processing, and signal generation are implemented in a digital signal processor (DSP) (TMS320F28335) and an FPGA (EP4CE10E22C8). In this section, several comparative experiments are carried out to validate the salient performance of the proposed method from different aspects. The main difference from simulation lies in the nonideality of control implementation (including control delay, dead time of driving signals, measurement errors, etc.) and number of SMs per arm.

A. Comparison With NLM-Based and NLPWM-Based Methods

Fig. 15 shows the experimental waveforms of MMC under three different methods, where $u_{cap1} \sim u_{cap6}$, u_{ap}, g_{ap1}, i_{sa}, and i_{ca} denote the SM capacitor voltages, upper arm voltage, SM switching state, output current, and circulating current, respectively. Due to fewer SMs in experiment, the arm voltage under NLM has to suffer from greater staircase approximation error, resulting in worse output waveforms. As shown in Fig. 15(a), the THD of output current is so high and cannot satisfy the application requirement. Since the probability of $n_{nlm} = n_{nlm1}$ increases with the decrease of N, the voltage imbalance under conventional NL-PWM is more serious in experiment. The maximum voltage difference is around 27 V, equal to $33.75\%U_c$. If the basic sort-plus-select strategy is adopted in conventional NL-PWM [23], the average switching frequency will reach 1800 Hz and the subsequent switching loss is unacceptable.

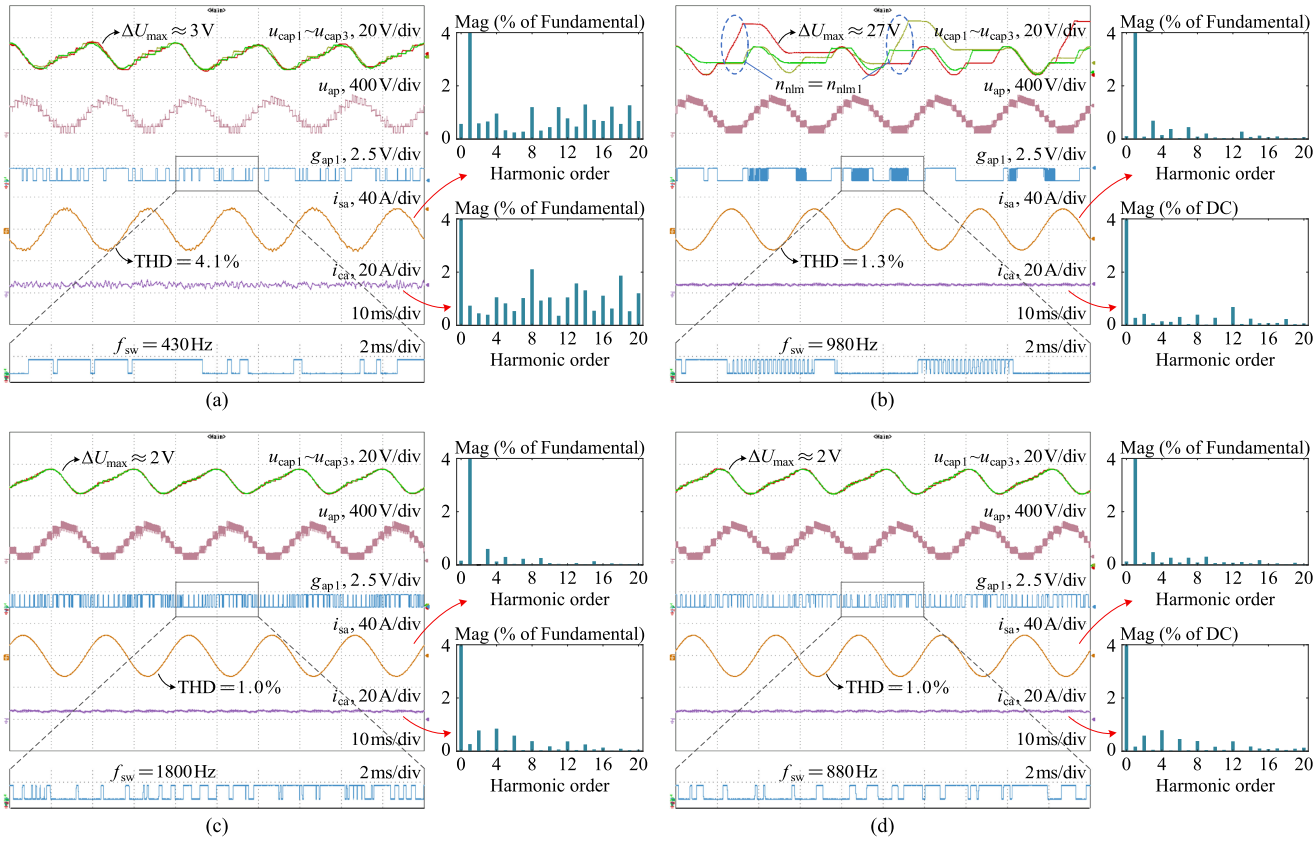

Fig. 15. Experimental waveforms of MMC under the following terms. (a) Reduced switching frequency NLM ($U_{\text{th}} = 2$V). (b) Conventional NL-PWM with optimization of switching frequency. (c) Conventional NL-PWM without optimization of switching frequency. (d) Proposed decomposed NL-PWM ($U_{\text{th}} = 2$V).

TABLE II
COMPREHENSIVE COMPARISON OF MODULATION METHODS

Modulation method	Harmonic characteristics	Balancing accuracy	Switching loss
Threshold-based NLM [27]	Not good	Medium	Very low
Level-increased NLM [15]	Good	Medium	Low
Conventional CPS-PWM [4]	Very good	High	Low
Selective-mapping PD-PWM [8]	Great	Medium	High
Conventional NL-PWM [20]	Great	High	Very high
Decomposed NL-PWM	Great	High	Low

In contrast, the proposed decomposed NL-PWM method can achieve a better tradeoff among harmonic characteristics, voltage-balancing effect, and switching frequency. The maximum voltage difference $\Delta U_{\max}$ is within 2 V, which coincides with the analytical result 1.8 V in MATLAB [by discrete calculation of (8)]. The switching frequency of 880 Hz under the proposed method mainly contains 40 Hz for essential NLM part ($N_{\text{nlm}}/2NT_1$) and 833.3 Hz for essential PWM part ($N_{\text{pwm}}/2NT_1$). Since the essential NLM and PWM parts account for a higher portion with the decrease of N, the reduction of average switching frequency (980 to 880 Hz) is not as much as that in simulation (610 to 310 Hz). But, due to the remarkable superiority in control performance, the control frequency under the proposed method can be properly reduced to further lower the switching frequency.

B. Comparison With CPS-PWM-Based Method

As shown in Fig. 16, the voltage reference of SM_1 is initially 100 V and regulated to the rated value 80 V after a while. Similar to Fig. 12, the difference of voltage-balancing control under conventional CPS-PWM and decomposed NL-PWM leads to the different dynamic process. During the dynamic process under decomposed NL-PWM, the SM with higher capacitor voltage (SM_1) is always inserted when $i_{\text{arm}} < 0$ and bypassed when $i_{\text{arm}} \geq 0$. However, the individual balancing control loop in CPS-PWM can only regulate the modulation signal a bit, thus, it requires a longer time to restore to the steady state. Besides, the THD of output current under decomposed NL-PWM is lower than that under CPS-PWM, which coincides with the theoretical analysis and simulation results. However, it should be pointed out that f_{sw} under CPS-PWM can be further decreased by regulating carrier frequency, while f_{sw} under decomposed NL-PWM cannot be further optimized here due to no additional switching transitions. Unlike simulation, $\Delta U_{\max}$ is only about $2.5\%U_{\text{c}}$, therefore the voltage-balancing effect under properly reduced carrier frequency is still acceptable.

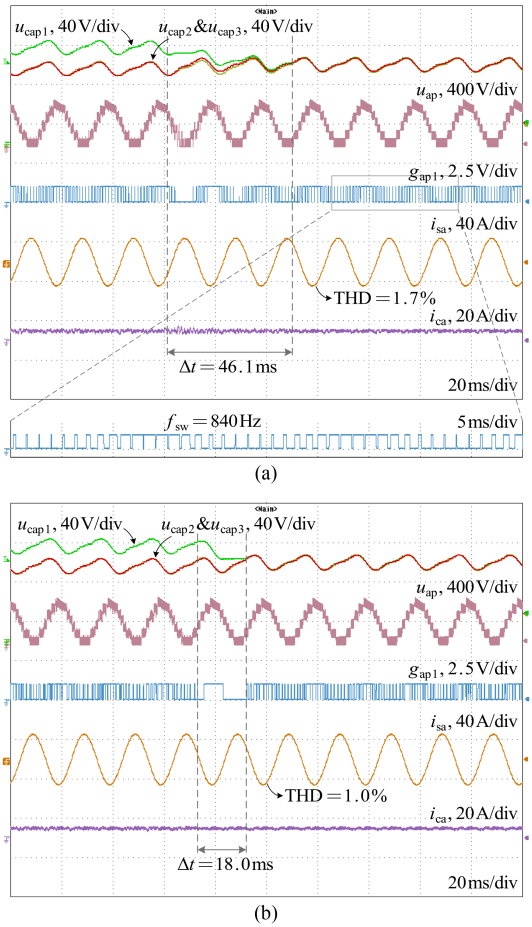

Fig. 16. Experimental waveforms of MMC under the following terms. (a) Conventional CPS-PWM. (b) Proposed decomposed NL-PWM.

From this perspective, CPS-PWM is irreplaceable in some circumstances.

C. Comprehensive Evaluation of Different Modulation Methods

For the MMC in medium-voltage applications, a comparison of some typical modulation methods and the proposed method, which encompasses a broad range of features, is given in Table II. There are some limitations in the existing methods, while the various aspects of performance under the proposed method are found to be satisfactory.

VI. Conclusion

This article proposed a decomposed NL-PWM method together with an improved voltage-balancing strategy for MMC in medium-voltage applications. By decomposing the PWM part and introducing two new switching modes, the essential switching transitions under NL-PWM can be more fully utilized to restrict the voltage difference of SM capacitors. On this basis, totally five switching modes and three types of switching transitions are considered in the proposed voltage-balancing strategy. In each control period, SMs are sorted and paired off, and the additional switching transitions are generated only if voltage differences of SM pairs cannot be restricted within the preset threshold by the essential NLM and PWM parts. Besides, to provide a guideline for determining voltage threshold, the quantitative relationship between voltage threshold and switching frequency is analyzed. With such a complete method, the switching frequency and losses in NL-PWM-based MMC can be significantly reduced without sacrificing the voltage-balancing effect, which is confirmed by simulation and experimental results. Due to the competitive advantages, the proposed method provides an alternative for modulation in MMC. Moreover, for high-voltage applications where the NLM-based methods may be preferable, the proposed paired operation for determining additional switching transitions can also be utilized.

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