An Active Equalization Method Based on an Inductor and a Capacitor for Series Battery Pack

Xiangwei Guo, *Member, IEEE*, Qi Wu, Cheng Xing, Wei Qian, *Senior Member, IEEE*, and Wenping Cao, *Senior Member, IEEE*

***Abstract*—Combining the characteristics of the high precision of inductive energy storage equalization and the fast speed of capacitive energy storage equalization, an active equalization method is proposed for a series battery pack based on an inductor and capacitor. The energy storage devices responsible for energy transfer have only one inductor and one capacitor. First, we propose the topology, analyze the working principle, and elaborate on its parameter design process. Second, an adaptive equalization control strategy matching the topology is designed. Third, based on the simulation models, the speed and efficiency characteristics of the new equalization method are verified, and the significant cost and volume advantages and the simple control characteristics are analyzed in detail. Finally, an experimental platform was built for a four-cell series battery pack to verify the effectiveness of the new equalization method for the battery pack charging and discharging process. The voltage difference is less than 80 mV.**

***Index Terms*—Active equalization, an inductor and a capacitor, easy to control, low cost, series battery pack.**

I. Introduction

As THE world moves toward the decarbonization of the power grid, industry, and transport due to environmental concerns, Li-ion battery packs have emerged as a critical early technology. They are enabling the electrification of transport as energy storage in electric vehicles and the move toward a distributed smart grid both as local energy storage for smart homes and large grid storage. A large number of cells are needed to connect in series and parallel to form a battery pack. However, battery cells can be different due to manufacturing imperfection and aging conditions, there are inevitable differences in the internal resistance, capacity, and voltage between cells. It will be more with repeated charging and discharging cycles. The inconsistency between individual cells will reduce the usable capacity and lead to excessive heat and even catch fire [1]. To improve the energy utilization rate of the battery pack and prolong its cycle life, effective equalization must be introduced to alleviate the inconsistent impact [2]. The impact of inconsistency on the series battery pack is more prominent than that on the parallel battery pack [3], [4], [5]. This article studies the equalization method of the series battery pack. The key to the research of the equalization method is the equalization topology. According to different energy transfer modes, equalization topologies are mainly divided into passive equalization and active equalization [6], [7]. Among them, active equalization uses energy storage devices, such as inductors, capacitors, transformers, or their combination to transfer energy, and the equalization process has less energy loss and high efficiency. Inductive energy storage topologies [8], [9], [10], [11] have high equalization accuracy, but the number of switches and inductors is often large, and the structure is complex. Capacitive energy storage topologies [12], [13] have the advantages of small volume and easy control. However, when there is little voltage difference between the equalization object and the capacitor, the equalization speed decreases significantly. Transformer energy storage topologies [14], [15], [16], [17], [18] have high equalization efficiency and are easy to isolate. However, the design process of winding transformers is complicated, and if there is a peak voltage, improper treatment may cause serious security risks.

Combining the characteristics of the high accuracy of inductive energy storage equalization and fast equalization speed of capacitive energy storage when the voltage difference is large, topologies based on *LC* (inductor-capacitor) energy storage have gradually become a research hotspot for active equalization methods in recent years. The topology in [19] is based on *LC* energy storage, and each cell must be configured with an *LC* series circuit. Uno and Kukita [20] used inductors, capacitors, and half-bridge converters for energy transfer. The entire topology requires only two switches, but each cell must be equipped with two capacitors, two inductors, and two diodes. Overall, the volume and cost advantages are not prominent. Dai et al. [21] used two inductors and a flying capacitor to transfer energy, and n cells needed $4n + 4$ switches, which required a large number of switches and can only achieve the discharge equalization of the target cell. The research work in [22] is based on *LC* resonance for energy transfer. Compared with that in [21], the number of switches is the same, but only an inductor, a capacitor,

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Xiangwei Guo, Qi Wu, Cheng Xing, and Wei Qian are with the School of Electrical Engineering and Automation, Henan Polytechnic University, Jiaozuo 454000, China (e-mail: gxwhpu@vip.qq.com; jxx@vip.126.com; xingcheng20210130@126.com; qwei@hpu.edu.cn).

Wenping Cao is with the School of Electrical Engineering and Automation, Anhui University, Hefei 230601, China (e-mail: caowenping@hotmail.com).

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and a diode are needed to achieve energy transfer between any single cell. The research work in [22] and [23] have similar equalization principles, but compared to that in [22], four more switches are used. The research work in [24] used a capacitor to improve the speed of inductor equalization. An inductor and a capacitor were also used to achieve energy transfer, and fewer switches were used in [24] than used in [22] and [23]. However, the energy of the capacitor in each charge or discharge cycle is not fully released, so the easy saturation of the capacitor needs to be addressed. The research work in [25], [26], and [27] used soft switching technology to switch the charge and discharge loop of the equalization object, which greatly reduced the switching loss. However, its control process was too complicated, and each switch needed to accurately calculate the duty cycle. The equalization process is a dynamic process in which multiple factors are coupled with each other, and the equalization object has a high degree of randomness due to its inconsistency, which leads to its poor anti-interference ability. Higher requirements are proposed for the switching characteristics and the operation speed of the controller, which is not conducive to hardware implementation. Moreover, in [27], each cell must be equipped with an *LC* series circuit, which is disadvantageous to the reduction in the volume and cost of the equalization system. The research work in [28] used equalizing subcircuits to transfer energy. n cells need to be equipped with $n-1$ subcircuits, but the structure of each subcircuit is slightly more complicated. Each subcircuit contains two switches, two inductors, and a capacitor, and the cost of the equalization system is higher.

Based on the above-mentioned analysis, an active equalization method with an inductor and a capacitor is proposed for the series battery pack. Compared with the previous methods, the number of switches and diodes required is moderate, but the energy storage device only needs an inductor and a capacitor. The inductor realizes the discharge equalization of the high-power cell, and the *LC* series circuit realizes the charge equalization of the low-power cell. It has the characteristics of a simple structure, simple control, low cost, fast equalization, and high efficiency.

This article is arranged as follows. Section II introduces the structure and working principle of the new topology. Section III analyzes and calculates the main parameters. In Section IV, an adaptive equalization control strategy is proposed and explained in detail. Section V analyzes the equalization performance. Section VI provides the experimental content, which verifies the effectiveness of the new method. Section VII concludes this article.

II. Topology and Equalization Principle

A. Topological Structure

The topology of the new active equalization method is shown in Fig. 1.

For the battery pack consisting of n cells, the new topology includes $2n+2$ MOSFETs, $2n-1$ diodes, and an *LC* series circuit. The topology can realize the transfer of balanced energy between cells and battery packs, battery modules, and battery packs. For the convenience of expression, take the transfer of balanced energy between cells and battery pack as an example to carry out the equalization principle analysis, parameter calculation, simulation analysis, and experimental analysis.

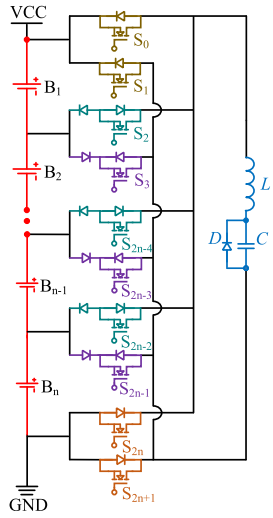


Fig. 1. Equalization topology.

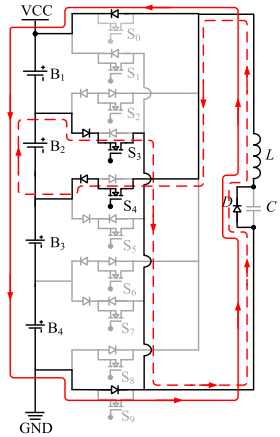


Fig. 2. Working principle of the discharge equalization of B_2.

B. Equalization Principle

The equalization principle is analyzed by taking the series battery pack composed of four cells as an example and mainly includes the discharge equalization principle of the highest power cell and the charging equalization principle of the lowest power cell. Suppose that the power of B_2 is the highest, each switching cycle of the equalization process includes two stages. Fig. 2 shows the schematic diagram of the discharge equalization principle of the highest power cell. The equalizing current diagram of one switching cycle is shown in Fig. 3.

At the initial moment, the current of the inductor is zero. At this moment, S_3 and S_4 of the MOSFET are turned ON, and the energy is transferred from B_2 to the inductor. The diode shorts the capacitor, and current flows through the diode to the inductor. The current flowing through the inductor gradually increases, as shown by the dotted line. When the current reaches the expected value, S_3 and S_4 are disconnected, and the first stage ends.

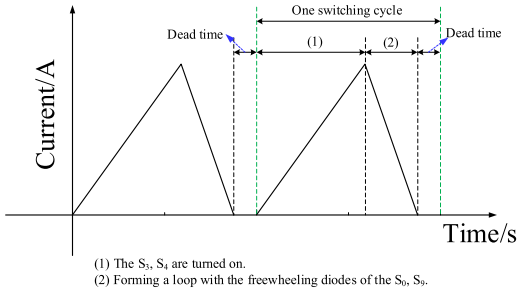


Fig. 3. Schematic diagram of discharge equalization current of B_2.

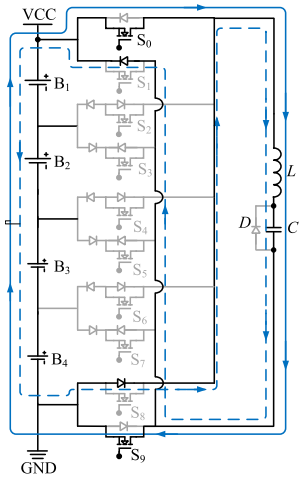


Fig. 4. Working principle of the first stage of the charge equalization of B_2.

At the same time, the inductor forms a loop with the freewheeling diodes of S_0 and S_9 of the MOSFET, as shown by the solid line. The inductor charges the series battery pack, and the inductor current gradually drops to zero. Thus far, the energy transfer of high-power cell discharge equalization for one switching cycle has been completed.

Suppose that the power of B_2 is the lowest. The equalization process of each switching cycle is also divided into two stages. Fig. 4 shows the schematic diagram of the *LC* series circuit being charged by the series battery pack in the first stage. At the initial moment, the current through the *LC* series circuit is zero. At this moment, S_0 and S_9 of the MOSFET are turned ON, diode *D* is reversed to cutoff, and the energy is transferred from the series battery pack to the *LC* series circuit. The current path is shown by the solid line. The *LC* series circuit current increases. When the equalization current reaches the expected value, S_0 and S_9 of the MOSFET are disconnected. The *LC* series circuit continues to flow through the freewheeling diodes of the MOSFET'S S_1 and S_8. The current path is shown as a dotted line. The current gradually decreases to zero, and the first stage ends. Throughout the above process, S_1 and S_8 are always disconnected, and no control signal is required.

Fig. 5 shows the schematic diagram of B_2 being charged by the *LC* series circuit in the second stage.

When the *LC* series circuit current is zero, S_2 and S_5 of the MOSFET are turned ON. At this moment, the *LC* series circuit,

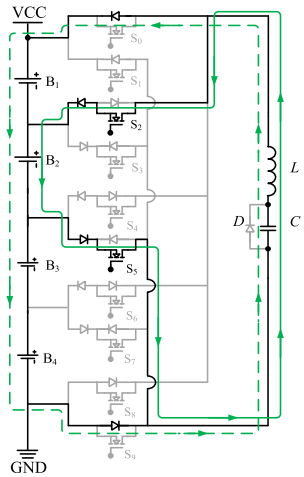


Fig. 5. Working principle of the second stage of the charge equalization of B_2.

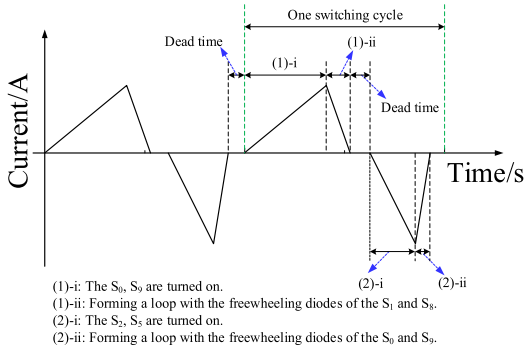


Fig. 6. Schematic diagram of charge equalization current of B_2.

B_2, and the turned-ON S_2 and S_5 of the MOSFET form a loop, as shown by the solid line. The *LC* series circuit charges B_2 and the charging current increases gradually. When the charging current reaches the expected value, S_2 and S_5 of the MOSFET are disconnected, and the current of the *LC* series circuit continues to flow through the freewheeling diodes of the MOSFET S_0 and S_9. The current path is shown by the dotted line. The current gradually drops to zero, and the second stage ends. Thus far, the energy transfer process of low-power cell charging equalization for one switching cycle has been completed.

The equalizing current diagram of one switching cycle is shown in Fig. 6.

Based on the above description, the characteristics of the new equalization method are summarized as follows.

1) The switch arrays of the battery pack are simple in structure.
2) The energy storage devices responsible for energy transfer have only one inductor and one capacitor, and the entire topology requires fewer switches, which has a significant cost advantage over the *LC* topologies in [20], [21], [22], [23], [25], [26], [27], and [28].
3) The switch and the diode are connected in series as the switch unit, the control is simple and the reliability of stable operation is high.

4) By making full use of the advantages of inductive equalization and capacitive equalization, a good balance can be achieved in terms of equalization efficiency and speed.

When using an inductor to discharge a high-power cell, the inductive discharge process does not need to control any switch conduction, which is conducive to improving the equalization efficiency. Due to the large voltage difference between a single cell and a battery pack, the duty cycle of the high-power cell discharge control signal can be increased as much as possible in one switching cycle to improve the equalization speed. When using the *LC* series circuit to charge the low-power cell, compared with inductive freewheeling equalization [8], [9], [10], [24], the equalization current increases from zero rather than from the peak current, which reduces the switching loss and improves the equalization efficiency. By introducing both an inductor and a capacitor to store energy, the equalization speed is improved under the conditions of the same switching cycle and duty cycle. Introducing an inductor and a capacitor series overcomes the problem of the decrease in the equalization speed and accuracy of the capacitor equalization process when the capacitor voltage is not much different from the equalization object.

III. Equalization Parameters Design

The parameter design includes the design for the discharge equalization of the highest power cell and the charge equalization of the lowest power cell.

Assuming that B_i has the highest power, if *i* is 1 or *n*, the B_i discharge current passes through two diodes, and if *i* is not 1 or *n*, the B_i discharge current passes through three diodes. *i* is 1 or *n*, compared with *i* is not 1 or *n*, the equalization parameters design ideas are identical, only the number of diodes in which the equalization current flows differs by 1. Since the case where *i* is not 1 or *n* is more common, taking the case where *i* is not 1 or *n* as an example illustrates the parameter design. When *i* is not 1 or *n*, suppose the voltage of B_i is V_i, the voltage of the series battery pack is *V*, the diode conduction voltage is V_D, and the MOSFET control signal period is *T*. The duty cycle of the pulsewidth modulation (PWM) that controls the conduction of S_{2i-1} and S_{2i} of the MOSFET is D_1, and the duty cycle of the inductor discharge time is D_2. The current through the inductor in one switching cycle can be expressed by

$$i_L = \begin{cases} \frac{V_i - 3V_D}{L} t, & 0 \le t \le D_1 T \\ \frac{V_i - 3V_D}{L} D_1 T & \\ -\frac{V + 3V_D}{L}(t - D_1 T), & D_1 T \le t \le (D_1 + D_2) T \\ 0, & (D_1 + D_2) T < t. \end{cases} \tag{1}$$

To prevent magnetic saturation, the inductor must work in the current discontinuous mode, when $t = T$

$$t > (D_1 + D_2) T. \tag{2}$$

Then,

$$\frac{V_i - 3V_D}{L} D_1 T - \frac{V + 3V_D}{L}(T - D_1 T) < 0. \tag{3}$$

Namely,

$$D_1 < \frac{V + 3V_D}{V + V_i}. \tag{4}$$

Since the discharge process of the inductor does not need to be controlled by the MOSFET, the D_2 parameter does not need to be designed. In one switching cycle, the maximum equalization current of the inductor is

$$I_{L\max} = \frac{V_i - 3V_D}{L} D_1 T \tag{5}$$

where I_{Lmax} is the maximum equalizing current flowing through the inductor. According to (5), *L* of the inductor can be calculated by the known switching period and maximum equalization current, combined with the duty cycle.

Assuming that B_j has the lowest power, its voltage is represented by V_j. In the first equalization stage, the duty cycle of the PWM that controls the conduction of S_0 and S_{2n+1} of the MOSFET is D_3, and the duty cycle of the PWM that controls the conduction of S_{2j-2} and S_{2j+1} of the MOSFET in the second stage is D_4. The voltage of the capacitor is u_C, and the current of the inductor is i_L, the loop resistance is *R*.

According to Kirchhoff's voltage law, the loop equations in the first stage of the equalization principle are

$$\begin{cases} V = i_L R + u_C + L\frac{di_L}{dt} \\ i_L = C\frac{du_C}{dt} \end{cases}. \tag{6}$$

From the above equations, the following can be obtained

$$V = LC\frac{d^2 u_C}{dt^2} + RC\frac{du_C}{dt} + u_C. \tag{7}$$

Solving (7) yields

$$LC\lambda^2 + RC\lambda + 1 = 0. \tag{8}$$

The discriminant of (8) is

$$\Delta = b^2 - 4ac = R^2C^2 - 4LC < 0. \tag{9}$$

Since the equivalent resistance *R* of the loop is very small and the inductance and capacitance are on the same order of magnitude, the discriminant is less than zero, and the characteristic equation has two conjugate complex root solutions. If the two solutions are λ_1 and λ_2, then

$$\begin{cases} \lambda_1 = -\frac{R}{2L} + \sqrt{\frac{4L - R^2C}{4L^2C}}\, i = \alpha + \beta i \\ \lambda_2 = -\frac{R}{2L} - \sqrt{\frac{4L - R^2C}{4L^2C}}\, i = \alpha - \beta i. \end{cases} \tag{10}$$

According to the characteristic equation method, the general solution to (8) is

$$u_{C,\text{general}} = C_1 e^{\alpha t}\cos\beta t + C_2 e^{\alpha t}\sin\beta t \tag{11}$$

where $u_{C,general}$ represents the general solution of (8). C_1 and C_2 are constants. In addition, according to (6), a special solution to (8) is

$$u_{C,\text{special}} = V. \tag{12}$$

In summary, the solution to (6) is

$$\begin{aligned} u_C &= u_{C,\text{general}} + u_{C,\text{special}} \\ &= C_1 e^{\alpha t}\cos\beta t + C_2 e^{\alpha t}\sin\beta t + V. \end{aligned} \tag{13}$$

Among them,

$$\begin{cases}\alpha = -\frac{R}{2L} \\ \beta = \sqrt{\frac{4L-R^2C}{4L^2C}}.\end{cases} \tag{14}$$

If (6) and (13) are substituted into the initial conditions $i_{\mathrm{L}}(0) = 0$ and $u_{\mathrm{C}}(0) = V_{\mathrm{Cmin}}$, then

$$u_{\mathrm{C1}} = (V_{\mathrm{C\,min}} - V)\,\mathrm{e}^{\alpha t}\left(\cos\beta t - \frac{\alpha}{\beta}\sin\beta t\right) + V \tag{15}$$

where V_{Cmin} is the initial voltage of the capacitor at the beginning of the first stage and u_{C1} is the capacitor voltage of the first stage. Similarly, the capacitor voltage u_{C2} in the second stage is

$$u_{\mathrm{C2}} = (V_{\mathrm{C\,max}} - V_j)\,\mathrm{e}^{\alpha t}\left(\cos\beta t - \frac{\alpha}{\beta}\sin\beta t\right) + V_j \tag{16}$$

where V_{Cmax} is the initial voltage of the capacitor at the beginning of the second stage. Substituting (15) and (16) into (6), the inductor current in the first and second stages can be written as

$$\begin{cases} i_{\mathrm{L1}} = C\frac{\mathrm{d}\left[(V_{\mathrm{C\,min}}-V)\mathrm{e}^{\alpha t}\left(\cos\beta t - \frac{\alpha}{\beta}\sin\beta t\right)+V\right]}{\mathrm{d}t} \\ i_{\mathrm{L2}} = C\frac{\mathrm{d}\left[(V_{\mathrm{C\,max}}-V_j)\mathrm{e}^{\alpha t}\left(\cos\beta t - \frac{\alpha}{\beta}\sin\beta t\right)+V_j\right]}{\mathrm{d}t}\end{cases} \tag{17}$$

where i_{L1} and i_{L2} represent the inductor currents of the first stage and the second stage, respectively. Simplifying (17), the expressions of i_{L1} and i_{L2} are

$$\begin{cases} i_{\mathrm{L1}} = \frac{1}{L}\,(V - V_{\mathrm{C\,min}})\,\frac{\mathrm{e}^{\alpha t}}{\beta}\sin\beta t \\ i_{\mathrm{L2}} = \frac{1}{L}\,(V_{\mathrm{j}} - V_{\mathrm{C\,max}})\,\frac{\mathrm{e}^{\alpha t}}{\beta}\sin\beta t.\end{cases} \tag{18}$$

Equations (15) and (16) are combined because the capacitor voltages are equal when the first and second phases alternate; that is, $u_{\mathrm{C1}}(0) = u_{\mathrm{C2}}(D_4T)$ and $u_{\mathrm{C2}}(0) = u_{\mathrm{C1}}(D_3T)$. By substituting this boundary condition,

$$\begin{cases} V_{\mathrm{C\,min}} = (V_{\mathrm{C\,max}} - V_j)\,\mathrm{e}^{\alpha D_4 T}\left(t\cos\beta D_4 T - \frac{\alpha}{\beta}\sin\beta D_4 T\right) + V_j \\ V_{\mathrm{C\,max}} = (V_{\mathrm{C\,min}} - V)\,\mathrm{e}^{\alpha D_3 T}\left(\cos\beta D_3 T - \frac{\alpha}{\beta}\sin\beta D_3 T\right) + V.\end{cases} \tag{19}$$

Equation (19) can be arranged as follows:

$$\begin{cases} V_{\mathrm{C\,min}} = k_1\,(V_{\mathrm{C\,max}} - V_j) + V_j \\ V_{\mathrm{C\,max}} = k_2\,(V_{\mathrm{C\,min}} - V) + V.\end{cases} \tag{20}$$

Among them,

$$\begin{cases} k_1 = e^{\alpha D_4 T}\left[\cos(\beta D_4 T) - \frac{\alpha}{\beta}\sin(\beta D_4 T)\right] \\ k_2 = e^{\alpha D_3 T}\left[\cos(\beta D_3 T) - \frac{\alpha}{\beta}\sin(\beta D_3 T)\right].\end{cases} \tag{21}$$

Substituting the known data, the equivalent resistance of the loop is close to zero, and the inductance and capacitance are on the same order of magnitude; it is easy to obtain $k < 1$.

After sorting (20) and eliminating V_{Cmax} and V_{Cmin}, we can obtain

$$\begin{cases} (1 + k_1k_2)\,V_{\mathrm{C\,min}} = k_1\,(V - V_j - k_2V) + V_j \\ (1 + k_1k_2)\,V_{\mathrm{C\,max}} = k_2\,(V_j - V - k_1V_j) + V.\end{cases} \tag{22}$$

Then,

$$\begin{cases} V_{\mathrm{C\,min}} = \frac{k_1(V - V_j - k_2V) + V_j}{1 - k_1k_2} \\ V_{\mathrm{C\,max}} = \frac{k_2(V_j - V - k_1V_j) + V}{1 - k_1k_2}.\end{cases} \tag{23}$$

Substituting (23) into (15), (16), and (18) gives

$$\begin{cases} u_{\mathrm{C1}} = V - \left(\frac{(1-k_1)(V-V_j)}{1-k_1k_2}\right)e^{\alpha t}\left(\cos\beta t - \frac{\alpha}{\beta}\sin\beta t\right) \\ u_{\mathrm{C2}} = V_j - \left(\frac{(1-k_2)(V_j-V)}{1-k_1k_2}\right)e^{\alpha t}\left(\cos\beta t - \frac{\alpha}{\beta}\sin\beta t\right)\end{cases} \tag{24}$$

$$\begin{cases} i_{\mathrm{L1}} = \left(\frac{(1-k_1)(V-V_j)}{1-k_1k_2}\right)\cdot\frac{e^{\alpha t}}{L\beta}\sin\beta t \\ i_{\mathrm{L2}} = \left(\frac{(1-k_2)(V_j-V)}{1-k_1k_2}\right)\cdot\frac{e^{\alpha t}}{L\beta}\sin\beta t.\end{cases} \tag{25}$$

According to the above equations, the maximum current and minimum current of the inductor (i.e., the maximum reverse current) can be obtained, and the expressions of i_{L1max}, i_{L2min} are

$$\begin{cases} i_{L1\,\max} = \left(\frac{(1-k_1)(V-V_j)}{1-k_1k_2}\right)\cdot\frac{e^{\alpha D_3 T}}{L\beta}\sin(\beta D_3 T) \\ i_{L2\,\min} = \left(\frac{(1-k_2)(V_j-V)}{1-k_1k_2}\right)\cdot\frac{e^{\alpha D_4 T}}{L\beta}\sin(\beta D_4 T)\end{cases} \tag{26}$$

where i_{L1max} and i_{L2min} represent the maximum equalization currents of the first stage and the second stage, respectively. In the above parameter design process, the switching frequency and duty cycle, the maximum equalization current, inductance, and capacitance are coupled. The first choice is to determine the switching frequency, duty cycle, inductance, and capacitance based on the maximum equalization current. Since the equalization efficiency is also related to the equalization object and the voltage of the equalization object has a strong uncertainty, the specific equalization efficiency value is not listed. In summary, the design of equalization topology parameters can be completed.

IV. Adaptive Equalization Control Strategy

To formulate an equalization control strategy, it is first necessary to define the characterization parameters of the consistency difference of each cell in the battery pack, namely the index of consistency. Common indexes of consistency include voltage, state of charge (SOC), internal resistance, etc. Because it is easier to set up an experimental platform and it is common to use the battery voltage as the index [16], [17], [18], [19], [20], [21], [22], [23], [24], this article takes the voltage as the index of consistency. Based on the transfer characteristics of the equalization energy in the equalization topology, to better judge the equalization object, the following adaptive equalization control strategy is designed.

First, the equalization threshold φ is set. Second, the equalization object is determined. The difference between the maximum voltage and the average voltage is set to $\Delta 1$, and the difference between the average voltage and the minimum voltage is set to $\Delta 2$. In each sampling period, when $\Delta 1$ or $\Delta 2$ is greater than the equalization threshold, if $\Delta 1 \geq \Delta 2$, the cell corresponding to the highest voltage will be discharged and balanced; if $\Delta 1 < \Delta 2$, the cell corresponding to the lowest voltage will be charged and balanced. When both $\Delta 1$ and $\Delta 2$ are less than the equalization threshold, the equalization circuit stops working.

The core problem to be solved by the equalization control is how to effectively select the equalization object when the number of cells is large. When the number of cells is large, the

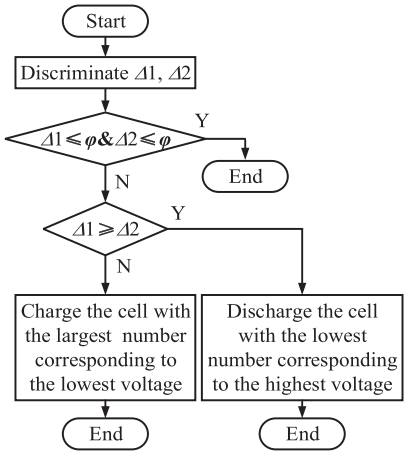


Fig. 7. Flowchart of adaptive equalization control.

TABLE I
BATTERY PARAMETERS

Parameters	Specifications
Rated Capacity	3.2 Ah
Nominal Voltage	3.7 V
Discharging End Voltage	2.5 V
Charging End Voltage	4.20±0.03 V
Internal Resistance	100 mΩ

direct result is that the number of the maximum voltage cells or the minimum voltage cells is not one. In this case, by formulating corresponding rules, the cells with the largest voltage or the cells with the smallest voltage can be selected in sequence. In this article, when the number of highest voltage cells is not one, the cell with the smallest sequence number is selected for discharge equalization, and when the number of lowest voltage cells is not one, the cell with the largest sequence number is selected for charge equalization. The equalization control strategy is shown in Fig. 7.

V. EQUALIZATION PERFORMANCE ANALYSIS

In this section, the characteristics of the new equalization method are analyzed based on the shelving state of the battery pack through the simulation model. First, we analyze the equalization speed and efficiency with different parameters. Second, we compare the equalization efficiency and speed of the new equalization method with those of the mainstream equalization methods of the same type. Finally, the more significant cost, volume advantages, and simple control of the new equalization topology are analyzed.

A. Equalization Efficiency and Speed Analysis

A battery pack composed of four cells is used as an example to build the simulation models in MATLAB/Simulink. The cell parameters are shown in Table I.

It can be seen from the parameter design process in Section III that the main factors affecting the equalization speed and efficiency include such parameters as the switching frequency, duty cycle, inductance, and capacitance. When the number of cells and the cell parameters in the pack are determined, the duty cycle of the switch control signal can be designed first. The principle of duty cycle design is to make the inductor in a critical saturation state during each switching cycle. Combining the parameter design process in Section III, the model parameters are shown in Table II.

TABLE II
PARAMETERS OF THE BALANCING MODEL

Type	Parameters	Value
Simulation model	Initial voltage/V	3.977, 3.979, 3.974, 3.973
	PWM1, PWM2, PWM3 duty cycle/%	60, 20, 40
	Dead time duty cycle/%	20
	Equalization threshold/mV	1mV
	Switching frequency/kHz	5, 10, 16, 20, 25, 32
MOSFET	FET resistance/Ω	0.1
	Internal diode resistance/Ω	0.01
	Internal diode forward voltage/V	0.6
Diode	Resistance/Ω	0.001
	Forward voltage/V	0.6

The size of the inductor and capacitor, switching frequency, equalization current, and equalization efficiency have a strong coupling relationship. Taking the equalization of the battery pack on the shelving state as an example, we study the equalization efficiency and speed under different inductance, capacitance, and switching frequency conditions. To be consistent with the actual typical values of inductors and capacitors, 12 groups of inductors and capacitors are set for efficiency and speed analysis.

The equalization efficiency is defined as the ratio of the sum of the charge of the battery pack before and after equalization, and the expression is shown in (27). Among them, SOC is obtained by the Ah integral method.

$$\eta = \frac{Q_{\text{end}}}{Q_{\text{initial}}} = \frac{C \cdot \sum_{i=1}^{n} SOC_{i,\text{end}}}{C \cdot \sum_{i=1}^{n} SOC_{i,\text{initial}}} \tag{27}$$

where Q_{end} and Q_{initial} indicate the battery pack charge at the end of equalization and before equalization. $\text{SOC}_{i,\text{end}}$ and $\text{SOC}_{i,\text{initial}}$ denote the SOC at the end of equalization and before equalization of the cell with the serial number *i*. *C* represents the rated capacity of a cell, *n* is the number of cells, $n = 4$, and the remaining power of the cell is characterized by multiplying the SOC by the rated capacity. Fig. 8 shows the simulation results.

It can be seen from Fig. 8 that when the inductance increases, the overall balancing efficiency becomes lower and the balancing speed becomes slower. This is because when the inductance increases, the current on the inductor decreases at the same time, and the equalization energy transferred per unit of time decreases. The experimental content of this article takes the inductance value of 33 μH.

When the inductance is determined, the change of capacitance has almost no effect on the balancing efficiency and speed.

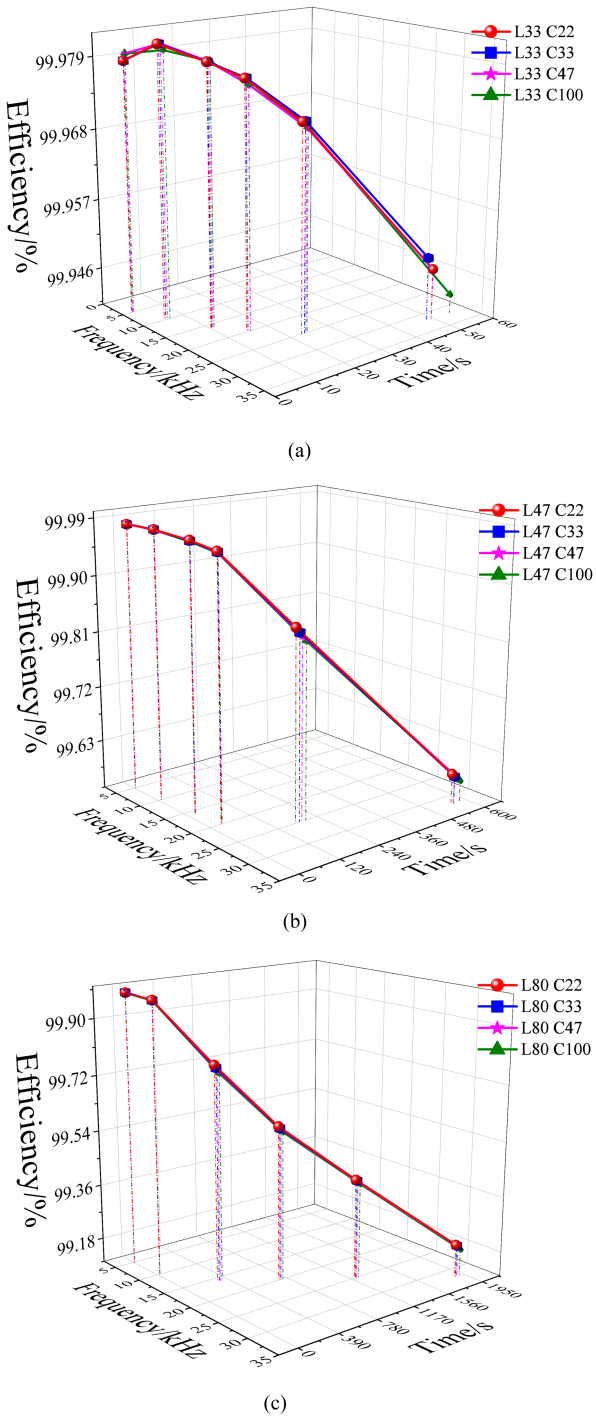


Fig. 8. Simulation results at different inductances and capacitances. (a) Equalization efficiency and time for a 33 μH inductor. (b) Equalization efficiency and time for a 47 μH inductor. (c) Equalization efficiency and time for a 80 μH inductor.

This is because the capacitor charging and discharging circuit resistance is small, and the circuit resistance is mainly composed of resistors with an internal resistance of the order of mΩ, whereas the capacitor is of the order of μF, resulting in a very small capacitor charging and discharging time constant. In the common switching frequency range, the capacitor can be fully charged or discharged in time, and the capacitor is taken as 22 μF in the experimental part of this article.

TABLE III
EQUALIZATION MODEL SIMULATION PARAMETERS

Parameter	Value
Initial voltage/V	3.977, 3.979, 3.974, 3.973
Equalization threshold/mV	1
Operating frequency/kHz	5, 10, 20
Inductance/μH	33
Capacitance/μF	22

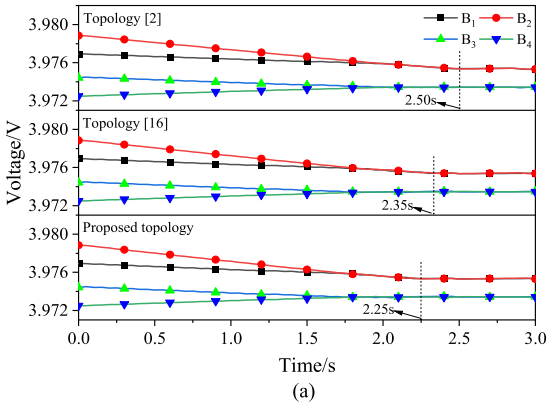
For the equalization efficiency and speed, when the switching frequency is lower, the equalization efficiency is higher and the equalization speed is faster. This is because the switching frequency decreases, the equalization current increases, the energy transferred per unit time increases, and thus the efficiency is higher and the speed is faster. When the switching frequency is higher, the equalization efficiency decreases, and the equalization speed becomes slower. This is because the equalization current is smaller when the switching frequency is higher, and the energy transferred per unit time is reduced, resulting in lower efficiency and slower speed. The greater the equalization current is, which is not better, the greater the equalization current and the greater the impact on the battery's charge and discharge efficiency and aging. In summary, the experimental part of this article finally selects a control signal switching frequency of 20 kHz.

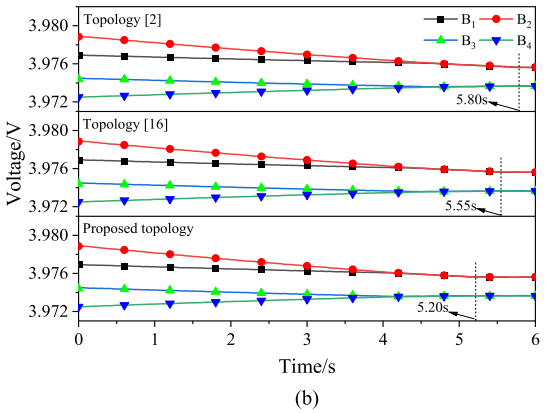
B. Comparative Analysis of Equalization Speed and Efficiency

In this article, the balanced energy is transferred between the cells and the battery pack. In this section, we compare the equalization speed and efficiency with the topologies in which the balanced energy is also transferred between the cells and the battery pack in [2] and [16]. A battery pack composed of four cells is taken as an example, and the simulation models are established in MATLAB/Simulink. The aim of the design of three topological control signals is to make the equalization current as large as possible in each equalization stage. The remaining parameters are shown in Table III, and the simulation results are shown in Fig. 9.

Table III and Fig. 9 show that the maximum initial voltage difference is 6 mV, which meets the start-up condition of the equalization circuit, and when equalization ends, the maximum difference is 2 mV, which meets the equalization stop condition. As can be seen from Fig. 9, the equalization speed of the new equalization method has certain advantages compared with the current mainstream equalization methods of the same type.

Compared with the new topology, the topology in [2], the number of diodes in which the equalization current flows is basically the same, but it includes a peak voltage absorption circuit, and part of the equalization energy is consumed by the absorption circuit, which has a certain impact on the equalization speed. In the topology presented in [16], the number of diodes in which the equalizing current flows is small, but the number of windings that it flows through is large; this is not conducive





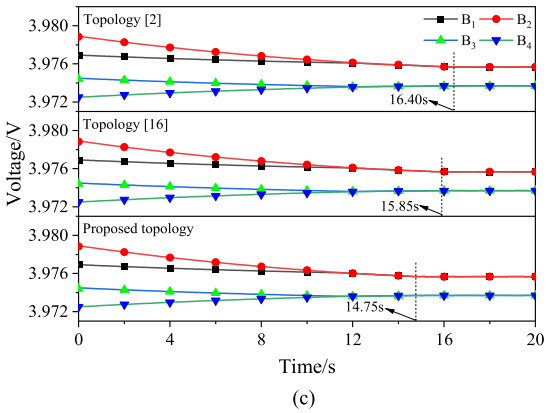


Fig. 9. Simulated equalization speeds at different switching frequencies. (a) 5 kHz. (b) 10 kHz. (c) 20 kHz.

to the effective use of the equalizing current. Compared with the topology presented in [2] and [16], the new topology does not need to go through windings in the process of equalization energy transfer, and the number of energy storage devices is small, which is beneficial to the improvement of the equalization speed. From the simulation results, the new method has a faster equalization speed than the method in [2] and [16]. Under different switching frequency conditions, compared with the topology in [2], the equalization speed of the new equalization method is improved by 10.0%, 10.3%, and 10.1% , respectively, and about 4.3%, 6.3%, and 6.9% , respectively, when compared with the topology in [16].

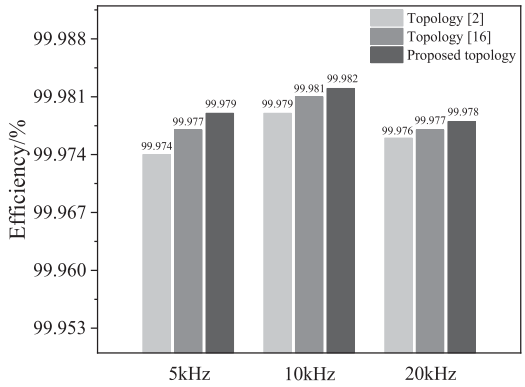


Fig. 10. Simulation results of equalization efficiency.

In addition, based on the analysis in Fig. 9, when the switching frequency is 5 kHz, the overall equalization speed of the three topologies is the highest. This is because for the same duty cycle, the lower the switching frequency is, the greater the equalization current, and the energy transferred per switching cycle also increases, which in turn leads to an increase in equalization speed. The greater the equalization current is, which is not better, the greater the equalization current and the greater the impact on the battery's charging and discharging efficiency and aging, and it is prone to overequalization. When the switching frequency is 20 kHz, the equalization current decreases and the equalization speed becomes slower, but the influence of the equalization current on the battery is also reduced.

Comparative analysis of equalization efficiency mainly studies the influence of switching frequency on equalization efficiency. Similarly, the same type of equalization method in [2] and [16] is taken as the comparison object, and the simulation model is established based on the parameters in Table III. The simulation results of the equalization efficiency are shown in Fig. 10.

It can be seen from Fig. 10 that when the switching frequency takes different values, the equalization efficiency of the new topology is higher than that of the topologies in [2] and [16]. In addition, when the switching frequency is 10 kHz, the three equalization methods have the highest efficiency. When the switching frequency is less than 10 kHz, the equalization efficiency decreases, because with the decrease of the switching frequency, the equalization current increases, and the energy loss of the energy storage device and the diode also increases. When the switching frequency rises to 20 kHz, the equalization efficiency will also decrease, because as the switching frequency increases, the equalization current decreases, and the energy loss of the energy storage device decreases, but the loss of the switch increases.

As the switching frequency increases, the difference between the new topology and the other two topologies decreases. When the switching frequency is 20 kHz, the new topology has the highest equalization efficiency and the smallest difference. In general, the new equalization method has higher equalization efficiency than the methods in [2] and [16] under different switching frequency conditions.

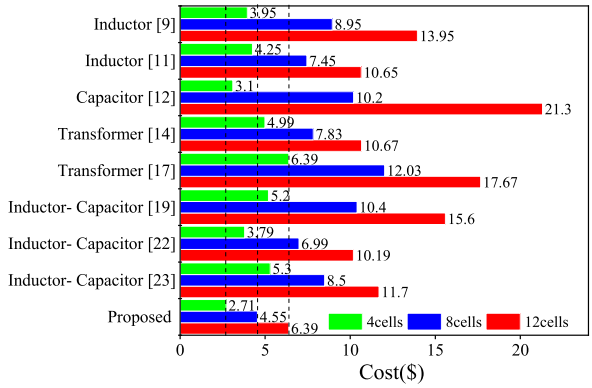


Fig. 11. Analysis of equalization topology cost.

Note that the equalization time and efficiency here is only a particular simulation example, not the speed and efficiency of the actual working process. The study in this section focuses on the trends in speed and efficiency, and not on the specific magnitudes of the actual efficiency. The actual operating process, different operating times, different initial values, different switching frequencies, and duty cycles will have an impact on the actual efficiency, but the trend of the equalization efficiency change is consistent with the simulation models.

C. Topological Cost and Volume Analysis

The 18 650 ternary lithium battery packs consisting of 4 cells, 8 cells, and 12 cells are taken as an example. Compared with that of the current mainstream topologies, the unit price of each device is determined based on [23]. The specific analysis results are shown in Fig. 11(component cost per unit ($): MOSFET (M) (0.2), diode (D) (0.03), winding (W) (0.2), transformer core (T) (0.5), inductor (L) (0.25), and capacitor (C) (0.25)).

Fig. 11 shows that compared with the current mainstream topologies, the cost of the new equalization topology is reduced. As the number of cells increases, the cost advantage becomes increasingly obvious. The topologies in [9] and [11] are based on an inductor for energy transfer. In [9], each cell must be equipped with an inductor, which is not conducive to reducing the volume and cost of the system. In [11], although the energy storage device only needs one inductor, each cell needs to be equipped with four switches, which is not conducive to reducing the cost of the equalization system. The number of topological switches in [12] is small, but the number of switching capacitors is large, which is not conducive to reducing the cost and volume of the equalization system. The research work in [14] and [17] are based on the transformer for energy transfer. Each cell of the topologies in [14] and [17] needs to be equipped with a winding and an inductor at least, which is not conducive to the reduction in the system volume and cost. The topological switch arrays in [19], [22], and [23] have the same structure and are all based on *LC* energy storage for energy transfer. Compared with the new topology, it does not require diodes but requires more switches. Moreover, in [19], each cell in the topology must be equipped with an inductor-capacitor series circuit, which greatly increases the system volume and cost.

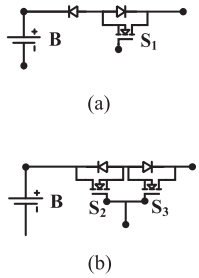


Fig. 12. Switch array unit. (a) New topology switch array unit. (b) Common topology switch array unit.

In summary, compared with the current mainstream topologies, the new topology requires an inductor and a capacitor, and each cell needs to be equipped with two switches, which is beneficial to the reduction in the equalization system cost and volume. Although the topology requires a large number of diodes, the volume and cost of diodes are much smaller than those of switches, which is beneficial to balance the reduction in system volume and cost. The proposed topology has a significant advantage in the cost and volume of the equalization system.

D. Fault Tolerance Analysis of the Control Signal Duty Cycle

Simple switch control is another significant characteristic of the new topology. The new topology switch array unit and the switch array unit based on the common *LC* energy storage topologies [22], [23] are shown in Fig. 12.

In Fig. 12(a), S_1 is turned ON, and cell B is charged. When the charging current drops to zero, the diode is reversely cutoff. At this time, even if S_1 drive signal is still present, cell B will not discharge through S_1. In Fig. 12(b), S_2 and S_3 share a common driving signal. S_2 and S_3 are turned ON, and cell B is charged. When the charging current drops to zero, S_2 and S_3 must be turned OFF immediately, otherwise, cell B is discharged through S_2 and S_3, which affects the equalization effect, and even the equalization fails. If S_2 and S_3 are turned OFF in advance, the energy storage device may be saturated. In addition, when the equalization object changes, the duty cycle of the switch array drive signal in Fig. 12(b) needs to be recalculated to ensure the smooth switching of the battery charge and discharge loop, which puts higher requirements on the computing ability of the controller. In general, the fault tolerance of the new topology control signal duty cycle is significantly higher than that of the current common topologies, and the applicability to all cells in the group is better.

VI. Equalization Experiment Analysis

A. Equalization Experiment Parameters

To verify the effectiveness of the new equalization method, an experimental platform for a four-cell series battery pack, as shown in Fig. 13, was built. The cell is a 18650 ternary lithium battery produced by Sony Corporation of Japan. The data was displayed by the DL850E oscilloscope from Yokogawa, Japan, with a maximum sampling rate of 1 MS/s. The integrated

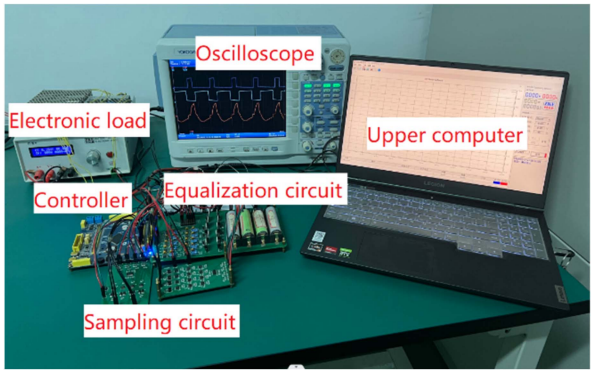


Fig. 13. Equalization experiment platform.

operational amplifiers LM124 and OP07 produced by ADI Company are used to design the signal acquisition circuit. The LM124 has good anti-common-mode voltage characteristics and is suitable as an input stage for arithmetic circuits. OP07 is a low-noise, low-offset bipolar operational amplifier, which is suitable for improving the load-carrying capacity as a voltage follower. The switch used is IRF630NPBF type N-channel enhanced MOSFET produced by Infineon Company, which has the advantages of ruggedness, low on-resistance, and fast conversion speed. Infineon's MOSFET dedicated high-speed driver chip 1EDI20N12AF is used for driving circuit design. The chip has a single-channel isolated gate driver, and has independent source current and pot current outputs to meet the experimental design requirements. Schottky diode B540C with low conduction voltage drop is selected as the diode, whose ON-state voltage drop is 0.5 V, effectively reducing the impact of the diode ON-state voltage drop on the equalization effect.

The process of equalization control is given as follows.

1) Use the A/D ports to read the cell voltage.
2) Compare the voltage of each cell and determine whether to equalize, determine the equalization object according to the control strategy.
3) The PWM wave is output to control the ON/OFF of the corresponding switches of the equalization object to complete the charging or discharging equalization process.

STM32F103ZET6 produced by STMicroelectronics is selected as the controller, which can operate at up to 72 MHz and has 16 enhanced I/O ports for inputs and outputs. the controller is used to sample the voltage signal, discriminate the equalization object and output the corresponding PWM control signal.

Based on Section III of the parameters design and Section V of the simulation models, the relevant hardware parameters of the experiment system are shown in Table IV. PWM1 is the control signal of the first stage of the high-voltage cell discharge equalization process, and PWM2 and PWM3 are the control signals of the first stage and the second stage of the low-voltage cell charge equalization process, respectively.

B. Experimental Analysis of the Equalization Function

Setting the voltage of B_2 to be the highest. Fig. 14 shows the control signal waveform, inductor current waveform, and voltage waveforms of the four cells during the five switching cycles of the B_2 discharge equalization process.

TABLE IV
PARAMETERS OF THE EQUALIZATION TOPOLOGY

Parameter	Value
Rated capacity	3.2 Ah
Rated voltage	3.7 V
PWM1 duty cycle	75%
PWM2, PWM3 duty cycle	45%, 20%
PWM2, PWM3 dead zone interval	7.5 μs
Operating frequency	20 kHz
Inductance	33 μH
Capacitance	22 μF
Equalization threshold	80 mV

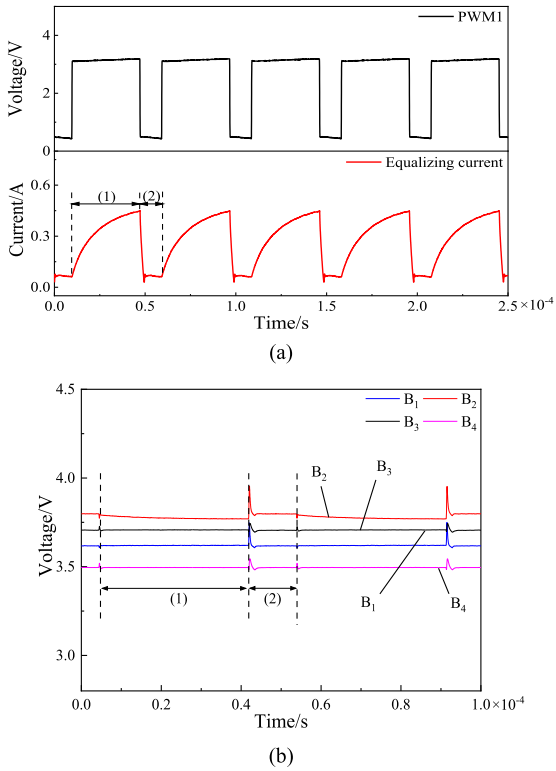


Fig. 14. Experimental waveforms of the discharge equalization of cell B_2. (a) PWM1 and inductor current. (b) Voltage of each cell.

Fig. 14(a) shows that in the first stage of a switching cycle, the current through the inductor is zero at the initial moment, and the MOSFETS S_3 and S_4 are turned ON. When the inductor current gradually increases to the expected value, the MOSFET'S S_3 and S_4 are disconnected. After that, it enters the second stage. The inductor and the freewheeling diodes of the MOSFET'S S_0 and S_9 form a loop, and the inductor charges the battery pack until the current is zero.

Fig. 14(b) shows that in the first stage, cell B_2 charges the inductor, and the voltage of B_2 drops; after that, it rises again due to the polarization effect of the lithium battery. In the second stage, the inductor charges the battery pack, and the voltages of the four cells rise as a whole. When the equalization current drops to zero, due to the polarization effect, voltages drop again.

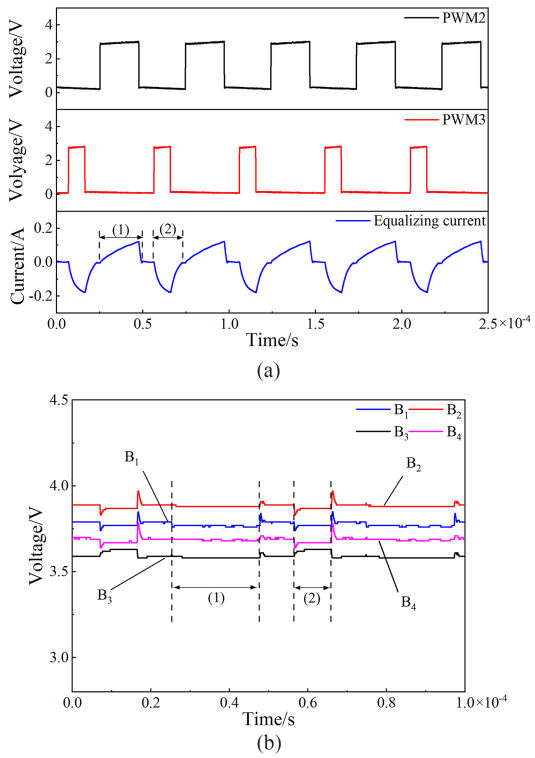


Fig. 15. Experimental waveforms of the charging equalization of cell B_3. (a) PWM2, PWM3, and LC circuit current. (b) Voltage of each cell.

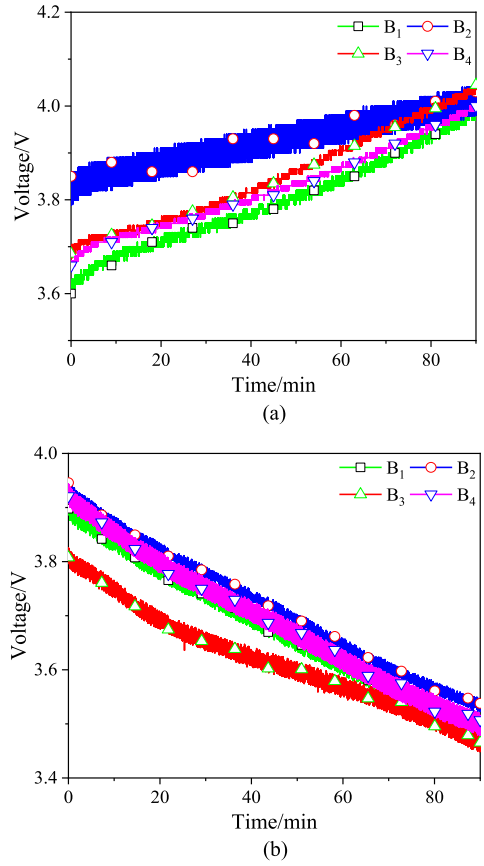


Fig. 16. Battery pack equalization experiment waveforms. (a) Equalization of the battery charging process. (b) Equalization of the battery discharging process.

Setting the voltage of B_3 to be the lowest. Fig. 15 shows the control signal waveforms, inductor current waveform, and voltage waveforms of the four cells during the five switching cycles of the B_3 charge equalization process.

Fig. 15(a) shows the control signal PWM2 of the MOSFET'S S_0 and S_9, PWM3 of the MOSFET'S S_4 and S_7, and the current of the *LC* series circuit. The energy transfer process is also divided into two stages. In the first stage, the current through the *LC* series circuit is zero at the initial moment, and the MOSFET'S S_0 and S_9 are controlled and turned ON at this moment. The battery pack charges the *LC* series circuit and the current of the *LC* series circuit increases. When the expected value is reached, the MOSFET'S S_0 and S_9 are disconnected. The *LC* series circuit and the freewheeling diodes of the MOSFET'S S_1 and S_8 form a loop, and the current begins to drop. The capacitor voltage continues to increase during the current dropping. When the current in the *LC* series circuit drops to zero, the first stage ends. After a certain dead time, equalization enters the second stage, the MOSFET'S S_4 and S_7 are turned ON, the *LC* series circuit charges cell B_3, and the current of the *LC* series circuit increases in the opposite direction. When the expected value is reached, the MOSFET'S S_4 and S_7 are disconnected, and the *LC* series circuit and the freewheeling diodes of the MOSFET'S S_0 and S_9 form a loop. At this moment, the current begins to drop, and when it drops to zero, the second stage ends. Fig. 15(b) shows the voltage change waveforms of the four cells in two switching cycles. In the first stage, the battery pack charges the *LC* series circuit. The voltage of the four cells drops overall. After charging is completed, the voltage of each cell rises, partly due to the polarization effect. In the second stage, the *LC* series circuit charges B_3, and the voltage of B_3 rises. When the equalization current drops to zero, voltages drop again due to the polarization effect.

C. Experimental Analysis of the Equalization Effect

To verify the overall equalization effect of the new method, the following two sets of equalization experiments are designed: the battery pack charging (0.7 A) equalization experiment, and the discharging (0.7 A) equalization experiment. The voltage change curves of each cell during the equalization process are shown in Fig. 16, and the change of each cell before and after equalization is shown in Fig. 17. The reason for the fluctuation in the voltage waveform is that the lithium battery has a polarization effect, and the voltage jumps when the current through the battery cell changes. When the sampling frequency is relatively high, the amount of data is large, and the phenomenon of voltage fluctuation of the resulting waveform is prone to occur, but the voltage waveform range is small, which does not affect the verification of the equalization effect.

Figs. 16 and 17 show that the initial voltage polar differences in the battery pack are 0.252 and 0.153 V in the charging state and discharging state, respectively. All of them satisfy the equalization circuit starting condition, and the equalization circuit works. After equalization for 90 min, the polar differences of each cell decrease to 72 mV and 75 mV. All of them are less

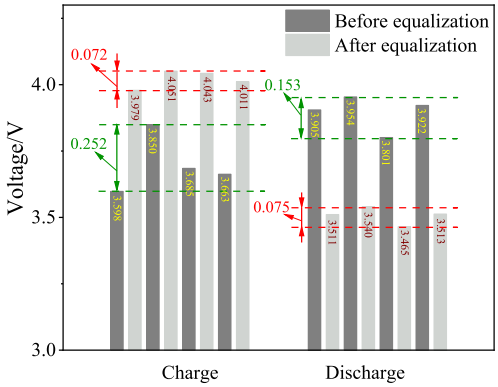


Fig. 17. Voltage change before and after equalization.

TABLE V
SOC OF EACH CELL BEFORE AND AFTER EQUALIZATION

Battery pack status	Charge	Discharge
Initial SOC/%	36.9, 67.9, 48.2, 44.9	73.0, 77.6, 62.4, 74.9
Initial SOC polar differences	31%	15.2%
Equalization time/min	90	90
Final SOC/%	80.3, 85.4, 85.4, 82.0	23.9, 28.9, 23.4, 25.1
Final SOC polar differences	5.1%	5.5%
Efficiency/%	92.672	89.993
Speed/mAh·min^{-1}	9.352	8.311

than the equalization threshold, and the equalization circuit stops working.

In addition, the equalization efficiency and speed were calculated based on the change in the remaining power of each cell before and after equalization. The following equations are to calculate the equalization efficiency and speed:

$$\eta_{\mathrm{ch}} = \frac{Q_{\mathrm{end}}}{Q_{\mathrm{initial}} + nIt} = \frac{C \cdot \sum_{i=1}^{n} \mathrm{SOC_{i,end}}}{C \cdot \sum_{i=1}^{n} \mathrm{SOC_{i,initial}} + \mathrm{nIt}} \tag{28}$$

$$\eta_{\mathrm{dis}} = \frac{Q_{\mathrm{end}} + nIt}{Q_{\mathrm{initial}}} = \frac{C \cdot \sum_{i=1}^{n} \mathrm{SOC_{i,end}} + nIt}{C \cdot \sum_{i=1}^{n} \mathrm{SOC_{i,initial}}} \tag{29}$$

$$S_{\mathrm{ch}} = \frac{\sum_{i=1}^{n} |[C \cdot (\mathrm{SOC_{i,end}} - \mathrm{SOC_{i,initial}}) - It]|}{t} \tag{30}$$

$$S_{\mathrm{dis}} = \frac{\sum_{i=1}^{n} |[C \cdot (\mathrm{SOC_{i,end}} - \mathrm{SOC_{i,initial}}) + It]|}{t} \tag{31}$$

where Q_{end} indicates the battery pack charge at the end of equalization, and Q_{initial} indicates the initial charge of the battery pack before equalization. $\mathrm{SOC}_{i,\mathrm{end}}$ denotes the SOC at the end of the equalization of the cell with the serial number i. $\mathrm{SOC}_{i,\mathrm{initial}}$ denotes the initial SOC before the equalization of the cell with the serial number i. C represents the rated capacity of a cell and t represents the duration of the equalization experiment, which is 90 min. n is the number of cells (here $n = 4$), and the remaining power of the cell is characterized by multiplying the SOC by the rated capacity. The SOC at the beginning and end of the equalization is obtained by the open-circuit voltage method [24], and Table V gives the specific calculation results of the equalization efficiency and speed. It should be noted that the equalization efficiency and speed in Table V are only the values of this experimental case. Several equalization experiments show that when the initial voltage of the equalization object, load current, energy storage device parameters, switching frequency, and duty cycle change, the equalization efficiency and speed also change accordingly.

Table V shows that the polar differences of SOC of each cell at the end of the equalization are significantly reduced compared with that before the equalization. In summary, the proposed active equalization method based on an inductor and a capacitor in this article has a good equalization effect in the charging and discharging process, and can significantly improve the consistency of the series battery pack.

VII. CONCLUSION

Aiming at the inconsistency of the cells in the series battery pack, a single-inductor and single-capacitor energy storage active equalization method is proposed, which has a simple topology, simple control, and significant cost advantages. The simulation model verifies the characteristics of the new equalization method in terms of equalization speed and efficiency compared with the same type of equalization method. Through the analysis of the cost and control method of different types of topologies, the more significant cost advantages and simple control characteristics of the new equalization topology have been verified. The effectiveness of the new equalization method in the charging and discharging process of the battery pack is verified by building an experimental platform. In general, the new equalization method can significantly improve the consistency of the series battery pack, thereby improving the overall performance of the battery pack, and is suitable for electric vehicles or energy storage systems. Future research mainly focuses on, when the number of battery cells increases, how to reduce the impact of the equalization process on the battery pack, thereby improving the adaptability of the equalization topology. One of the ideas is to use the cluster equalization control method to improve the efficiency, speed and adaptability of the proposed topology.

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Xiangwei Guo (Member, IEEE) received the M.S. degree in power engineering from Henan Polytechnic University, Jiaozuo, China, in 2012, and the Ph.D. degree in power electronics from South China University of Technology, Guangzhou, China, in 2016.

In 2016, he joined the School of Electrical Engineering and Automation, Henan Polytechnic University as an Assistant Professor. He has authored one book and more than 30 articles and holds more than 10 Chinese inventions. His primary research interests include power electronics and their applications in battery management systems.

Qi Wu was born in Anyang, Henan Province, China, in 1999. He received the bachelor's degree in electrical engineering in 2020 from Henan Polytechnic University, Jiaozuo, China, where he is currently working toward the master's degree

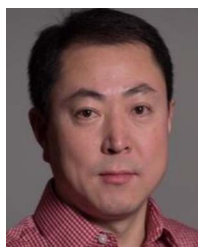
His research interests include energy management for lithium-ion batteries, especially the research of battery balancing topology and control strategy.

Cheng Xing received the B.S. degree in 2020 from the School of Electrical Engineering, Henan Polytechnic University, Jiaozuo, China, where he is currently working toward the M.S. degree with the School of Electrical Engineering and Automation.

His research interests include electric vehicle battery management system and power electronics and power drives.

Wei Qian (Senior Member, IEEE) received the B.S. degree in mechanical engineering from Zhengzhou University, Zhengzhou, China, in 1999, the M.S. degree in control theory and control engineering from Southeast University, Nanjing, China, in 2005, and the Ph.D. degree in control theory and control engineering from Zhejiang University, Hangzhou, China, in 2009.

Since 2015, he has been a Professor with Henan Polytechnic University, Jiaozuo, China,. His research interests include networked control systems, delayed systems, and switching systems.



Wenping Cao (Senior Member, IEEE) received the B.Eng. degree in electrical engineering from Beijing Jiaotong University, Beijing, China, in 1991, and the Ph.D. degree in electrical machines and drives from the University of Nottingham, Nottingham, U.K., in 2004.

He is currently a Chair Professor of Electrical Power Engineering with Aston University, Birmingham, U.K., and also a Distinguished Professor with the School of Electrical Engineering and Automation, Anhui University, Hefei, China. His research interests include fault analysis and condition monitoring of electrical machines and power electronics.

Prof. Cao is the Chairman of the Industrial Electronics Society, IEEE U.K. and Ireland Section, and a "Royal Society Wolfson Research Merit Award" holder, U.K.