A New Shared Module Soft Open Point for Power Distribution Network

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***Abstract*—The soft open point (SOP), as a sort of promising flexible power electronic device in place of the normal open point, can improve the operating flexibility of a distribution network. However, the traditional cascaded-H-bridge (CHB)-based SOP requires a large number of H-bridge modules and high-frequency transformers, which are costly and bulky. In this article, a shared module SOP (SMSOP) topology is proposed based on CHB. The modules of the SMSOP topology are divided into shared modules and nonshared modules. Both the input and output stages of the nonshared modules are connected in series with the terminals of the shared modules to connect two ac grids. Compared with the traditional CHB-based SOP, this topology can reduce the number of H-bridge modules and high-frequency transformers. Mathematical models are derived, and control strategies as well as feasible areas are discussed. A design method is proposed to minimize the number of modules. Finally, the correctness and validity of the proposed SMSOP are verified by simulation and experimental results.**

***Index Terms*—Distribution network (DN), double-loop control, shared module, soft open point (SOP).**

I. Introduction

NOWADAYS, the power system is undergoing tremendous changes with more and more distributed generators (DGs) and energy storage systems being equipped into the utility. The growth of DGs and loads, such as photovoltaic plants and electric vehicles, brings serious problems for the distribution network (DN) due to the higher peak demand and voltage drop on feeders. Traditional regulation methods, such as normally open points (NOPs) and on-load tap changers of transformers, cannot satisfy the requirements of real-time continuous regulation [1], [2]. Therefore, soft open points (SOPs) are proposed to obtain a flexible DN with power flow control [3], [4].

The SOP is a new power electronic device applied to DNs and is responsible for flexibly interconnecting between two feeders to replace the NOP as shown in Fig. 1 [5], [6]. Compared with the traditional NOP, the SOP not only continuously regulates active power flow between feeders [7], [8], [9], [10] but also provides numerous auxiliary functions, such as improved load balancing [11], [12], multiple port interfaces [13], and fast fault isolation and supply restoration [14], [15].

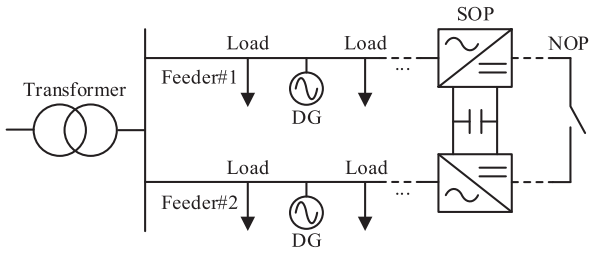

Fig. 1. Basic architecture of the SOP in DNs.

The SOP can be classified into the following two categories: ac–ac topology and ac–dc–ac topology. The ac–ac topology features fewer power conversion stages and lower power losses. However, the ac–ac topology cannot compensate for reactive power due to the lack of dc-link capacitors. In addition, disturbances on one side may also affect the other side [16]. In practical applications, the ac–dc–ac topology is more popular because dc-link connectivity is available [17] and more functions can be provided.

Several SOP topologies can be used for DN, such as cascaded-H-bridge-based SOP (CHB-based SOP) [17], [18], back-to-back modular multilevel converters (BTB-MMC) [19], direct MMC [20], and M3C-based SOP [21], [22]. In [18], a CHB-based SOP is designed to interconnect two 6.6-kV DNs, as shown in Fig. 2(a). It consists of three stages, i.e., an input stage based on an H-bridge rectifier, an isolation stage with a high-frequency transformer, and an output stage based on the H-bridge inverter. This topology can regulate power factor, reduce voltage stress, and allow bidirectional power flow as well as electrical isolation. But the cost is higher due to a large number of H-bridge modules and high-frequency transformers. In [19], a BTB-MMC topology is proposed as shown in Fig. 2(b), which is suitable for higher voltage applications. The MMC has six arms, each of which includes several submodules and filter inductors. The arm circulating current suppression [23] and submodule dc voltage balancing [24] of the MMC are the key problems. In addition, BTB-MMC requires a large number of submodules. Pereda and Green [20] proposed a direct MMC topology. It uses the same number of semiconductors as the BTB-MMC, but it requires half the number of capacitors and coupling inductors. However, direct MMC has the same drawback as BTB-MMC, that is, it requires a large number of submodules. Erickson and Al-Naseem [21] proposed an M3C converter with the advantages of low

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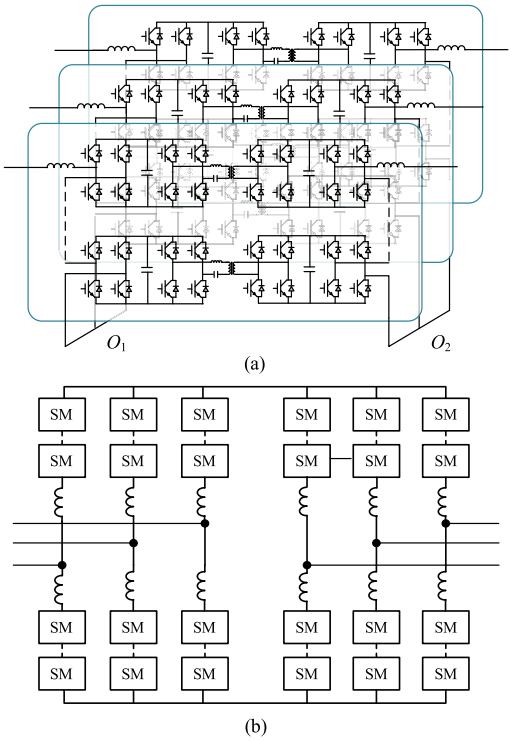

Fig. 2. Traditional SOP Topologies. (a) Topology of CHB-based SOP. (b) Topology of BTB-MMC.

switching losses and small device size. However, the topology of M3C-SOP is complex and the arm circulating current suppression is difficult. Li et al. [22] compared the M3C-SOP with the BTB-MMC and concluded that the operating range of the M3C-SOP is narrower than that of the MMC.

Compared with the previous work on the SOP, this article makes multiple contributions, which are summarized as follows.

1) A new shared module SOP (SMSOP) for power DN is proposed, which can save on the quantity of submodules and high-frequency transformers. Most of the power flows directly through the shared modules, whereas the rest flows through the isolation stage of nonshared modules, which can reduce the switching losses and transformer losses of the isolation stage and hence improve the overall efficiency. In addition, the operation principles are illustrated, and mathematical models are derived.
2) In order to ensure the stable operation of SMSOP, control strategies are proposed and feasible operation areas are given. The SMSOP is suitable for connecting two grids with the same amplitudes but different phases. If the two grid voltages are in phase, the SMSOP requires a slight change in power factor.
3) A design method for minimizing the quantity of modules is illustrated and an example is given. In addition, the power loss analysis is illustrated to explain why the SMSOP has low power loss.

The rest of this article is organized as follows. The proposed SMSOP topology, together with the modeling and operation principles, are described in detail in Section II. Section III is dedicated to the control strategy of the proposed SMSOP. In Section IV, a design method to minimize the number of modules is proposed, a design example is given, and the comparison of the proposed SMSOP with other SOP topologies is listed. In addition, the power loss analysis is illustrated. Simulations and experiments are presented in Section V to verify the effectiveness of the proposed SMSOP. Finally, Section VI concludes this article.

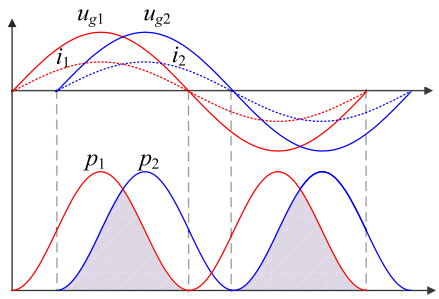

Fig. 3. Instantaneous power of two ac grids.

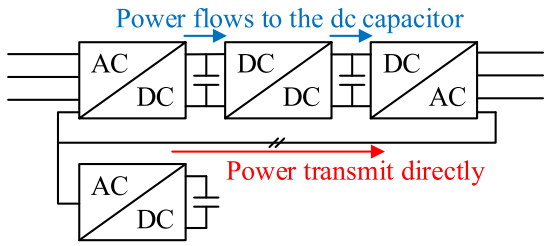

Fig. 4. Power flow in the proposed three-phase SMSOP.

II. Proposed SMSOP

A. Basic Idea and the Derivation of the Proposed SMSOP

The basic idea of the proposed SMSOP topology is as follows. When there is a phase difference between two ac grids, there is also a phase difference between the input instantaneous power p_1 and the output power p_2, as shown in Fig. 3. The power of the overlapped part can be transmitted directly without the dc capacitor. Therefore, the shared module is proposed to transmit the power of the overlapped part directly, and the rest of the power flows to the dc capacitor of the nonshared modules. Fig. 4 shows the power flow in the proposed three-phase SMSOP. The power flow shown by a red line in Fig. 4 corresponds to the overlapped part in Fig. 3, and the rest of the power flow is shown by a blue line in Fig. 4.

Fig. 5 illustrates the topology of the proposed three-phase SMSOP for DN. The topology consists of two types of modules: shared modules and nonshared modules. Each nonshared module is divided into three stages: the rectifier stage, the isolation stage, and the inverter stage, which is similar to the conventional CHB-based SOP topology connected to two ac terminals with a Y connection. The SMSOP differs from traditional SOP topologies in that it contains shared modules. It can be seen that each shared module consists of full bridges only. To reduce the number of components, both the input and output stages of the

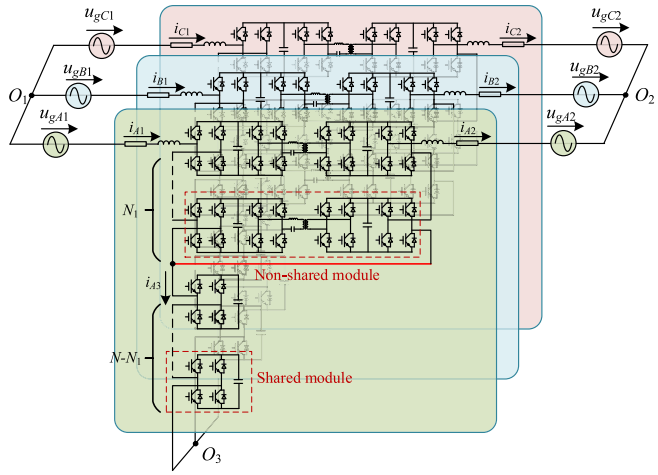

Fig. 5. Topology of the proposed three-phase SMSOP.

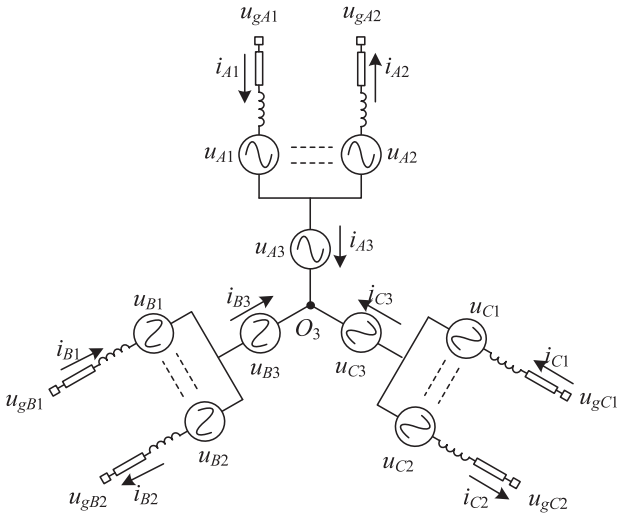

Fig. 6. Simplified equivalent circuit of the proposed SMSOP.

nonshared modules are connected in series with the ac terminals of the shared modules. As can be seen from Fig. 5, the shared module, as a common part, can reduce the quantity of H-bridge modules and high-frequency transformers, thus reducing the size and cost and improving the efficiency. Each phase of this topology consists of N_1 nonshared modules and $(N-N_1)$ shared modules.

Most of the power flows directly to the output stage through the wire (the red solid line in Fig. 5), connecting the ac terminals of shared modules to the output terminals of nonshared modules, whereas the rest flows through the isolation stage of nonshared modules.

B. Modeling of the Proposed SMSOP

The rectifier stage of the nonshared module is responsible for converting the ac bus voltage to the dc-link voltage while regulating the unity power factor. The simplified equivalent circuit of the proposed SMSOP is shown in Fig. 6. The voltage equations of the input and output stages are given as follows:

$$u_{gi1} = L_1 \frac{di_{i1}}{dt} + u_{i1} + u_{i3} \tag{1}$$

$$u_{gi2} = -L_2 \frac{di_{i2}}{dt} + u_{i2} + u_{i3} \tag{2}$$

where u_{gi1} and u_{gi2} (i = A, B, C) are the input-side and output-side grid voltages, respectively. u_{i1} and u_{i2} are the input-side and output-side ac terminal voltages of the nonshared modules, respectively. u_{i3} is the ac terminal voltage of the shared module. L_1 and L_2 are filter inductors.

The current equation of the SMSOP is given as follows:

$$i_{i1} = i_{i2} + i_{i3} \tag{3}$$

where i_{i1} and i_{i2} are the input-side and output-side ac currents, respectively. i_{i3} is the ac current flowing into the shared modules.

The *dq* transformation is applied to (1)–(3), and the differential equations in *dq* coordinates are derived as follows:

$$L_1 \frac{di_{1dq}}{dt} = \pm\omega L_1 i_{1qd} + u_{g1dq} - u_{1dq} - u_{3dq} \tag{4}$$

$$-L_2 \frac{di_{2dq}}{dt} = \mp\omega L_2 i_{2qd} + u_{g2dq} - u_{2dq} - u_{3dq} \tag{5}$$

$$i_{1dq} = i_{2dq} + i_{3dq}. \tag{6}$$

The isolation stage SRC, which is comprised of two full bridges, a series resonant *LC,* and a high-frequency isolation transformer, is a key part of SMSOP. It is worth mentioning that the isolation stage is necessary. If the isolation stage is removed and the nonshared module is constructed by the BTB-VSC, the dc capacitor will be shorted due to the presence of the middle line (the red solid line in Fig. 5).

The control strategy of SRC is illustrated in Section III. The voltage gain of SRC is as follows [25]:

$$U_R = \frac{U_{\mathrm{dc2}}}{U_{\mathrm{dc1}}} = \frac{w_R^2}{w_R^2(P_R+1) + j \cdot Q_R(w_R^2-1)} \tag{7}$$

where w_R is the ratio of the switching frequency to the resonant frequency. U_{dc1} and U_{dc2} are the primary and secondary dc voltages, respectively. P_R and Q_R represent the ratio between losses in the series parasitic resistance R_s and series inductor L_s with respect to the base power.

C. Feasible Area

The vector diagram is analyzed to illustrate the feasible area of the proposed SMSOP topology. For simplicity, the SMSOP operates at unity power factor.

The ac currents i_1 and i_2 can be determined as follows:

$$p = \frac{3}{2}\left(u_{g1d}i_{d1} + u_{g1q}i_{q1}\right) = \frac{3}{2}\left(u_{g2d}i_{d2} + u_{g2q}i_{q2}\right). \tag{8}$$

Here, we only consider the case that u_{g1} and u_{g2} have the same amplitude but different phases. Therefore, ac currents i_1 and i_2 also have the same amplitude but different phases. As shown in Fig. 7, i_1 is in phase with u_{g1}, and i_2 is in phase with u_{g2}. According to (3), the vector of i_3 can be calculated as $i_1 - i_2$. The maximum amplitude of u_1 and u_2 is restricted by the dc-link

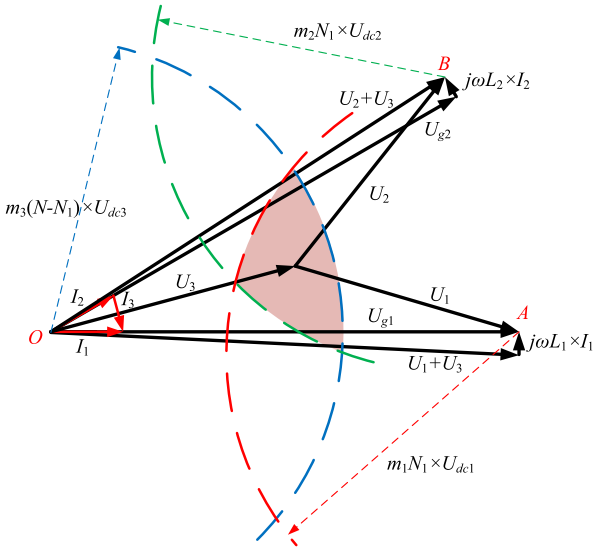

Fig. 7. Feasible area of SMSOP.

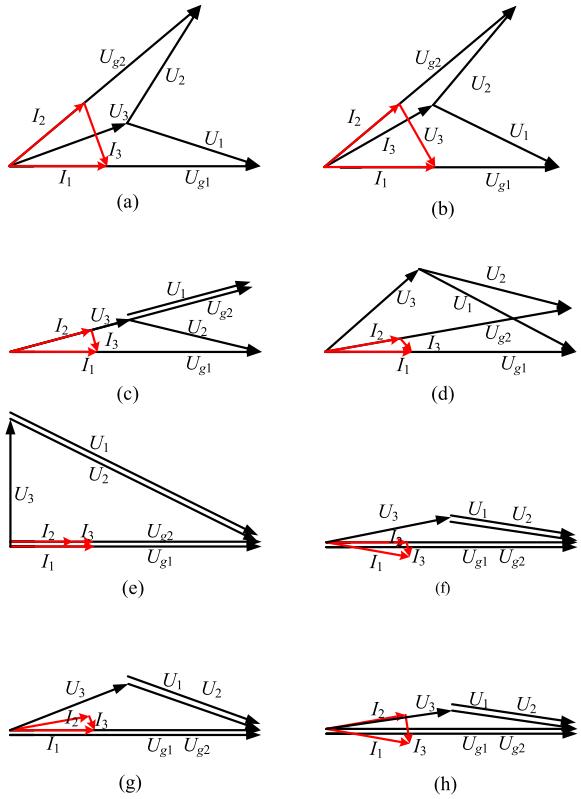

Fig. 8. Vector diagram of SMSOP in different cases. (a) U_{g1} and U_{g2} have the same amplitude but with a 30° phase difference. (b) Amplitude of U_{g1} and U_{g2} is different. (c) Phase difference of U_{g1} and U_{g2} is equal to the threshold value. (d) Phase difference of U_{g1} and U_{g2} is smaller than the threshold value. (e) U_{g1} and U_{g2} are in phase. (f) Changing the power factor of the input stage. (g) Changing the power factor of the output stage. (h) Change the power factor of input and output stages.

capacitor voltages $U_{\rm dc1}$ and $U_{\rm dc2}$, the modulation indexes m_1 and m_2, and the quantity of nonshared modules N_1. Similarly, the maximum amplitude of u_3 is restricted by the dc-link capacitor voltage $U_{\rm dc3}$, the modulation index m_3, and the quantity of shared modules N–N_1. The operation range of the nonshared modules in the input and output stages can be determined by drawing a circle with A and B as the origin, and $m_1N_1U_{\rm dc1}$ and $m_2N_2U_{\rm dc2}$ as the radius (the green and red dashed arcs in Fig. 7), respectively. Similarly, the operation range of the shared modules can also be determined by drawing a circle with O as the origin, and $m_3(N\text{-}N_1)U_{\rm dc3}$ as the radius (the blue dashed arc in Fig. 7). Finally, the shaded (overlapped) area surrounded by the three circles is the feasible area of steady operation. Since the shared modules are only connected to the capacitors but not to the active loads, the shared modules only consume reactive power. Therefore, the current of shared module i_3 is orthogonal to terminal voltage u_3, which determines the amplitude and phase of i_3 and u_3.

It can be seen from Fig. 7, when u_3 is operating outside the shaded area, the ac terminals of the nonshared module cannot provide a large enough ac voltage, and the SMSOP will not be able to operate stably in this case. Therefore, the SMSOP can operate steadily only if u_3 is operating in the shaded area.

D. Operating Point Analysis in Different Cases

According to the phase difference between the two grids, Fig. 8 shows the vector diagram of SMSOP under different operating conditions. Fig. 8(a) and (b) shows a large phase difference between the two grids, and Fig. 8(c) indicates a threshold phase difference. The phase difference in Fig. 8(d) is smaller than the threshold value, and Fig. 8(e)–(h) shows no phase difference. For simplicity, the voltages across the filter inductor are ignored.

In Fig. 8(a), two grid voltages U_{g1} and U_{g2} have the same amplitude but with a 30° phase difference. In this case, the larger the amplitude of U_3, the smaller the amplitude of U_1 and U_2. Therefore, a large output voltage U_3 of shared modules is necessary to ensure that the steady-state point operates in the feasible area. However, there may be a 5% deviation in the amplitude of the two ac grids connected by the SOP in practice. For the sake of clarity, here $U_{g1} = 87.5\%\ U_{g2}$ as shown in Fig. 8(b). It can be seen that the terminal voltages U_1 and U_2 of the nonshared modules are reduced due to the presence of the shared module terminal voltage U_3. This conclusion remains the same as long as the phase of U_3 is between the angle formed by U_{g1} and U_{g2}. Since U_3 is orthogonal to i_3, the phase of U_3 is mainly affected by i_1 and i_2, and the deviation of the grid voltage amplitude has less influence on the operating state of SMSOP.

The amplitude of i_2 is smaller than the amplitude of i_1 due to the power loss of SMSOP. When the phase difference between U_{g1} and U_{g2} is small, the amplitude difference of i_1 and i_2 due to power losses has a significant effect on the operating state of SMSOP, as shown in Fig. 8(c)–(e). The efficiency of SMSOP is assumed to be 95%, i.e., $i_2 = 95\%\ i_1$. It can be seen from Fig. 8(c) that when the phase difference between U_{g1} and U_{g2} is 18°, U_3 is exactly in phase with U_{g2}. In Fig. 8(d), the phase difference between U_{g1} and U_{g2} is less than 18° and U_3 lies outside the angle formed by U_{g1} and U_{g2}. Fig. 8(d) also shows the vector diagram of U_{g1} and U_{g2} in the same phase. It can be seen that U_3 is orthogonal to U_{g1} and U_{g2} due to power loss. In this case, insulated gate bipolar transistors (IGBTs) are subjected to a higher voltage stress and the operating point of

SMSOP is outside the feasible area. Therefore, situations such as shown in Fig. 8(c)–(e) should be avoided.

To avoid the operating point of SMSOP outside the feasible area when the phase difference between U_{g1} and U_{g2} is small, the power factor of the SMSOP can be changed appropriately, thus changing the phase of U_3, as shown in Fig. 8(f)–(h). In Fig. 8(f), the input stage operates at the unit power factor, whereas the output stage generates inductive reactive power with a power factor of 0.985. In Fig. 8(g), the output stage operates at unit power factor, whereas the input stage generates capacitive reactive power with the same power factor of 0.985. In Fig. 8(f), the power factor is 0.985 for both the input and output stages, where the input stage generates inductive reactive power, and the output stage generates capacitive reactive power. In Fig. 8(f)–(h), SMSOP can effectively reduce the voltage stress of IGBTs.

According to the above-mentioned analysis, the proposed SMSOP topology is suitable for connecting two ac power grids with the same amplitudes but different phases. If the two grid voltages are in phase, the SMSOP requires a slight change in power factor.

In the case of two ac grids with the same amplitudes but different phases, a large modulation index of the shared module can ensure that the SMSOP operates in a feasible area. However, this does not mean that the larger output voltage amplitudes of shared modules, the less quantity of modules required for SMSOP. In Section IV, a design method will be proposed to minimize the quantity of modules.

III. Control of SMSOP

The control of the SMSOP, including that of both nonshared modules and shared modules, is developed in this section. The nonshared modules consist of three stages, which are similar to traditional power electronic transformer cells. Therefore, the control is also similar to it. However, the traditional CHB control scheme cannot be directly applied to shared modules because the ac terminal voltage and current of the shared module are orthogonal. To address this problem, a new control scheme suitable for the shared module is proposed in this section.

The control block diagram of the proposed SMSOP is shown in Fig. 9. The control targets of shared modules are to maintain the voltage of the dc capacitor constant and provide ac voltage to support the grid voltage together with the nonshared modules. The grid currents of input and output stages are regulated by the control of nonshared modules. The control schemes of the nonshared module are elaborated in Section III-A, and the proposed control schemes of the shared module are elaborated in Section III-B.

A. Control Scheme of Nonshared Module

The nonshared module is divided into an input stage, an isolation stage, and an output stage. The control scheme of the three stages will be introduced in this section.

The control objectives of the input stage are to maintain the dc capacitor voltage constant and realize the unity power factor. Similar to the traditional CHB control strategy, as shown in Fig. 10(a), the *dq* vector control is applied in the rectifier

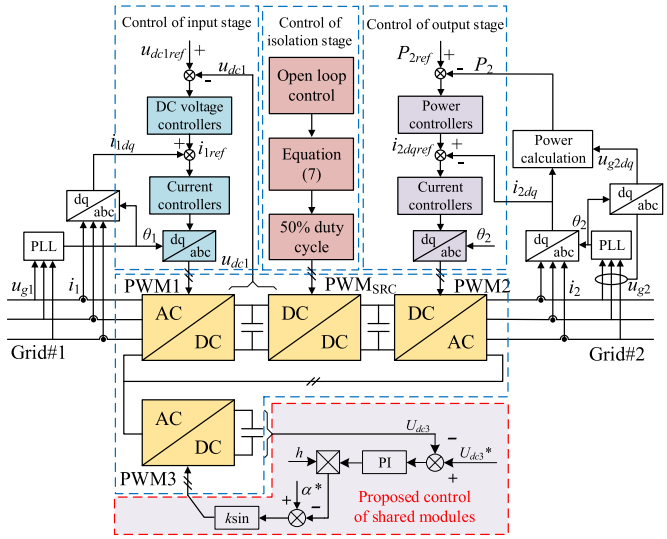

Fig. 9. Control block diagram of the proposed SMSOP.

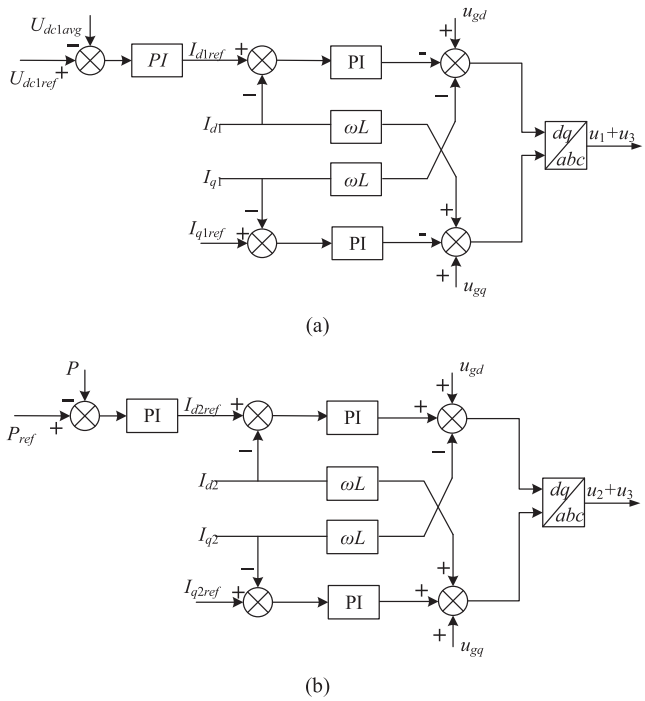

Fig. 10. Control scheme of the nonshared modules. (a) Control scheme of the input stage. (b) Control scheme of the output stage.

controller of the input stage. The main difference is that the output of the controller is the sum of u_1 and u_3.

The functions of the output stage are to provide constant output power. The *dq* vector control is applied in the output stage controller as shown in Fig. 10(b). In the proposed controller, the outer power loop regulates the output power and generates the current reference, whereas the inner current loop tracks the same current reference. Finally, $u_2 + u_3$ is generated as a modulation signal. Both the modulation schemes of input and output stages adopt the carrier-phase-shifted pulsewidth modulation (CPS-PWM) scheme [26].

The isolation stage SRC adopts open-loop control. Similar to conventional dc–dc transformers, the IGBTs in each arm of the primary and secondary sides adopt complementary conduction with a 50% duty cycle. The shift phase between the two arms on the primary and secondary sides is set to 0. The voltage gain is denoted as (7).

B. Control Scheme of the Shared Module

The control objectives of the shared module are to maintain the voltage of the dc-link capacitors constant and transmit power from the input stage to the output stage directly.

The dc capacitor energy of the shared module can be described as follows:

$$\begin{aligned} W_{s3} &= \int_0^T U_3 I_1 \sin(\omega t - \varphi_1)\sin(\omega t + \alpha)dt \\ &\quad - \int_0^T U_3 I_2 \sin(\omega t + \alpha)\sin(\omega t + \varphi_2 + \theta)dt \\ &= \frac{1}{2}U_3 T[I_1 \cos\varphi_1 \cos\alpha - I_1 \sin\varphi_1 \sin\alpha \\ &\quad - I_2 \cos(\varphi_2 + \theta)\cos\alpha - I_2 \sin(\varphi_2 + \theta)\sin\alpha] \end{aligned} \quad (9)$$

where φ_1 and φ_2 are power factors of the input and output stages, respectively. α is the phase difference between the input stage voltage U_1+U_3 and the shared module voltage U_3. θ is the phase difference between the input stage voltage U_1+U_3 and the output stage voltage U_2+U_3.

According to (9), if $W_{s3} > 0$, the voltage of the dc capacitor rises. If $W_{s3} < 0$, the voltage of dc capacitor drops. For a steady-state operation, $W_{s3} = 0$, then

$$\begin{aligned} &[I_1 \sin\varphi_1 + I_2 \sin(\varphi_2 + \theta)]\frac{\sin\alpha}{\cos\alpha} \\ &\quad = [I_1 \cos\varphi_1 - I_2 \cos(\varphi_2 + \theta)]. \end{aligned} \quad (10)$$

Obviously, $\cos\alpha > 0$ due to $\alpha \in (-90°, 90°)$.

According to (10), the steady-state phase α can be derived as follows:

$$\alpha* = \arctan\frac{I_1 \cos\varphi_1 - I_2 \cos(\varphi_2 + \theta)}{I_1 \sin\varphi_1 + I_2 \sin(\varphi_2 + \theta)}. \quad (11)$$

According to the sign of $I_1\sin\varphi_1 + I_2\sin(\varphi_2 + \theta)$, two cases are discussed below.

case I: $I_1\sin\varphi_1 + I_2\sin(\varphi_2 + \theta) > 0$

In this case, the key factor in deciding whether to charge or discharge a dc capacitor is the result of comparing α and α^*. If $\alpha < \alpha^*$, then $W_{s3} > 0$ and the voltage of the dc capacitor rises. If $\alpha > \alpha^*$, then $W_{s3} < 0$ and the voltage of dc capacitor decreases.

case II: $I_1\sin\varphi_1 + I_2\sin(\varphi_2 + \theta) < 0$

Case II is similar to case I, i.e., if $\alpha < \alpha^*$, then $W_{s3} < 0$ and the voltage of dc capacitor drops. If $\alpha > \alpha^*$, then $W_{s3} > 0$ and the voltage of the dc capacitor rises.

According to the above-mentioned analysis, the shared module control proposed in this article is shown in Fig. 11. The dc voltage loop regulates the capacitor voltage and generates the phase α reference. α^* is the feedforward value to improve dynamic. The amplitude of modulation signal k is preset as 0.8 according to the analysis presented in Section II-C. In this figure, the symbol Sign means the sign of $I_1\sin\varphi_1 + I_2\sin(\varphi_2 + \theta)$.

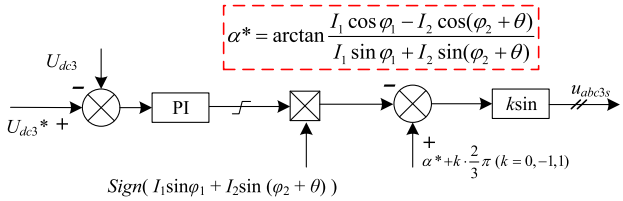

Fig. 11. Control scheme of the shared module.

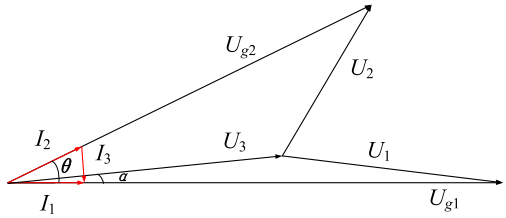

Fig. 12. Vector diagram of SMSOP operation at the steady-state point.

IV. Design and Comparisons

According to the analysis presented in Section II-C, as long as the amplitude and phase of the two grids connected by SMSOP are determined, the minimum quantity of modules required by SMSOP can be designed. In this section, a designed method is proposed and an example is given. In addition, the comparison of the SMSOP and other SOP topologies is listed.

A. Analysis and Design of Minimum Quantity of Modules

According to details presented in Section II-A, the SMSOP required N_1 nonshared modules and $(N - N_1)$ shared modules.

To simplify the analysis, assume that

1) the dc-link capacitor voltage references of shared and nonshared modules are equal, i.e., all dc capacitor voltages are equal;
2) the voltage across the filter inductor is ignored, thus $\dot{U}_1 + \dot{U}_3 \approx \dot{U}_{g1}$ and $\dot{U}_2 + \dot{U}_3 \approx \dot{U}_{g2}$;
3) the SMSOP operates at unit power factor, i.e., the voltage and current are in phase.

Since the minimum quantity of shared modules and nonshared modules is proportional to the amplitude of the ac voltage, the optimization objective can be equivalently expressed as follows:

$$\min G = 2U_1 + 2U_2 + U_3. \quad (12)$$

Fig. 12 shows the vector diagram of SMSOP operation at a steady-state point. As shown in the triangle $I_1I_2I_3$, edge I_3 can be obtained according to the cosine law, which is expressed as follows:

$$I_3 = \sqrt{I_1^2 + I_2^2 - 2I_1I_2\cos\theta}. \quad (13)$$

Considering that U_3 and I_3 are orthogonal, according to the sine law in the triangle $I_1I_2I_3$, the relationship between I_3 and

I_2 can be expressed as follows:

$$\frac{I_3}{\sin\theta} = \frac{I_1}{\sin(\frac{\pi}{2} - \theta + \alpha)}. \tag{14}$$

Therefore, substituting (13) into (14) yields the following:

$$\cos(\theta - \alpha) = \frac{I_1 \sin\theta}{I_3} = \frac{I_1 \sin\theta}{\sqrt{I_1^2 + I_2^2 - 2I_1 I_2 \cos\theta}}. \tag{15}$$

Obviously, according to (15), α is derived as follows:

$$\alpha = \theta - \arccos\left(\frac{I_1 \sin\theta}{\sqrt{I_1^2 + I_2^2 - 2I_1 I_2 \cos\theta}}\right). \tag{16}$$

According to the cosine law, U_1 in the triangle $U_1U_3U_{g1}$ can be derived as follows:

$$U_1 = \sqrt{U_1^2 + U_3^2 - 2U_1U_3\cos\alpha}. \tag{17}$$

Similarly, U_2 in the triangle $U_2U_3U_{g2}$ can be derived as follows:

$$U_2 = \sqrt{U_3^2 + U_{g2}^2 - 2U_3U_{g2}\cos(\theta - \alpha)}. \tag{18}$$

Substituting (17) and (18) into (12) yields the following:

$$\begin{aligned} G &= 2U_1 + 2U_2 + U_3 \\ &= 2\sqrt{U_{g1}^2 + U_3^2 - 2U_{g1}U_3\cos\alpha} \\ &\quad + 2\sqrt{U_3^2 + U_{g2}^2 - 2U_3U_{g2}\cos(\theta - \alpha)} + U_3. \end{aligned} \tag{19}$$

In (19), only U_3 is the variable, thus G is the function of U_3. Therefore, a minimum of G can be obtained as long as

$$\frac{\partial G}{\partial U_3} = 0. \tag{20}$$

It is difficult to obtain the analytical solution of (20); however, numerical methods can be used to obtain its numerical solution. Once U_3 is obtained, we can obtain U_1 and U_2 according to (17) and (18). Then, the minimum quantity of modules can be obtained as follows:

$$N_{\rm nm} = \max\left\{\frac{U_1}{m_1 k_{\rm pwm} U_{\rm dc}}, \frac{U_2}{m_2 k_{\rm pwm} U_{\rm dc}}\right\} \tag{21}$$

$$N_{\rm sm} = \frac{U_3}{m_3 k_{\rm pwm} U_{\rm dc}} \tag{22}$$

where max (x, y) denotes the maximum value of x and y. m is the modulation index for the pulsewidth modulation (PWM) at rated power. $N_{\rm sm}$ and $N_{\rm nm}$ are the quantities of shared modules and nonshared modules, respectively. $k_{\rm pwm}$ indicates PWM gain.

$N_{\rm nm}$ and $N_{\rm sm}$ calculated according to (21) and (22) are not integers. Therefore, the quantities of shared and nonshared modules can be selected as ceil($N_{\rm nm}$) and ceil($N_{\rm sm}$), respectively. However, those results are conservative. The combination of (ceil($N_{\rm nm}$), floor($N_{\rm sm}$)) or (floor($N_{\rm nm}$), ceil($N_{\rm sm}$)) may be feasible, where ceil (x) rounds x to the nearest integers greater than or equal to x and floor (x) rounds x to the nearest integers greater than or equal to x.

To design the minimum quantity of modules, the following steps can be performed. Let $N_{\rm nm}{}^* = {\rm ceil}(N_{\rm nm})$ and $N_{\rm sm}{}^* = {\rm ceil}(N_{\rm sm})$. First, keep $N_{\rm nm}{}^*$ constant and gradually decrease $N_{\rm sm}{}^*$ by 1 until the feasible area is not satisfied. Record the last combination ($N_{\rm nm}{}^*$, $N_{\rm sm\_last}{}^*$) that satisfies the feasible area. Secondly, keeping $N_{\rm sm}{}^*$ constant and gradually decrement $N_{\rm nm}{}^*$ by 1 until the feasible area is not satisfied. Record the last combination ($N_{\rm nm\_last}{}^*$, $N_{\rm sm}{}^*$) that satisfies the feasible area. Finally, compare the quantity of modules required in these two combinations ($N_{\rm nm}{}^*$, $N_{\rm sm\_last}{}^*$) and ($N_{\rm nm\_last}{}^*$, $N_{\rm sm}{}^*$), then choose the combination that requires the least quantity of modules.

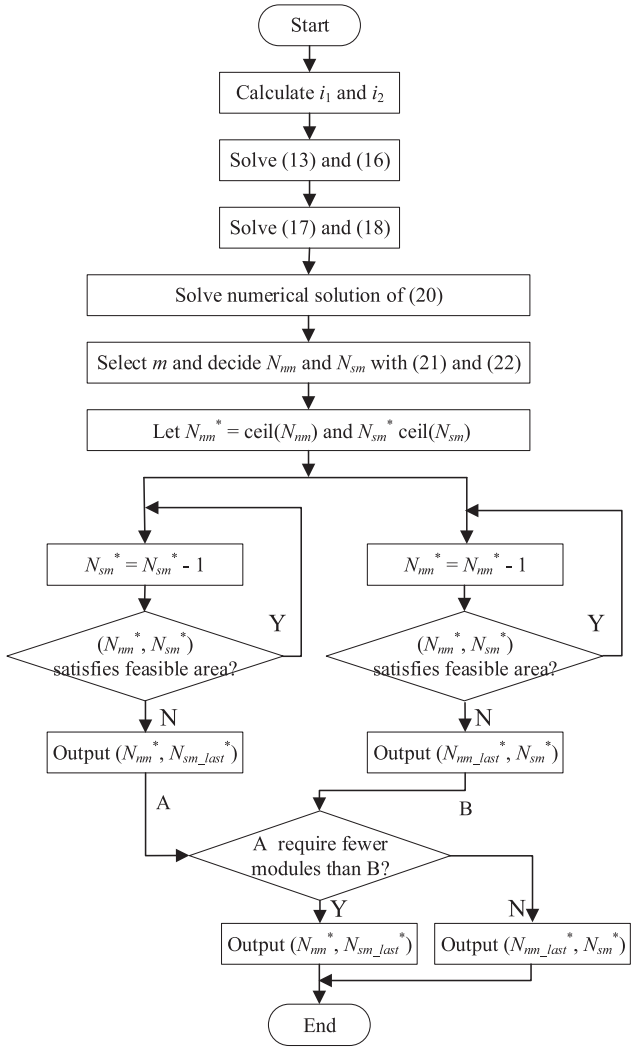

Fig. 13. Flowchart of the design procedure.

From the above-mentioned analysis, a design procedure can be concluded, as shown in Fig. 13.

B. Design Example and Comparison of SMSOP With Other SOP Topologies

From the above-mentioned analysis and design procedure, a design example is presented to provide an intuitive understanding of the proposed design method. In addition, the comparison of the SMSOP and another SOP topology is listed.

The example prototype parameters are presented in Table I.

Here, $U_{g1} = 10\angle 0°$ kV and $U_{g2} = 10\angle 30°$ kV are adopted. According to the rated power 1 MVA, the corresponding currents

TABLE I
DESIGN EXAMPLE PARAMETERS

Parameters	Value
Rated input voltage	$10\angle 0°$ kV
Rated output voltage	$10\angle 30°$ kV
Rated dc-link capacitor voltage	750 V
Rated power	1 MVA

I_1 and I_2 are $816\angle 0°$ A and $816\angle 30°$ A, respectively, thus $\theta = 30°$. Therefore, α can be obtained according to (16) that is $\alpha = 15°$. Then, according to (17) and (18), it follows that both U_1 and U_2 are functions of U_3. Therefore, G is also a function of U_3.

MATLAB is used here to solve the numerical solution of (20). The numerical solution of U_3 is 5.2 kV.

Then, considering $m = 0.85$, the quantities of nonshared modules and shared modules can be obtained according to (21) and (22) as ${N_{\rm sm}}^* = 12$ and ${N_{\rm nm}}^* = 4$, respectively. However, $({N_{\rm sm}}^*, {N_{\rm nm}}^*) = (11, 4)$ or $({N_{\rm sm}}^*, {N_{\rm nm}}^*) = (12, 3)$ may be feasible. According to the vector diagram of SMSOP, ${N_{\rm sm}}^* = 11$ and ${N_{\rm nm}}^* = 4$ are the minimum numbers of modules.

Under the same conditions, the component numbers of CHB-based SOP, BTB-MMC, DMMC-SOP, M3C-SOP, and SMSOP are listed in Table II. It can be seen that the CHB-based SOP, BTB-MMC, and DMMC-SOP require 624 IGBTs, whereas SMSOP requires 324 IGBTs. In addition, 39 high-frequency transformers are required in CHB-based SOP and 12 in SMSOP. Therefore, SMSOP is lighter in weight and more economical in cost than CHB-based SOP, BTB-MMC, and DMMC-SOP.

It can also be seen from Table II that 78, 312, and 156 dc capacitors are required in CHB-based SOP, BTB-MMC, and DMMC-SOP, respectively, whereas only 57 dc capacitors are required in the SMSOP. In high-voltage applications, the large number of capacitors is the major factor in the large size of the cascade converter, so the SMSOP is smaller in size than the CHB-based SOP, BTB-MMC, and DMMC-SOP. In summary, the SMSOP can save IGBTs and high-frequency transformers, thus reducing cost, size, and weight.

C. Power Loss Analysis

In SMSOP, the conduction losses of IGBT are much higher than the switching losses and diode losses and are the dominant loss component of the converter [27], [28]. Since conduction loss has a positive correlation with current, the higher the current, the higher the conduction loss [29]. According to Fig. 7, the current i_3 of the shared module is small due to the small phase difference between i_1 and i_2. Therefore, the power loss of shared modules is lower than that of nonshared modules. For practical applications, the number of shared modules is large but the losses are lower than that of nonshared modules, and the number of nonshared modules is small but losses are higher than that of shared modules. Therefore, the SMSOP have low power loss.

V. SIMULATION AND EXPERIMENTAL VERIFICATION

In order to verify the validation of SMSOP and its control scheme, simulation model and experiment platforms are built in this section.

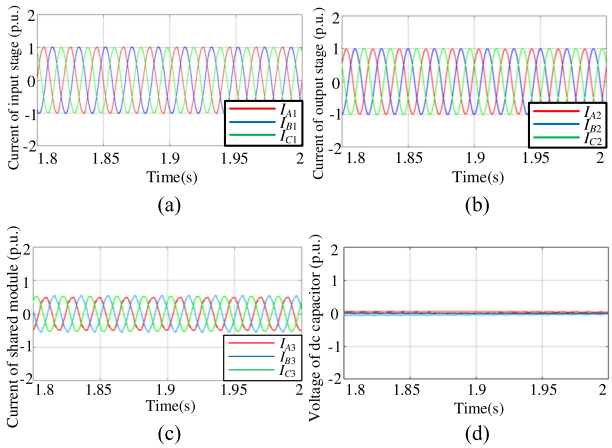

Fig. 14. Simulation waveforms of case A. (a) Current of input stage. (b) Current of output stage. (c) Current of shared module. (d) Voltage waveforms of all dc capacitors.

A. Simulation Validation

An SMSOP topology used for simulation is built in MATLAB/Simulink. In the simulation, the SMSOP consists of four shared modules and two nonshared modules. The rated input and output voltages are 10 kV, and the rated dc-link voltages are 1600 V. The rated power of the SMSOP is 1 MW. In the following, two cases are studied according to the phase difference of two grid voltages. All voltage and current shown in Figs. 14 and 15 are normalized by their rated value. The system parameters are shown in Table III.

Case A: The phase difference between the two grids is 30°

In this case, the input and output voltages have the same amplitude but with a 30° phase difference. The waveforms are shown in Fig. 14. It can be seen from Fig. 14(a) to (c), purely sinusoidal currents are injected into the grid. The current amplitude of the shared module is half the amplitude of the input and output currents according to (3). The waveforms of all dc voltages are shown in Fig. 14(d). It can be seen that all dc voltages are almost equal. The simulation results shown in Fig. 14 verify the correctness of the topology and control strategy in the presence of phase difference between the two grids.

Case B: The two grid voltages are in phase.

In this case, the input and output voltages have the same amplitude and are in phase. The q-axis current reference $i_{q2\rm ref}$ of the nonshared module at the input stage is set to 0.2 to ensure stable operation of SMSOP, i.e., a power factor of around 0.98 and a power factor phase of around 11°. The waveforms are shown in Fig. 15. It can be seen from Fig. 15(a) to (c), purely sinusoidal currents are injected into the grid. The amplitude of the shared module current i_3 is small because the phase and amplitude of i_1 and i_2 are almost the same according to (3). Fig. 15(d) and (e) show the dq-axis component of i_1 and i_2, and the q-axis component of i_2 is around 0.2, which is the same as the reference value. Fig. 15(f) shows the voltage average value of dc capacitor at the input stage, and Fig. 15(g) shows all dc capacitor voltages. In this simulation, all dc voltages are

TABLE II
COMPARISON OF THE SMSOP WITH EXISTING TOPOLOGIES

Parameters	CHB-SOP[17]	BTB-MMC[18]	DMMC-SOP[20]	SMSOP
Number of inductors	6	12	6	6
Number of Capacitors	78	312	156	57
Number of submodules	156	312	156	81
Number of IGBTs	624	624	624	324
Number of transformers	39	0	0	12

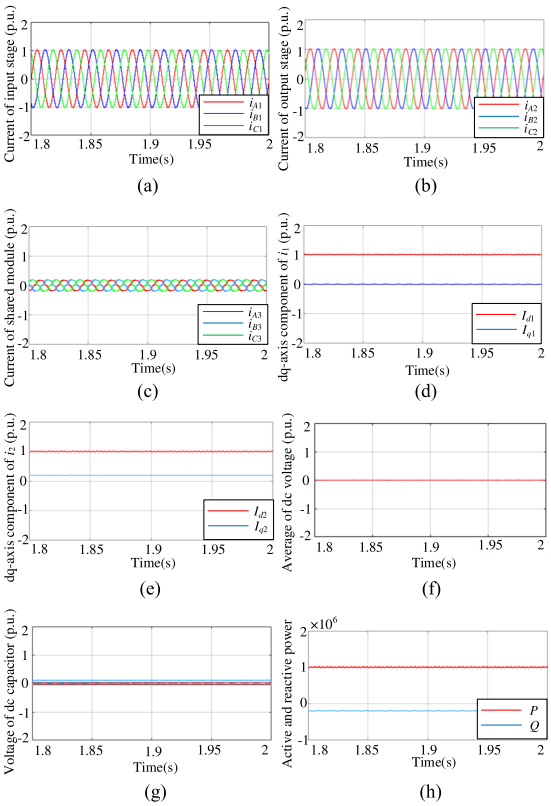

Fig. 15. Simulation waveforms of case B. (a) Current of the input stage. (b) Current of the output stage. (c) Current of the shared module. (d) *dq*-axis current component of the input stage. (e) *dq*-axis current component of the output stage. (f) Voltage average value of all dc capacitors. (g) Voltage of all dc capacitors. (h) Active power P and reactive power Q.

TABLE III
SIMULATION PARAMETERS OF SMSOP

Parameters	Value
Rated input voltage	10 kV
Rated output voltage	10 kV
Rated dc-link capacitor voltage	1600 V
Rated power	1 MW
Filter inductor	10 mH
dc-link capacitor	10 mF
SRC resonant inductor	57 μH
SRC resonant capacitor	1 μF
High-frequency transformer ratio	1:1
Number of shared modules	4
Number of non-shared modules	2

almost equal. The active power and reactive power are shown in Fig. 15(h). Since the output stage power factor is not 1, the system generates capacitive reactive power. The simulation results shown in Fig. 15 verify the effectiveness of the topology and control strategy in the case of two grid voltages in phase.

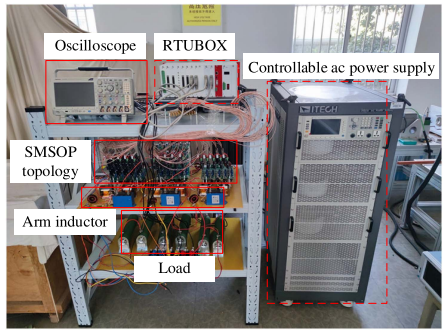

Fig. 16. Experimental prototype.

B. Experimental Validation

An experimental platform is constructed and tested to verify the effectiveness of the proposed SMSOP topology and control schemes. The experimental prototype is shown in Fig. 16. The power grid at the input stage is emulated by ITECH IT7600, which is a controllable ac power supply, and the rated grid voltage/frequency is 380 V/50 Hz. Three resistors are connected in Y-connection to the output stage, and each one has a resistance of 50 Ω. The prototype has a total of 15 H-bridge converters, which means each phase consists of one shared module and one nonshared module. The input stage of SMSOP is connected to the grid, converting 50 Hz, 380 VAC voltage to 200 VDC bus, and then, the isolation stage SRC of SMSOP converts 200 VDC to 200 VDC with a 1:1 high-frequency transformer, thus the voltage gain U_R is designed to be 1. The converter is made up of 60 IGBTs power modules (Infineon IKW50N60T, 600 V/50 A). A real-time simulator of RTUBOX based on a CPU board operates as the controller of SMSOP with a 100 μs control step.

Without loss of generality, the phase difference between input and output voltages is set to 30°. The system parameters are shown in Table IV.

Fig. 17 shows the steady-state ac waveforms of SMSOP. In the experiment, as shown in Fig. 17(a), the phase-A grid voltage and current of the input stage are in phase, which indicates that the SMSOP operates at unity power factor. Fig. 17(b) and (c) shows the experimental waveforms of the input and output currents. As shown in the figure, purely sinusoidal currents are injected to the grid and resistive load. The amplitude of the input current is 6.4 A and that of the output current is 6.1 A. The difference in amplitude of input and output currents is mainly caused by the power loss of the SMSOP topology.

The phase difference between input and output voltages is controlled to be 29.8°, as shown in Fig. 18. The measured results are almost the same as the set value of 30°. Therefore,

TABLE IV
SMSOP TOPOLOGY PARAMETERS

Parameters	Value
Rated input voltage	$380\angle 0°$ V
Rated output voltage	$380\angle 30°$ V
Rated dc-link capacitor voltage	200 V
Rated load	50 Ω
Rated power	2.8 kW
Filter inductor	2.5 mH
dc-link capacitor	1 mF
SRC resonant inductor	57 μH
SRC resonant capacitor	1 μF
High-frequency transformer ratio	1:1
Number of shared module	1
Number of non-shared module	1

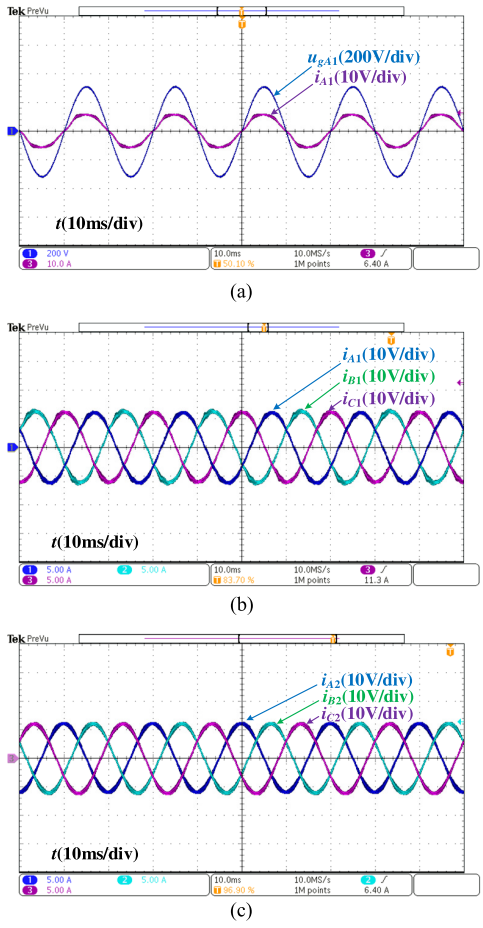

Fig. 17. Steady-state waveforms of ac current. (a) Steady-state waveform of input voltage and current in phase A. (b) Steady-state waveforms of input current. (c) Steady-state waveforms of output current.

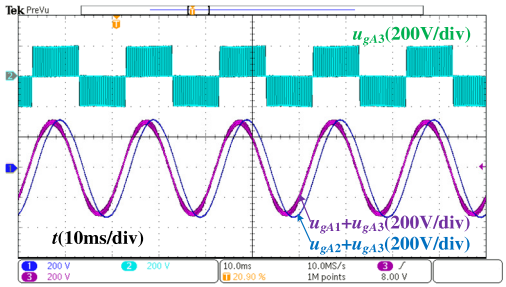

Fig. 18. Phase difference among input voltage, output voltage, and shared module voltage.

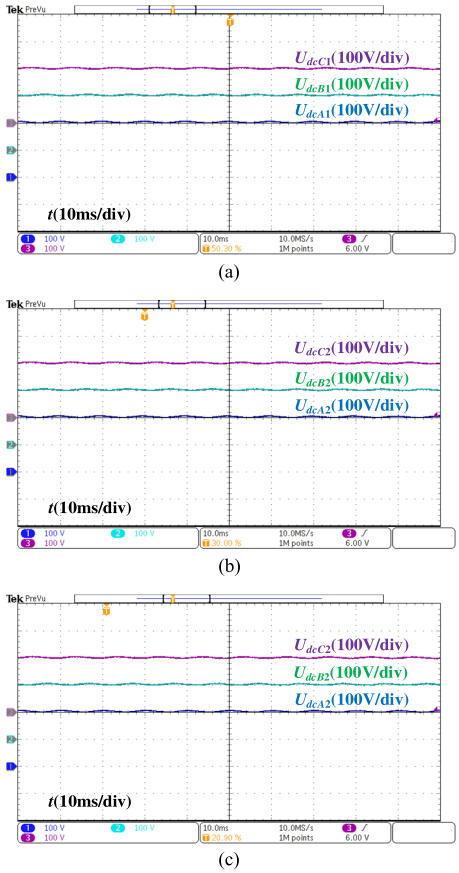

Fig. 19. Steady-state waveforms of dc voltage. (a) Steady-state dc voltage of input stage nonshared modules. (b) Steady-state dc voltage waveforms of output stage nonshared modules. (c) Steady-state dc voltage waveforms of input stage shared modules.

according to the analysis presented in Section II-C, the voltage phase difference between shared and nonshared modules should be 15°. As shown in the figure, the PWM voltage phase U_{gA3} of the shared module is measured as 14.5°, which verifies the correctness of the analysis.

Fig. 19 depicts the experimental waveforms of dc-link voltage with the voltage balance control. As is shown, all dc-link voltages are controlled to be set value at 200 V and well balanced in steady state. The voltage ripple at twice the grid frequency is seen at converter's dc bus due to the active power coupling of the single H-bridge. These experimental results verify the rectifier and isolation stage control.

Fig. 20 displays both input and output dynamic waveforms of voltage and current. In Fig. 20(a), input current changes as the load is step increased or halved, distortion appears in the current waveforms but settles within about two fundamental cycles. In Fig. 20(b), one can see that the output voltage and current are stable under a step change of load. Obviously, the step change in load has no visible influence on the waveform of the output voltage.

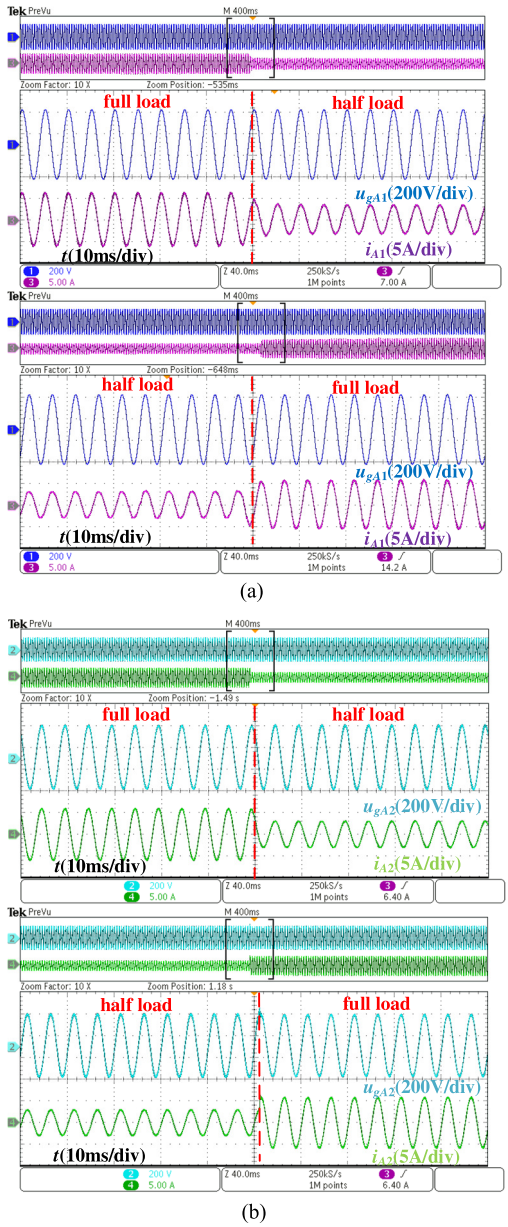

Fig. 20. Dynamic waveforms of ac voltage and current. (a) Dynamic waveforms of input voltage and current. (b) Dynamic waveforms of output voltage and current.

VI. Conclusion

Based on the traditional CHB-based SOP, a novel three-phase SMSOP topology suitable for power DN is proposed. This article establishes mathematical models and proposes control strategies for SMSOP topology. The feasible area is analyzed by means of a vector diagram. The vector diagram illustrates that the SMSOP is suitable for connecting two grids with the same amplitudes but different phases. A large amplitude of shared module output voltage can ensure that SMSOP operates in the feasible area. If the two grid voltages are in phase, the SMSOP requires a slight change in power factor. In addition, a design method is proposed to minimize the quantity of modules, and a comparison of the SMSOP with existing SOP topologies is listed. From the list, it can be concluded that the SMSOP can save IGBTs, dc capacitors, and high-frequency transformers compared with the CHB-based SOP and BTB-MMC, which reduces the cost, weight, and volume significantly.

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