A Faulty Submodule Mathematical Model-Based Localization Strategy for Switch Open-Circuit Fault of Module Multilevel Converter

Zehao Liu, Lan Xiao, *Member, IEEE*, Xin Cao, *Member, IEEE*, and Zhiquan Deng

***Abstract*—A faulty submodule (SM) mathematical model-based switch open-circuit fault diagnosis and localization (FDL) method for module multilevel converter (MMC) is investigated in this article, which can diagnosis the faulty switch in time. Initially, the mathematical model is established through the modified switching function of the faulty SM, which can express the real switching state of the faulty SM accurately. Based on the proposed mathematical model, an innovative FDL method for MMC is proposed. The faulty switch is located by comparing the capacitor voltage calculated through the proposed mathematical model with the sampled capacitor voltage value. To enhance the accuracy and anti-interference ability of the model, the capacitance observation method is proposed in the capacitor precharge stage. The proposed FDL method can diagnose and locate faulty switch in any state of the SM, even if the operating state of the faulty SM is the same as that of the normal SM. Single or multiple switch open-circuit faults can be accurately located by this method under either light or heavy load conditions. Finally, the mathematical model and FDL method are verified through simulation and experiment.**

***Index Terms*—Mathematical model of the faulty SM, modular multilevel converter (MMC), open-circuit fault diagnosis and localization, submodule (SM).**

I. Introduction

SINCE the module multilevel converter (MMC) was proposed by Lesnicar and Marquardt [1], it is widely researched by scholars and industry because of the advantages, such as modular structure, low switching frequency, and high output voltage. So far, it has been widely used in high voltage direct current (HVdc) transmission systems, motor drive, and static reactive power compensation [2], [3], [4]. Nonetheless, dozens or even hundreds of power switches are installed in MMC for medium and high voltage applications, which are considered to be the most vulnerable devices because 31% of system failures are caused by power semiconductor devices [5]. Consequently, the switch open-circuit (OC) fault of the submodule (SM) is unavoidable in the MMC operation, which makes the current path in the faulty SM alter under certain conditions. In this case, the capacitor voltage of the faulty SM rises rapidly and the SM output voltage is abnormal. The rapid rise of the capacitor voltage not only increases the voltage stress of the device, which is easy to cause secondary faults, but also distorts the output voltage, and generates odd harmonic components in the circulating current. If the switch OC fault is not dealt with in time, the MMC even stops running or is damaged by the fault [5], which is not allowed in the HVdc transmission system. While, the OC faults are not recognized promptly in the early stages of their occurrence. Therefore, high sensitivity is inevitably necessitated in switch open-circuit fault diagnosis and localization (FDL) methods. In addition, the FDL methods should have the advantages of high computational efficiency, noise isolation, simple detection circuit, and low cost, to meet the requirements of swift and accurate positioning, decent robustness and strong anti-interference ability. Hence, numerous FDL methods have been presented to handle the faults [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35]. These methods can be broadly categorized as hardware-based [6], [7], [8], [9], [10], artificial intelligent-based [11], [12], [13], [14], [15], [16], [17], and model-based [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35].

In order to obtain the fault status directly, different hardware detection circuits such as sampling resistor circuit, supervisory sensors circuit, additional windings circuit combined rectifying and filtering, fast response voltage sensors circuit have been presented in [6], [7], [8], [9], and [10]. By the sampling resistor-based detection circuit, the SM output voltage is transmitted to the field programmable gate array (FPGA) through a comparator and photocoupler, and then the faulty switch is located utilizing the drive signals with the data lock function [6]. The FDL method using supervisory sensors can locate the faulty SM by compare the measured voltages with the theoretical voltages [7]. In [8], the secondary windings are used to monitor the high voltage pulse signal in the arm inductors, which can detect whether a fault

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occurs. In [9], the FDL method locates the faulty switch through high-speed response voltage sensors combined with Boolean logic circuit. A rearranged bleeding resistance circuit is installed in the SM to monitor the capacitor voltage, which can locate faults in time when the MMC is operating under light loads [10]. Naturally, hardware-based FDL methods locate the faulty switch by adding additional detection circuits, which makes the MMC circuit system more complex. Simultaneously, the cost of the MMC system rises considerably.

Compared with hardware-based FDL methods, artificial intelligence (AI) based FDL methods promote higher accuracy, lower hardware costs, and better antijamming capabilities. Moreover, the abovementioned methods do not rely on the mathematical model of the system and additional detection circuits in the diagnosis process, which are inherent in AI algorithms. Thus, many AI algorithms, such as clustering algorithm [11], machine learning algorithm [12], one-dimensional (1-D) convolutional neural network (1-D-CNN) [13], 2-D convolutional neural network (2-D-CNN) [14], machine learning (ML) [15], deep learning [16], and isolation forest [17], are used for MMC switch open circuit fault diagnosis and location. Notable, the data processing techniques in [13] and [14] have been considerably improved. In [13], a monitoring system based on 1-D-CNN was used to diagnosis the faulty switch, which can use the sampling data directly. In [14], a 2-D-CNN based FDL method was investigated to locate the faulty switch with low-data-volume. In [15], an FDL method based on ML was proposed with accuracy of 99.6%. To reduce the calculation complexity, the binary neural network and isolation trees are presented in [16] and [17], respectively. However, as for AI-based FDL methods, one challenge is the selection principle of the observed state. Excessive monitoring states will lead to more complicated AI algorithms, prolonged learning, and training time. Although the accuracy of the fault diagnosis is very high, they cannot achieve real-time online diagnosis without data training. Another challenge is the comparatively high computational pressure on the CPU [11], especially during data processing.

Given these limitations, mathematical model-based FDL methods [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35] have been extensively researched to locate the faulty switch by employing different observers. Among them, the theoretical value of the state, such as the SM capacitor voltage, the arm voltage, the circulating current, and the arm current, are precisely estimated by corresponding mathematical models. The observer-based FDL method utilizing sliding mode observer [18], [19], Kalman filter [20], [21], capacitor current observer [22], and so on were proposed in [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], and [28]. Furthermore, considering the under the numerous SMs, the single ring theorem was proposed in [25], which can locate the faulty SM efficiently under hundreds of SMs. The FDL methods based on model predictive control algorithm and the SM capacitor voltage similarity were proposed in [26] and [27], respectively, where the arm voltage was used to identify the occurrence of faults, and the SM capacitor voltage was used to locate the fault switch. A FDL method combining state observer and tolerance control was investigated in [28]. However, those methods are no longer applicable when the open-circuit fault occurs in multiple switches. To deal with this problem, the FDL methods based on distributing fault diagnosis method and auxiliary monitoring algorithm were proposed in [29], [30], [31], [32], [33], and [34]. In particular, a fault code and *Pauta* criterion in [31] are proposed based on the circulating current error signal and capacitor voltage, respectively. In the aforementioned methods, they are only applicable to the inverter mode of MMC. Recently, some methods, utilizing the SM voltage [33] and switch signal [34], have been proposed to resolve this problem. In [35], an FDL method for modular multilevel matrix was investigated, but it cannot be used for MMC directly.

To sum up, the existing methods and mathematical models in the abovementioned literatures cannot express the SM capacitor voltage quantitatively when the switch fault. In this article, the mathematical model of the faulty SM employing modified switching function $S_{i\_\mathrm{Q}x\mathrm{fault}}$ to express the faulty SM capacitor voltage is established. The proposed mathematical model comprises the modified switching function and the integral formula of the faulty SM capacitor voltage, which can accurately depict the dynamic process of the capacitor voltage. Then, a novel FDL method based on the proposed model is investigated. The proposed method can locate the faulty switch under light load condition with lower computation burden. In conclusion, the main innovations of this article are as follows.

1) A mathematical model of the faulty SM based on the modified switching function is established for the first time, which can track the faulty SM capacitor voltage accurately.
2) A novel mathematical model based FDL method is proposed, which locates the faulty switch through the MMC control data and does not require additional detection circuit.
3) The FDL method can diagnosis fault in any state of the SM, and single or multiple switch open-circuit faults can be accurately located by this method under either light or heavy load conditions.

The rest of this article is organized as follows. In Section II, the detailed SM characteristics under the switch fault are introduced. Then, the mathematical model of the faulty SM is established in Section III and a FDL method based on the model is presented simultaneously. The FDL method is analyzed and discussed in detail in Section IV. In Sections V and VI, the mathematical model and FDL method are verified by the simulation and the experiment, respectively. Finally, Section VII concludes this article.

II. Structure of MMC and Characteristics of Fault SM

In this section, the detailed SM characteristics are illustrated under the switch Q_1 and Q_2 open circuit fault shown in Figs. 2 and 3, respectively. The capacitor current and SM output voltage are shown in Table I.

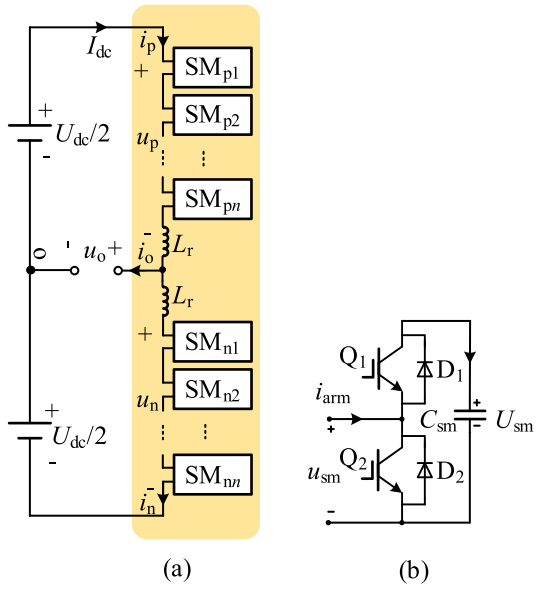

Fig. 1. MMC and SM circuit topology.

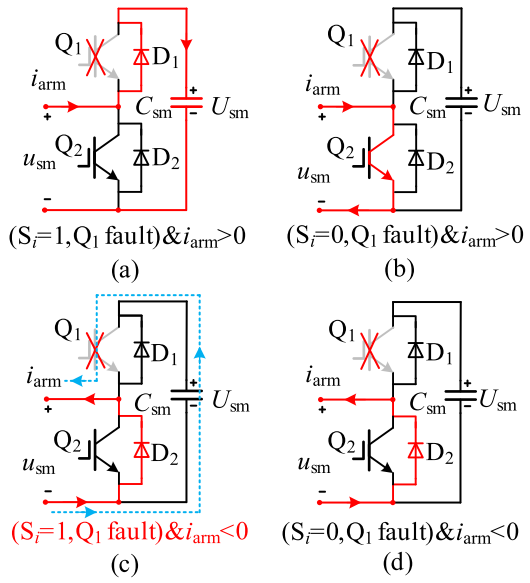

Fig. 2. Fault analysis of switch Q_1.

TABLE I
BEHAVIOR OF SM UNDER DIFFERENT CONDITIONS

Switching condition	i_{arm}	Capacitor current and its state		
		Normal	Q_1 fault	Q_2 fault
$S_i(t)$=1	>0	$i_c = i_{arm}$ $u_{sm} = U_{sm}$	$i_c = i_{arm}$ $u_{sm} = U_{sm}$	$i_c = i_{arm}$ $u_{sm} = U_{sm}$
	<0	$i_c = i_{arm}$ $u_{sm} = U_{sm}$	$i_c = 0$A $u_{sm} = 0$V	$i_c = i_{arm}$ $u_{sm} = U_{sm}$
$S_i(t)$=0	>0	$i_c = 0$A $u_{sm} = 0$V	$i_c = 0$A $u_{sm} = 0$V	$i_c = i_{arm}$ $u_{sm} = U_{sm}$
	<0	$i_c = 0$A $u_{sm} = 0$V	$i_c = 0$A $u_{sm} = 0$V	$i_c = 0$A $u_{sm} = 0$V

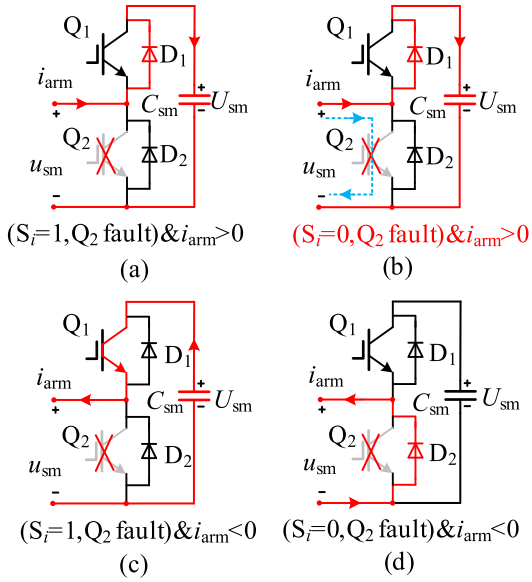

Fig. 3. Fault analysis of switch Q_2.

A. Circuit Topology of MMC

Fig. 1(a) shows the circuit topology of the single-phase MMC, in which each phase is composed of the upper arm and the lower arm. Each arm is composed of SMs with the same structure in series. In Fig. 1(b), the structure of the half-bridge SM is illustrated, which contains two switches Q_1 and Q_2 with the antiparallel body diodes D_1 and D_2, respectively. The capacitor C_{sm} is deployed in the SM DC side. u_p and u_n denote the voltages of the upper and the lower arms, respectively. u_o is the phase voltages on the ac side and u_{sm} is the SM output voltage. i_p and i_n represent the currents of the upper and the lower arm, respectively. i_{arm} is the SM input current, and its value is equal to the arm current of the i_p or i_n.

B. Operation States of the SM

The operation states of the SM are divided into inserted state and bypassed state by the gate signals of switch Q_1 and Q_2. When $Q_1 = 1$ and $Q_2 = 0$, the SM is in the inserted state (1 indicates the switch on, while 0 indicates switch OFF). Similarly, when $Q_1 = 0$ and $Q_2 = 1$, the SM is in the bypassed state. In order to describe the SM states more clearly, the switching function S_i can be defined as

$$S_i = \begin{cases} 1, & \text{when } Q_1 = 1,\ Q_2 = 0 \\ 0, & \text{when } Q_1 = 0,\ Q_2 = 1. \end{cases} \tag{1}$$

According to (1), the SM output voltage u_{sm} is derived by

$$u_{sm} = S_i U_{sm}. \tag{2}$$

The current circulates into the SM capacitor can be obtained by

$$i_c = S_i i_{arm} \tag{3}$$

where i_c is the capacitor current and i_{arm} is arm current.

Using (3), the capacitor voltage $U_{\rm sm}$ of SM is obtained

$$U_{\rm sm} = \frac{1}{C_{\rm sm}} \int_{t_1}^{t_2} i_{\rm c} dt + U_{\rm sm\_t1} \tag{4}$$

where $U_{\rm sm\_t1}$ is the capacitor voltage at time t_1.

C. Characteristics of the SM Under Q_1 Fault

Fig. 2 illustrates the SM current path under the switch Q_1 open-circuit fault, which is divided into four current paths according to the switching function S_i and the direction of the arm current. Fig. 2(a) shows that arm current $i_{\rm arm}$ flow into capacitor $C_{\rm sm}$ through diode D_1 when $S_i = 1$ and $i_{\rm arm} > 0$, where $u_{\rm sm} = U_{\rm sm}$ and $i_{\rm c} = i_{\rm arm}$. In Fig. 2(b), $i_{\rm arm}$ flow through diode D_2 when $S_i = 0$ and $i_{\rm arm} > 0$. The SM is bypassed and $u_{\rm sm} = 0$ V and $i_{\rm c} = 0$ A. In Fig. 2(c), the arm current $i_{\rm arm}$ forces flow through the diode D_2 due to the faulty switch Q_1 blocked rather than Q_1 under $S_i = 1$ and $i_{\rm arm} < 0$. At this condition, the capacitor $C_{\rm sm}$ cannot be connected to the arm. Therefore, $u_{\rm sm}$ and $i_{\rm c}$ are equal to 0 V and 0 A (when the SM normal, $u_{\rm sm} = U_{\rm sm}$ and $i_{\rm c} = i_{\rm arm}$), respectively. The $i_{\rm arm}$ in Fig. 2(d) flow through D_2 under $S_i = 0$ and $i_{\rm arm} < 0$, where $u_{\rm sm} = 0$ V and $i_{\rm c} = 0$ A.

Based on the abovementioned analysis, the *path A1*[see Fig. 2(a)], *path B1* [see Fig. 2(b)], and *path D1* [see Fig. 2(d)] are the same as the normal SM. Hence, the FDL methods based on the SM output voltage or arm voltage cannot recognize the defective SM during those conditions. Only the faulty characteristics of SM under *path C1* [see Fig. 2(c)] can be used to locate the faulty SM.

D. Characteristics of the SM Under Q_2 Fault

Fig. 3 depicts the SM conditions under the switch Q_2 open-circuit fault, where the current flowing into the SM is split into four paths: *path A2* [see Fig. 3(a)], *path B2* [see Fig. 3(b)], *path C2* [see Fig. 3(c)], and *path D2* [see Fig. 3(d)], according to S_i and the direction of the arm current. In *path A2*, $i_{\rm arm}$ flow into capacitor $C_{\rm sm}$ through diode D_1 when $S_i = 1$ and $i_{\rm arm} > 0$, and $u_{\rm sm} = U_{\rm sm}$ and $i_{\rm c} = i_{\rm arm}$. In *path B2*, $i_{\rm arm}$ will flow into $C_{\rm sm}$ through the diode D_1 rather than flow through Q_2 during $S_i = 0$ and $i_{\rm arm} > 0$. In this time, the capacitor $C_{\rm sm}$ is connected to the arm, and the $u_{\rm sm}$ and $i_{\rm c}$ are equal to $U_{\rm sm}$ and $i_{\rm arm}$ (when the SM normal, $u_{\rm sm} = 0$ V and $i_{\rm c} = 0$ A), respectively. In Fig. 3(c), *path C2* is not disrupted, and the arm current $i_{\rm arm}$ passes through the capacitor $C_{\rm sm}$ and switch Q_2, where $u_{\rm sm} = U_{\rm sm}$ and $i_{\rm c} = i_{\rm arm}$. When $S_i = 0$ and $i_{\rm arm} < 0$, *path D2* is normal as the healthy SM. In this state, the $u_{\rm sm}$ and $i_{\rm c}$ are 0 V and 0 A, respectively.

Similarly, the current paths in the three working states shown in Fig. 3(a), (c), and (d) are the same as the current paths of the normal SM. Therefore, the FDL methods in the existing literatures cannot identify the faulty switch by utilizing the logical relationship between $u_{\rm sm}$ and S_i.

Table I shows the relationship between SM output voltage $u_{\rm sm}$ and SM capacitor voltage $U_{\rm sm}$ for different fault conditions. Moreover, the relationship between capacitor current $i_{\rm c}$ and arm current $i_{\rm arm}$ shown in Table I as well.

From the table, the Q_1 and Q_2 open circuit faults have a specific state that is different from the normal state. The *path C1* and *path B2* of the faulty SM shown in Figs. 2(c) and 3(b) are changed due to the Q_1 and Q_2 fault, respectively, and the relationship between $u_{\rm sm}$ and SM capacitor voltage $U_{\rm sm}$ cannot be expressed by (2). Since the existing mathematical models can only represent the SM capacitor voltage in the normal working state, it is necessary to establish a mathematical model that can describe the state of the SM capacitor under the switch open-circuit fault. Then, using the proposed mathematical model, which depicts the SM capacitor voltage $U_{\rm sm}$ under the switch fault, the faulty switch can be precisely located.

III. Proposed Mathematical Model of Faulty SM and the FDL Method

In this section, the mathematical models of the faulty SM are established by the modified switching functions illustrated in (6) and (11). A novel FDL method, based on the proposed mathematical model, is then presented.

A. Mathematical Model of SM Under Switch Q_1 Fault

Since the switching function S_i cannot specify the switch states of the faulty SM at certain conditions, i.e., in Fig. 2(c), the $U_{\rm sm}$ is constant rather than decries under Q_1 fault. Thus, the S_i should be redefined when $S_i = 1$ and $i_{\rm arm} < 0$.

If the $u_{\rm sm} = 0$ V and $i_{\rm c} = 0$ A under the conditions of the $S_i = 1$ and $i_{\rm arm} < 0$, it can be concluded that the switch Q_1 of SM has an open circuit fault. In this state, the final switching function $S_{i\_\rm Q1fault}$ can be defined as 0 when the $S_i = 1$ and $i_{\rm arm} < 0$. In other states, $S_{i\_\rm Q1fault}$ is equal to S_i.

To express the final switching function $S_{i\_\rm Q1fault}$ more clearly, the modified switching function $S_{i\_\rm Q1open}$ is defined in (6). Therefore, the $S_{i\_\rm Q1fault}$ can be regarded as a modified switching function $S_{i\_\rm Q1open}$ subtracted from the switching function S_i. The $S_{i\_\rm Q1fault}$ can be obtained as

$$S_{i\_\rm Q1fault} = S_i - S_{i\_\rm Q1open} \tag{5}$$

with

$$S_{i\_\rm Q1open} = \begin{cases} 1, \text{ when } S_i = 1 \text{ and } i_{\rm arm} < 0 \\ 0, \text{ other conditions} \end{cases}. \tag{6}$$

According to (5), the relationship between $u_{\rm sm}$ and SM capacitor voltage $U_{\rm sm}$ can be expressed as

$$u_{\rm sm} = S_{i\_\rm Q1fault} U_{\rm sm}. \tag{7}$$

Similarly, the relationship between $i_{\rm c}$ and $i_{\rm arm}$ can be expressed as

$$i_{\rm c} = S_{i\_\rm Q1fault} i_{\rm arm}. \tag{8}$$

The capacitor voltage $U_{{\rm sm}i\_\rm Q1fault}$ of SM under Q_1 fault can be obtained through (5)–(8)

$$\begin{aligned} U_{{\rm sm}i\_\rm Q1fault} &= \frac{1}{C_{\rm sm}} \int_{t_1}^{t_2} i_{\rm c} dt + U_{{\rm sm}i\_t1} \\ &= \frac{1}{C_{\rm sm}} \int_{t_1}^{t_2} \left(S_i - S_{i\_\rm Q1open}\right) i_{\rm arm} dt + U_{{\rm sm}i\_t1} \end{aligned} \tag{9}$$

where $U_{\mathrm{sm}\ i\_t1}$ is the capacitor voltage at time t_1.

Equation (9) is discretized by the modified Euler algorithm. The discrete formula of the capacitor voltage $U_{\mathrm{sm}i\_\mathrm{Q1fault}}$ is shown in (10) which can apply to the DSP controller

$$U_{\mathrm{sm}i\_\mathrm{Q1fault}}(t) = \frac{1}{C_{\mathrm{sm}}}\int_{t_1}^{t_2}\left(S_i - S_{i\_\mathrm{Q1open}}\right) i_{\mathrm{arm}}dt + U_{\mathrm{sm}i\_t1}$$
$$= \frac{\Delta t}{2C_{\mathrm{sm}}}\left[i_{\mathrm{arm}}(t) + i_{\mathrm{arm}}(t-\Delta t)\right]\left[S_i(t) - S_{i\_\mathrm{Q1open}}(t)\right]$$
$$+ U_{\mathrm{sm}i}(t-\Delta t) \tag{10}$$

where Δt is the duration of the control cycle.

B. Mathematical Model of SM Under Switch Q_2 Fault

If $u_{\mathrm{sm}} = U_{\mathrm{sm}}$ and $i_{\mathrm{c}} = i_{\mathrm{arm}}$ under the conditions of the $S_i = 0$ and $i_{\mathrm{arm}} > 0$, it can be concluded that switch Q_2 has an open circuit fault. Similarly, the final switching function S_{i_Q2fault} can be defined as 1 when the $S_i = 0$ and $i_{\mathrm{arm}} > 0$. In this state, the S_{i_Q2fault} can be regarded as a modified switching function S_{i_Q2open} plus the switching function S_i. To make S_{i_Q2fault} applicable in other states of Q_2 fault, S_{i_Q2open} and S_{i_Q2fault} under Q_2 fault are shown in

$$S_{i\_\mathrm{Q2open}} = \begin{cases} 1, \text{ when } S_i = 0 \,\&\, i_{\mathrm{arm}} > 0 \\ 0, \text{ other conditions} \end{cases} \tag{11}$$

$$S_{i\_\mathrm{Q2fault1}} = S_i + S_{i\_\mathrm{Q2open}}. \tag{12}$$

When the switch Q_2 fault, the relationship between u_{sm} and SM capacitor voltage U_{sm} can be derived

$$u_{\mathrm{sm}} = S_{i\_\mathrm{Q2fault}} U_{\mathrm{sm}}. \tag{13}$$

Similarly, the relationship between i_{c} and i_{arm} under switch Q_2 fault can be expressed as

$$i_{\mathrm{c}} = S_{i\_\mathrm{Q2fault}} i_{\mathrm{arm}}. \tag{14}$$

According to (11)–(14), the capacitor voltage $U_{\mathrm{sm}i\_\mathrm{Q2fault}}$ of SM under Q_2 fault can be calculated by

$$U_{\mathrm{sm}i\_\mathrm{Q2fault}} = \frac{1}{C_{\mathrm{sm}}}\int_{t_1}^{t_2} i_{\mathrm{c}}dt + U_{\mathrm{sm}i\_t1}$$
$$= \frac{1}{C_{\mathrm{sm}}}\int_{t_1}^{t_2}\left(S_i + S_{i\_\mathrm{Q2open}}\right) i_{\mathrm{arm}}dt + U_{\mathrm{sm}i\_t1}. \tag{15}$$

Equation (15) through the Euler algorithm can be converted as

$$U_{\mathrm{sm}i\_\mathrm{Q2fault}}(t) = \frac{1}{C_{\mathrm{sm}}}\int_{t_1}^{t_2}\left(S_i + S_{i\_\mathrm{Q2open}}\right) i_{\mathrm{arm}}dt + U_{\mathrm{sm}i\_t1}$$
$$= \frac{\Delta t}{2C_{\mathrm{sm}}}\left[i_{\mathrm{arm}}(t) + i_{\mathrm{arm}}(t-\Delta t)\right]\left[S_i(t) + S_{i\_\mathrm{Q2open}}(t)\right]$$
$$+ U_{\mathrm{sm}i}(t-\Delta t). \tag{16}$$

The mathematical model of the faulty SM diagram based on S_{i_Q1open} and S_{i_Q2open} is shown in Fig. 4.

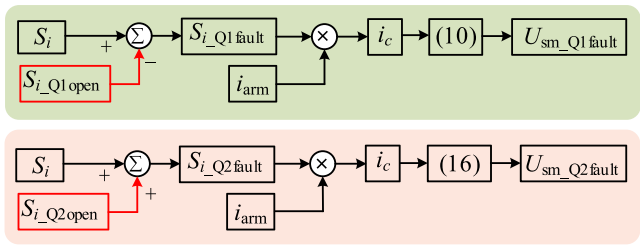

Fig. 4. Mathematical model of the faulty SM diagram.

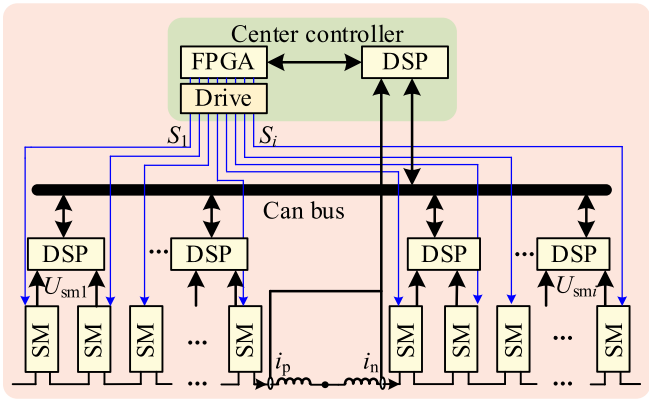

Fig. 5. Schematic diagram of MMC data transmission.

C. Data Transmission

From (10) and (16), the capacitor voltages $U_{\mathrm{sm}i\_\mathrm{Q1fault}}(t)$ and $U_{\mathrm{sm}i\_\mathrm{Q2fault}}(t)$ under switch open circuit at time t can be calculated relies on the $i_{\mathrm{arm}}(t)$, $i_{\mathrm{arm}}(t\text{-}\Delta t)$, $S_i(t)$, $U_{\mathrm{sm}i}$ $(t\text{-}\Delta t)$ and the modified switch function $S_{i\_\mathrm{Q1fault}}(t)$ or $S_{i\_\mathrm{Q2fault}}(t)$. All of the abovementioned states can be recorded by the DSP controller through the sampling circuit.

The detailed data transmission structure of MMC is depicted in Fig. 5. The voltages of the SM capacitors are sampled by the subcontroller TMS320F2812 and then transmitted through the Can bus to the center controller TMS320F28335. The arm currents are sensed in real-time by the center controller. Through the carrier shift modulation, the gating signals of the SMs are generated by the FPGA, where the communication between the center controller and FPGA through the external interface module XINTF. Accordingly, the gating signals can be transmitted to the center controller.

D. Capacitance Monitoring

When the capacitor is installed in the SM, its capacitance is difficult to be directly measured by a capacitance measuring instrument such as precision LCR meter. In addition, the degradation of the SM capacitance will degrade the accuracy of the MMC control. Therefore, different capacitance monitoring methods have been proposed [9], [36], [37], [38]. Traditionally, the SM capacitance can be monitored directly using i_{arm}, U_{sm}, and S_i, which can calculate the SM capacitance accurately, and the relative error is within 1%. Nevertheless, the integral

computation of these methods can occupy the CPU resource [9], [36]. To further simplify the method, peak-to-peak capacitor voltage and the discharging time of the SM capacitor are used to monitor the capacitance [37], [38]. However, when monitoring the capacitance, it is essential to halt the corresponding SM from working for a period of time, which increases the complexity of the control algorithm.

Avoiding capacitor aging impair the accuracy of the capacitor voltages $U_{\mathrm{sm}i\_\mathrm{Q1fault}}(t)$ and $U_{\mathrm{sm}i\_\mathrm{Q2fault}}(t)$, which are computed by formulas (10) and (16), and occupying the computing resources, an effective capacitance monitoring method is proposed without adding extra sensors. This method can monitor capacitance online in the capacitor precharge stage when the MMC starts up. Therefore, the MMC control method does not need to be modified. At the capacitor precharge stage, using the capacitor voltage U_{sm}, charging current i_{m}, and sampling period T_{s}, the capacitance $C_{\mathrm{sm}i}$ can be obtained using

$$C_{\mathrm{sm}i}\frac{dU_{\mathrm{sm}}}{dt}=i_{\mathrm{m}}. \tag{17}$$

The detailed model for calculate the capacitance shown as follows:

$$C_{\mathrm{sm}i}=\frac{i_{\mathrm{m}}\left(t\right)T_{\mathrm{s}}}{\Delta U_i}=\frac{i_{\mathrm{m}}\left(t\right)T_{\mathrm{s}}}{U_{\mathrm{sm}}\left(t\right)-U_{\mathrm{sm}}\left(t-T_{\mathrm{s}}\right)} \tag{18}$$

where ΔU_i is the voltage rise of the charging capacitor.

Since the charging time of the capacitor lasts 1 to 2 s, (19) can estimate the capacitance of the capacitor numerous times under different sampling periods T_{s}

$$\begin{cases} C_{\mathrm{sm1}}=\frac{i_{\mathrm{m}}(t)T_{\mathrm{s}}}{\Delta U_1} \\ C_{\mathrm{sm2}}=\frac{i_{\mathrm{m}}(t)T_{\mathrm{s}}}{\Delta U_2} \\ \cdots \\ C_{\mathrm{sm}i}=\frac{i_{\mathrm{m}}(t)T_{\mathrm{s}}}{\Delta U_i}. \end{cases} \tag{19}$$

The average capacitance $C_{\mathrm{sm\_a}}$ can be obtained using

$$C_{\mathrm{sm\_a}}=\frac{C_{\mathrm{sm1}}+C_{\mathrm{sm2}}+C_{\mathrm{sm3}}+\cdots+C_{\mathrm{sm}i}}{i}. \tag{20}$$

The detailed process of this method is shown in Fig. 6. The proposed method is carried out during the SM capacitor charged by the voltage sources, where the capacitor voltage U_{sm} and arm current i_{arm} are measured by the SM voltage senser and arm current senser, respectively. The sampling period T_{s} can be flexibly adjusted according to the length of the charging time. In the period T_{s}, the increment of capacitor voltage ΔU_i is obtained by the difference between the sampled voltages at t and t-1. Based on the abovementioned measured values, the capacitance $C_{\mathrm{sm}i}$ obtained by (18). After multiple capacitor monitoring values are obtained through cyclic sampling and calculation, the average capacitance $C_{\mathrm{sm\_a}}$ is obtained by (20).

In practice, the assumed capacitance may deviate from the actual capacitance due to manufacturing biases or capacitor aging. Therefore, to correct the deviation, a capacitance monitoring method based on MMC startup process is proposed, and the capacitance is estimated by (20), which is updated only under the capacitor precharge stage during the MMC manual maintenance.

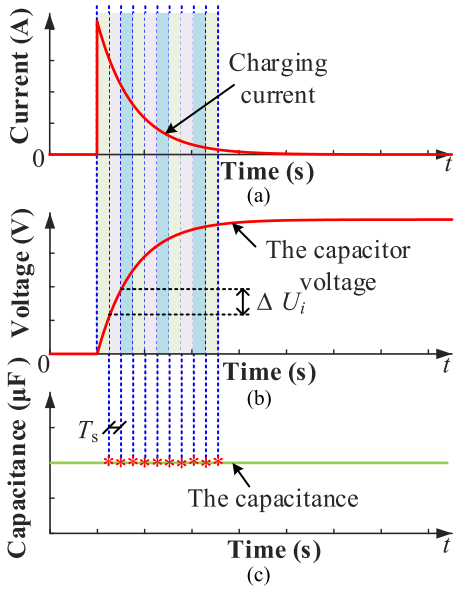

Fig. 6. Schematic diagram of capacitance monitoring.

It does not require real-time updates during MMC operation, which avoids excessive use of computational resources.

If the capacitance is changing all the time, $C_{\mathrm{sm\_a}}$ can be easily perturbed by sampling noise and sensor accuracy. The incorrect capacitance is obtained if these singular values are used for capacitance calculation by (20), which will deviate from its true value. Meanwhile, the estimated capacitor voltage using (10) or (16) with the incorrect capacitance will diverge from the real capacitor voltage and the faulty switch may not be accurately located. In order to avoid capacitance estimation being influenced by sampling noise, bubble sorting algorithm is used to discard singular values during sampling.

E. FDL Method

The FDL method proposed in this article incorporates two stages: 1) fault monitoring and 2) fault location.

1) Stage I. Fault Monitoring Based on Capacitor Voltage: Based on the analysis of the SM characteristics under the switch open circuit fault, the capacitor voltage will increase rapidly within a short period of time. Therefore, this characteristic can be used to sound an alarm for a switch failure. When the SM capacitor voltage is higher than the normal voltage, it can be considered that there is a possibility of an open circuit fault. First, the maximal fluctuation amplitude $\max|\Delta u_c|$ of the SM capacitor voltage can be attained according to the power level of the MMC operation in

$$\max\left|\Delta u_c\left(t\right)\right|=\frac{1}{3}\frac{S_{\mathrm{vN}}}{N\omega C_{\mathrm{sm}}U_{\mathrm{sm\_av}}} \tag{21}$$

where the S_{vN} is the full reactive power capacity of MMC. N is the SM numbers in the arm. $U_{\mathrm{sm\_av}}$ is the rated working voltage of the SM and its value is U_{dc}/N.

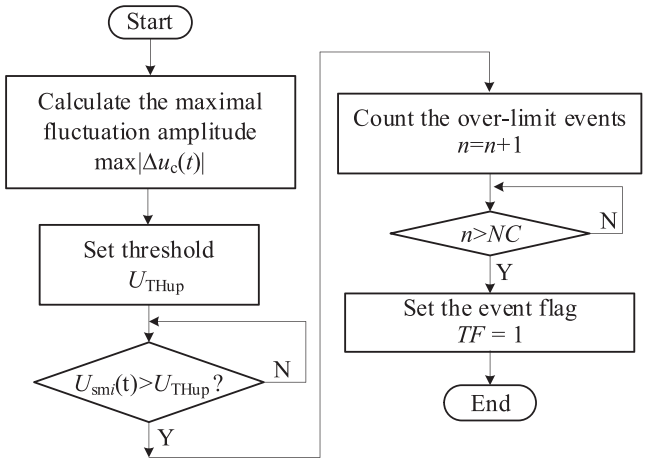

Fig. 7. Flowchart of fault monitoring stage.

Then, inspired by the detailed analysis of the event-triggering threshold in [19], the expression for U_{THup} is given as

$$U_{\mathrm{THup}} = U_{\mathrm{sm\_av}} + m\left(\max\left|\Delta u_c\left(t\right)\right|\right) = U_{\mathrm{sm\_av}} + \frac{1}{3}\frac{mS_{\mathrm{vN}}}{N\omega C_{\mathrm{sm}}U_{\mathrm{sm\_av}}}. \quad (22)$$

At this stage, gain *m,* which is set to 1.2 is adopted to evade the fault alarm caused by noise disturbance. The threshold U_{THup} can be dynamically adjusted with different power capacity S_{vN}, so that the change in the operating state of the MMC will not generate false alarms.

Next, the capacitor voltage $U_{\mathrm{sm}i}$ for the *i*th SM is compared with the U_{Thup}. If the capacitor voltage $U_{\mathrm{sm}i}$ is greater than U_{Thup} at time *t*, as shown in (23), the counter *n* is increased by one

$$n = \begin{cases} n+1, \text{ if } U_{\mathrm{sm}i} \geq U_{\mathrm{THup}} \\ n, \text{ if } U_{\mathrm{sm}i} < U_{\mathrm{THup}}. \end{cases} \quad (23)$$

To prevent false alarms caused by sampling noise and sensor accuracy, a secure threshold *NC* is set, which is chosen based on the maximum number of singular values for *N* consecutive sampled capacitive voltage data points. The abovementioned sampling is repeated to determine the number of anomalous data points for different operating conditions of the MMC. Finally, the maximum number of outliers is denoted by *M*, which is chosen as the basis for designing *NC*.

It is worth noting that *NC* is set 1.2 times larger than *M*, to avoid misdiagnosis and minimize diagnosis time. In general, the larger the threshold value of *NC*, the stronger the ability to avoid noise interference, the fewer false alarm events, and the higher the accuracy of fault detection. However, larger threshold *NC* often results in a longer time for fault diagnosis.

If *n* exceeds *NC*, the event flag $TF_{\mathrm{sm}i}$ is set to 1, which is used to indicate that the switch of the *i*th SM may be faulty

$$TF_{\mathrm{sm}i} = \begin{cases} 1, \text{ if } n \geq NC \\ 0, \text{ if } n < NC \end{cases}. \quad (24)$$

The workflow of the monitoring stage is shown in Fig. 7. In this stage, the computational stress of the monitoring algorithm is diminished due to only the SM capacitor voltages are compared with the U_{Thup} during the fault monitoring stage. The event-triggering threshold U_{THup} is set 56.32 V, which is the same as in [19].

2) Stage II. Fault Location Stage: The principle of locating the fault switch is as follows: if the event flag $TF_{\mathrm{sm}i} = 1$, the estimated capacitor voltages $U_{\mathrm{sm}i\_\mathrm{Q1fault}}(t)$ and $U_{\mathrm{sm}i\_\mathrm{Q2fault}}(t)$ are calculated by the proposed mathematical models of the faulty SM. Simultaneously, if $U_{\mathrm{sm}i\_\mathrm{Q1fault}}(t)$ or $U_{\mathrm{sm}i\_\mathrm{Q2fault}}(t)$ is the same as the measured capacitor voltage $U_{\mathrm{sm}i}(t)$, it means that the corresponding switch has an open circuit fault. Based on the abovementioned principle, the procedures of the fault location stage can be divided into the following steps.

Step 1: Through the modified switch function S_{i_Q1open} and S_{i_Q2open} proposed in (6) and (11), the S_{i_Q1fault} and S_{i_Q2fault} of the *i*th SM are obtained, respectively.

Step 2: $U_{\mathrm{sm}i\_\mathrm{Q1fault}}(t)$ and $U_{\mathrm{sm}i\_\mathrm{Q2fault}}(t)$ are observed by (10) and (16), respectively.

Step 3: Through steps 1 and 2, the estimated and measured voltages are compared in real time. The difference value $\Delta U_{\mathrm{sm}i\_\mathrm{Q1}}(t)$ and $\Delta U_{\mathrm{sm}i\_\mathrm{Q2}}(t)$ are obtained by

$$\Delta U_{\mathrm{sm}i\_\mathrm{Q1}}\left(t\right) = \left|U_{\mathrm{sm}i\_\mathrm{Q1fault}}\left(t\right) - U_{\mathrm{sm}i}\left(t\right)\right| \quad (25)$$

$$\Delta U_{\mathrm{sm}i\_\mathrm{Q2}}\left(t\right) = \left|U_{\mathrm{sm}i\_\mathrm{Q2fault}}\left(t\right) - U_{\mathrm{sm}i}\left(t\right)\right| \quad (26)$$

where $U_{\mathrm{sm}i}(t)$ is the measured voltage of the *i*th SM at time *t*.

Step 4: The faulty switch is located by the approximation principle in (27). If $\Delta U_{\mathrm{sm}i\_\mathrm{Q1}}(t) < \Delta U$, the counter $Q_{1\mathrm{sm}\_i}$ is increased by one. Until $Q_{1\mathrm{sm}\_i}$ exceeds *NQ*, it is concluded that the switch Q_1 in the *i*th SM fault. Similarly, if $\Delta U_{\mathrm{sm}i\_\mathrm{Q2}}(t) < \Delta U$, the counter $Q_{2\mathrm{sm}\_i}$ is increased by one. Until $Q_{2\mathrm{sm}\_i}$ exceeds *NQ*, it can be conclude that the switch Q_2 in the *i*th SM has an open-circuit fault. The flowchart of the location stage is shown in the Fig. 8

$$\begin{cases} \mathrm{Q}_1\mathrm{fault}, & \text{when } \left(\Delta U_{\mathrm{sm}_i\_\mathrm{Q1}}\left(t\right) < \Delta U\right) \& \left(Q_{1\mathrm{sm}\_}i \geq NQ\right) \\ \mathrm{Q}_2\mathrm{fault}, & \text{when } \left(\Delta U_{\mathrm{sm}i\_\mathrm{Q2}}\left(t\right) < \Delta U\right) \& \left(Q_{2\mathrm{sm}\_}i \geq NQ\right) \end{cases} \quad (27)$$

where ΔU is the threshold used to locate the faulty switch. $Q_{1\mathrm{sm}\_i}$ and $Q_{2\mathrm{sm}\_i}$ are the counters of the judgment condition. *NQ* is anti-interference factors, which used to prevent sampling noise interference, and their values are set to 500.

Due to the proposed mathematical model can express the capacitor voltage quantitatively, the $U_{\mathrm{sm}i\_\mathrm{Q1fault}}(t)$ and $U_{\mathrm{sm}i\_\mathrm{Q2fault}}(t)$ can be compared with the capacitor voltage $U_{\mathrm{sm}i}(t)$ at all operating states. Therefore, the FDL method can diagnosis and locate of the faulty switch in every control cycle, and the diagnosis time is shorter compared with the other FDL method.

As mentioned previously, the proposed FDL method consists of two stages: 1) fault monitoring and 2) fault location, which are shown in Figs. 7 and 8 for specific flow graphs, respectively. In the fault monitoring stage, the measured capacitor voltages are compared with the threshold U_{THup} to determine whether the SM is faulty or not. At this stage, only the capacitor voltages of

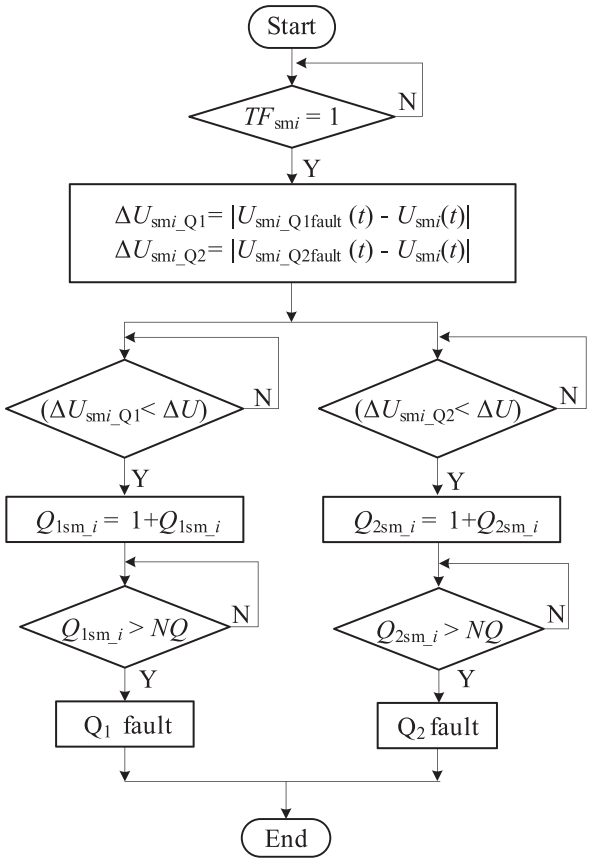

Fig. 8. Flowchart of fault location stage.

each SM need to be measured and compared. The mathematical models are not applied in this stage. However, in the fault location stage, the mathematical models are immediately enabled when a SM fault is detected. At this stage, the mathematical models are used to estimate the capacitor voltage, and the estimated value is compared with the measured value to locate the specific fault switch.

F. Comparison Between the FDL Method

Table II summarizes the characteristics of the FDL methods, which are mainly divided into three categories: 1) hardware-based [6], [7], [8], [9], [10], 2) artificial intelligent-based [11], [12], [13], [14], [15], [16], [17], and 3) model-based [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35]. The characteristics of the proposed FDL method are listed at the bottom of the table. The hardware-based FDL methods [8], [10] have the shortest location time, which is about 5 μs, and the faulty SM can be swiftly identified and isolated. However, the use of additional devices not only leads to complex hardware circuits, but also introduces potential failures and higher system costs. The AI-based FDL methods such as machine learning [12], convolutional neural network [13], [14], and clustering algorithm, have an accuracy rate of about 100%. However, the controller performance of these methods is generally higher than that of existing converter controllers, which virtually increases the cost of the diagnostic system.

By Table II, the most popular method for switch fault diagnosis is the model-based FDL method [18], [19], [20], [21], [22], [23], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], because they do not require additional hardware and have relatively low computational costs. The positioning time of the proposed FDL method in the fault location stage is about 3 to 5 ms and its diagnosis time is shorter compared to these methods. Moreover, the FDL method based on the mathematical model of the faulty SM can locate the faulty switch in every control period even if the state of the faulty SM is the same as that of the normal SM. In addition, this method is also applicable to the case of multiple switch open circuit faults.

IV. Discussion

A. Robustness Analysis

According to the established mathematical model, the robustness of the proposed FDL method based on this model may be limited by factors such as physical parameter accuracy, sampling accuracy, capacitance aging, and sampling noise. For example, the accuracy of the estimated capacitor voltage will be reduced when there is a deviation between the capacitance set in the model and the actual capacitance of the SM. Similarly, in the case of sampling deviation, the estimated capacitor voltage by the model will also lead to inaccuracy. In addition, sampling noise and MMC operating state changes may induce false alarms of the FDL method.

The main causes of false alarm are different in fault monitoring and fault location stages. In the fault monitoring stage, the sampling noise and the MMC operation state are the main causes of false alarm, in which the sampled capacitor voltage may exceed the U_{Thup} and the false alarms is induced. In the fault location stage, the main causes of false alarm are the modeling accuracy and sampling noise. If there are deviation between the assumed capacitance in mathematical model and the actual capacitance, the estimated capacitor voltage does not accurately reflect the true value of the capacitor voltage. To address the abovementioned issues, different measures such as capacitor voltage threshold U_{Thup}, counter threshold *NC*, sampling filter, and capacitance correction algorithm have been used to address false alarms caused by noise interference and changes in the operational state of MMC systems. To verify the effectiveness of the abovementioned measures, as shown in the experimental and simulation sections, the proposed method can accurately locate the fault switches and avoid the occurrence of false diagnostics when the sampled system is accompanied by Gaussian noise, MMC power jumps, and inaccurate parameters.

In conclusion, the robustness of the FDL method requires that it can achieve a keen perception and rapid diagnosis the switch faults in the case of the abovementioned parameter uncertainty and noise interference. At the same time, the false alarm of the FDL method can be reduced to a low level, or even no alarm is activated.

TABLE II
COMPARISON BETWEEN THE FDL METHOD

Ref.	Detection and location method	Detection time	Location time	Additional hardware	Multi faults	Category of FDL	Calculation burden	Precision
[6]	Supervisory sensors	/	<= 5 ms	yes	/	HD	Low	/
[8]	Logical method	/	5 μs	yes	yes	HD	Low	/
[9]	Capacitor voltage	/	<= 300μs	no	/	HD	Low	/
[10]	Bleeding resistor circuit	/	5 μs	yes	yes	HD	Low	/
[11]	Monitoring capacitance	/	13.7~36 ms	no	/	AI, MD	Medium	/
[12]	Machine learning	/	2 ms	no	/	AI	High	98.8%
[13]	1D-CNN	/	100 ms	no	/	AI	High	99.7%
[14]	2D-CNN	/	~10 ms	no	/	AI	High	99.4%
[18]	Arm current, SM voltage	700 steps	100 ms	no	no	MD	High	/
[19]	Circulating current	0.4 ms	20 ms	no	/	MD	Medium	/
[20]	Circulating current	/	8~77 ms	no	yes	MD	Low	/
[22]	Capacitor voltage	/	20~40 ms	no	/	MD	Low	/
[23]	Capacitor voltage	6 ms	~25 ms	no	/	MD	Low	/
[25]	Single ring theorem	/	~40 ms	no	yes	MD	Medium	/
[27]	Arm voltage	1.5 ms	10.3 ms	no	no	MD	Low	/
[28]	Circulating current	/	few ms	no	no	MD	Low	/
[29]	Arm current, drive	/	~5 ms	no	yes	MD	Low	/
[30]	Capacitor voltage	/	~0.1 s	no	yes	MD	Medium	/
[31]	Capacitor voltage	10 ms	10 ms	no	/	MD	Low	/
[32]	Arm voltage	/	~μs	no	yes	MD	Low	/
[33]	SM capacitor	/	~151 ms	no	no	MD	Low	/
[34]	Drive, arm current	10 ms	20 ms	no	yes	MD	Low	/
This paper	Capacitor voltage Model for faulty SM	10~90 ms	3~ 5 ms	no	yes	MD	Low	96%

HD: hardware-based, AI: AI-based, MD: model-based, /: means not mentioned

To improve the robustness of the proposed FDL method, corresponding measures are taken according to the different interference factors.

1) *Antinoise interference capability:* In the fault detection stage, the capacitor voltage threshold U_{Thup}, and the counter threshold *NC* are implemented. U_{Thup} is calculated by (22) quantitatively and can be dynamically adjusted according to the power level of the MMC operation, so the threshold setting is more convenient. In addition, the counter threshold *NC* can effectively avoid false alarms caused by sampling noise. When the SM capacitor voltage exceeds U_{Thup} and the count value *n* exceeds *NC*, it proves that SM is operating in failure. The larger the counter threshold *NC* is set, the stronger the interference ability to noise, but it will lead to an increase in the detection time. In this article, synthesizing the detection time and immunity to noise, the *NC* is set to 100.
2) *More accurate capacitance parameters and parameter deviation immunity:* The setting of the capacitance in the capacitor voltage estimation formula (10), (16) may lead to the deviation of the estimated capacitor voltage from the real value. In Section III, a capacitance monitoring method is proposed, which realizes the rapid identification of SM capacitance in the precharging stage. Therefore, the estimated value of the capacitor voltage is more accurate. In addition, the simulation results under the condition of deviation of the capacitance value are shown in Fig. 11. This method has a certain immunity to parameter uncertainty within a certain range.
3) *Immunity to power jumps:* In order to verify the robustness of the method in the case of power jumps, the experimental results are presented in Fig. 18. The fault diagnosis method proposed in this article has no false alarms when switching between rated, light load, and heavy load conditions. The robustness of the method has been effectively verified.
4) *Accurate measurement:* The black-box correction method is adopted in the sampling process in this experiment, which directly combines the capacitor voltage value with the controller binary value. The error of the sampled value obtained by this method can be regulated within one percent.

In summary, this method can accurately diagnose and locate the fault switch in the case of parameter uncertainty, noise interference, inaccurate sampling, and operating condition change. The robustness of the proposed fault diagnosis and localization method is effectively verified by simulation and experimental results, respectively.

B. Calculation Complexity Analysis

By employing the runtime cycles theory in [31], the computational complexity of the abovementioned methods is shown in Table II. Compared with existing FDL methods, the computational complexity of the proposed FDL method is lower. First, in the fault monitoring stage, the fault SM is detected by comparing the capacitor voltage with the threshold value. In this stage, only the comparison is used, and the executed time within a few microseconds. As the number of SMs increases, the computational pressure increases linearly. However, the calculation in this monitoring stage can be placed in the subcontroller, which can reasonably utilize the computing resources and avoid adding additional control chips.

TABLE III
2 × 2 CONFUSION MATRIX

Real	Truth		
		N	F
	N	TN = 29	FN = 3
	F	FP = 1	TP = 57

TABLE IV
EVALUATION INDEX

Precision	Value
Fault experiments	TP/(TP+FN) = 0.95
normal experiment	TN/(TN+FP) = 0.967
all	(TP+TN)/(TP+FN+ TN+FP) = 0.96

In the fault localization stage, the execution time of the proposed fault mathematical model in DSP (TMS320F28335) is about 8 μs, which main frequency is 150 MHz, and the instruction cycle is 6.62 ns. Therefore, the number of faulty SMs determines the execution time of the program. In practical applications, it is almost impossible for multiple SMs to fail at the same time. Therefore, the method has less computational complexity and can be applied to existing DSP control chips.

C. Performance of Proposed Method

In this article, the simulation and experiment are carried out according to the actual situation. Among them, three kinds of power level steady-state experiments (1.0 p.u., 0.7 p.u., 1.7 p.u.,) and four different power jump experiments are carried out. Experiments on single switch open circuit faults such as Q_1 or Q_2 faults, and multiple switch faults at different power levels are carried out, respectively. In addition, simulations under the condition of sampling noise interference and parameter uncertainty verify the accuracy and effectiveness of the proposed method. The abovementioned experiments and simulations are divided into 18 types, in which each type of experiment is repeated 5 times for a total of 90 verifications. In all experiments, only 4 experiments had false alarms, and the accuracy of fault diagnosis reached 96%.

Table III shows the 2 × 2 confusion matrix, where N and F represent the experimental results are normal and fault, respectively. Through cross validation, the experimental results are divided into four categories through the comparison of experimental scenarios and experimental results: TP (result is fault, and actually fault); TN (result is normal, and actually normal); FP (result is fault, and actually normal); FN (result is normal, and actually fault).

In the open-circuit fault experiment, the accuracy of the fault diagnosis method is 95%. During the MMC operates normally, only one false alarm occurred, and the diagnostic accuracy of the FDL method is 96.7%. By Table IV, the proposed method can accurately locate the faulty switch, and the probability of false alarm is very low during the normal operation of the MMC.

The precision of fault diagnosis methods in the existing literature are listed in Table II. Although the accuracy of this method is lower than that of AI-based methods, it realizes fault diagnosis with high accuracy under limited computing resources.

TABLE V
SIMULATION PARAMETERS

Parameter	Value
$U_{\rm dc}$	220 V
$u_{\rm o}$	100 V
$L_{\rm r}$	1.8 mH
Capacitance of $C_{\rm SM}$	3300 μF
Frequency of $u_{\rm o}$	50 Hz
SM Number of the arm	4
Switching frequency $f_{\rm s}$	2 kHz

D. Current Residual and Detection Delay Analysis

Based on the proposed mathematical model, the capacitor voltage $U_{{\rm sm}i}$ and arm current $i_{\rm arm}$ mainly affected by the sampling circuit transmission delay $t_{\rm ct}$, and the driving signal S_i is mainly affected by the signal transmission delay $t_{\rm st}$. However, the above transmission delay $t_{\rm ct}$ and $t_{\rm st}$ are within nanoseconds, so the estimated capacitor voltage is barely affected by the time delay. In addition, although the above signals are delayed, the above states used to calculate the estimated capacitor voltage in the DSP controller are sampled practically at the same time. In theory, the delay time cannot alter the estimated capacitor voltage.

In the process of capacitor voltage estimation, the current residual under the transient power change is commonly large, which will lead to large fluctuations and singular value phenomena of the estimated capacitor voltage. In the fault location stage, the voltage threshold ΔU and the counter threshold NQ are implemented to filter out the above noise interference and singular values. ΔU and NQ are set to 0.5 V and 500, respectively, which can effectively avoid false alarms caused by sampling noise. In addition, the larger counter threshold NQ is set, the stronger the interference ability to noise, but the detection time will be increased. Therefore, this method can effectively avoid the influence of the current residual.

V. SIMULATION

To verify the mathematical model and the effectiveness of the FDL method, a five-level MMC converter is built by simulation software. The key simulation parameters are shown in Table V.

A. Case A. Model Accuracy and Noise Immunity

Figs. 9 and 10 show the waveforms of $U_{\rm sm1\_Q1fault}$ and $U_{\rm sm5\_Q2fault}$, which are observed by (10) and (16), respectively. In this simulation, the white Gaussian noise under different levels is added to the sampling circuit in units of signal-to-noise ratio (SNR) dB.

Fig. 9(a) shows the $U_{\rm sm1\_Q1fault}$ and $U_{\rm sm1}$ waveforms when the Q_1 in SM_1 fault, where the Gaussian noise with100 dB is added to the sampled value of the capacitor voltage. The

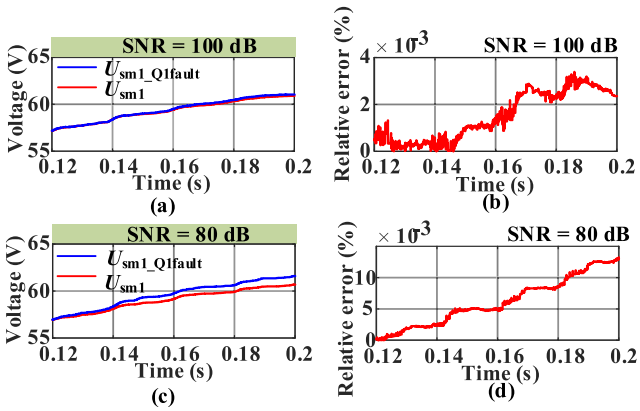

Fig. 9. Simulation results for *case A*. (a) $U_{\mathrm{sm1\_Q1fault}}$ and U_{sm1} under SNR = 100 dB. (b) Relative error of $U_{\mathrm{sm1\_Q1fault}}$ under SNR = 100 dB. (c) $U_{\mathrm{sm1\_Q1fault}}$ and U_{sm1} under SNR = 80 dB. (d) Relative error of $U_{\mathrm{sm1\_Q1fault}}$ under SNR = 80 dB.

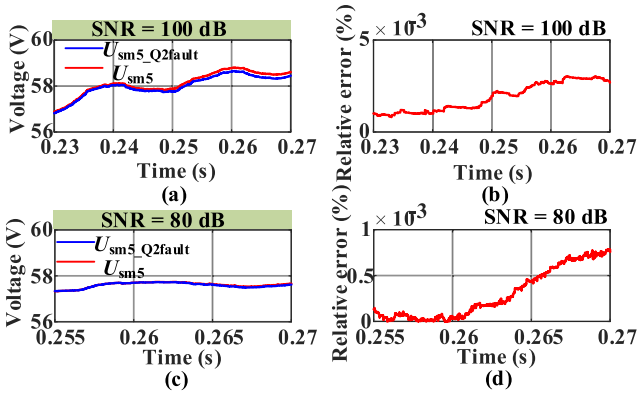

Fig. 10. Simulation results for *case A*. (a) $U_{\mathrm{sm5\_Q2fault}}$ and U_{sm5} under SNR = 100 dB. (c) $U_{\mathrm{sm5\_Q2fault}}$ and U_{sm5} under SNR = 80 dB. (b), (d) Relative error of $U_{\mathrm{sm5\_Q2fault}}$ under SNR = 100 dB and SNR = 80 dB, respectively.

$U_{\mathrm{sm1\_Q1fault}}$ can track the U_{sm1} accurately. Similarly, when the Gaussian noise with 80 dB is added to the capacitor voltage, the $U_{\mathrm{sm1\_Q1fault}}$ can also track the U_{sm1} accurately, as shown in Fig. 9(c). In Fig. 9(b) and (d), the relative error between the estimated capacitor voltage and the actual value is about 1% under the different amplitudes noise interference. Therefore, the proposed model (10) can accurately estimate the capacitor voltage under the Q_1 fault and has a certain anti-interference ability.

Fig. 10(a) shows the $U_{\mathrm{sm5\_Q2fault}}$ and U_{sm5} waveforms when the Q_2 in SM_5 fault, where the Gaussian noise with100 dB is added to the sampled value of the capacitor voltage. Fig. 10(c) shows the $U_{\mathrm{sm5\_Q2fault}}$ and U_{sm5} waveforms with the 80 dB Gaussian noise. The $U_{\mathrm{sm5\_Q2fault}}$ can track the U_{sm5} accurately. In Fig. 10(b) and (d), the relative error between $U_{\mathrm{sm5\_Q2fault}}$ and U_{sm5} is about 0.5% under the different amplitudes noise interference. Therefore, the established mathematical model (16) is accurate and resistant to noise interference.

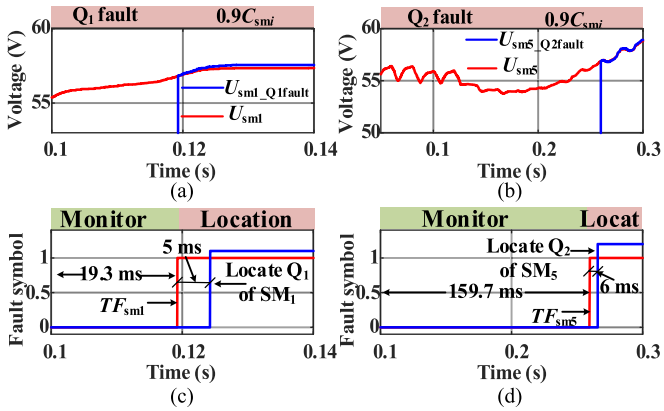

Fig. 11. Simulation results for *case B*. (a) $U_{\mathrm{sm1\_Q1fault}}$ and U_{sm1}. (b) Fault symbol under Q_1 fault. (c) $U_{\mathrm{sm5\_Q2fault}}$ and U_{sm5}. (d) Fault symbol under Q_2 fault.

B. Case B. Immunity for Parameter Inaccuracy

Fig. 11 presents the simulation waveforms when Q_1 and Q_2 fault under the condition that the capacitance $C_{\mathrm{sm}i}$ setting in (10) and (16) is biased. Fig. 11(a) and (b) shows results $U_{\mathrm{sm1\_Q1fault}}$ and fault location waveform for fault diagnosis in which the capacitance value is set to $0.9C_{\mathrm{sm}i}$. It is clearly found that $U_{\mathrm{sm1\_Q1fault}}$ can accurately track U_{sm1} and the fault switch is located within 5 ms in location stage. When Q_2 in SM_5 fault, $U_{\mathrm{sm1\_Q1fault}}$ and fault location waveform are shown in Fig. 11(c) and (d). The $U_{\mathrm{sm5\_Q2fault}}$ can track the U_{sm5} accurately when there is an error in the $C_{\mathrm{sm}i}$. In Fig. 11(d), when TF_{sm5} is set to 1, the fault switch Q_2 in SM_5 is located immediately within 6 ms. Therefore, the FDL method proposed in this article has a certain immunity to parameter inaccuracy.

C. Case C. Q_1 in SM_1 Fault at 0.1 s

Fig. 12 shows the waveforms of capacitor voltages U_{sm1}–U_{sm8}, $U_{\mathrm{sm1\_Q1fault}}$ and fault symbol under Q_1 fault with the100 dB or 80 dB Gaussian noise. When the switch Q_1 of SM_1 has an open-circuit fault at time 0.1 s. Fig. 12(a) shows the voltages of U_{sm1}–U_{sm8}, where the U_{sm1} rises rapidly after the Q_1 fault. In Fig. 9(c), the flag TF_{sm1} is set to 1 at time 0.116 s. Then, the FDL method is activated. The result shows that the event-triggered program can judge the capacitor voltage timely. Finally, the switch Q_1 is located in 0.121 s with 100 dB Gaussian noise by the proposed FDL method. The fault diagnosis time of the FDL method is within 21 ms. In the positioning stage, the FDL method locate the faulty switch Q_1 only takes 5 ms. In Fig. 9(b), the $U_{\mathrm{sm1\_Q1fault}}$ can track the SM_1 capacitor voltage U_{sm1} accurately during the FDL method is activated.

Fig. 12(f) shows the location process under Q_1 fault with 80 dB Gaussian noise. The TF_{sm1} is set to 1 at time 0.119 s and the switch Q_1 is located in 0.122 s by the proposed FDL method. In the positioning stage, the FDL method locate the faulty switch Q_1 only takes 3 ms. In Fig. 12(e), the $U_{\mathrm{sm1\_Q1fault}}$ is nearly agreement with U_{sm1}. Therefore, the proposed FDL

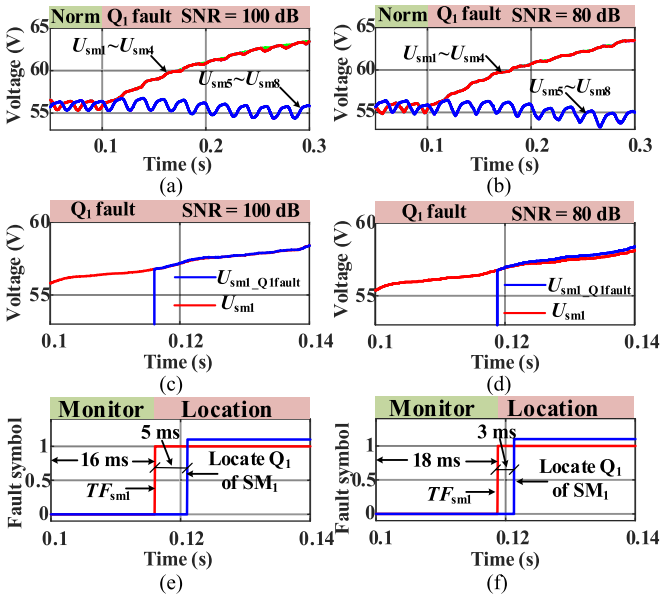

Fig. 12. Simulation results for *case C*. (a)–(c) Waveforms for U_{sm1}–U_{sm8}, $U_{\mathrm{sm1\_Q1fault}}$, and the fault symbol under Q_1 fault with SNR = 100 dB, respectively. (d)–(f) Waveforms for U_{sm1}–U_{sm8}, $U_{\mathrm{sm1\_Q1fault}}$, and the fault symbol under Q_1 fault with SNR = 100 dB, respectively.

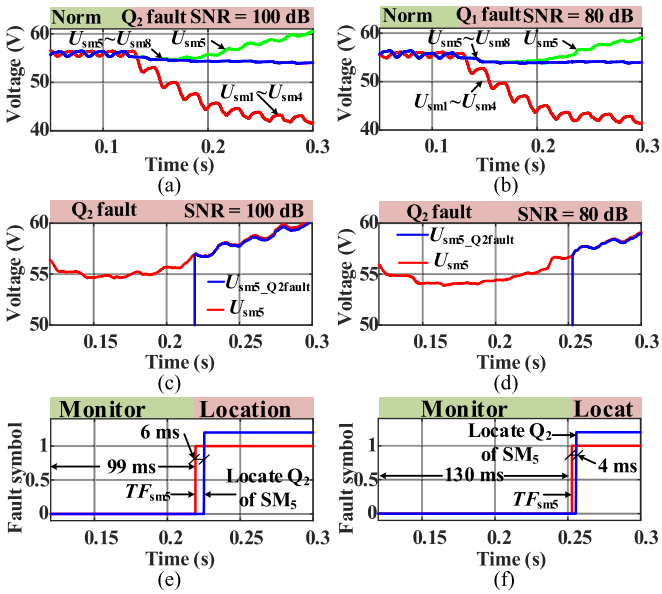

Fig. 13. Simulation results for *case D*. (a)–(c) Waveforms for U_{sm1}–U_{sm8}, $U_{\mathrm{sm5\_Q2fault}}$, and the fault symbol under Q_2 fault in SM_5 with Gaussian noise 100 dB, respectively. (d)–(f) Waveforms for U_{sm1}–U_{sm8}, $U_{\mathrm{sm5\_Q2fault}}$, and the fault symbol under Q_2 fault in SM_5 with Gaussian noise 80 dB, respectively.

method can accurately locate the faulty switch in the case of Q_1 fault and is immune to noise interference.

D. Case D. Q_2 in SM_5 Fault at 0.12 s

Fig. 13 is the simulation waveforms when the switch Q_2 of SM_5 fault at time 0.12 s. Fig. 13(a)–(c) shows the waveforms of U_{sm1}–U_{sm8}, $U_{\mathrm{sm1\_Q1fault}}$ and fault symbol with 100 dB

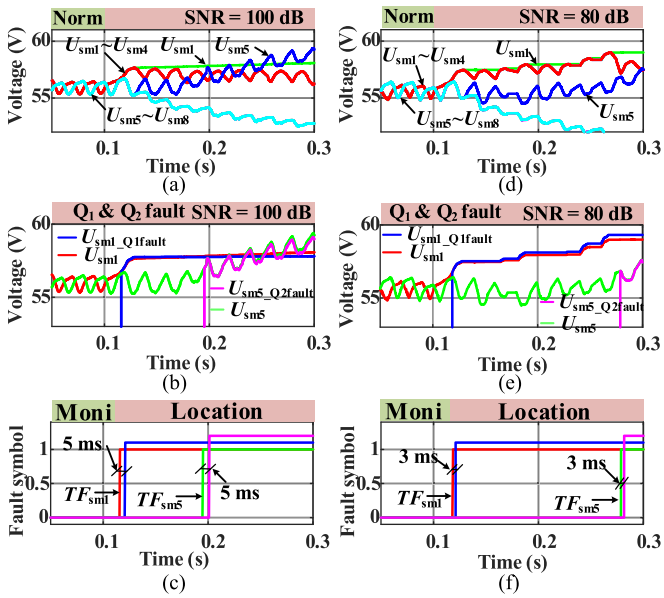

Fig. 14. Simulation results for *case E*. (a)–(c) Waveforms for U_{sm1}–U_{sm8}, $U_{\mathrm{sm1\_Q1fault}}$, $U_{\mathrm{sm5\_Q2fault}}$, and the fault symbol when multiple faults of Q_1 in SM_1 and Q_2 in SM_5 with Gaussian noise 100 dB, respectively. (d)–(f) Waveforms for U_{sm1}–U_{sm8}, $U_{\mathrm{sm1\_Q1fault}}$, $U_{\mathrm{sm5\_Q2fault}}$, and the fault symbol for multiple faults with Gaussian noise 80 dB, respectively.

Gaussian noise, respectively. From Fig. 13(b), U_{sm5} does not exceed the the U_{THup} until 0.219 s under the control of the voltage equalization algorithm. Therefore, from Fig. 13(c), the Q_2 in SM_5 can be located at time 0.225 s within 105 ms. And, the FDL method only took 6 ms to locate the Q_2 fault from the moment the flag TF_{sm5} was set to 1.

In addition, U_{sm1}–U_{sm8}, $U_{\mathrm{sm1\_Q1fault}}$ and fault symbol with 80 dB Gaussian noise can be observed from Fig. 13(d)–(f), respectively. From Fig. 13(d), U_{sm5} does not exceed the U_{THup} until 0.257 s under the control of the voltage equalization algorithm. Then, the Q_2 in SM_5 can be located at time 0.261 s within 4 ms from the moment the flag TF_{sm5} was set to 1. Simulation results confirm that the proposed FDL method can rapidity locate the faulty switch in the case of Q_1 fault and is immune to noise interference.

E. Case E. Multiple Faults of Q_1 in SM_1 and Q_2 in SM_5

The simulation results for multiple faults of Q_1 in SM_1 and Q_2 in SM_5 are illustrated in Fig. 14. The Q_1 of SM_1 and Q_2 of SM_5 have open-circuit faults at time 0.1 s and time 0.12 s, respectively. As shown in Fig. 14(c), the FDL method accurately locates the fault switch Q_1 and Q_2 in 0.121 s and 0.201 s, respectively. Among them, the positioning time of the fault switch is between 3 and 5 ms. Therefore, the FDL method proposed in this article can realize the diagnosis and location of multiple faults when the switches of different SMs have open-circuit faults at different times.

In addition, the $U_{\mathrm{sm1\_Q1fault}}$ shown in Fig. 14(b) coincides well with U_{sm1} with Gaussian noise 100 dB in the sampling voltage. Similarly, the $U_{\mathrm{sm5\_Q2fault}}$ shown in Fig. 14(e) coincides well with U_{sm5} with Gaussian noise 80 dB. It can be

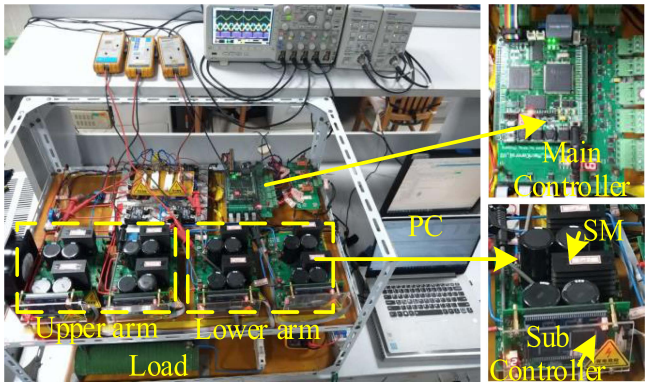

Fig. 15. Five-level MMC platform in the laboratory.

TABLE VI
EXPERIMENTAL PARAMETERS

Parameter	Value
U_{dc}	150 V
u_o	40 V
i_o	8 A
L_r	1.8 mH
C_{SM}	3300 μF
SM Number of the arm	4
Control frequency f_c	4 kHz
Switching frequency f_s	2 kHz

concluded that the mathematical model proposed in this article can accurately estimate the capacitor voltage of faulty SM in the case of multiple faults.

VI. EXPERIMENT VERIFICATION

To verify performance of the proposed FDL method, a single phase MMC platform is built, which the main controller adopts DSP (TMS320F28335) and FPGA (EP3C5E144I7). Fig. 15 shows the photograph of MMC platform. The FDL method is implemented in the main controller, and FPGA generates the SM drive signals. The subcontroller DSP (TMS320F2812) is used to the sampling the capacitor voltage and protect the SM. The dc source adopts high frequency switching dc power (TN-KGZ01).

In order to avoid the experimental platform being damaged by the fault experiment, the voltage of the experiment was depressurized. Furthermore, this experimental condition does not affect the experimental results because the mathematical model of faulty SM is only related to the switch drive and the SM capacitor voltage. The key parameters of the MMC platform are shown in Table VI.

A. Case A. Normal Operation at Rated, Light and Heavy Load

In Case A: the MMC was tested in rated load ($u_o = 40$ V, $i_o = 8$ A), light load ($u_o = 40$ V, $i_o = 5$ A) and heavy load ($u_o = 40$ V, $i_o = 13.3$ A), respectively. The experimental results are shown in Fig. 16. When the MMC is under light load, the u_o, i_o, i_p, U_{sm1}, and U_{sm5} achieve steady-state output, as shown in Fig. 16(a) and (b). Moreover, the fault signal shown in Fig. 16(b) and there is no false alarm occurred during the entire steady-state operation. Similarly, from Fig. 16(c) and (d), the waveforms of the u_o, i_o, i_p, U_{sm1}, and U_{sm5} are stable at rated load and no false alarm occurs. The waveforms of MMC operates under heavy load are shown in Fig. 16(e) and (f). We can observe that the key operating states of MMC such as u_o and i_o, can be output normally and stably. And at the same time, the misdiagnosis does not occur during the entire steady-state operation of the MMC.

Through the experimental results, the FDL method proposed in this article has no fault false alarm under the normal condition of MMC. Therefore, the method works well when the MMC is running normally and can effectively suppress the interference of correlated noise.

B. Case B. Immunity Test on Transient

To verify the robustness of the proposed FDL method, three experiments under output current i_o step change are performed. Fig. 17(a) and (b) shows the waveforms of u_o, i_o, i_p, U_{sm1}, U_{sm5}, drive signal, and fault signal when the i_o jumps from 5 to 8 A. We can find that the FDL method does not produce fault signals under transient conditions. Fig. 17(c) and (d) shows the waveforms of u_o, i_o, i_p, U_{sm1}, U_{sm5}, drive signal, and fault signal when the i_o jumps from 8 to 5 A. No false alarm occurs at this transient. In order to verify the robustness of this method when switching from heavy load to rated load (13.3 A to 8 A), the experimental results are shown in Fig. 17(e) and (f). No false alarm was issued throughout the experiment.

From the results, the FDL method proposed in this article has ability against the transient change of load current. Therefore, the robustness of this method under different load current switching conditions is effective.

C. Case C. Q_1 Fault in SM_1 Under Rated and Light Load

Fig. 18(a)–(c) shows the experimental waveforms when the Q_1 of SM_1 fault under light load. Among them, the partial amplified waveforms of u_o, i_o, and i_p in several cycles are shown in Fig. 18(c). In Fig. 18(a), the u_o and i_o can track the reference value accurately when the MMC is normal. After the switch Q_1 has an open-circuit fault, u_o and i_o are distorted. The SM_1 capacitor voltage U_{sm1} rises quickly from the rated voltage 41.5 to 81 V within 1.4 s. The SM_5 capacitor voltage U_{sm5} in the lower arm drops from 41.5 to 38.1 V. The experimental results of capacitor voltages in Fig. 18(a) verify the simulation results in Fig. 12(a).

Fig. 18(b) is the fault diagnosis and location experiment waveform. In this experiment, the switch open-circuit fault is simulated by setting the drive to low. When the Q_1 in SM_1 has an open-circuit fault, the U_{sm1} rises rapidly and exceeds the fault diagnosis trigger threshold U_{THup}, and the event trigger flag TF_{sm1} is set to 1. Then, the FDL method is working to locate the faulty switch Q_1. In Fig. 18(b), the switch Q_1 is located accurately within 28 ms.

Fig. 18(d)–(f) shows the experimental waveforms when the Q_1 fault under rated load. The partial waveforms of u_o, i_o, and

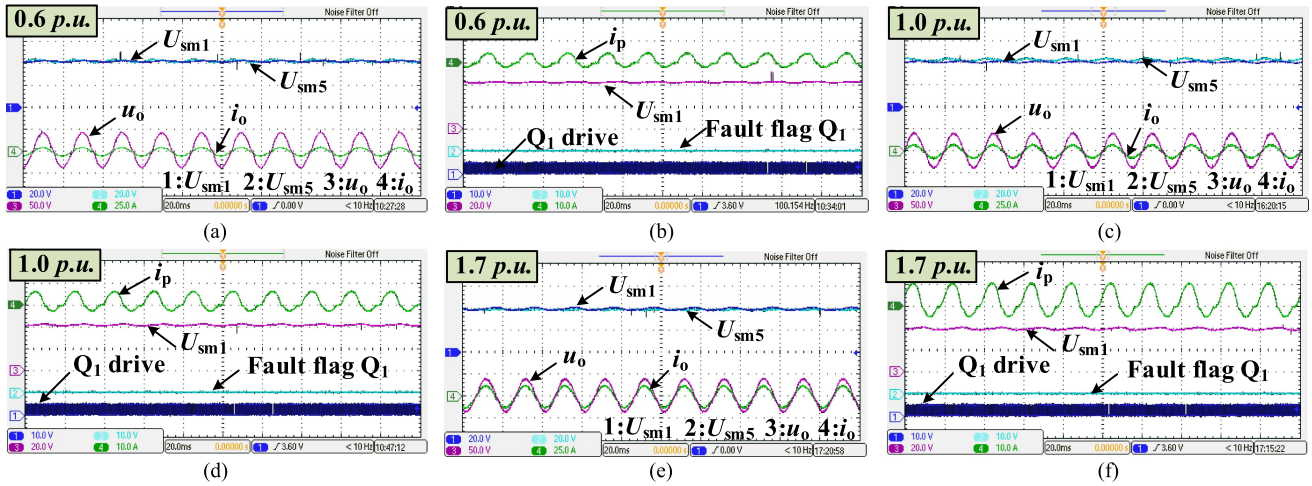

Fig. 16. Experimental waveforms for MMC normal operation. (a), (b) Waveforms for u_o, i_o, i_p, U_{sm1}, U_{sm5} and fault signal under light load. (c), (d) Waveforms for u_o, i_o, i_p, U_{sm1}, U_{sm5} and fault signal under rated load. (e), (f) Waveforms for u_o, i_o, i_p, U_{sm1}, U_{sm5} and fault signal under heavy load.

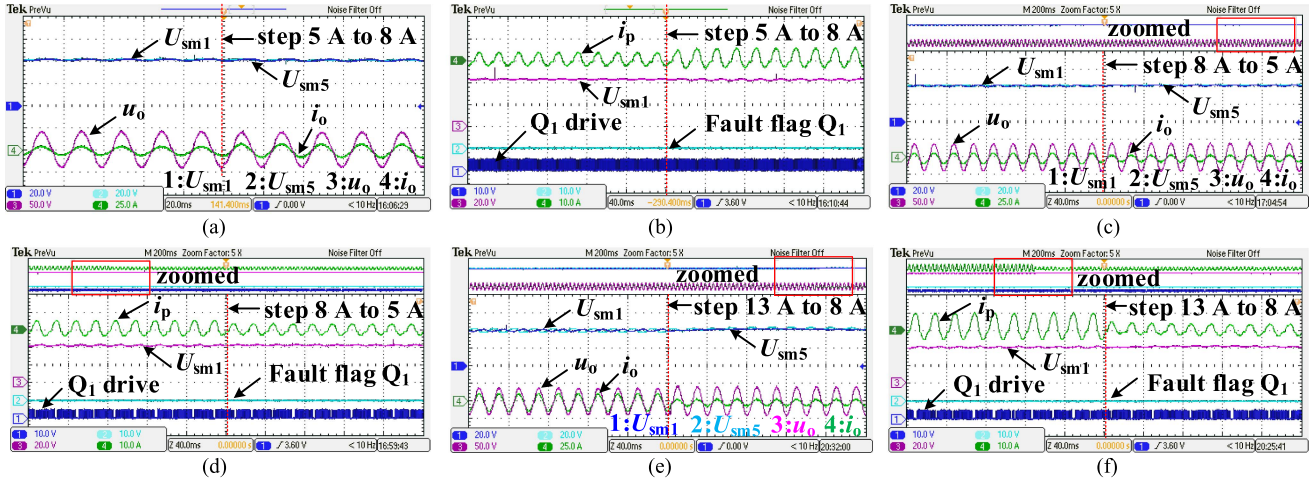

Fig. 17. Experimental waveforms for immunity test under step change of i_o. (a), (b) Results under i_o jumps from 5 to 8 A. (c), (d) Results under i_o jumps from 8 to 5 A. (e), (f) Results under i_o jumps from 13.3 to 8 A.

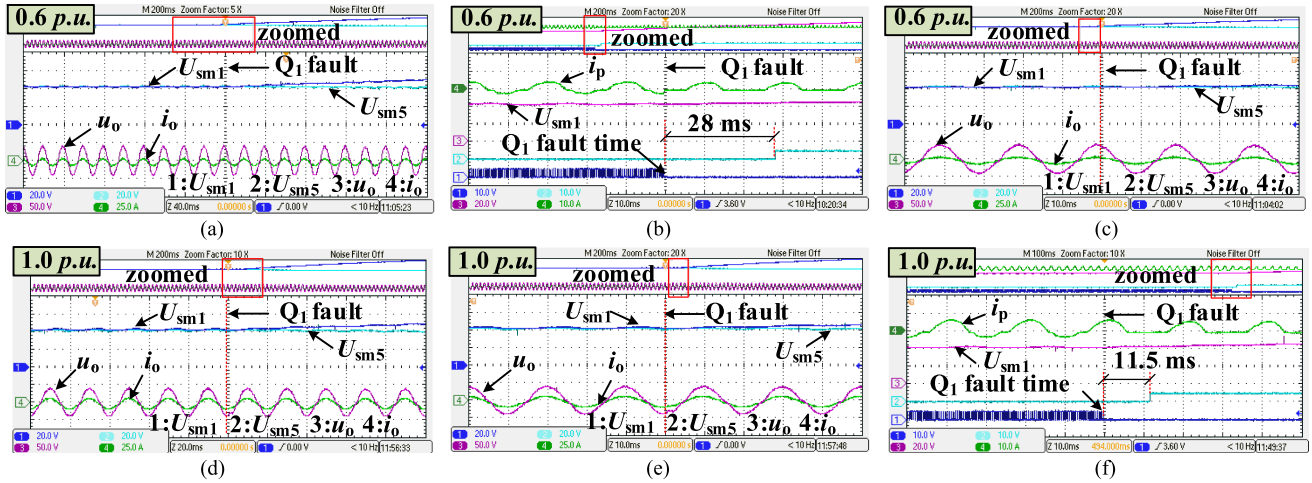

Fig. 18. Experimental results for Q_1 fault in SM_1 under rated and light load.

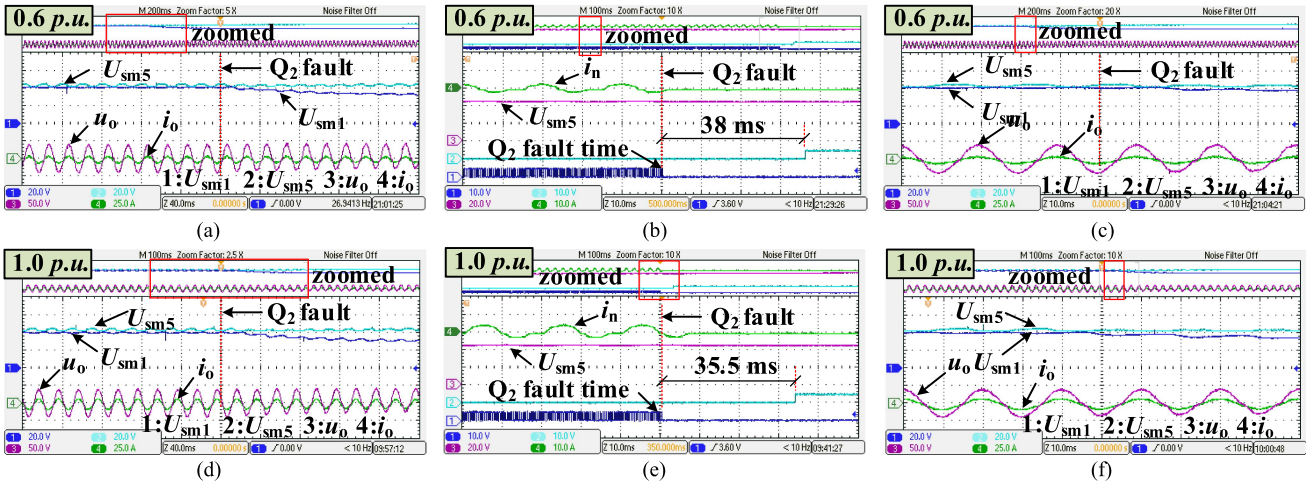

Fig. 19. Experimental results for Q_2 fault in SM_5 under rated and light load.

i_p in several cycles are shown in Fig. 18(e). After the switch Q_1 fault, U_{sm1} rises quickly and exceeds the threshold U_{Thup}. Then, the event trigger flag TF_{sm1} is set to 1, and the FDL method is working to locate the faulty switch Q_1. In Fig. 18(f), the switch Q_1 is located accurately within 11.5 ms.

The experimental results show that the mathematical model of the faulty SM can express the capacitor voltage accurately. The FDL method based on this model can detect the faulty switch in time whether under light load or rated load condition. Simultaneously, the MMC downtime event is avoided.

D. Case D. Q_2 Fault in SM_5 Under Rated and Light Load

Fig. 19(a)–(c) shows the experimental waveforms when the Q_2 of SM_5 fault under light load. Among them, the partial amplified waveforms of u_o, i_o, and i_p in several cycles are shown in Fig. 19(c). The U_{sm1}, U_{sm5}, u_o, and i_o are shown in Fig. 19(a). When Q_2 fault, the U_{sm5} rises slowly due to the capacitor voltage equivalent algorithm. The U_{sm5} rises from 41.5 to 57.7 V within 1.4 s. The U_{sm1} drops from 41.5 to 35.1 V. The capacitor voltage trend of U_{sm1} and U_{sm5} in Fig. 19(a) are the same as the simulation waveforms in Fig. 13(a). Therefore, the experimental results verify the correctness of the simulation. In Fig. 19(a), the negative half cycle of u_o is missing a level. The u_o and i_o of the MMC can not track reference accurately.

Fig. 19(b) shows the fault location experiment waveform for Q_2 fault. The event-triggered flag TF_{sm5} is set to 1 after the Q_2 open-circuit and the faulty switch Q_2 is quickly located within 38 ms by the proposed FDL method. In addition, the rising rate of the capacitor voltage U_{sm5} is smaller than the capacitor voltage U_{sm1} in Fig. 19(b). The reason is that the capacitor voltage of SM_5 has a discharge loop, and the amplitude of the lower arm current is reduced by the closed-loop controller. Therefore, the experimental results verify the feasibility of this method.

Fig. 19(d)–(f) shows the experimental waveforms when the Q_2 of SM_5 fault under rated load. Among them, the partial amplified waveforms of u_o, i_o, and i_p in several cycles are shown in Fig. 19(f).

Fig. 19(e) shows the fault location experiment waveform for Q_2 fault. The event-triggered flag TF_{sm5} is set to 1 after the Q_2 open-circuit and the faulty switch Q_2 is quickly located within 38 ms by the proposed FDL method. In addition, the rising rate of the capacitor voltage U_{sm5} is smaller than the capacitor voltage U_{sm1} in Fig. 19(e). The reason is that the capacitor voltage of SM_5 has a discharge loop, and the amplitude of the lower arm current is reduced by the closed-loop controller. Therefore, the experimental results verify the feasibility of this method.

E. Case E. Multiple Faults Under Rated and Light Load

The experimental waveforms under rated load for multiple faults of Q_1 in SM_1 and Q_2 in SM_5 are illustrated in Fig. 20. Fig. 20(a) shows the experimental waveform of the whole process of multiple faults, where the U_{sm1} and U_{sm5} rise quickly after the switch Q_1 and Q_2 fault. Fig. 20(b) and (c) are the partially amplified waveforms of Q_1 and Q_2 faults, respectively. We can see that the FDL method proposed in this article achieves fault location within 16.8 ms and 15.7 ms, respectively, after the corresponding switch fault occurs. Fig. 20(d)–(f) shows the experimental waveforms of i_p, i_n, drive signal of Q_1 and Q_2. The zoomed waveforms of these states are shown in Fig. 20(e) and (f).

The experimental waveforms under light load for multiple faults of Q_1 in SM_1 and Q_2 in SM_5 are illustrated in Fig. 21. The U_{sm1}, U_{sm5}, U_{sm6}, and u_o are shown in Fig. 21(a), where U_{sm1} and U_{sm5} rise quickly after the switch Q_1 and Q_2 fault. Fig. 21(b) and (c) are the partially amplified waveforms of Q_1 and Q_2 faults, respectively. The FDL method locate the faults switch Q_1 and Q_2 within 16.1 ms and 24 ms, respectively, under light load. Fig. 21(d)–(f) shows the experimental waveforms of i_p, i_n, drive signal of Q_1 and Q_2. The zoomed waveforms of these states are shown in Fig. 21(e) and (f).

The abovementioned experimental results show that the proposed FDL method can realize rapid diagnosis and localization of multiple faults, and is robust to different power levels of MMC operation.

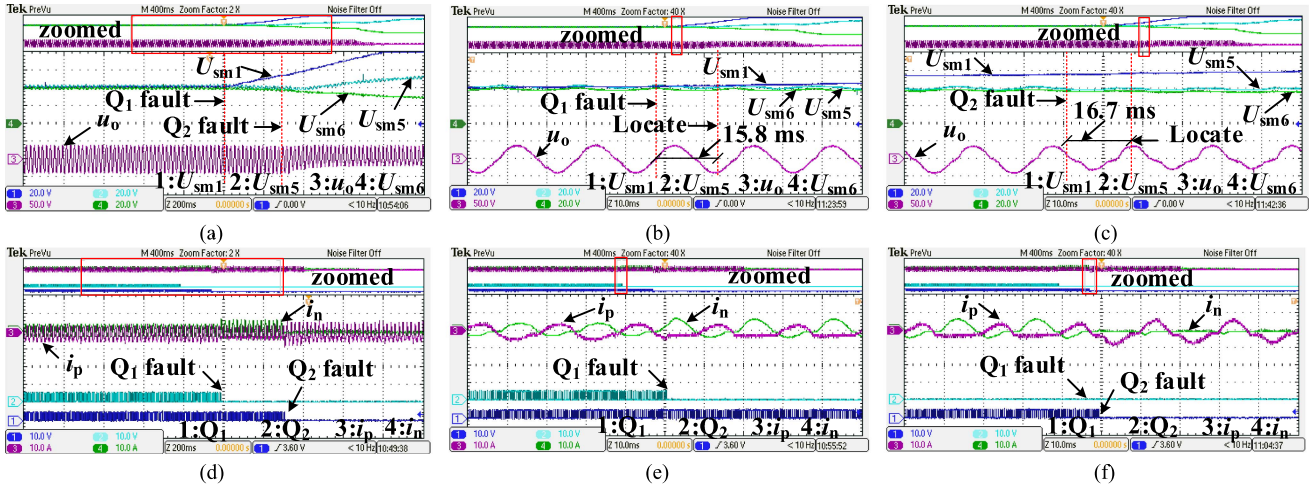

Fig. 20. Experimental waveforms for multiple faults under rated load.

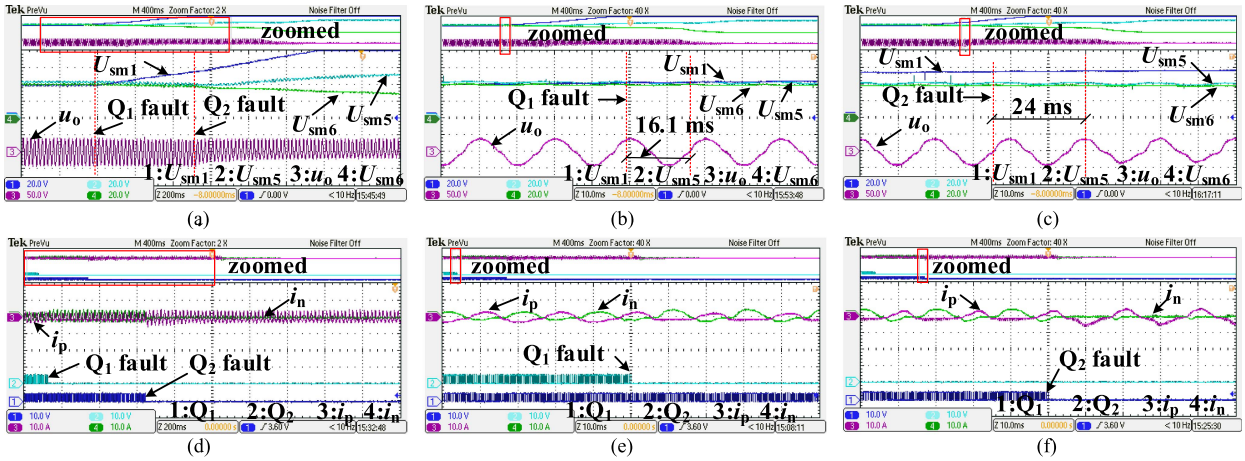

Fig. 21. Experimental waveforms for multiple faults under light load.

VII. Conclusion

In this article, the SM characteristics of the capacitor voltage and current under the switch open-circuit fault are analyzed. A novel FDL method is present by using a modified switching function $S_{i\_Qx\text{fault}}$ and the mathematical model of the faulty SM. Finally, simulation and experimental platforms were built to verify the FDL method. Three conclusions of this article are drawn as follows.

1) A mathematical model of the faulty SM can accurately express the capacitor voltage behavior of the faulty SM through the modified switching function $S_{i\_Q1\text{open}}$ and $S_{i\_Q2\text{open}}$.
2) The FDL method based on the mathematical model can locate the faulty switch in time, whether it is a single switch fault or a multiswitch fault.
3) This FDL method is robust to interference factors such as sampling noise, power jump, and parameter uncertainty. And it can locate fault switch under different working conditions within one to two fundamental cycles.

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