A Fast Transient Current-Mode Buck Converter With Linear Regulation Mode

Pang-Jung Liu, *Senior Member, IEEE*, Wei-Yi Cheng, Lin-Hao Chien, and Jing-Yuan Lin, *Member, IEEE*

***Abstract*—This article proposes a configurable supply mechanism in the power stage to simultaneously improve the load transient response and power conversion efficiency. The power stage, comprising a dc–dc converter and an auxiliary power circuit (APC), can be organized depending on the variable load conditions. During step-load changes, the APC can provide an additional charging or discharging current to the output capacitance of the dc–dc converter to compensate for any differences between the load current and inductor current. Meanwhile, two auxiliary transient transistors are employed to immediately adjust the output level of the error amplifier because the peak current-mode control is used in the dc–dc converter. Thus, the recovery time and output transient ripple are enhanced significantly. At the steady state, the APC is inactivated; thus, the conversion efficiency of the dc–dc converter does not degenerate. Above medium loads, only the dc–dc converter is activated to deliver adequate power with high efficiency. At light loads, the APC acts as a linear regulator to take over the energy delivery scheme because power consumption is reduced effectively while the output voltage is kept. Therefore, the hybrid operation can guarantee improvements in load transient response and power conversion efficiency at light loads. The proposed converter was fabricated with 0.35-μm CMOS technology. The experimental results showed that the recovery times for 450-mA step-down and step-up loads are 1.6 and 2.0 μs, respectively. Comparing to when the transient mode is disabled, the recovery time of the output voltage is improved by over ten times when the transient mode is enabled. Further, the efficiency improvements with the proposed method at load current of 20 mA under the output voltages of 2.5 V and 1.8 V are 13.8% and 4.9%, respectively.**

***Index Terms*—Current mode, dc–dc converter, efficiency, error amplifier, transient response.**

I. Introduction

OWING to high conversion efficiency, switching power converters are widely employed in battery-powered electronic products to convert an input voltage to a desire output value. Portable electronic products require fast processing speed; therefore, the load transient response of power converters are critical because the correct operation function should be ensured. Moreover, users also prefer that systems respond as quickly as possible, especially portable electronic products.

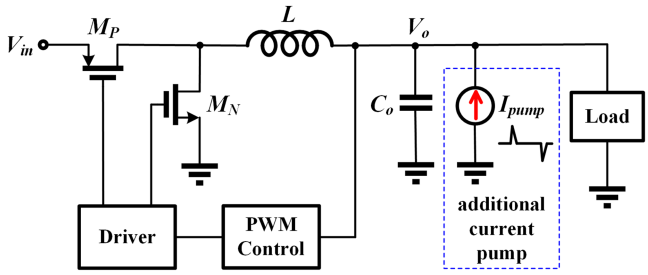

Fig. 1. Auxiliary current pump module for voltage-mode PWM control.

Although there are many options for designing such power supply, a dc–dc buck converter is an attractive option. However, designing a high-performance buck converter capable of handling fast transient response, high conversion efficiency, constant switching frequency, low output voltage ripple, and small system size is quite challenging. For instant, since the inductor of a buck converter restricts the slew rate of the output current, the step-load changes cause a transient ripple on the output voltage of the buck converter for a certain period of time. Reducing the converter inductance can increase the output current slew rate and decrease the form factor of inductor; however, this will also lead to a larger output voltage ripple and larger inductor current ripple simultaneously. To alleviate this issue, one of the methods is to increase switching frequency, leading to high converter bandwidth. Nevertheless, this method suffers large switching loss and then severely degrades efficiency under light loads. As a result, there is a tradeoff among the required features of the buck converter.

Various techniques have been presented to enhance the transient response of dc–dc buck converters [1], [2], [3], [4], [5], [6], [9], [10], [11], [12], [13]. Both hysteretic control and on-time control can achieve a fast transient response because their feedback delays are reduced and their duty cycles could be saturated to either 100% or 0% [1], [2], [3], [4], [5], [6]. However, their switching frequencies are dynamically altered, which depends on the operation conditions, such as the load current, input voltage, and parasitic resistance. Thus, the two controls are prone to the electromagnetic interference (EMI) issue. Further, it is difficult to optimize the design of an EMI

Manuscript received 26 June 2022; revised 27 August 2022 and 20 October 2022; accepted 16 November 2022. Date of publication 21 November 2022; date of current version 26 December 2022. This work was supported by the Ministry of Science and Technology, Taiwan, under Grant MOST 109-2628-E-027-001-MY3. Recommended for publication by Associate Editor X. Ruan. *(Corresponding author: Pang-Jung Liu.)*

Pang-Jung Liu and Lin-Hao Chien are with the Department of Electrical Engineering, National Taipei University of Technology, Taipei 10608, Taiwan (e-mail: pjliu@ntut.edu.tw; m6429792@gmail.com).

Wei-Yi Cheng is with the Etron Technology, Inc., Hsinchu 30078, Taiwan (e-mail: peter1993110@gmail.com).

Jing-Yuan Lin is with the Department of Electronics Engineering, National Taiwan University of Science and Technology, Taipei 10617, Taiwan (e-mail: jylin@mail.ntust.edu.tw).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3223680.

Digital Object Identifier 10.1109/TPEL.2022.3223680

filter. To alleviate this EMI issue, pulsewidth modulation (PWM) control is widely adopted in switching dc–dc converters because a constant switching frequency is employed [7], [8]. The PWM control of a dc–dc converter can be divided into the voltage mode and current mode. Owing to the advantages of the input voltage feedforward property, automatic over-current protection, and simpler frequency compensation, the peak current-mode control is widely used [8], [9].

Chen et al. [3] utilizes a current-mode hysteretic control and presents an active current-sensing circuit without a sample-and-hold circuit to realize short transient response time. To alleviate the issue of switching frequency variation, a phase-frequency-locked circuit is used. However, the improvement of light-load efficiencies with hysteretic control is degraded. In addition, since the inductor current is controlled by the hysteretic control, the presented converter could not operate in discontinuous conduction mode (DCM) when load current is small. Even if the converter could operate in DCM, the power loss would increase significantly. For [7], a dual operating modes (DOMs) control is presented to cooperate with an error amplifier for improving the load transient of a dc–dc converter with voltage mode control. To enhance the slew rate of the error amplifier during transient, the DOM control is adopted to raise/reduce the gate voltages of the output-stage transistors of the error amplifier for enhancing its current driving capability. The implementation of DOM control is simple, but the output-stage transistors of the error amplifier always receive logic low and log high levels when the DOM control is enabled. Thus, the current driving capability of error amplifier is always the same even under different load current changes. Based on the peak current-mode control, Hwang et al. [9] presents an optimum-damping circuit to stabilize the converter and speed up the transient response during load current changes. To realize the optimum-damping control, the current slopes of the dynamic slope generator and the current-sensing circuit should be identical. However, according to (11) of [9], resistance, capacitance, and transconductance are changed with manufacturing process and temperature, especially for resistance. Thus, it is difficult to fulfill (11) and the transient response will be degraded.

Shih et al. [10] used an auxiliary circuit connected to the output node to improve the transient response. However, only the transient response of step-up load is improved because only one auxiliary power transistor is used. In addition, [10] adopts voltage mode control; therefore, there is a single voltage control loop. In [11], [12], and [13], an auxiliary current pump module, as shown in Fig. 1, was adopted to instantly provide charging or discharging current through the output capacitor for both the step-down and step-up loads. Although the aforementioned methods are beneficial in terms of enhancing the load transient response, all of them were designed for a single-loop PWM voltage-mode control rather than a dual-loop peak current-mode control. Further details about the design of the peak current-mode control will be provided in Section II.

In addition to fast transient response, portable electronic products need to extend battery endurance. Enhancing the power efficiency is a practical method to extend battery durability, especially for light loads. However, the major challenge is to determine how the efficiency of a buck converter can be improved. Pulse-frequency modulation control and pulse skipping control are popular strategies to enhance light-load efficiency because the dominant power loss of buck converters at light loads is switching loss [14], [15]. Nonetheless, these techniques are prone to large output voltage ripple and EMI. The gate-driving voltage reduction technique and the adaptive sizing control of power transistors are other valid methods to reduce switching loss; however, they result in larger conduction losses in power transistors [16], [17]. Moreover, to implement such controls, additional complicated control circuits are required.

In recent years, three-level buck dc–dc converters gain more attention for low-voltage applications. Comparing to the traditional buck converters, three-level buck dc–dc converters have advantages including half switch voltage stress, double effective switching frequency, and smaller inductance and output capacitance [18]. With smaller inductance, the three-level buck dc–dc converter has beneficial effects on transient response and converter bandwidth. However, not only the output voltage should be regulated, but also the flying capacitor voltage has to be balanced at half of the input voltage in order to benefit from those mentioned advantages.

To simultaneously consider the issues of load transient response and power conversion efficiency, an auxiliary power circuit (APC) combined with a dc–dc converter is presented in this article. A configurable supply mechanism in the power stage can be effectively organized based on the variable load conditions. During the step-load changes, the APC provides an additional charging or discharging current through the output capacitor of the dc–dc converter to compensate for any differences between the load current and inductor current, leading to a small output transient ripple. At the steady state, the APC is inactivated; thus, the conversion efficiency of the dc–dc converter does not degenerate. Above the medium-load conditions, only the dc–dc converter is activated to deliver adequate power to load with high efficiency. At light loads, the APC acts as a linear regulator to take over the supply function in the proposed converter and maintain the regulated output voltage. Compared to a switching converter, the power loss consumed by the linear regulator at light loads is relatively small; thus, the efficiency in linear mode is maintained. Therefore, the hybrid operation can guarantee improvements in the load transient response and power conversion efficiency. In Section II, the transient response of the buck converter with peak current-mode control will be addressed. Sections III and IV will introduce the design of the proposed converter and the circuit implementation. The experimental results will be illustrated in Section V. Finally, the conclusion will be drawn in Section VI.

II. Analysis of Peak Current-Mode Controlled Buck Converter During Transient State

Before introducing the proposed architecture, the transient response of the peak current-mode controlled buck converter will be reviewed first. As shown in Fig. 2, a buck converter with peak current-mode control has two control loops: One is a current control loop through a current sensor and the other is a

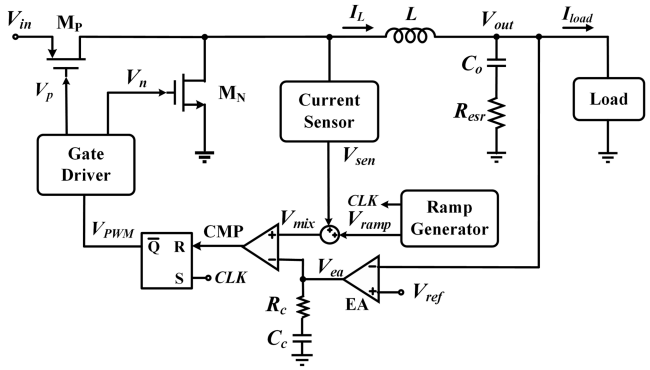

Fig. 2. Conventional peak current-mode controlled buck converter.

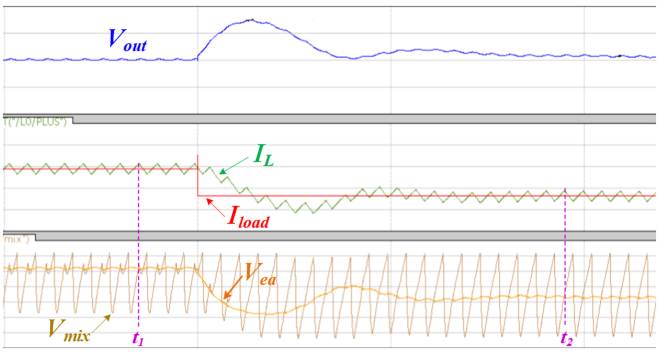

Fig. 3. Simulated transient waveforms of a conventional peak current-mode control for a step-down load. From top to bottom, vertical scale: 100; 340; and 250 mV/div and horizontal scale: 10 μs/div.

voltage control loop through an error amplifier. To prevent subharmonic oscillation for peak current-mode control, the sensed signal $V_{\rm sen}$ of the inductor current is combined with the ramp signal $V_{\rm mix}$ to fulfill the slope compensation. Thus, $V_{\rm mix}$ can be expressed as

$$V_{\rm mix} = V_{\rm ramp} + V_{\rm sen} = V_{\rm ramp} + I_L \cdot R_{\rm sen} \tag{1}$$

where I_L is the inductor current, and $R_{\rm sen}$ is the gain of the current sensor. Since the dc level $I_{L,\rm dc}$ of the inductor current is equal to the value of the load current $I_{\rm load}$, the dc level of $V_{\rm mix}$ is proportional to $I_{\rm load}$. Thus, to ensure a balance between the current and voltage control loops under distinct load currents, the dc level of $V_{\rm ea}$ should be adjusted to diminish the difference.

The simulated transient waveforms of a peak current-mode controlled buck converter, when load current changes from heavy load to light load, are shown in Fig. 3. After a step-down load change, $V_{\rm ea}$ is reduced by the error amplifier to a lower level to ensure that both the current and voltage control loops attained equilibrium. The decreased dc amount of $V_{\rm mix}$ under the two load currents can be expressed as

$$\begin{aligned}\Delta V_{\rm mix} &= V_{\rm mix}(t_2) - V_{\rm mix}(t_1) \\ &= [I_{L,\rm dc}(t_2) - I_{L,\rm dc}(t_1)] \cdot R_{\rm sen} \approx \Delta I_{\rm load} \cdot R_{\rm sen}\end{aligned} \tag{2}$$

where t_1 and t_2 are the times before and after the load-transient response, where the converter operates in the steady state. On the other hand, the decreased dc amount of $V_{\rm ea}$ can be expressed

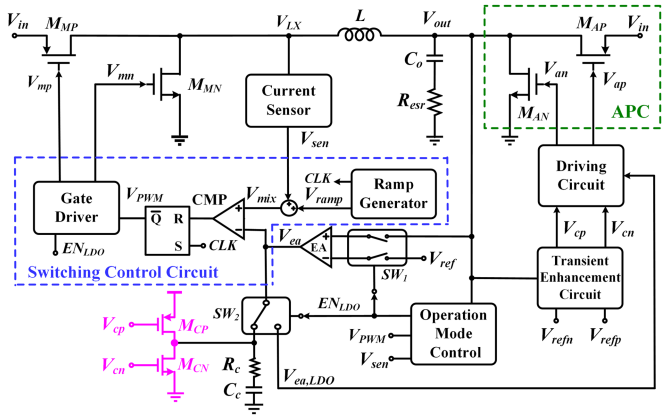

Fig. 4. Architecture of the proposed converter.

through the formula

$$\Delta V_{\rm ea} = \left[g_m \cdot \int_{t_1}^{t_2} (V_{\rm ref} - V_{\rm out})\, dt \right] \Big/ C_c \tag{3}$$

where g_m is the transconductance of the error amplifier. To attain the balance between the two control loops after the step-down load change, (2) and (3) should be identical. Equation (4) can then be obtained as follows:

$$\int_{t_1}^{t_2} (V_{\rm ref} - V_{\rm out})\, dt \approx \frac{C_c \cdot \Delta I_{\rm load} \cdot R_{\rm sen}}{g_m} \tag{4}$$

When a step load change is known, the value on the right-hand side in (4) can be calculated. Moreover, the compensation capacitance is usually large. Thus, if only an APC is employed in a peak current-mode controlled buck converter, the voltage difference between $V_{\rm out}$ and $V_{\rm ref}$ will diminish quickly, which are the input sources for the error amplifier. Consequently, the APC leads to the integration time of the error amplifier more sluggish and the recovery time of a buck converter with peak current-mode control will be affected by the error amplifier to adjust $V_{\rm ea}$.

III. Operation of an Auxiliary Power Circuit Combined With DC–DC Converter

Fig. 4 shows the architecture of the proposed converter. The power stage includes a buck converter and an APC. The control circuits, recognized as the switching control circuit, operation mode control, transient enhancement circuit, and auxiliary transient transistors (M_{CP} and M_{CN}), properly regulated the output voltage $V_{\rm out}$ based on different load current situations.

To derive good power conversion efficiency from heavy- to light-load conditions, the proposed converter is able to operate in the switching mode (from heavy to medium loads) or in linear mode (at light loads). As shown in Fig. 5(a), for the switching mode, the buck converter operates with constant switching peak current-mode control. At the switching mode, $V_{\rm out}$ and the reference signal $V_{\rm ref}$ are connected to the inverting and non-inverting pins of error amplifier EA, respectively. The error amplifier EA helps in maintaining a high loop gain for producing the error signal $V_{\rm ea}$ and determining the duty cycle and reliable output

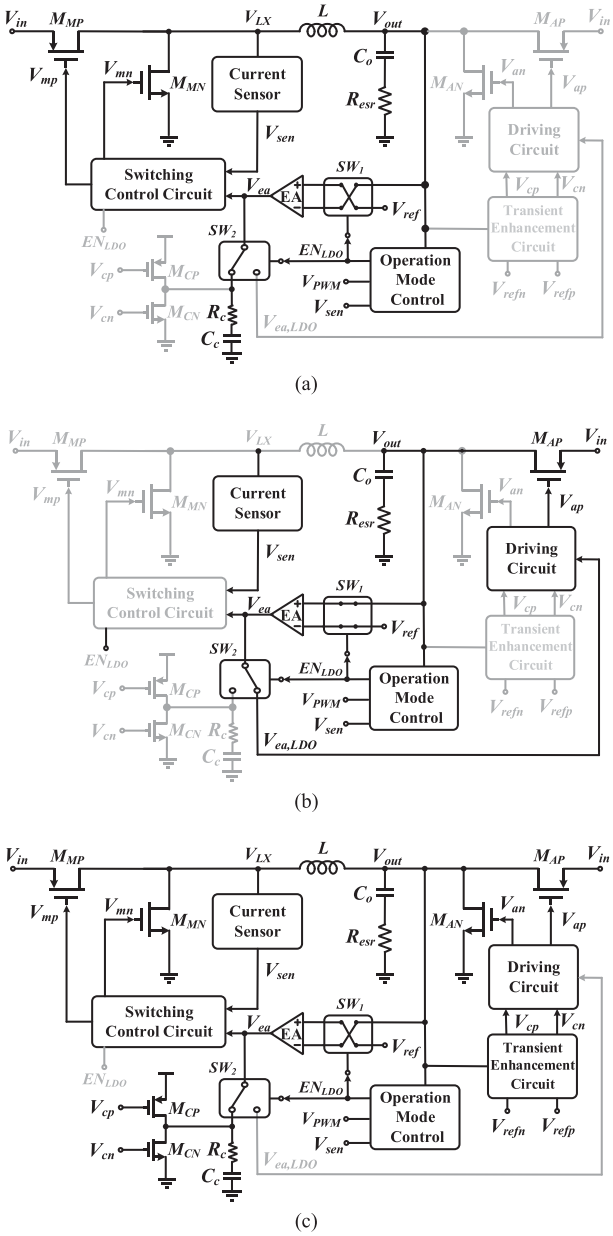

Fig. 5. Proposed converter operation under different load conditions. (a) Switching mode. (b) Linear mode. (c) Transient mode.

voltage regulation. The details of the switching control circuit are shown in Fig. 4. The current sensor and ramp generator are used to realize the current sensing of inductor current and slope compensation, respectively. To avoid subharmonic oscillation when duty ratio is higher than 0.5, the slope m_c of the ramp signal $V_{\rm ramp}$ must be larger than half of the slope m_2 of inductor current when the power transistors M_{MP} and M_{MN} are turned OFF and on, respectively [19]. In other words, it can be expressed as

$$m_c > \frac{1}{2} m_{2,\max} = \frac{1}{2} \frac{V_{o,\max}}{K \cdot L} \tag{5}$$

where K is the current-to-voltage conversion ratio of the current sensor. In our case, K and m_c are set to 1 A/V and 500 kV/s, respectively, to avoid subharmonic oscillation. The converter is compensated by the compensation capacitor C_c and compensation resistor R_c, and the values of C_c and R_c are 80 pF and 42 kΩ, respectively. The comparator CMP and SR latch generate a PWM signal $V_{\rm PWM}$, and the gate driver drives the power transistors M_{MP} and M_{MN}.

To minimize the switching and gate driving losses of M_{MP} and M_{MN} at light loads, the proposed converter serves as a linear regulator, as shown in Fig. 5(b). The transistor M_{AP} of the APC acts as a pass device of the linear regulator to adjust the output voltage. The operation mode control monitors the load current condition and produces a signal EN_{LDO}. To ensure proper operation in the linear mode, $V_{\rm out}$ and $V_{\rm ref}$ are connected to the noninverting and inverting pins of EA through the switch SW_1, respectively, and $V_{\rm ea}$ is connected to $V_{\rm ea,LDO}$ through the switch $\rm SW_2$. $\rm SW_1$ and $\rm SW_2$ are controlled by $\rm EN_{LDO}$. Since the output capacitor C_o is large, the dominant pole for the linear mode is to be set at the output node. Two low-frequency nondominant poles occur at the output of EA and the gate of the auxiliary transistor M_{AP}. To avoid degrading the loop stability, $V_{\rm ea}$ is directly sent to the driving circuit without connecting to C_c and R_c. Further, two unity-gain buffers are employed in the driving circuit to produce a small output resistance. As a result, the two low-frequency non-dominant poles are separated into high frequency to acquire a sufficient loop phase margin. Moreover, the system bandwidth is enlarged by removing C_c and R_c, and the slew rate of the driving circuit is enhanced by the two unity-gain buffers, the details of which will be presented in Section III.

To enhance the transient operation with a change in step-load current, the APC with the transient enhancement circuit is activated as shown in Fig. 5(c). The transient response of the switching converter is restrained by the inductor and the control loop bandwidth, which is usually limited to within 10%–20% of the switching frequency. Due to a larger current slew rate and larger system bandwidth compared to switching converters, the APC achieves a remarkable load transient response. At this mode, $V_{\rm ea}$ is connected to R_c and C_c, and $V_{\rm out}$ and $V_{\rm ref}$ are connected to the inverting and non-inverting pins of EA, respectively. By detecting $V_{\rm out}$, the transient enhancement circuit and driving circuit generate signals V_{ap} and V_{an} for the transistors M_{AP} and M_{AN} to produce additional charging or discharging currents through the output capacitor. Thus, the current slew rate of the proposed converter is enhanced and the output transient ripple is quickly diminished.

As mentioned in Section II, for the peak current-mode controlled buck converter, $V_{\rm ea}$ is varied with a change in the step-load current. Thus, a smaller output transient ripple, which is the input source for the error amplifier, causes a longer transient response of $V_{\rm ea}$. To solve this issue, the auxiliary transient transistors M_{CP} and M_{CN} are employed to charge and discharge the compensation capacitor C_c in the transient mode and dynamically regulate the signal level of $V_{\rm ea}$. The control signals V_{cp} and V_{cn} for M_{CP} and M_{CN} are generated by the transient enhancement circuit. The amount of additional charging/discharging currents provided by the APC and auxiliary transient transistors decreased automatically while the output voltage tends toward

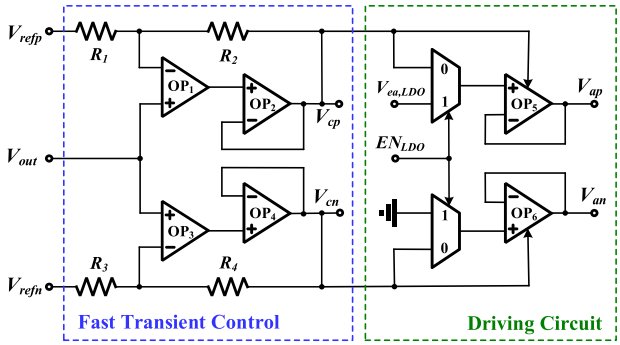

Fig. 6. Schematic diagram of transient enhancement circuit and driving circuit.

the nominal value. Finally, when the output voltage is back to its nominal value, the APC and auxiliary transient transistors are turned off for power saving, thus bringing the operation mode back to the switching mode.

IV. Circuit Implementation

To fulfill the fast transient dc–dc converter with the linear regulation mode, the transient enhancement circuit, driving circuit, and operation mode control are utilized. The detailed circuit implementation for these function blocks is presented in this section.

A. Transient Enhancement Circuit and Driving Circuit

The driving circuit comprises two multiplexers and operational amplifiers OP_5 and OP_6 as shown in Fig. 6. To generate a small output resistance and deliver analog level on signals V_{ap} and V_{an}, OP_5 and OP_6 act as the unit-gain buffers. In the linear mode, signal EN_{LDO} is at logic high and V_{ap} and V_{an} are $V_{\mathrm{ea,LDO}}$ and zero. Thus, the auxiliary power transistors M_{AP} and M_{AN} are regulated by $V_{\mathrm{ea,LDO}}$ and OFF, respectively. On the other hand, when EN_{LDO} changes to logic low, V_{ap} and V_{an} become V_{cp} and V_{cn}, respectively.

The transient enhancement circuit shown in Fig. 6 comprises operational amplifiers OP_1–OP_4 and resistors R_1–R_4. OP_2 and OP_4 are employed to prevent the loading effect and provide a wide swing for V_{cp} and V_{cn}. V_{cp} and V_{cn} can be expressed as

$$V_{cp} = V_{\mathrm{ref}p} + (1 + R_2/R_1)\,(V_{\mathrm{out}} - V_{\mathrm{ref}p}) \tag{6}$$

$$V_{cn} = V_{\mathrm{ref}n} + (1 + R_4/R_3)\,(V_{\mathrm{out}} - V_{\mathrm{ref}n}) \tag{7}$$

The reference signals $V_{\mathrm{ref}n}$ and $V_{\mathrm{ref}p}$ are set as larger and smaller than the nominal V_{out} value, respectively. Thus, in the steady state, V_{cp} and V_{cn} are at high and low levels to turn off the APC, M_{CP}, and M_{CN}. $V_{\mathrm{ref}n}$ and V_{refp} are set as 1.85 V and 1.75 V, respectively. The values of R_1-R_4 are 5, 90, 5, and 90 kΩ, respectively. After a step-up load change, V_{out} drops from its nominal value. When V_{out} falls below $V_{\mathrm{ref}p}$ and EN_{LDO} changes to logic low, V_{cp} and V_{ap} temporarily become a low level. Thus, C_o and C_c are charged rapidly by M_{AP} and M_{CP}, respectively. Since the output undershoot ripple is diminished dramatically and the dc-level difference of V_{ea} is compensated instantly, the recovery time of the proposed converter is shortened significantly. Compared to digital controls, the transient enhancement circuit regulates V_{cp} adaptively depending on the difference between V_{out} and $V_{\mathrm{ref}p}$ to avoid output voltage ringing. When V_{out} is back to the nominal value, M_{AP} and M_{CP} are turned off, and the buck converter and error amplifier subsequently take over V_{out} and V_{ea}, respectively. Similarly, V_{out} rises above $V_{\mathrm{ref}n}$ after a step-down load change. Since V_{cn} and V_{an} temporarily become high level, M_{AN} and M_{CN} are turned on to rapidly discharge C_o and C_c, respectively. Thus, the proposed converter shows an excellent transient response.

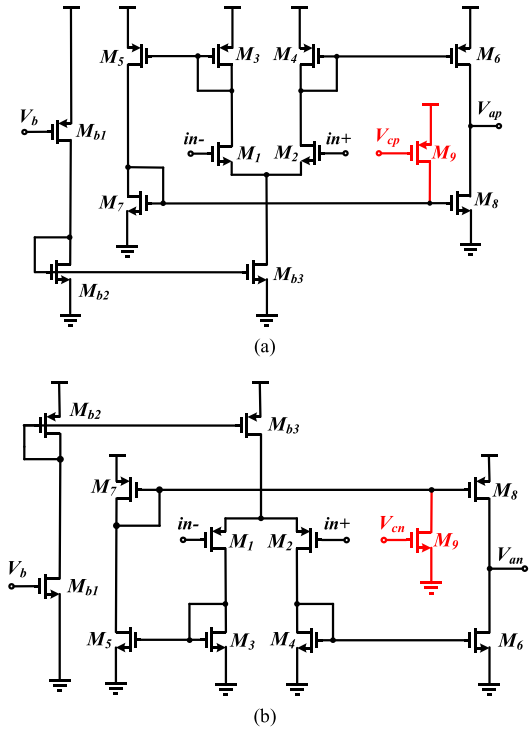

Fig. 7. Schematic diagram of (a) OP5 and (b) OP6.

The schematic diagram of OP_5 and OP_6 are shown in Fig. 7 [20]. Transistors M_1 to M_8 constitute a conventional transconductance amplifier to obtain wide output swing. With regard to OP_5, V_{cp} is at high level in the steady state; thus, transistor M_9 is off. When the switching converter suffers a step-up load current, V_{cp} becomes low level, and M_9 is turned ON. Since the gate of M_8 is raised instantly, the falling time of V_{ap} is reduced significantly. Thus, the start operation of APC is accelerated with a small silicon area when the load step-current changes. Similarly, as seen in Fig. 7(b), the rising time of V_{an} decreases dramatically when a step-down load occurs.

B. Schematic Diagram of Operation Mode Control

The schematic diagram of the operation mode control is shown in Fig. 8. To obtain the load current information, the inductor current and the current flowing through the output capacitor are required. A differentiator is used to differentiate the output voltage and achieve signal V_{iC}, containing the information of the output capacitor current. When the sensed signal

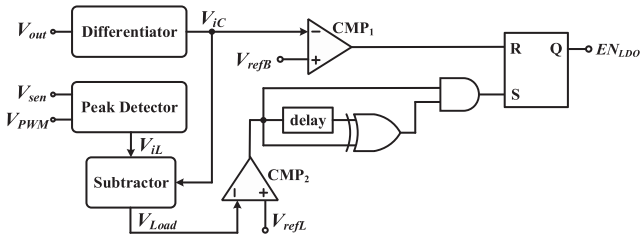

Fig. 8. Schematic diagram of the operation mode control.

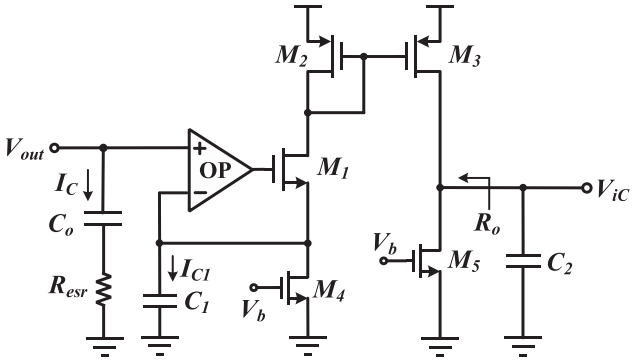

Fig. 9. Schematic diagram of the differentiator.

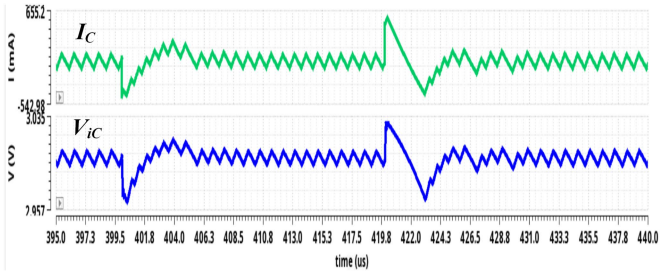

Fig. 10. Simulated waveforms of the differentiator when the load current changes instantaneously.

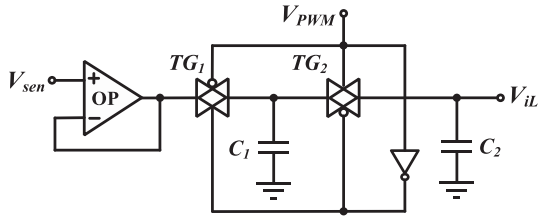

Fig. 11. Schematic diagram of the peak detector.

$V_{\rm sen}$ and PWM signal $V_{\rm PWM}$ are sent to the peak detector, a signal V_{iL}, including the peak value of the inductor current, is generated. By subtracting V_{iC} from V_{iL}, the signal $V_{\rm Load}$ of the load current information is produced.

When $V_{\rm Load}$ is smaller than the reference signal $V_{{\rm ref}L}$, the output of the comparator CMP$_2$ becomes the high state, implying that the load current changes to light load. Through the digital circuits, a pulse is then transmitted to the S terminal of the SR Latch. Signal EN$_{\rm LDO}$ is subsequently set to the high state. Consequently, the operation mode of the proposed converter changes from the switching mode to the linear mode. On the other hand, when the reference signal $V_{{\rm ref}B}$ is larger than V_{iC}, EN$_{\rm LDO}$ become the low state, meaning that the load current is greater than the designed light-load level, and the operation mode of the proposed converter changes to the switching mode. When a step-up load occurs, the response time of V_{iC} is faster than that of V_{iL}; thus, V_{iC} rather than $V_{\rm Load}$ is adopted. $V_{{\rm ref}L}$ and $V_{{\rm ref}B}$ are set as 0.5 and 1.35 V, respectively.

The schematic diagram of the differentiator is shown in Fig. 9. Since the amplifier OP and the transistor M_1 form a negative feedback loop, the voltage across the capacitor C_1 is $V_{\rm out}$. Thus, the current I_{C1} is equal to $C_1(dV_{\rm out}/dt)$, which scales down with the current flowing through the output capacitor. The dc current I_{d4} is determined by the transistor M_4 and the bias voltage V_b. The values of C_1 and C_2 are 1 pF and 100 fF, respectively. After through a current mirror comprising transistors M_2 and M_3, I_{C1} and I_{d4} are amplified. The capacitor C_2 is employed as a high-frequency filter, and the signal V_{iC} is produced, which can be expressed as

$$V_{i\rm C} = C_1 R_{\rm o} \frac{(W/L)_{M3}}{(W/L)_{M2}} \frac{dV_{\rm out}}{dt} \tag{8}$$

where R_o is the equivalent resistance at the output node of the differentiator.

Fig. 10 shows the waveforms of V_{iC} and the output capacitor current I_C when the load current immediately changes from the light to the heavy load and then back to light load. It is clear that the waveforms of V_{iC} and I_C are similar even during the load transient periods. Thus, the differentiator could obtain the current information of the output capacitor.

The schematic diagram of the peak detector is shown in Fig. 11. The sensed signal $V_{\rm sen}$ passes a unit-gain buffer to prevent the loading effect and is sent to two sample-and-hold circuits. The two sample-and-hold circuits are controlled by $V_{\rm PWM}$. When $V_{\rm PWM}$ is at the low state, the transmission gates TG$_1$ and TG2 are turned ON and OFF, respectively. The signal across the capacitor C_1 then tracked $V_{\rm sen}$, and V_{iL} is maintained at the previous value. When $V_{\rm PWM}$ changes to the high state, TG$_1$ and TG$_2$ are turned OFF and ON, respectively. Subsequently, the peak value of $V_{\rm sen}$ is kept on V_{iL}.

V. Experimental Results

To verify the circuit validity, a laboratory prototype of the proposed converter was built with a nominal input voltage of 3.3 V and maximum output current of 500 mA. The output capacitor and output inductor were 4.7 and 4.7 μH, respectively. The proposed converter was fabricated with standard 0.35-μm CMOS technology. The chip microphotograph is shown in Fig. 12 and chip area, including the pads, is 1491 $\times$ 1800 μm^2. In Fig. 12, the chip area of the APC, driving circuit, transient enhancement circuit, and operation mode control are represented in the areas with black dash lines. In addition, the chip size of the APC, auxiliary transient transistors, driving circuit, and transient enhancement circuit is about 0.119 mm^2. Compared to the total chip area with PADs, which is 2.047 mm^2, it occupies only 5.8%. Fig. 13 shows the measured waveforms of the proposed

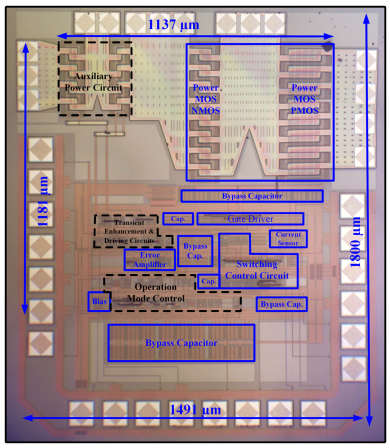

Fig. 12. Chip microphotograph of the proposed converter.

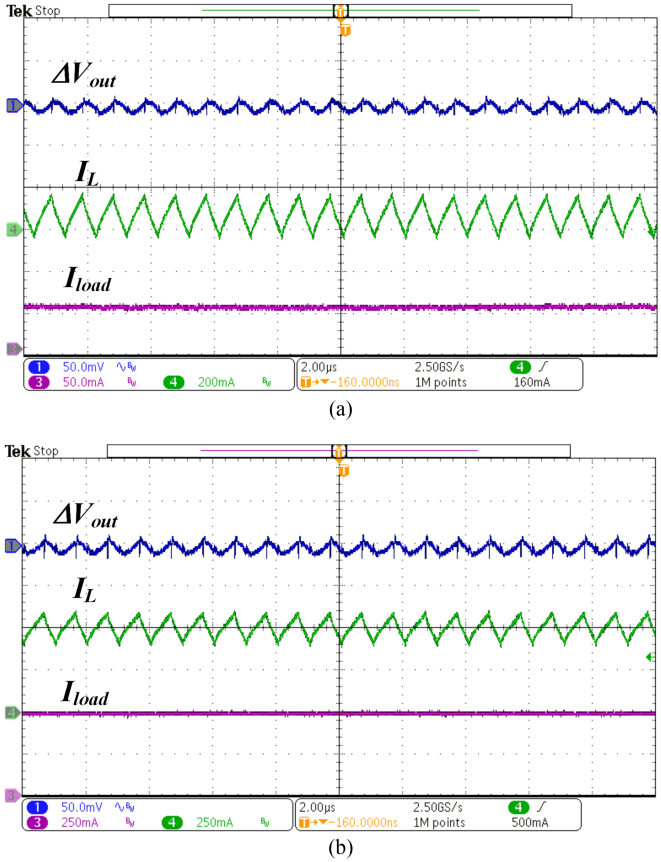

Fig. 13. Measured waveforms of the proposed converter in the switching mode at the load currents of (a) 50 mA and (b) 500 mA.

converter operating in the switching mode at the load currents of 50 mA and 500 mA when the output voltage is set as 1.8 V. The output voltage ripple ΔV_{out} is about 20 mV.

Fig. 14 shows the transient responses of the proposed converter when both the transient and linear modes are disabled for the load current change between 500 and 50 mA. The output voltage ripple ΔV_{out}, inductor current I_L, and load current I_{load} are shown in Fig. 14. The recovery time and the transient

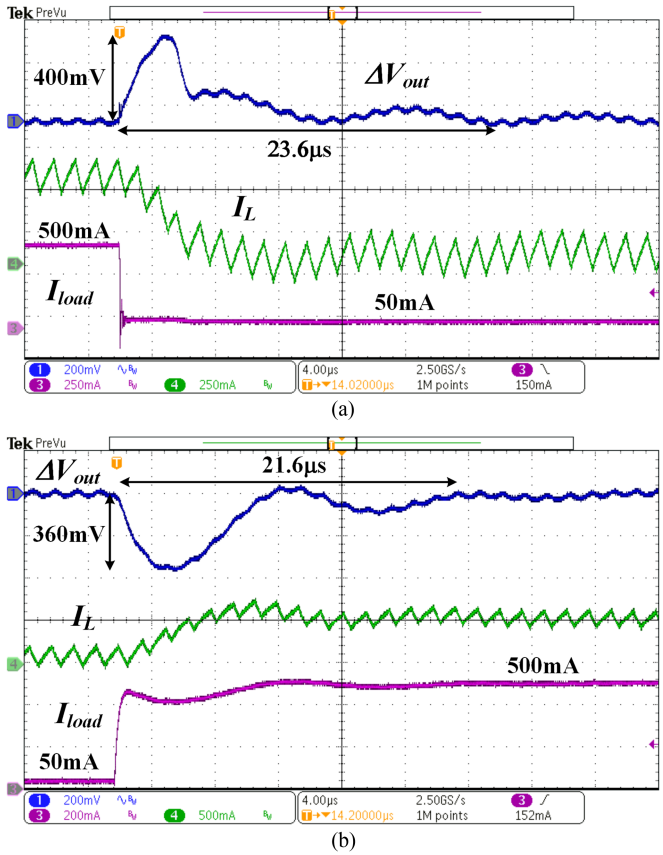

Fig. 14. Transient responses of the proposed converter when both the transient and linear modes are disabled for (a) step-down load and (b) step-up load.

ripple for the step-down and step-up loads are 23.6 μs, 400 mV, 21.6 μs, and 360 mV, respectively.

Fig. 15 shows the transient responses of the proposed converter when the transient mode is enabled and the linear mode is disabled. For conventional peak current-mode control, the duty cycle is changed slowly due to the slope compensation mechanism. However, for I_L shown in Fig. 15(b), the implication is that the duty cycle with the proposed method is saturated to 100%. The recovery times for the step-down and step-up loads are 1.6 and 2.0 μs, and the transient ripples for the step-down and step-up loads are 80 and 70 mV, respectively. Comparing to when the transient mode is disabled, the recovery time of the output voltage is improved by over ten times when the transient mode is enabled. It should be noted although V_{out} resumes its regulated value after the load current changes, I_L is slowly adjusted to its final level. This implies that the additional charging and discharging currents provided by APC are changed gradually to prevent any variation in V_{out}.

Fig. 16 shows the transient waveforms of the proposed converter when the operation changes from the switching mode to the linear mode and then back to the switching mode. Since the transient mode is enabled, the transient duration of both the changing modes is less than 2.6 μs. In the linear mode, the power transistors M_{MN} and M_{MP} are turned off for power saving; thus, the inductor current ripple becomes zero. Moreover, the output voltage is also maintained at almost an identical level to provide

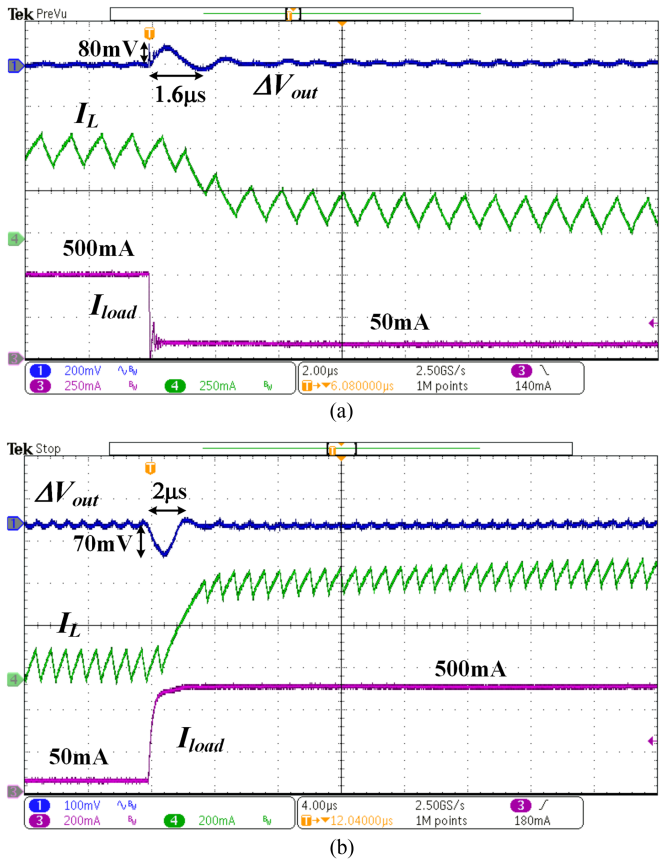

Fig. 15. Transient responses of the proposed converter when the transient mode is enabled and linear mode is disabled for (a) step-down load and (b) step-up load.

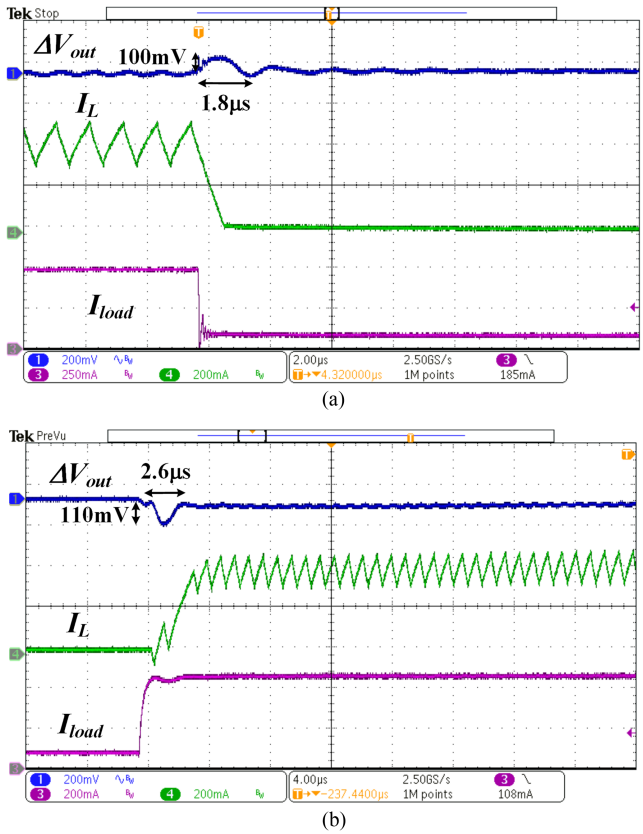

Fig. 16. Transient waveforms of the proposed converter when the operation changes (a) from switching mode to linear mode and (b) from linear mode to switching mode.

energy for the load. In Fig. 16(b), since M_{MN} is temporarily turned on at the beginning of the operation mode change, I_L becomes negative, but the converter still operates.

Fig. 17 shows the measured efficiency of the proposed converter for the output voltages of 1.8 and 2.5 V. When the converter operates with the switching mode at light loads, the conversion efficiency degrades significantly. Thus, with the different operation modes based on different load conditions, the power efficiency can be maintained within a relatively high value, especially at higher output voltages. Comparing to with switching and proposed modes, the efficiency improvements at load current of 20 mA under the output voltages of 2.5 and 1.8 V are 13.8% and 4.9%, respectively. When the input and output voltages were 3.3 and 2.5 V, the maximum and minimum efficiencies measured are 95.02% and 74.99%, respectively. When the output voltage changes to 1.8 V, the maximum efficiency is 89.76% at the load current of 400 mA.

Table I gives the measured performance of the state-of-the-art switching buck converters. The recovery time is defined as the time required for the output voltage to reach and steady within a given tolerance band. The tolerance band used in Table I is about 0.8%. Two figure of merits (FOMs) are utilized in Table I. FOM_1 is employed from [6] to compare the dynamic performance. Since inductor, output capacitor, and switching frequency are important for the transient response of a buck

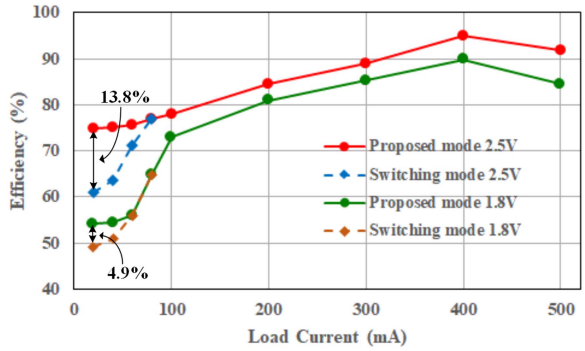

Fig. 17. Power conversion efficiency of the proposed converter.

converter, FOM_1 includes those parameters. Moreover, the slew rate of load current change also affects the recovery time and output voltage overshoot/undershoot. FOM_2 contains the parameters of the load current slew rate and voltage overshoot/undershoot. However, the information of load current slew rate for some works is not applicable because the waveform of load current change for those works cannot be found. Large FOM_1 and FOM_2 stand for fast transient response. From FOM_1 and FOM_2, the proposed buck converter has a better transient response than the other buck converters excluding [7]. In addition, the proposed converter has maximal peak efficiency when the output voltage is 2.5 V.

TABLE I
COMPARISON OF REPORTED CMOS DC–DC CONVERTERS

	Ting et al. [2]	Chen et al. [3]	Jung et al. [5]	Hsu et al. [7]	Hwang et al. [9]	Shih et al. [10]	This article
Technology (μm)	0.18	0.35	0.25	0.35	0.35	0.25	0.35
Input voltage (V)	3.3	3.3–3.6	3.3	5	2.8–4	2.7–4.2	2.8–3.6
Output voltage (V)	1–2.6	0.9–2.5	1.5–1.8	3.3	1.4–2.5	1.8	1.8–2.5
Switch frequency (MHz)	2.5	1	2	1	1	1	1
Inductor (μH)	0.33	4.7	2.2	4.7	2.2	4.7	4.7
Output Capacitor (μF)	3.3	10	4.7	8	10	4.7	4.7
Peak efficiency (%)	90.1	90	92	94	88.3	94	95.02, 89.76
Light-load efficiency (%)	70% @ 100mA	77–79% @ 100mA	73% @ 25mA	78% @ 50mA	79.4% @ 100mA	54.5%@ 20mA	54.2–75% @ 20mA
Transient load step (mA)	600	400	510	400	550	300	450
Step-down and step-up recovery times (μs)	0.6, 0.5	4.2, 2.1	1.3, 2.3	2, 2	3.5, 3.5	12, 15	1.6, 2.0
Overshoot, Undershoot (mV)	70, 70	60, 30	20, 38	30, 30	40, 45	25, 35	80, 70
Chip area with PADs (mm^2)	1.81	2.25	0.913	2.00	2.25	1.65	2.047
Step-down and step-up slew rates of load current change (A/μs)	1, 1	N/A	N/A	4.5, 0.9	0.38, 0.38	N/A	4.5, 0.85
FOM_1 (step-down and step-up)	4, 4.8	4.48, 7.23	9.18, 5.19	11.75, 11.75	3.46, 3.46	2.5, 2	28.13, 22.5
FOM_2 (step-down and step-up)	0.57, 0.69	N/A	N/A	17.63, 3.53	0.33, 0.29	N/A	15.8, 2.73

$$\mathrm{FOM}_1=\frac{Inductor\times Transient\ load\ step\times 10^2}{Output\ capacitor\times Switch\ frequency\times \mathrm{Recovery}\ time}$$

$$\mathrm{FOM}_2=\frac{Inductor\times Transient\ load\ step\times Load\ current\ slew\ rate\times 10^{-6}}{Output\ capacitor\times Switch\ frequency\times \mathrm{Recovery}\ time\times\left(Overshoot/Undershoot\right)}$$

VI. CONCLUSION

In this article, a configurable power architecture, comprising a buck converter combined with an APC, is presented to handle distinct load conditions for simultaneously enhancing the transient response and power efficiency. The configurable supply mechanism is organized based on the variable load conditions. Under heavy- to medium-load situations, the switching dc–dc converter operation is activated to deliver adequate energy with high power efficiency. During the load transient period, the APC instantly delivers an additional charging/discharging current for the output capacitance, leading to a small output transient ripple. Meanwhile, two auxiliary transient transistors are employed to quickly regulate the output level of the error amplifier because peak current-mode control is adopted in the switching converter. Therefore, fast transient response and acceptable conversion efficiency are achieved over a wide load range. The proposed converter was fabricated with 0.35-μm CMOS technology. The experimental results demonstrate that the recovery times for 450-mA step-down and step-up loads are 0.8 and 1.2 μs, respectively, and that the transient ripples for the step-down and step-up loads are 90 and 80 mV, respectively. Comparing to when the transient mode is disabled, the recovery time of the output voltage is improved by over ten times when the transient mode is enabled. Further, the efficiency improvements with the proposed method at load current of 20 mA under the output voltages of 2.5 and 1.8 V are 13.8% and 4.9%, respectively.

ACKNOWLEDGMENT

The authors wish to thank Taiwan Semiconductor Research Institute, Taiwan, for chip fabrication.

REFERENCES

[1] P.-J. Liu, W.-S. Ye, J.-N. Tai, H.-S. Chen, J.-H. Chen, and Y.-J. E. Chen, "A high-efficiency CMOS dc-dc converter with 9-μs transient recovery time," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 3, pp. 575–583, Mar. 2012.

[2] C.-Y. Ting, J.-Y. Lin, and C.-P. Chen, "A Quasi-V^2 hysteretic buck converter with adaptive COT control for fast DVS and load-transient response in RF applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol. 67, no. 3, pp. 531–535, Mar. 2020.

[3] J.-J. Chen, Y.-S. Hwang, Y. Ku, Y.-H. Li, and J.-A. Chen, "A current-mode-hysteretic buck converter with constant-frequency- controlled and new active-current-sensing techniques," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 3126–3134, Mar. 2021.

[4] W.-H. Yang et al., "A constant-on-time control DC–DC buck converter with the pseudowave tracking technique for regulation accuracy and load transient enhancement," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6187–6198, Jul. 2018.

[5] D.-H. Jung, K. Kim, S. Joo, and S.-O. Jung, "0.293-mm^2 fast transient response hysteretic Quasi-V^2 DC–DC converter with area-efficient time-domain-based controller in 0.35-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1844–1855, Jun. 2018.

[6] K.-Y. Cheng, F. C. Lee, and P. Mattavelli, "Adaptive ripple-based constant on-time control with internal ramp compensations for buck converters," in *Proc. IEEE Power Electron. Conf. Expo.*, 2014, pp. 440–446.

[7] Y.-C. Hsu, C.-Y. Ting, L.-S. Hsu, J.-Y. Lin, and C. C.-P. Chen, "A transient enhancement DC–DC buck converter with dual operating modes control technique," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol. 66, no. 8, pp. 1376–1380, Aug. 2019.

[8] P.-J. Liu, C.-Y. Liao, and M.-H. Kuo, "A spur-reduction dc-dc converter with active ripple cancellation technique," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 2206–2214, Dec. 2018.

[9] Y.-S. Hwang, J.-J. Chen, Y.-T. Ku, and J.-Y. Yang, "An improved optimum-damping current-mode buck converter with fast-transient response and small-transient voltage using new current sensing circuits," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9505–2203, Oct. 2021.

[10] C.-J. Shih, K.-Y. Chu, Y.-H. Lee, W.-C. Chen, H.-Y. Luo, and K.-H. Chen, "A power cloud system (PCS) for high efficiency and enhanced transient response in soC," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1783–1794, Mar. 2013.

[11] P.-J. Liu, H.-J. Chiu, Y.-K. Lo, and Y.-J. Chen, "A fast transient recovery module for dc–dc converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2522–2529, Jul. 2009.
[12] V. Svikovic, J. A. Oliver, P. Alou, O. Garcia, and J. Cobos, "Synchronous buck converter with output impedance correction circuit," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3415–3427, Jul. 2013.
[13] P.-J. Liu, Y.-K. Lo, H.-J. Chiu, and Y.-J. E. Chen, "Dual-current pump module for transient improvement of step-down dc-dc converters," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 985–990, Apr. 2009.
[14] S. J. Kim, W. Choi, R. Pilawa-Podgurski, and P. K. Hanumolu, "A 10-MHz 2–800-mA 0.5–1.5-V 90% peak efficiency time-based buck converter with seamless transition between PWM/PFM modes," *IEEE J. Solid-State Circuits*, vol. 53, no. 3, pp. 814–824, Mar. 2018.
[15] J.-S. Kim, J.-O. Yoon, and B.-D. Choi, "A high-light-load-efficiency low-ripple-voltage PFM buck converter for IoT applications," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5763–5772, May 2022.
[16] K. H. Chen, C. C. Chien, C.-H. Hsu, and L.-R. Huang, "Optimum power-saving method for power MOSFET width of dc-dc converters," *IET Circuits Devices Syst.,* vol. 1, pp. 57–62, Feb. 2007.
[17] M. Mull igan, B. Broach, and T. Lee, "A constant-frequency method for improving light-load efficiency in synchronous buck converters," *IEEE Power Electron. Lett.*, vol. 3, no. 1, pp. 24–29, Mar. 2005.
[18] G. Bonanno and L. Corradini, "Digital predictive current-mode control of three-level flying capacitor buck converters," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4697–4710, Apr. 2021.
[19] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, Norwell, MA, USA: Kluwer, 2001.
[20] P.-J. Liu, T.-H. Chen, and S.-R. Hsu, "Area-efficient error amplifier with current-boosting module for fast-transient buck converters," *IET Power Electron.*, vol. 9, pp. 2147–2153, Oct. 2016.

Pang-Jung Liu (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical and electronics engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 1998 and 2000, and the Ph.D. degree from the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan, in 2010.

From 2000 to 2003, he was the Engineer with TSMC. From 2003 to 2005, he was working on digital IC design with ELAN Microelectronics Corporation. From August 2010 to January 2012, he was with the Department of Electrical Engineering, National Ilan University, Yilan, Taiwan. Since 2012, he has been with the Department of Electrical Engineering, National Taipei University of Technology, Taipei, Taiwan, where he is currently a Professor. His research interests include power management IC, switching-mode power converters, LED drivers, and mixed-mode IC design.

Wei-Yi Cheng was born in Taipei, Taiwan, in 1993. He received the B.S. degree in electronic engineering from Chung Yuan Christian University, Taoyuan, Taiwan, in 2015 and the M.S. degree in electronic and computer engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 2017. He is currently with Etron Technology, Inc., Hsinchu, Taiwan. His research interests include integrated power management system designs and analog integrated circuits.

Lin-Hao Chien was born in Kaohsiung, Taiwan, in 1991. She received the B.S. degree in electronic engineering from National Kaohsiung First University of Science and Technology, Kaohsiung, Taiwan, in 2014 and the M.S. degree in electrical engineering from National Taipei University of Technology, Taipei, Taiwan, in 2016.

Her areas of interests include integrated power management system designs and analog integrated circuits.

Jing-Yuan Lin (Member, IEEE) was born in Kao-Hsiung, Taiwan. He received the M.S. and Ph.D. degrees in electronic engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 2002 and 2007, respectively.

In 2013, he was with the Faculty of the Department of Electrical Engineering, National Taitung Junior College, Taitung, Taiwan. Since 2014, he has been with the Faculty of the Department of Electronic, National Taiwan University of Science and Technology, Taipei, where he is currently an Associate Professor. His research interests include the design and analysis of zero-voltage-switching dc/dc converter, power factor correction techniques, converter modeling, and power IC design.