A Compact High-Efficiency Boost Converter With Time-Based Control, RHP Zero-Elimination, and Tracking Error Compensation

Mauro Leoncini, Alessandro Dago, Alessandro Bertolini, Alessandro Gasparini, Salvatore Levantino, *Senior Member, IEEE*, and Massimo Ghioni, *Senior Member, IEEE*

***Abstract*—Time-based signal processing has been recently demonstrated to be more area- and power-efficient compared with traditional analog based, making it an interesting approach for the design of compact high-efficiency dc–dc converters for portable applications. This work presents a novel boost converter, with a time-based control, a scheme for right-half plane (RHP) zero mitigation requiring no extra power switch nor external capacitor, and a pulse frequency modulation (PFM) operating mode with steady-state error correction and seamless PFM-to-continuous conduction mode (CCM) transition. The prototype implemented in a 0.18-μm bipolar-CMOS-DMOS (BCD) process generates an output voltage of 5 V from an input voltage ranging between 2.5 and 4.5 V, and has an 800-mA load current capability. The controller area occupation is 0.27 mm ^{2} and the quiescent current in CCM is 300 μ A for the controller and 40 μA for the tracking error compensation. The peak efficiency is 96% at 4.5-V input and above 90% at light loads down to 50 mA current. Compared with a peak-current mode control, both the controller area and the current consumption of the proposed time-based architecture are lower by about 40%. The achieved closed-loop bandwidth of 130 kHz is six times larger than in a conventional boost converter with RHP zero.**

***Index Terms*—DC–DC power converters, nonminimum phase, right-half plane (RHP) zero, time-based control.**

I. Introduction

POWER efficiency and silicon area occupation are key features of nowadays integrated power converters for wearable and handheld electronic devices. Switching power converters are capable of reaching large peak efficiencies while providing power regulation. Interleaved multiphase converters [1], [2], [3], [4] have been proposed to increase power efficiency over conventional converters, reduce the output voltage ripple, or alternatively achieve large conversion ratios. However, despite their advantages, the increased area occupation makes them unsuitable for portable applications. The two-output switched-capacitor converter in [5] improves power density, but its efficiency is strongly dependent on the input-to-output voltage ratio, dropping below 70% in the worst case. Other approaches, such as the hybrid converter with two flying capacitors in [6], aiming to increase power density, are limited to buck-type converters with large input–output ratios. Time-based control has been demonstrated to be a promising alternative to standard voltage mode [7], [8], [9]. The block diagrams in Fig. 1 compare a standard analog controller and a time-based controller applied to a boost converter. The main advantage of a time-based controller is that it encodes the information in the time difference between events. Thus, the compensation network, i.e., the proportional–integral–derivative (PID) filter, processes binary signals, allowing the time-based controller

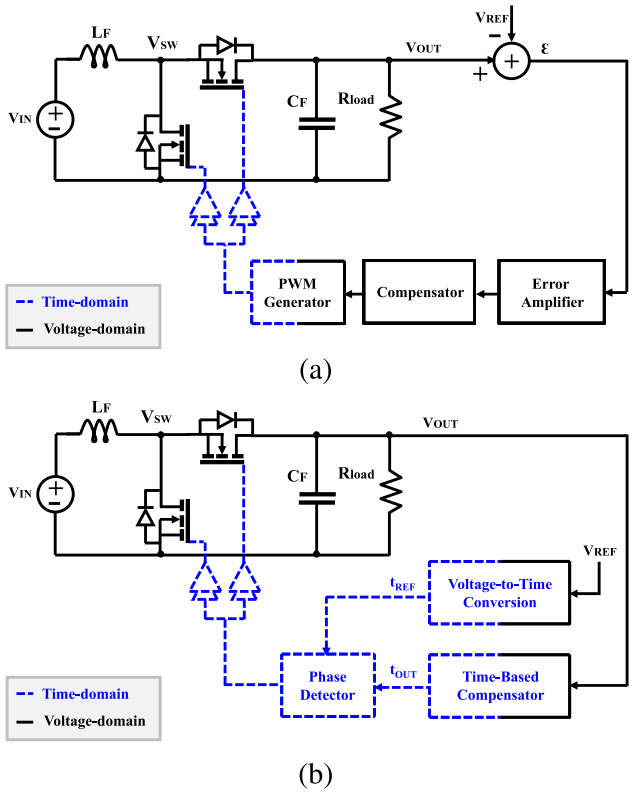

Fig. 1. Boost converter with (a) analog versus (b) time-based control.

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to benefit from technology scaling in terms of area and power consumption. Unlike a digital controller, it introduces no quantization, preventing the generation of limit cycles.

The adoption of time-based control in power converters has been, however, so far limited to buck converters. In boost-type converters operating in continuous conduction mode (CCM), the loop bandwidth is limited by the typical RHP zero, which spoils most of the above described advantages of time-based control. Several approaches to eliminate the RHP zero and improve transient response of boost converters have been explored in the literature. Control strategies, such as ripple-based control [10], result in a variable switching frequency operation in steady state, which might be a serious drawback. The authors in [11] act on the duty cycle to improve the load transient during a load variation. Since the converter bandwidth is unchanged, this technique only improves the load regulation but it has no impact on the line transient response. A different approach is to compensate for the RHP-zero effect acting on the loop compensator [12], [13]. These techniques, however, require sophisticated algorithms based on the integration of analog to digital converters (ADCs) with high sampling rate, which are responsible for a large increase of the controller area and quiescent current. Another solution is to provide a forward energy transfer to the inductor, during the "ON" time interval of the power switch, using magnetically coupled inductors [14], [15], [16]. This comes at the cost of a larger number of magnetic components, leading to a reduced power density. The technique proposed in [17] aims instead at eliminating the RHP zero by injecting a scaled version of the inductor current. Its implementation requires no extra power switches or external flying capacitor, but only few extra building blocks, such as an inductor current sensor, a transimpedance amplifier, and a voltage summation, which have irrelevant impact in power and area consumption. On the downside, the injection of a scaled inductor current into the output node generates a shift in the dc steady-state output voltage (i.e., a tracking error) that is unacceptable in practical applications.

In this article, we introduce a novel boost converter with a time-based control [18], a technique to mitigate the RHP zero based on [17], and a novel strategy to correct the tracking error. A pulse frequency modulation (PFM) operating mode with seamless PFM-to-CCM transition is also adopted to increase efficiency at light loads and an adaptive reference voltage of the PFM comparator is realized to improve dc regulation in PFM.

The rest of this article is organized as follows. Section II introduces the architecture of the boost converter with time-based controller. Section III is devoted to the RHP-zero elimination technique and to the tracking-error correction. Section IV is focused on system design. Section V provides circuit design details, whereas Section VI illustrates measurement results which validate the presented architecture. Finally, Section VII concludes this article.

II. Boost Converter With Time-Based Control

In a standard analog control loop, the signal is converted from the voltage to the time domain thanks to the pulsewidth modulation (PWM) generator, which compares the output of the error amplifier with a saw-tooth voltage reference to generate a variable duty-cycle square-wave signal. However, this voltage-to-time conversion introduces a delay in the loop that reduces the phase margin and limits the minimum achievable duty cycle.

The idea of time-based control is to implement the voltage-to-time conversion already at the input of the compensator and then realize the compensator directly in the time domain [7], as shown in Fig. 1. The voltage-to-time conversion is performed by means of two elementary components, namely the voltage-controlled delay line (VCDL) and the voltage-controlled oscillator (VCO). The VCDL, being an element whose output is the input signal delayed by a phase proportional to the control voltage, implements the proportional path of the compensator. In formulas, the transfer function from its control voltage, $\widetilde{v}_{\rm ctrl}$, and its output phase, $\widetilde{\Phi}_{\rm out}$, is

$$\frac{\widetilde{\Phi}_{\rm out}}{\widetilde{v}_{\rm ctrl}} = K_{{\rm VCDL}_P} \tag{1}$$

where $K_{{\rm VCDL}_P}$ is the conversion gain of the VCDL of the proportional path.

The integral path of the compensator is instead implemented by means of a VCO. The latter generates a periodic signal whose frequency is proportional to the control voltage applied to it. Given the integral relationship between frequency and phase, the VCO acts as an ideal integrator and its transfer function from its control voltage $\widetilde{v}_{\rm ctrl}$ and its output phase $\widetilde{\Phi}_{\rm out}$ can be written as

$$\frac{\widetilde{\Phi}_{\rm out}}{\widetilde{v}_{\rm ctrl}}(s) = \frac{K_{\rm VCO}}{s}, \tag{2}$$

where $K_{\rm VCO}$ is the VCO gain.

The compensation network of a dc–dc converter is usually designed with a PID compensator. To this aim, it is necessary to generate also a derivative gain. Although there is no such a component that can perform the derivative directly in time domain, a solution is to place the derivative gain in voltage domain before converting it into time domain [7]. This is obtained placing a first-order high-pass filter (with capacitor C_D and resistor R_D) in series before feeding it into the VCDL. So, the transfer function from the control voltage of the derivative path $\widetilde{v}_{\rm ctrl}$ and its output phase $\widetilde{\Phi}_{\rm out}$ becomes

$$\frac{\widetilde{\Phi}_{\rm out}}{\widetilde{v}_{\rm ctrl}}(s) = \frac{sR_DC_D}{1+sR_DC_D} K_{{\rm VCDL}_D}. \tag{3}$$

where $K_{{\rm VCDL}_D}$ is the conversion gain of the VCDL of the derivative path.

The boost converter with time-based control is shown in Fig. 2, where $1/n$ is the output voltage attenuation, and the *PD* block is a phase detector used to compare the rising edge of the controller output Φ_F with a reference one Φ_R in order to generate the PWM signal. As evident from the block diagram, the time-based control strategy eliminates the use of the PWM modulator and its limitations in terms of delay and minimum "ON" time, because the PWM generation is implicit in the time-based processing. In other words, the output of the compensator

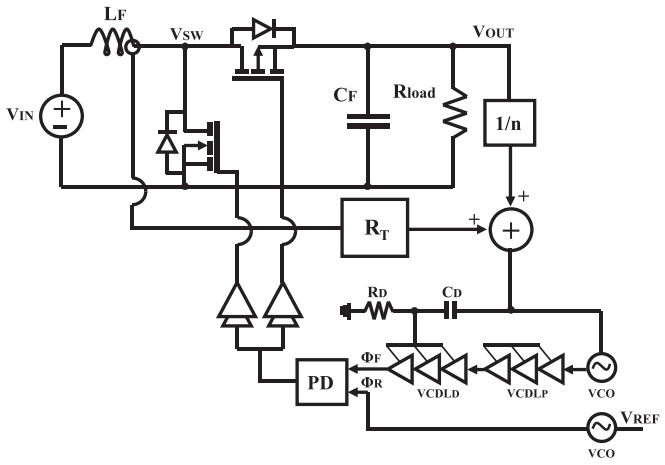


Fig. 2. Boost converter with time-based PID compensator and inductor current-based RHP-zero elimination.

itself is a PWM signal that can be used to drive the power stage. The nature of the R_T transimpedance block will be discussed in the following section.

III. RHP Zero and Tracking Error

As any boost converter operating in CCM, the control-to-output transfer function of the time-based converter in Fig. 2 contains an RHP zero whose angular frequency depends on the converter operating condition and can be expressed as

$$\omega_{z,\mathrm{rhp}} = \frac{R_{\mathrm{load}} \cdot D'^2}{L_F} \tag{4}$$

with $R_{\mathrm{load}} = V_{\mathrm{out}}/I_{\mathrm{load}}$ being the load resistance, $D' = 1 - D = V_{\mathrm{in}}/V_{\mathrm{out}}$ and L_F the inductance of the second-order filter. Therefore, to get sufficient phase margin, the bandwidth of the converter has to fulfil the following inequalities [19], [20]:

$$\omega_{bw,\max} < \frac{\omega_{z,\mathrm{rhp,min}}}{5} \tag{5a}$$

$$\omega_{bw,\max} < \frac{\omega_{sw}}{5} \tag{5b}$$

where $\omega_{bw,\max}$ is the maximum converter bandwidth, $\omega_{z,\mathrm{rhp,min}}$ is the minimum angular frequency of the zero, and ω_{sw} is the angular frequency of the PWM signal.

In applications, such as LED display power supply, where the required current capability is high, the first inequality, (5a), is the limiting one, because the large load current decreases the zero frequency and, consequently, the converter bandwidth. Unfortunately, a narrow converter bandwidth negatively affects the dynamic response to both line and load perturbations, and significantly spoils the area and efficiency advantages of the time-based control. For this reason, time-based control has been so far applied only to buck-type dc–dc converters.

To overcome the RHP-zero limitation and widen the loop bandwidth of the boost converter, the left-half-plane (LHP) zero present in the duty cycle to inductor current transfer function $\widetilde{i}_L/\widetilde{d}$ can be exploited [17]. The $\widetilde{i}_L/\widetilde{d}$ transfer function is given by

$$\frac{\widetilde{i}_L}{\widetilde{d}}(s) = \frac{2V_{\mathrm{in}}}{R_{\mathrm{load}}D'^3} \frac{1 + sR_{\mathrm{load}}C_F}{1 + s\frac{L_F}{D'^2R_{\mathrm{load}}} + s^2\frac{L_FC_F}{D'^2}} \tag{6}$$

where C_F is the output filter capacitance. The duty cycle to output transfer function $\widetilde{v}_{\mathrm{out}}/\widetilde{d}$ is given by

$$\frac{\widetilde{v}_{\mathrm{out}}}{\widetilde{d}}(s) = \frac{V_{in}}{D'^2} \frac{1 - s\frac{L_F}{R_{\mathrm{load}}D'^2}}{1 + s\frac{L_F}{D'^2R_{\mathrm{load}}} + s^2\frac{L_FC_F}{D'^2}}. \tag{7}$$

Since the two transfer functions (6) and (7) share the same denominator, they can be linearly combined, as shown in Fig. 2, to provide an error signal $\widetilde{v}_\epsilon$ at the input of the time-based network given by

$$\widetilde{v}_\epsilon(s) = \widetilde{d}(s)\frac{V_{\mathrm{in}}}{nD'^2} \frac{1 + \frac{2nR_T}{R_{\mathrm{load}}D'} + s\left(\frac{nR_TC_F}{D'} - \frac{L_F}{R_{\mathrm{load}}D'^2}\right)}{1 + s\frac{L_F}{D'^2R_{\mathrm{load}}} + s^2\frac{L_FC_F}{D'^2}} \tag{8}$$

where R_T is the transimpedance gain of the inductor current sensor. Considering the condition $1 + \frac{2nR_T}{R_{\mathrm{load}}D'} \simeq 1$, (8) has a single zero whose magnitude is

$$\omega_{z,\mathrm{rhp}} = \frac{D'}{\frac{L_F}{R_{\mathrm{load}}D'} - nR_TC_F} \tag{9}$$

The designer can select the transimpedance gain R_T to influence the position of the zero in (9). The value of R_T has an impact not only on the magnitude of the zero but also on its sign. With a sufficiently large R_T value, the sign of (9) becomes negative, which means that the zero is shifted to the left-hand side of the complex plane (LHP zero) and can be used for compensation. The latter strategy not only removes the limitation in (5a) but also reduces the complexity of the compensation network from a PID to a simpler proportional–integral (PI) type. The denominator in (9) is set by two factors: $L_F/(R_{\mathrm{load}}D')$ is the standard RHP contribution of the control to output transfer function, the factor nR_TC_F is generated by the RHP-zero elimination technique. Only the first component is affected by the circuit operating condition, and the second is a fixed term. To generate a stable LHP zero that can be used for compensation, it is sufficient to guarantee that the denominator in (9) is dominated by nR_TC_F in all operating conditions. At the same time, the value of the zero $\omega_{z,\mathrm{rhp}}$ needs to match the desired zero required for the compensation, i.e., $\omega_{z,\mathrm{rhp}} = \omega_{z,\mathrm{target}}$. Selecting the worst-case scenario

$$nR_TC_F \gg \frac{L_F}{R_{\mathrm{load,min}}D'_{\mathrm{min}}}. \tag{10}$$

Even if (10) is verified, the zero in (9) has a residual dependence with the converter operating condition set by its numerator. Such a behavior, however, is the same as the complex pole pair of the output filter $\omega_0 = D'/\sqrt{L_FC_F}$. As demonstrated in [21], this is a favorable effect since it makes the zero tracks the complex pole pair reducing the variation of the crossover frequency over the operating range.

Unfortunately, a major drawback arises from the application of the abovementioned technique. Since the controller compares the reference voltage with the sum of the output voltage and a

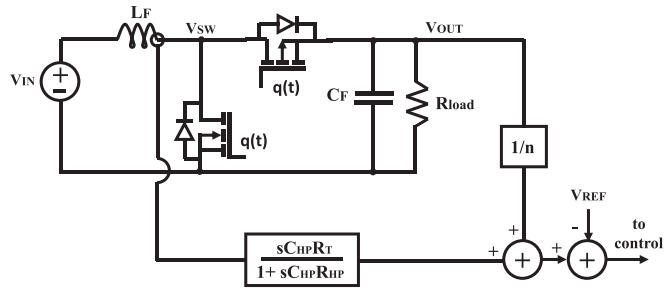


Fig. 3. Power stage architecture of a boost converter with inductor current-based RHP-zero elimination and tracking error correction.

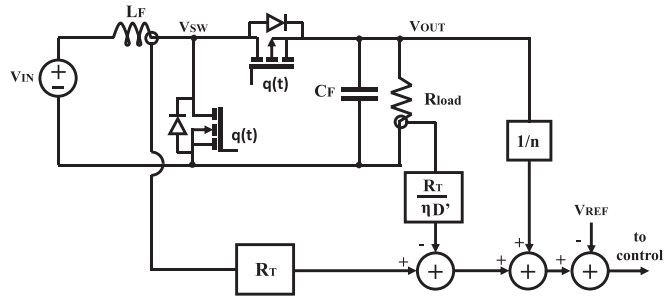


Fig. 4. Power stage architecture of a boost converter with inductor current-based RHP-zero elimination and load current-based tracking error correction.

voltage proportional to the inductor current, a tracking voltage error appears at the output. Referring to the circuit in Fig. 2, at steady state the output voltage can be written as

$$V_{\text{out}} = nV_{\text{REF}} - nR_T I_{L_F} \tag{11}$$

where I_{L_F} is the average inductance current, and $nR_T I_{L_F}$ is the tracking voltage error. Being the maximum inductor current set by the application, the only design parameter left to reduce the error would be the transimpedance gain R_T. The latter, however, is set to eliminate the RHP zero [see (9)] and cannot be reduced.

A possible solution to the tracking error is to high-pass filter (with capacitor C_{HP} and resistor R_{HP}) the inductor current before injecting it into the loop [17], as shown in Fig. 3. The high-pass filter frequency, however, has to be set well below the RHP-zero frequency, in order not to affect system stability [21]. So, although the static error is removed, the transient performance of the converter is adversely affected. When a load step variation occurs, the controller first quickly sets the output voltage to the new steady-state with the tracking error in (11), then a slow recovery tail occurs dictated by the relatively low corner frequency of the high-pass filter.

To improve the transient response while still correcting the tracking error, we devised the technique shown in the block diagram in Fig. 4, where the load current is sensed and used to and correct the error. In a standard boost converter, the relationship between load and inductance current is

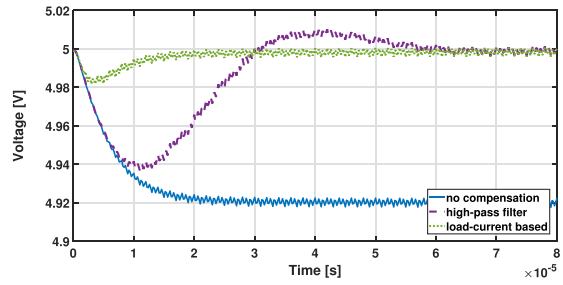
$$I_{L_F} = \frac{I_{\text{load}}}{\eta D'} \tag{12}$$

where η is the converter efficiency. Therefore, sensing I_{load} and knowing η and D', it is possible to get an estimation of the dc value of I_{L_F}, and subtract it from the inductor current before injecting it into the loop, thus removing the steady-state tracking error. The duty cycle D' is computed starting from the input and the output voltage, whereas the efficiency η could be in principle obtained from a direct measurement of the power MOSFET on-resistance. This measurement, however, would require extra components, increasing complexity, area, and power consumption. Instead of measuring the efficiency, it is possible to replace η in (12) with the worst-case value. According to (11), the largest tracking error occurs when the inductor current is maximum, i.e., when the efficiency approaches its minimum value. Therefore, an estimation of the minimum η is taken into account in the load-current sensor. At lighter loads, the efficiency will differ significantly from the minimum one, leading to an imperfect correction of tracking error. However, the tracking error magnitude reduces as well at light loads, making the inaccuracy negligible. The key advantage of the proposed technique is that, unlike the method proposed in [17], it is able to correct the tracking error without worsening the transient response of the system. In fact, the tracking error correction is addressed by injecting a replica of the dc value of the inductor current into the loop, without affecting the ac component that is relevant for the RHP-zero elimination.

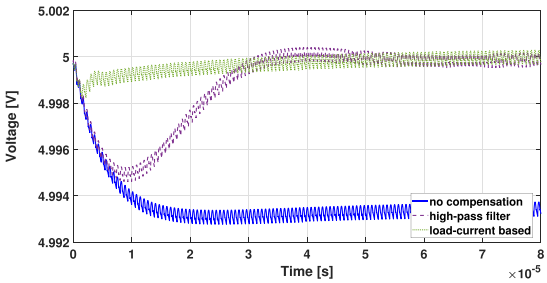
A comparison of the various techniques is carried out by simulating the transient responses of the boost converter to a 500-mA load-current step variation, in the case of no tracking error correction, high-pass filter correction, and proposed load-current-based correction. The simulations were performed using a Verilog-A behavioral model and the converter parameters discussed in the next section. As demonstrated in [21], the high-pass-filter corner frequency is chosen to be one-fourth of the RHP-zero frequency (in magnitude), not to appreciably degrade the loop phase margin. The transients, plotted in Fig. 5, show a large tracking error when no countermeasure is taken, and a slow tail due to the low frequency *RC* pole when the high-pass filter solution in Fig. 3 is adopted, and a quick correction of the tracking error when the load-current-based technique in Fig. 4 is used. This behavior is valid both for heavy [see Fig. 5(a)] and light [see Fig. 5(b)] current step variation.

IV. System Design

The presence of the RHP zero impacts the maximum converter bandwidth in a variety of applications where large switching frequency and/or large load currents are required. Among them, the generation of the supply rails for AMOLED display has been chosen as a particular case study. In this application, it is required to have both currents in the order of hundreds of mA and large bandwidth to avoid flickering of the display during line and load transients. The following design specifications have been adopted. The input voltage supply is provided by a standard Li-ion battery with a voltage ranging from 2.5 to 4.5 V and the output voltage is regulated at 5 V. The load current ranges from zero to a maximum of 800 mA. The switching frequency f_{sw} is 1.5 MHz. The off-chip filter components are $L_F = 2.2\,\mu$H



(a)



(b)

Fig. 5. Simulated transient response to a load-current step of (a) 500 mA and (b) 50 mA, with different tracking error correction strategies.

and $C_F = 44\,\mu$F. Consequently, the natural frequency of the complex-pole pair of the converter ranges from about 8–15 kHz, depending on the input voltage value. A PID compensator is commonly used to maximize the bandwidth and, thus, the converter transient response. The generic PID transfer function is given by

$$T_{\mathrm{PID}}(s) = K_{\mathrm{PID}} \frac{(1+s\tau_{zl})\,(1+s\tau_{zh})}{s\,(1+s\tau_{p1})\,(1+s\tau_{p2})} \tag{13}$$

where K_{PID} is the PID gain, τ_{zh} and τ_{zl} are the time constants of the LHP zeroes, and τ_{p1} and τ_{p2} are the time constants of the two high-frequency poles. The LHP zeroes are placed before and after the complex-pole pair to compensate for the phase shift introduced by the second order *LC* filter [20]. Accordingly, τ_{zh} and τ_{zl} are $f_{zl} = 1/(2\pi\tau_{zl}) = 5\,$kHz and $f_{zh} = 1/(2\pi\tau_{zh}) = 25$ kHz. The high-frequency poles have only a limited impact on system stability and they will be omitted in the following derivations for the sake of simplicity.

As demonstrated in [17], the magnitude of the transimpedance R_T of the inductor current sensor in the system block diagram in Fig. 2 influences the final position of the RHP zero. In particular, R_T can be selected such that the RHP zero is moved to the LHP and used as one of the two compensating LHP zeroes in (13). The theoretical analysis carried out in [21] demonstrates that the best choice for stability and transient response is to move the RHP zero to $s = -1/\tau_{zh}$, which is the position of the higher frequency zero of the PID. Doing so, the new compensator network only requires to introduce a single zero, meaning that it can be reduced to a simple PI network. Adopting this strategy (i.e., imposing $\omega_{z,\mathrm{rhp}} = -1/\tau_{zh}$) and solving (9) for the worst-case RHP zero, which occurs at maximum load current and minimum

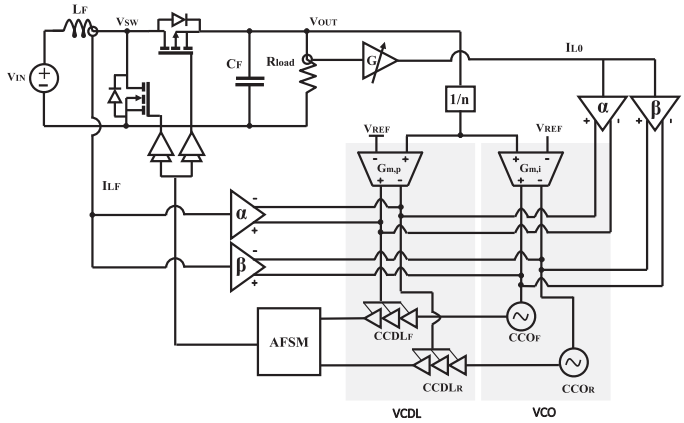


Fig. 6. Simplified block diagram of the proposed boost converter with time-based control, RHP-zero elimination, and proposed tracking error correction.

D', we obtain the following design equation:

$$nR_T = \frac{D'_{\mathrm{min}}}{C_F}\left(\tau_{zh} + \frac{L_F}{R_{\mathrm{load_{min}}} \cdot D'^2_{\mathrm{min}}}\right) \tag{14}$$

which, after plugging in the parameters (i.e., $R_{\mathrm{load_{min}}} = 6.25\,\Omega$, $D'_{\mathrm{min}} = 0.5$, and the other parameters abovementioned), provides a transimpedance value of $nR_T = 88\,\mathrm{m}\Omega$. Based on this result, the condition in (10) must be checked. The term on the right-hand side of the inequality in (10) has a magnitude of at most 18% compared with the one on the left-hand side, nR_TC_F. This means that the denominator of (9) changes by about 22% in the whole operating range giving only a marginal impact on the system bandwidth and stability.

As the $R_T \cdot I_{L_F}$ voltage at the transimpedance amplifier output has to be summed to the scaled converter output voltage, a voltage adder would be in principle required. To avoid such an extra component potentially increasing both power consumption and area occupation, we changed the voltage-controlled blocks, VCDL and VCO, to current-controlled ones driven by transconductors, i.e. a current-controlled delay line (CCDL) and a current-controlled oscillator (CCO). In this way, the signal summation is easily performed summing two currents in a converging node at the output of the transconductor. The relationship between the above-defined gains of the voltage-controlled blocks and the gains of the current-controlled ones is given by

$$\begin{aligned} K_{\mathrm{VCDL}} &= G_{m_p} \cdot K_{\mathrm{CCDL}} \\ K_{\mathrm{VCO}} &= G_{m_i} \cdot K_{\mathrm{CCO}} \end{aligned} \tag{15}$$

where G_{m_p} and G_{m_i} are the transconductances of the proportional and the integral transconductor, respectively.

The resulting block diagram of the boost converter with time-based control, RHP-zero elimination, and tracking error correction is shown in Fig. 6. A differential control topology is used to avoid the switching frequency dependency on the target output voltage [7]. A voltage attenuation $1/n = 0.2$ is introduced to decrease the output voltage to a level compatible with the 1.8 V supply voltage of the $0.18\,\mu$m CMOS transistors used in the compensation network, whereas V_{REF} is the external reference voltage of the controller.

The inputs of the CCOs and CCDLs are used as summing nodes of the currents from the transconductors and the inductor- and load-current sensors. Since the latter currents are injected at the transconductor output, they have to be properly scaled. Denoting α the needed attenuation from the inductor current to the G_{m_p} output, and β the needed attenuation from the inductor current to the G_{m_i} output, we obtain

$$\alpha = R_T G_{m_p}$$
$$\beta = R_T G_{m_i}. \tag{16}$$

Note that being α and β current attenuations, they can be easily implemented by means of ratioed current mirrors. Being the transconductor differential, the current mirrors has to be differential as well. Following the same approach, the tracking error is compensated by injecting the sensed load current into the same nodes (but with opposite polarity with respect to the inductor current to perform a subtraction).

The loop transfer function of the overall system is the product between the transfer function of the boost converter (with the RHP zero shifted to the LHP) and that of the PI compensator, and can be written as

$$G_L(s) = G_{\text{boost}_{\text{LHP}}}(s) \cdot G_{\text{PI}}(s) = G_{d0} \frac{\left(1 + s\frac{G_{m_p} K_{\text{CCDL}}}{G_{m_i} K_{\text{CCO}}}\right)(1 - s\tau_{z,\text{rhp}})}{s \cdot \left(\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1\right)} \tag{17}$$

where $G_{d0} = G_{m_i} K_{\text{CCO}} V_{\text{out}}/(nD')$ and $\tau_{z,\text{rhp}}$ is the inverse of $\omega_{z,\text{rhp}}$ in (9). The $G_{m_i} K_{\text{CCO}}$ product sets the closed-loop bandwidth. Having eliminated the RHP zero, the only limiting condition for the bandwidth is the switching frequency. Setting the bandwidth frequency to about one-tenth of f_{sw} and assuming minimum D', we obtain $G_{m_i} K_{\text{CCO}} = 850$ kHz/V. In this design, we set $G_{m_i} = 20\,\mu$A/V and $K_{\text{CCO}} = 42.5\,\text{kHz}/\mu\text{A}$.

Instead, the $G_{m_p} K_{\text{CCDL}}$ product sets the position of the low-frequency zero in (17). Setting it to $f_{zl} = 5$ kHz (as discussed previously), we get $G_{m_p} K_{\text{CCDL}} = G_{m_i} K_{\text{CCO}}/\omega_{zl} = 27.05\,\text{V}^{-1}$. The latter product can be interpreted as the sensitivity of the equivalent VCDL delay in number of switching cycles per volt. Thus, being $f_{\text{sw}} = 1.5$ MHz, it can be also expressed in seconds per volt, i.e. $18\,\mu$s/V. In this design, we set $G_{m_p} = 60\,\mu$A/V and $K_{\text{CCDL}} = 300\,\text{ns}/\mu\text{A}$. Compared with a standard time-based PID control, the proposed architecture requires an inductor sensor and a load sensor, but it spares the derivative control, which adds a current consumption at least comparable to the proportional control. At the same time, the standard implementation still requires the integration of a current sensor to generate the reference for the power MOS segmentation and to implement the over-current protection. As a result, the proposed technique is expected to give only a limited increase in the quiescent current consumption of the converter.

A. PFM Operation Mode

The boost converter in CCM strives to achieve high efficiency at light load conditions. However, in battery-powered devices, the current consumption when the device is idle or in standby mode has to be minimized. For this reason, a PFM operation mode for light loads has been included. The block diagram view of the implemented PFM control is shown in Fig. 7. To reduce the quiescent current, the time-based controller is turned OFF. The PFM is based on a peak inductor current control that is implemented by means of a peak current comparator driven by a voltage replica of the inductor current. As the output voltage V_{out} drops below the comparator threshold, the controller turns on the low-side switch, until the target inductor peak current is reached. After that, the high-side switch is activated, discharging the inductor until the zero-current-detector triggers. Those operation phases are managed by an asynchronous finite-state-machine.

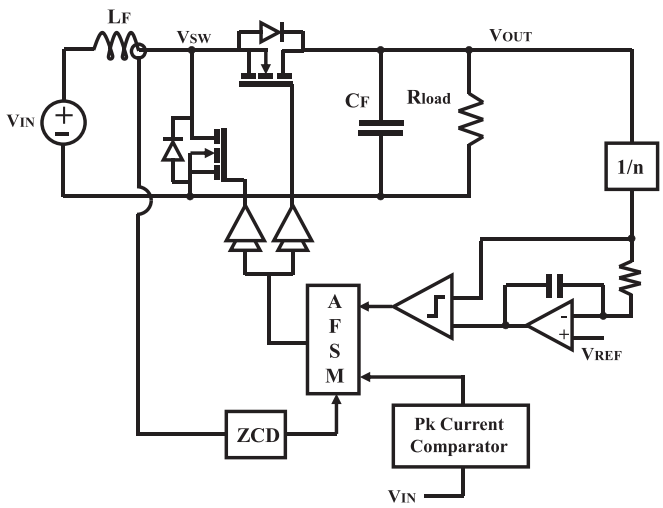


Fig. 7. PFM control structure for the proposed boost converter.

Using a comparator with constant voltage threshold to trigger the PFM charging phase, the V_{out} would show a tracking error given by

$$V_{\text{err}} = \frac{L_F I_{\text{pk,PFM}}^2}{4C_F\,(V_{\text{out}} - V_{\text{in}})} \tag{18}$$

where $I_{\text{pk,PFM}}$ is the chosen peak inductor current value. To remove such an error and increase the converter dc regulation, a voltage integrator is added that generates the reference voltage of the comparator.

The transitions between CCM and PFM modes are triggered on the basis of the average value of the inductor current, which is obtained from the current sensor already discussed in the previous section. A hysteresis between the two current thresholds of the two transitions has been introduced to avoid spurious events. Since the PFM control is based on a set of open-loop comparators, it does not need to be initialized and a seamless CCM-to-PFM transition together with the loop stability is always guaranteed. This is true with the only exception of the voltage integrator in Fig. 7, which, however, is bypassed during the transition as will be explained in detail in the next section. In the PFM-to-CCM transition, the proportional and integral controls have to be properly biased and initialized to avoid instability and undesirable output voltage transients. In the differential time-based control, the steady-state point is

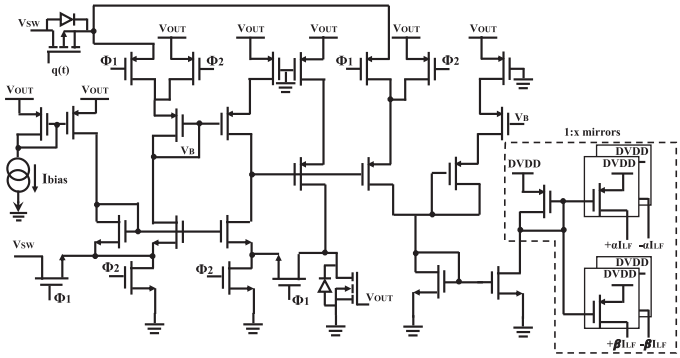


Fig. 8. Schematic diagram of the inductor current sensor. The node v_{sw} is the phase node of the boost converter and DVDD is the supply of the CMOS section.

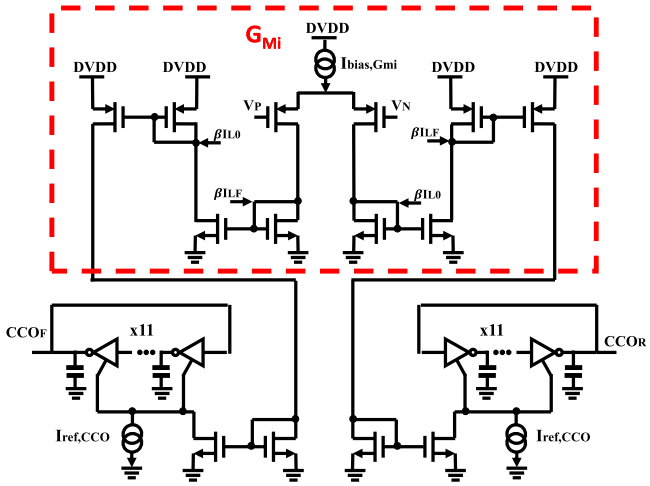


Fig. 9. Simplified schematic diagram of the integral control.

reached when the inputs of the transconductors (G_{m_p} and G_{m_i}) are equal. To emulate this condition, the inputs of the two transconductors are all connected to $V_{\rm REF}$, giving the bias to the two CCOs and CCDLs. The inductor current sensor, on the other hand, is the only component that is kept active also during the PFM operation (since it generates the current reference for the PFM/CCM transitions) and it does not need to be initialized. This means that, during the transition, the proposed time-based control is correctly biased, and its stability is assured by design. To guarantee the seamless transition, also the initial condition of the PWM duty cycle needs to be preset. This is obtained using the strategy described in [22], and the same hardware is also used for the soft start of the converter, thus minimizing area occupation. Starting from the PFM operation, when the average inductor current increases over the threshold, the system turns on the time-based controller and initializes all the internal variables. This initialization phase lasts two PFM cycles. During this period, the output voltage is still controlled by the PFM controller. The zero-current-detector inside the converter is turned-on only during the PFM operation, as a result the prototype converter is not designed to operate in DCM, meaning that the current in CCM can be inverted.

V. Circuit Design

A. Inductor Current Sensor

The application of the abovementioned RHP-zero elimination technique requires to sense the inductor current (up to 2 Amps), scale it and inject it into the control loop. For this reason, a simple average detector would be insufficient. The sensor bandwidth has to be comparable with the converter one, so that the transient response of the LHP zero (associated with the inductor) is correctly reproduced and the loop stability is unaffected by the delay added by the sensor itself. The schematic diagram of the implemented current sensor is shown in Fig. 8, whose detailed analysis can be found in [23]. Rather than reading directly the inductor current, the current at both high- and low-side power MOSFETs is sensed by means of two sensing MOSFETs. Two complementary signals ϕ_1 and ϕ_2, which are in phase with the power N-MOSFET and P-MOSFET driver, respectively, activate only half of the circuit when the power N-MOSFET is ON, and the other half, when the power P-MOSFET is ON. The current consumption of the sensor is about 65 μA.

B. Integral Control

The integral control, implemented as a 1.5 MHz CCO driven by a transconductor G_{m_i}, is shown in Fig. 9. The CCO, whose number of stages is chosen on the basis of the phases needed for the soft start-up and the PFM-to-CCM seamless transition [22], is made of eleven current-starved inverters loaded by capacitors. The CCO sensitivity is $K_{\rm CCO} = 33\,{\rm kHz}/\mu{\rm A}$ and its bias current is the sum of a zero to absolute temperature (ZTAT) current reference, $I_{\rm ref,CCO} \approx 7.7\ \mu$A, and the transconductor bias current $I_{{\rm bias},Gmi}/2 = 0.5\ \mu$A. By making the latter contribution negligible, the impact of mismatches and variability within the integral transconductor on the CCO operating point are greatly reduced. The transconductor has a simple differential topology with V_p and V_n inputs and with multiple 1:1 mirror stages, whose low-impedance node is used as a current-mode summing node for the scaled inductor current $\beta_{I_{LF}}$ and load current $\beta_{I_{L0}}$. The two currents are injected into two different parts of the mirror chain, to be summed to (and subtracted from) the signal current. The static current consumption of the integral transconductor is about 3 μA with $G_{m_i} = 20\ \mu$A/V.

C. Proportional Control

The schematic diagram of the proportional-control circuit, which is similar to that of the integral transconductor described previously, is shown in Fig. 10. The main difference is the addition of the two current references $I_{\rm ref,CCDL}$. The addition of these current sources gives two advantages. First, it allows to use a large bias current $I_{{\rm bias},Gmp} = 25\ \mu$A to set the transconductance gain $G_{m_p} = 40\ \mu$A/V while limiting the current consumption of the following mirror stages. Second, it decouples the bias of the proportional transconductor $I_{{\rm bias},Gmp}$ from the bias current that is used to drive the CCDLs. The latter current sets not only the static delay of the delay-line, but also its gain. The output mirrors of the proportional transconductor are used to determine

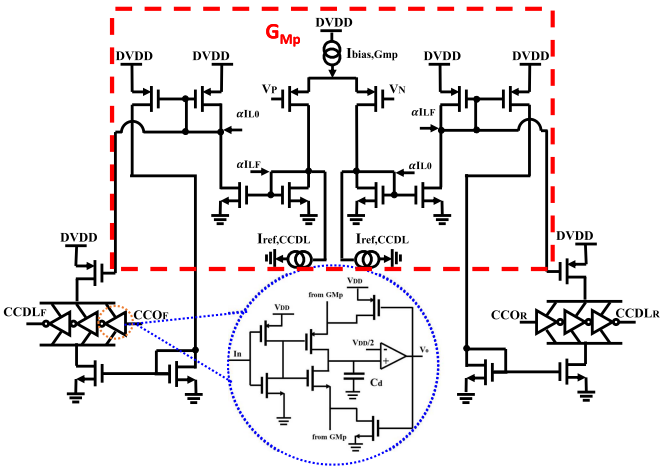


Fig. 10. Simplified schematic diagram of the proportional control.

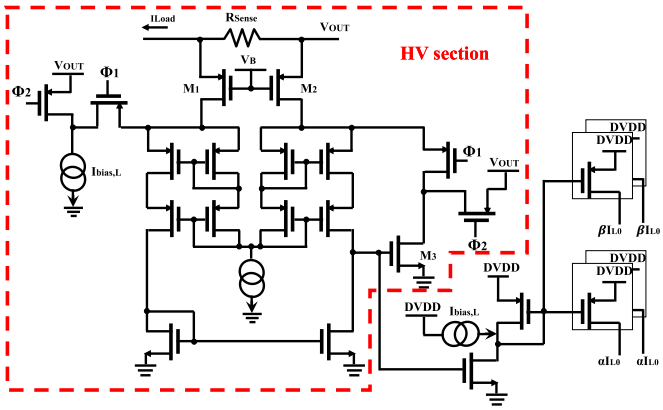


Fig. 11. Schematic diagram of the load current sensor.

the charging and discharging constant currents of the CCDL, which comprises eight delay cells. Each cell (shown in the inset in figure) inverts the input signal and enables the switches for charging/discharging the delay capacitor C_d. The delay-cell output is also fed back to boost the transition once the signal has crossed the comparator threshold. The CCDL sensitivity is $K_{\mathrm{CCDL}} = 300\,\mathrm{ns}/\mu\mathrm{A}$ and its current consumptions is $20\,\mu\mathrm{A}$.

D. Load-Current Sensor

The topology of the load current sensor was designed starting from the one proposed in [24] and is shown in Fig. 11. The circuit is a high-side current sensor. Denoting R_{sense} the integrated sense resistor and the $R_{\mathrm{on},M1}$ ohmic resistance of M1, the current flowing in M_3 (at the output of the "HV section") is given by $i_{M_3} = I_{\mathrm{load}} \cdot R_{\mathrm{sense}}/R_{\mathrm{on},M1}$, and it is mirrored and injected at the output of the transconductors used in the proportional and integral paths. Thus, the gain from the load current to the sensed current is set by the ratio between R_{sense} and $R_{\mathrm{on},M1}$ (and $R_{\mathrm{on},M2}$, i.e., the ohmic resistance of M_2). Although MOS resistors are process and temperature dependent, the dc gain of the sensor is tuned via the voltage V_B to compensate for process spreads, and V_B is generated from a proportional to absolute temperature (PTAT) current reference to compensate temperature variations. The sensor stability is ensured by a dominant pole, as the only high-impedance node is at the gate of M_3. However, the loop bandwidth strongly depends on the transconductance of M_3, which changes with the current of M_3 and in turn with the load current. Since the latter ranges from zero to about 1 amp, the sensor bandwidth varies significantly. To keep a sufficient bandwidth even in no-load condition, a fixed bias current I_{bias} is injected in the left-hand side branch of the circuit, forcing the system to have a minimum current to compensate. To avoid offset, the bias is removed after the mirroring of the current on M_3.

A set of switches driven by two opposite digital signals Φ_1 and $\Phi_2 = \overline{\Phi_1}$ are used to compensate for the duty-cycle-dependent gain between load and inductance current in (12). The latter changes dynamically during circuit operation and needs to be tracked. To this aim, Φ_1 has duty cycle (D) and Φ_2 has duty cycle $(1-D)$. This forces the circuit loop to be closed just for $(1-D)\cdot T_s$, where T_s is the switching period of Φ_1 and Φ_2. Being the bandwidth of the load sensor much narrower than $1/T_s$, the average current of M_3 is given by $\langle i_{M_3}\rangle = I_{\mathrm{load}} \cdot (1-D) \cdot R_{\mathrm{sense}}/R_{\mathrm{on}_{MOS}}$. The residual high-frequency component at $1/T_s$ is further filtered by the boost-converter control loop leaving no significant impact at the converter output. The integrated sensing resistance R_{sense} has a value of $25\,\mathrm{m}\Omega$, and it was implemented using a polysilicon resistor. The width of such a resistor was chosen large in order to sustain the current densities associated with the load, making it responsible of about 80% of the whole sensor's area occupation. The load current sensor area is $180\,\mu\mathrm{m} \times 630\,\mu\mathrm{m}$, whereas the current consumption is $40\,\mu\mathrm{A}$.

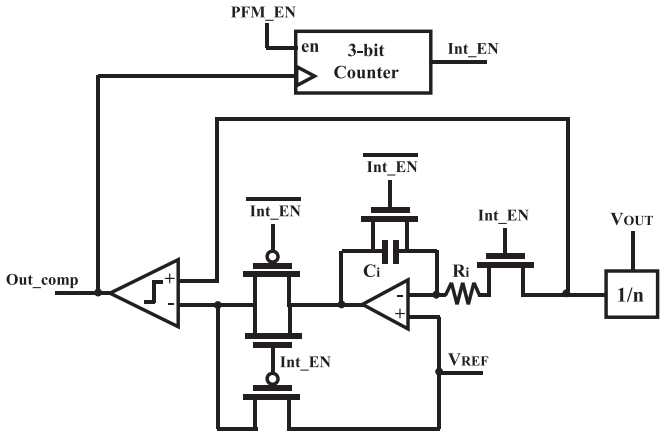


Fig. 12. Schematic diagram of the integrator circuit used in PFM mode.

E. Static Error Correction in PFM Mode

As discussed previously, a voltage integrator circuit is used to eliminate the static regulation error of the converter working in PFM mode. The operational-amplifier-based integrator, whose schematic is shown in Fig. 12, has an integrated capacitor C_i and is fed by the scaled converter output V_{out}/n. A large value of resistance R_i avoids to influence the resistive partition

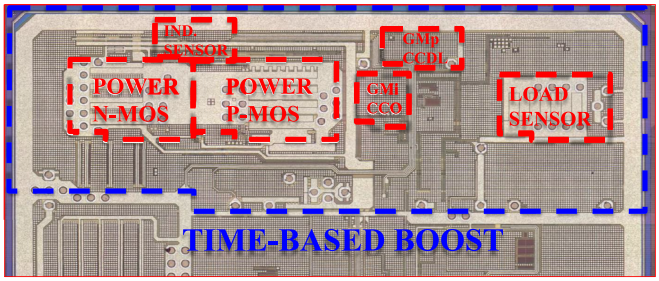
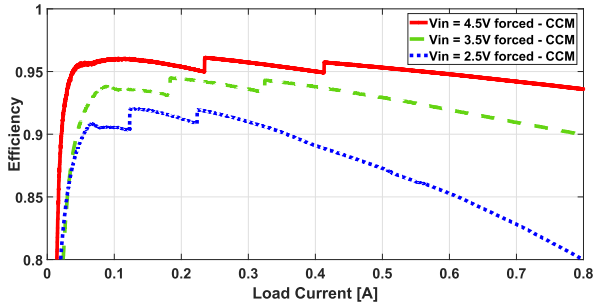


Fig. 13. Die microphotograph of the time-based boost converter.

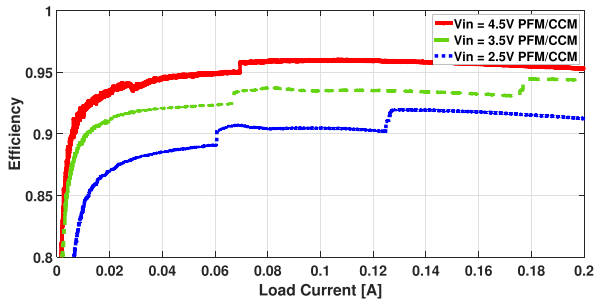
network $1/n$ at the convert output. By adapting the comparator reference voltage, the circuit is able to compensate the static errors introduced by the PFM comparator and the shift in the operating point related to PFM operation and described in (18). The only residual error is the offset of the operational amplifier which has to minimized by design. This integrator requires the C_i capacitance voltage to be properly initialized when the circuit is switched ON, i.e., during the CCM-to-PFM transition. This is necessary to ensure the stability of the control and avoid unwanted output voltage transients. A set of switches driven by int_EN initializes the voltage across C_i to zero, and bypass the integrator connecting the comparator negative input to the fixed threshold V_{REF}. Such condition lasts only for the first few triggers occurring after the CCM-to-PFM transition. This is necessary since, if the converter experiences a sudden drop in the load current during the transition, the output voltage may become slightly larger than its target value. As a result, the integrator would react by lowering the comparator threshold by a large amount, which would in turn cause the output voltage to reduce more than needed and the integrator to increase again the threshold level. In other words, the output voltage would increase and drop a few times, before reaching the steady-state condition. Instead, during the first few triggers, the converter operates with a fixed threshold PFM control, which guarantees stability but settles the output voltage with the small regulation error in (18). Once the counter overflows and the integrator are enabled, the threshold of the comparator is dynamically adapted and the error is corrected.

VI. Measurement Results

A prototype boost converter exploiting the described techniques was implemented in a 0.18 μm bipolar-CMOS-DMOS (BCD) technology. Fig. 13 shows the die microphotograph. The time-based PI controller area occupation is limited to 0.12 mm^2, whereas the inductor- and load-current sensors occupy 0.04 mm^2 and 0.11 mm^2, respectively. The quiescent currents are 235 μA for time-based PI control and 65 μA for the inductor current sensor, leading to an overall current consumption of the controller of 300 μA. The tracking error correction has a current consumption of 40 μA. Fig. 14(a) shows the measured converter efficiency for an input voltage of 4.5, 3.5, and 2.5 V. To improve the efficiency at medium and heavy loads, a binary weighted, three-level segmentation of the power-MOSFET is used that is controlled



(a)



(b)

Fig. 14. Measured efficiency for an input voltage of 4.5 (continuous line), 3.5 (dashed line), and 2.5 (dotted line). (a) Converter in CCM with load-current-depending activation of segmented power MOSFET. (b) Converter in PFM and CCM modes.

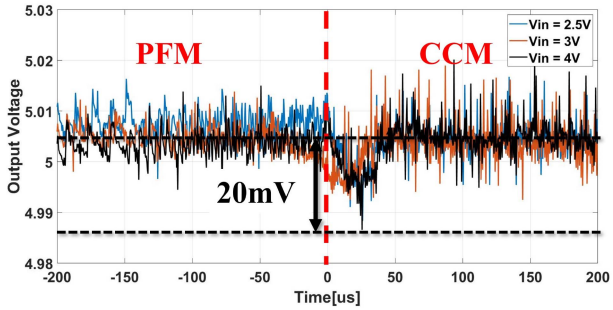


Fig. 15. Measured output voltage upon the PFM-to-CCM transition, at different input voltage values.

on the basis of the average inductor current. At $V_{\mathrm{in}} = 4.5$ V, the peak efficiency is about 96%, dropping below 90% at currents of about 50 to 10 mA, depending on the input voltage. The segmentation of the power stage was limited to only three level to limit the area occupation of the power stage and to optimize the converter efficiency for medium loads at low conversion ratio, i.e., when the Li-ion battery is fully charged. Fig. 14(b) shows the converter efficiency zoomed in the 0–200 mA load region, where the converter operates in PFM. The efficiency is always higher than 80% at currents above 10 mA. The voltage transient after a PFM-to-CCM transition in Fig. 15 shows a bumps lower than 20 mV demonstrating the effectiveness of the implemented seamless transition scheme.

Fig. 16(a) demonstrates the effective correction of the tracking error introduced by the RHP-zero elimination technique. Fig. 16

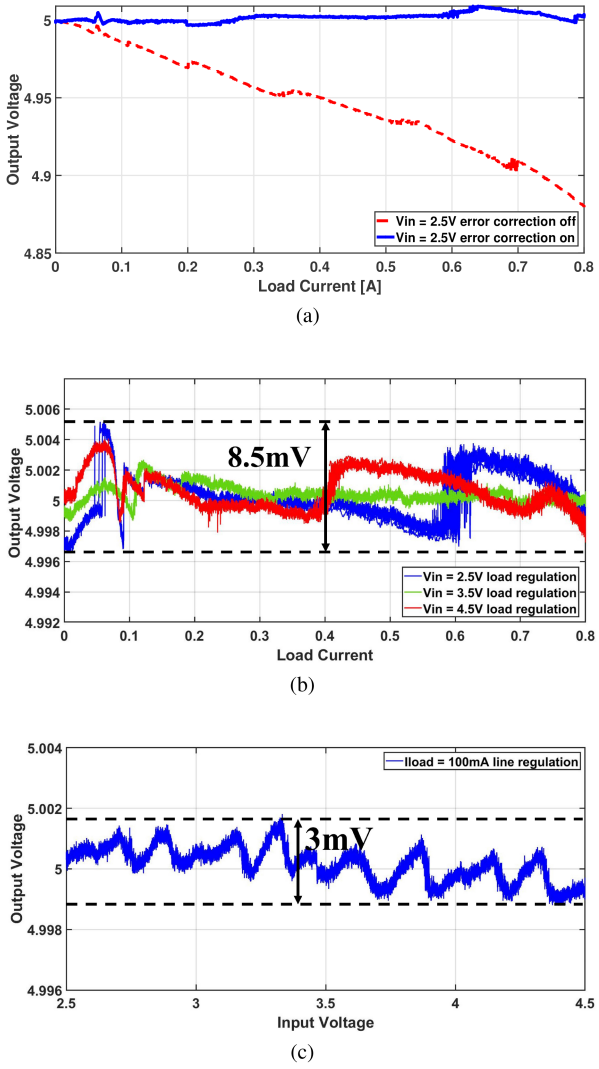


Fig. 16. Static load and line regulation. (a) Load regulation with tracking error correction in continuous line and without it in dashed line. (b) Load regulation with correction at different input voltage values. (c) Line regulation at 100 mA load current.

shows the measured static load regulation with tracking error correction enabled (continuous line) and disabled (dashed line) for the minimum input voltage of 2.5 V. The regulation error is reduced by a factor of 12×, from 120 mV down to less than 10 mV, and it is always below 0.2% along the whole range of input voltages, as evident in Fig. 16(b). The measured static line regulation is below 0.1% of the output voltage for a load current of 100 mA, as shown in Fig. 16(c). This error should be ideally null, as in principle the CCO should behave as an ideal integrator. However, an unwanted pulling between the reference and the feedback CCOs generates the unideal oscillating pattern visible in Fig. 16(c). All the values that are reported in Fig. 16 are obtained changing the input with a very slow ramp while measuring the average output voltage of the converter. As a result, all the information about the converter ripple are filtered out and cannot be recovered from these figures.

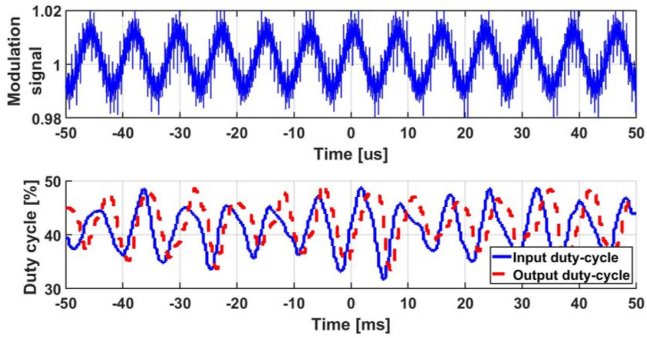


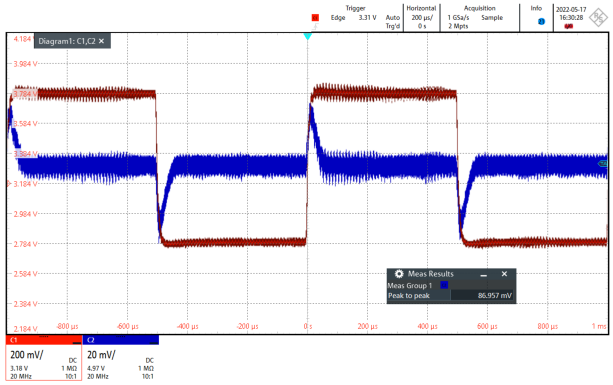
Fig. 17. Injected sinusoidal signal at 130 kHz (top plot). Input (continuous line, bottom plot) and output duty cycle (dashed line, bottom plot).

The open-loop crossover frequency been measured by using the technique described in [25]. A sinusoidal delay between $\mathrm{CCDL_R}$ and $\mathrm{CCDL_F}$ has been injected at the output of the two delay lines by means of two extra controlled delay lines. The induced duty-cycle variation, before and after the point of injection, has been detected via a flip-flop-based PD. To get the unitary-gain frequency f_u of the loop gain (that is a good estimate of the closed-loop bandwidth), the frequency of the injected sinusoidal delay has been varied until the magnitude of the signal before and after the injection was identical. This condition shown in Fig. 17 is reached at $f_u \approx 130$ kHz. This value is about a factor of 6× larger than that achieved in a plain loop without RHP-zero elimination and given by the combination of (5a) and (4). This bandwidth widening is beneficial for the transient behavior of the converter. The transient response to a 1-V input voltage variation is shown in Fig. 18(a). The input voltage is changed with a slope of 1 V/10 μ s. The measured peak variation at the output is only 0.8% of the nominal value. The transient response to a load-current variation from 0 to 300 mA and an input voltage V_{in}=3 V is shown in Fig. 18(b). The load current changes with a slope of 1 A/μs, which is the maximum allowed by the instrumentation. The peak output voltage variation is about 1.2% of its nominal value. The asymmetry between the two load transition in Fig. 18(b) is generated by the limited capability of the inductor sensor in Fig. 8 to reconstruct currents that are close to zero or negative. As the inductor current approaches zero during the high-to-low transition, the effective inductor current sensor gain "R_T" lowers, affecting the controller stability.

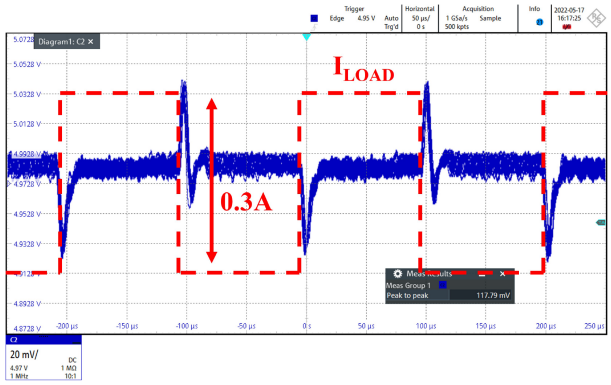
In Table I, the proposed circuit is compared with other state-of-the-art converter with RHP-zero elimination. To keep the comparison fair, we selected only papers reporting boost converters with specifications similar to those used in our prototype. In this frame, the power density is a key figure of merit that underline the area required for the implementation of a particular RHP-zero elimination technique. A numerical comparison, however, was not possible because the required data were not specified in the state-of-the-art converters reported in Table I. On the other hand, a qualitative comparison can be performed highlighting the extra number of components that are required by each RHP-zero elimination solution in Table I compared

TABLE I
PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART BOOST CONVERTERS

	This work	[26]	[27]	[28]	[29]	[30]
Control Scheme	**Time-based**	Interleaved Current-mode	Current-mode	Current-mode	Hybrid	Current-mode
Process	**0.18μm BCD**	0.3μm 5/18V CMOS	0.18μm CMOS	0.18μm CMOS	0.25μm CMOS	0.18μm BCD
Input Voltage	**2.5-4.5V**	3.1-3.3V	2.7-4V	1.55-1.8V	2.9-6.3V	2-4.2V
Output Voltage	**5V**	5V	4.5V	2.5V	4.6V	3-5V
Inductor	**2.2μH**	0.47μH	4.7μH	10μH	4.7μH	4.7μH
Capacitor	**44μF**	20μF	4.7μF	10μF	10μF	10μF
Load Current	**800mA**	400mA	150mA	200mA	600mA	800mA
Peak Efficiency (boost mode)	**96%**	–	92.44%	95.7%	96%	95.2%
Extra Components	**On-chip inductor sensor and load current sensor**	0.47μH inductor 2x Schottky diodes	flying capacitance	10μF flying capacitance	470nF flying capacitance	10μF flying capacitance
Extra Power Switches	–	–	2	1	2	2



(a)



(b)

Fig. 18. Transient responses (a) to a fast 1-V input voltage variation and (b) to a fast 0.3-A load current variation.

with a standard boost converter implementation. The proposed converter performs the RHP-zero elimination without requiring external flying capacitance/inductors or additional power MOS switches that are responsible for a significant increase of the converter volume and die size, respectively. On the other hand, the only components added by the proposed solution are one integrated inductor sensor and one integrated load sensor, whose overall area occupation is comparable to the one of a power MOS switch (as clearly visible from the die microphotograph in Fig. 13). Moreover, it should be noted that a load-current sensor is usually needed in a dc–dc converter for portable applications

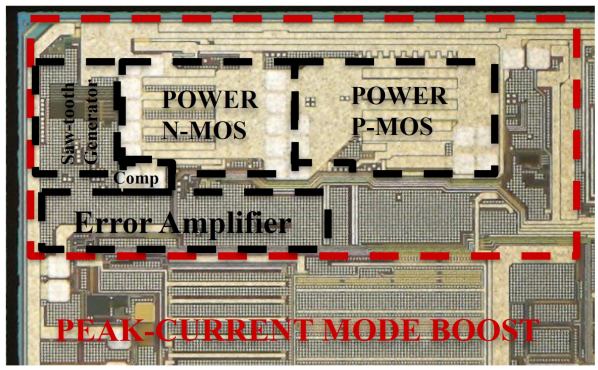
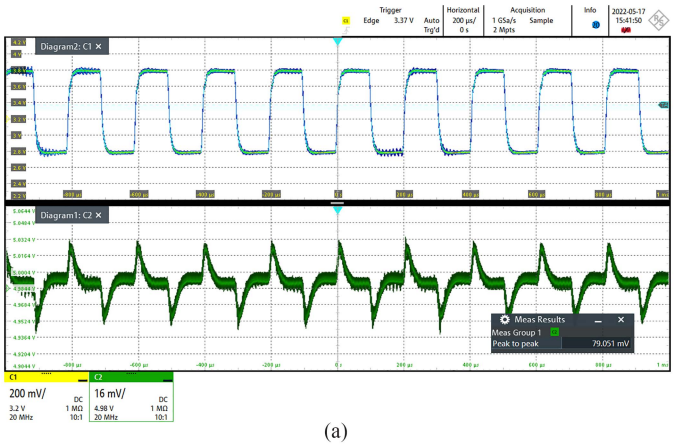


Fig. 19. Die microphotograph of the boost converter with peak-current mode control.

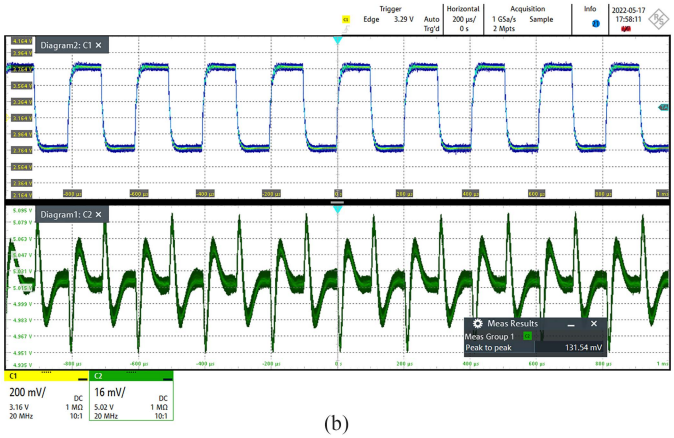
to control the power-stage segmentation and optimize efficiency over a large range of load currents.

A. *Performance Comparison With Peak-Current Mode Control*

To verify the advantages of the proposed time-based control with RHP-zero elimination in terms of area occupation, power consumption, and dynamic response, the prototype converter has been compared with a converter adopting a peak-current mode control designed using the same technology node for the same target application. In particular, the two converters share the same power stage, i.e., the power MOS switches and the external reactive elements (filter inductor and output capacitor) are identical. The converter with peak-current mode compensation was controlled with a standard PI control implemented by means of an error amplifier, a saw-tooth voltage generator and a PWM comparator. The die microphotograph of the converter with peak-current mode control is shown in Fig. 19, where the main circuit blocks are highlighted with dashed boxes. The saw-tooth voltage generator, the PWM comparator, and the error amplifier occupy an area of 0.166, 0.025, and 0.263 mm^2, respectively, leading to an overall area occupation of 0.45 mm^2. Compared with the 0.27 mm^2 of the proposed time-based control with RHP-zero elimination, the controller area was reduced by 40%. The quiescent currents of the error amplifier, PWM comparator, and saw-tooth generator are equal to 135, 225, and 240 μA, respectively. The overall current consumption of the

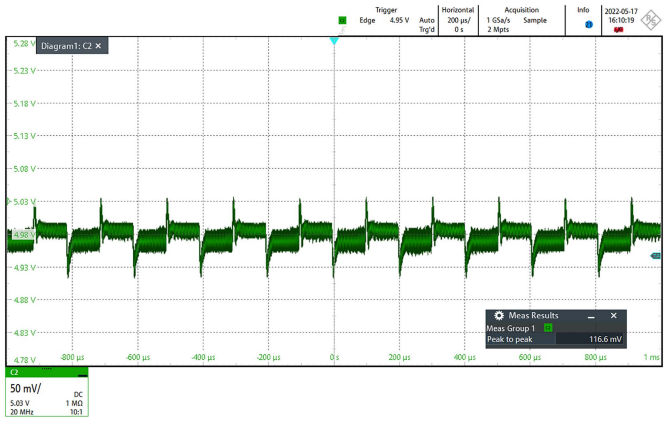


(a)

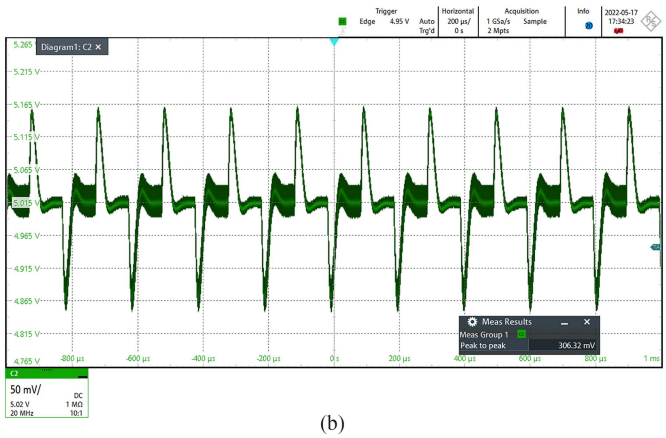


(b)

Fig. 20. Line transient response to a 1-V input voltage variation when no load current is applied. The (a) proposed converter shows a reduction of the peak output voltage variation of a factor 3.5 compared with the converter with (b) peak-current mode control.



(a)



(b)

Fig. 21. Load transient response to a square wave load current with 0.3 A amplitude. The (a) proposed converter has an improvement on the load transient performance by about 3 times compared with the converter with (b) peak-current mode control.

peak-current mode is 600 μA compared with the 340 μA of the proposed architecture (controller + load current sensor), leading to a 40% reduction in the controller quiescent current.

The line transient response of the two converters to a 1-V input voltage variation are reported in Fig. 20. The output voltage variation of the proposed converter (top) is about 32 mV compared with the 112 mV of the converter with peak-current mode control (bottom), leading to a reduction of about a factor 3.5. Although the converter with peak-current mode control exploits a feedforward compensation, the proposed converter provides a significant improvement of the dynamic performance, thanks to the increase of the control loop bandwidth by a factor 6×. The transient response of the two converters to a 300 mA square wave load variation is shown in Fig. 21. The measurement are obtained with an input voltage of 3 V. The peak voltage variation of the proposed converter (top) is about 50 mV while the peak-current mode counterpart (bottom) has a variation of 150 mV, leading to an overall increase in the transient performance by about a factor 3. According to the comparisons shown in Figs. 20 and 21, the increase in the control bandwidth has a twofold advantage in the dynamic response of the proposed converter. First, thanks to the faster loop response, the peak output voltage variation generated by the transition is reduced. Second, the recovery time, which is dependent both on the control loop bandwidth and the position of the LHP zeroes, is faster.

VII. Conclusion

This article reports a novel synchronous boost converter with time-based control and a novel scheme to move the RHP zero to the LHP and correct the resulting tracking error. We showed that the closed-loop bandwidth of the converter was increased by about a factor of 6× compared with a standard boost converter operating in CCM. Thanks to the bandwidth increase, the output voltage variation during a line and load transient is reduced by a factor 3.5 and 3, respectively. Moreover, by exploiting the LHP zero for loop compensation, the implemented compensator was reduced to a simpler PI time-based filter. Unlike other RHP-zero elimination techniques, the proposed structure does not require extra external capacitors or additional power MOS switches. A prototype boost converter for AMOLED display power supply was implemented in a 0.18 μm BCD technology, providing a larger than 85% efficiency in the 10–600 mA range in all the operating conditions, reaching a peak value of 96%. High efficiency is maintained at light loads thanks to a PFM mode with static error correction and seamless PFM-to-CCM transition. Static line and load regulation is below 0.1% and 0.2% over the

whole working range, respectively. The time-based controller occupies 0.12 mm^2 with an additional 0.04 and 0.11 mm^2 for the inductor- and the load-current sensor, respectively. Both the area occupation and the current consumption of all this components combined are about 40% lower compared with a peak-current mode control designed for the same application. The quiescent current of the proposed time-based control with RHP-zero elimination is 300 μA, whereas the tracking error correction has a bias current of 40 μA.

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