Understanding Inherent Implication of Thermal Resistance in Double-Side Cooling Module

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***Abstract*—The double-side cooling (DSC) packaging becomes more and more popular with the great demands of high power and fast speed, especially for silicon carbide metal oxide semiconductor field effect transistors. Measurements and modeling of thermal resistance are critical for thermal management of DSC module. However, the thermal resistance of DSC module is still unclear due to the asymmetric dual thermal paths. In this article, a clear understanding of thermal resistance of DSC module measured by transient dual-interface method (TDIM) is explained. The thermal impedance of DSC module is analyzed through time- and frequency-domain response of the DSC thermal model. The cooling conditions in TDIM have no influence on the measured thermal resistance of DSC module. The measured thermal resistance from junction to top case (or bottom case) is half of the actual value. The important conclusions are verified by transient simulations and experiments. Based on the results, a new definition of thermal resistance of DSC module is proposed for exact evaluation of thermal resistance and reliability.**

***Index Terms*—Double-side cooling (DSC) module, thermal resistance measurement, transient dual-interface method (TDIM).**

I. Introduction

THE high performance and high reliability of power semiconductor devices have become the most momentous requirements in the emerging fields [1], [2], [3], [4], such as electric vehicle, transmission, renewable energy, etc. In this context, the double-side cooling (DSC) module with various advantages greatly improves the power density of power converters [5], [6], [7]. First, the planar power packaging and large bonding area could achieve a minimum parasitic inductance and parasitic resistance. Second, the dual cooling paths increase the current handling capability and switching frequency, thus reducing the cost of cooling and filter. Finally, the improved thermal performance reduces the temperature swings and thermal stress. In addition, the wire-bondless configuration removes the one of the major failure modes [8], [9], [10]. The typical DSC modules based on silicon (Si) devices, such as press-pack module and double-side-soldered module, have been commercialized [11], [12], [13]. Even though the silicon carbide (SiC)-based DSC modules are less mature, the advantages of DSC packaging are extremely suitable for SiC devices, such as SiC metal oxide semiconductor field effect transistors (MOSFETs) and SiC IGBTs. Compared with Si devices, the SiC devices could achieve faster switching speed, which requires the lower parasitic inductance to reduce the electromagnetic interference. In addition, the DSC packaging makes SiC devices with high operation temperature become possible. The DSC module with high reliability reduce the system and maintenance costs in advanced SiC-based applications, such as electric vehicle, photovoltaic, drives, etc. Therefore, the advantages of DSC packaging make it become the first choice to improve the utilization and reliability of SiC devices [14], [15], [16].

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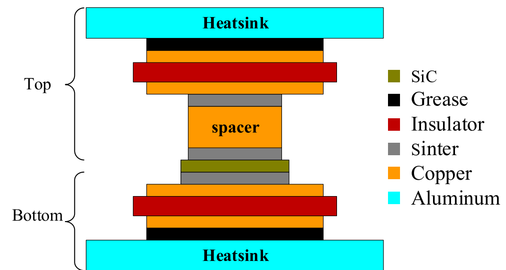

Fig. 1. Structure of the SiC DSC module.

Different from other packaging structures, the DSC structure achieves the lowest thermal resistance (R_{th}) through the dual paths of power flow. The power losses flowing through top and bottom sides of module are not symmetrical, due to the presence of the spacer [17], [18]. The additional spacer between die and substrate increases the R_{th} of that side, as shown in Fig. 1. The inconsistent R_{th} of two sides becomes a great challenge for R_{th} measurement and thermal modeling of DSC module, due to the absence of the case temperature (T_c). Therefore, the thermal resistance from junction to fluid ($R_{\mathrm{th\text{-}jf}}$) is used to reflect the R_{th} of DSC [13]. In most researches, the virtual R_{th} between junction and case is calculated by the paralleling the R_{th} of top and bottom sides, as given in (1). It worth noting that, the formula (1) could represent the real R_{th} of DSC module only when the case temperature of top is equal to that of bottom. The paralleling calculation could still reflect the overall R_{th} of the

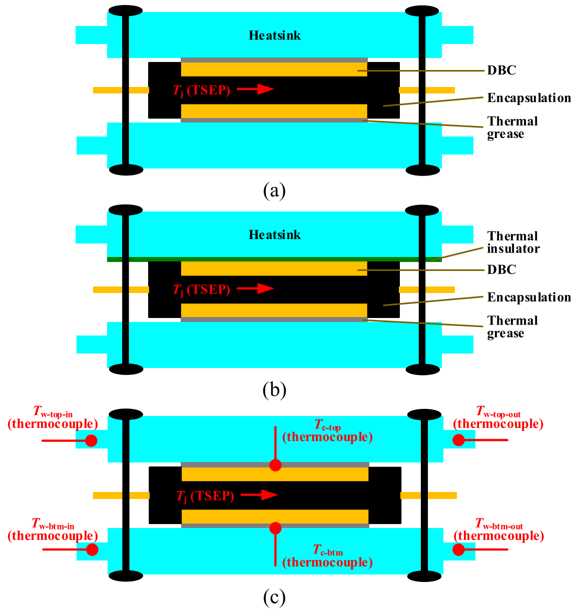

Fig. 2. Three test conditions for measuring the thermal resistance of DSC module [13], [20], [22]. "DBC" is direct bonding copper. (a) DSC by TDIM. (b) SSC by TDIM. (c) Direct thermocouple.

DSC module [19].

$$R_{\text{th-jc}} = \frac{R_{\text{th-jc-top}} \times R_{\text{th-jc-btm}}}{R_{\text{th-jc-top}} + R_{\text{th-jc-btm}}} \quad (1)$$

where $R_{\text{th-jc}}$ is the equivalent thermal resistance of DSC module and $R_{\text{th-jc-top}}$ and $R_{\text{th-jc-btm}}$ are the thermal resistances from junction to top and bottom sides of DSC module, respectively.

Although there is no standard measurement method for R_{th} of the DSC module so far, several measurement methods are proposed under various test conditions. These methods are mainly based on the measurement standard of single-side cooling (SSC) modules. There are three typical methods for measuring $R_{\text{th-jc}}$, as shown in Fig. 2. In the DSC mode in Fig. 2(a), the transient dual-interface method (TDIM) is used [13]. During the test, the thermal impedance (Z_{th}) of DSC module with and without a thermal interface material (TIM) between module and heatsink is measured. The separation point of the two curves is regarded as the equivalent $R_{\text{th-jc}}$ of DSC in the DSC condition in Fig. 2(a). In the SSC mode in Fig. 2(b), $R_{\text{th-jc-top}}$ and $R_{\text{th-jc-btm}}$ are measured, respectively. Then, the $R_{\text{th-jc}}$ of DSC module could be derived by (1). To achieve a separate measurement, a thermal insulator is inserted between module and heatsink of one side when the other side of R_{th} is measured [20], [21]. By this scheme, the $R_{\text{th-jc-top}}$ and $R_{\text{th-jc-btm}}$ measured by TDIM or thermocouple method are regarded as the R_{th} of each side of the DSC module. In the direct thermocouple method in Fig. 2(c), a method for simultaneously measuring $R_{\text{th-jc-top}}$ and $R_{\text{th-jc-btm}}$ is proposed, by inserting several thermocouples at cases and heatsinks [22]. Formula (1) is used to derive the $R_{\text{th-jc}}$ as well.

Although abovementioned methods claim that the measured R_{th} is the exact $R_{\text{th-jc}}$, the measurement results are various, such as the results measured by TDIM and thermocouple method in the SSC condition of Fig. 2(b) [20]. In addition, the influence of these test conditions on the test results is uncertain. The R_{th} measurement mechanism of DSC module is necessary for determining the thermal characteristics. Therefore, the inherent implication of thermal resistance of DSC module is analyzed in this article.

The rest of this article is organized as follows. The mechanism of R_{th} measurement of DSC module is analyzed in Section II. The theory results are verified by simulation in Section III. The test conditions and structures of DSC module are changed to find the mechanism. The thermal resistance tests under various external cooling conditions are performed to verify the findings in Section IV. Finally, Section V concludes this article.

II. Mechanism of R_{TH} Measurement

The TDIM and thermocouple method are typical solutions for measuring the $R_{\text{th-jc-top}}$ and $R_{\text{th-jc-btm}}$. As mentioned in [23], the thermocouple method is often not sufficiently reproducible. First, the temperature measured by thermocouple is determined by contact location. The measured temperature becomes uncertain because of the temperature distribution with a gradient on the module surface. Second, the sensing point of thermocouple is often not sufficient thermal insulated against the heatsink. The thermocouple may be cooled from the wire and heatsink, thus reducing the case temperature. Third, the clamping pressure applied to press the module against the heatsink varies during test, which may change the contact between thermocouple and case, thus changing the sensing temperature. Finally, there is no electrical insulation between thermocouple and heatsink. The potential of heatsink may disturb the output signal of the thermocouple. The TDIM is preferred in determining R_{th} of the power modules [24], [25], [26]. During the test, the Z_{th} curves of power module with and without TIM, called wet and dry curves, are measured, respectively [23]. The two Z_{th} curves are translated into structure function curves. Then, the separation point of two structure function curves is defined as $R_{\text{th-jc}}$. The essence of the TDIM is calculating time-constant spectrum of the Foster model by deconvolution of Z_{th} curve, and transforming Foster model to Cauer model.

The thermal response of the power module could be described by the Foster model and Cauer model. Since the Cauer model represents the physical regions of the module structure, the Cauer model of DSC module with two parallel *RC* networks are used, as shown in Fig. 3(a). The $R_{\text{th-jc-top}}$ and $R_{\text{th-jc-btm}}$ comprise of *n*-stage *RC* ladder network. The top case temperature ($T_{c\text{-top}}$) and bottom case temperature ($T_{c\text{-btm}}$) locate at the end of *n*th *RC* network. The time response curves of the Cauer network of DSC module under different cooling conditions are shown in Fig. 3(b). The top and bottom *RC* networks are paralleled when the condition of DSC is applied. If only one side of the module is cooled, i.e., top-side cooling or bottom-side cooling, the thermal resistance from top case (or bottom case) to fluid

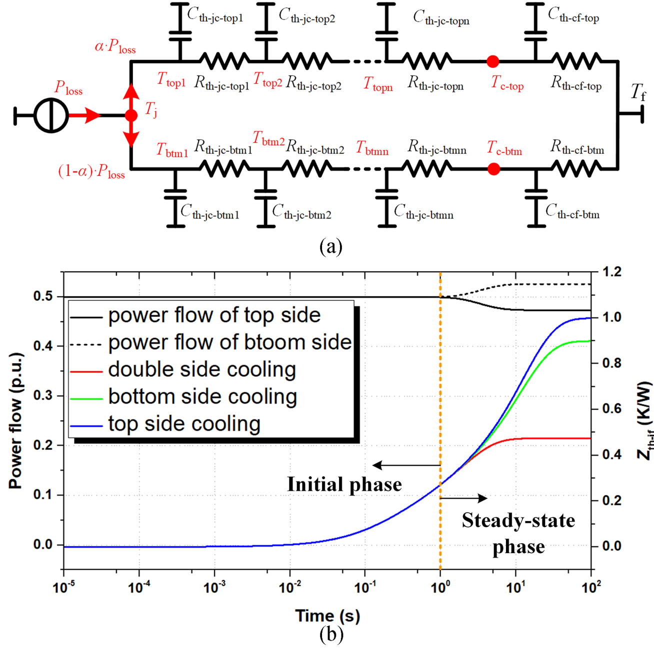

Fig. 3. Transient thermal response of DSC module. (a) Cauer network. (b) Simulation results of power loss distribution under double side cooling and $Z_{\rm th}$ curves under different cooling conditions.

($R_{\text{th-cf-top}}$ or $R_{\text{th-cf-btm}}$) will become a high value. Therefore, the overall $R_{\text{th-jf}}$ becomes larger.

Although the steady-state $Z_{\rm th}$ varies, the initial $Z_{\rm th}$ keep unchanged, as shown in Fig. 3(b). The frequency-domain expression of Cauer network in (2) could explain the mechanism. If the material of one layer is changed, the corresponding $R_{\text{th-jc-topn}}$ or $R_{\text{th-jc-btmn}}$ changes as well. The variation of $R_{\text{th-jc-topn}}$ or $R_{\text{th-jc-btmn}}$ influences the $Z_{\rm th}$ at lower complex frequency $s = jw$ (longer t), but hardly influences the $Z_{\rm th}$ at higher s (shorter t), according to (2). According to the initial value theorem, when s goes toward infinity, i.e., t goes toward zero, the $Z_{\rm th}$ is almost zero. It indicates that the initial $Z_{\rm th}$ of top and bottom sides is the same, so is the initial power flow. The influence of front *RC* networks on initial $Z_{\rm th}$ is greater than that of rear *RC* networks. In other words, the front *RC* networks change the early $Z_{\rm th}$ curve, while rear *RC* networks change the late $Z_{\rm th}$ curve. It is the base of separating the $Z_{\rm th}$ curves at the material-changed location.

Different from the SSC module, when the $Z_{\rm th}$ of one side is changed, the power losses flowing in this side and the other side are changed simultaneously. However, the $Z_{\rm th}$ of top and bottom sides are almost the same during the initial phase of $Z_{\rm th}$, due to the same power loss of two sides, as shown in Fig. 3(b). In addition, the rear $Z_{\rm th}$ hardly changes the initial $Z_{\rm th}$ as aforementioned. Therefore, there is an equivalent separate point when $Z_{\rm th}$ of one side is changed, as shown in Fig. 3(b). It could be concluded that no matter how the materials far away from top case or bottom case are changed, the $R_{\text{th-jc-top}}$ or $R_{\text{th-jc-btm}}$ remains the same.

When thermal resistance measurement of the DSC module is performed by TDIM, the single thermal network in Fig. 4(b)

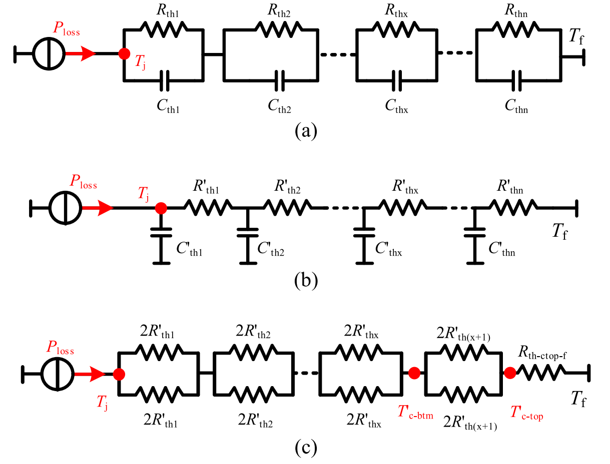

Fig. 4. Thermal model of the DSC module. (a) Single-path Foster network. (b) Single-path Cauer network. (c) Steady-state $R_{\rm th}$ distribution with dual paths.

is derived from dual-thermal network in Fig. 3(a) through the Foster thermal network in Fig. 4(a). The Foster model has no physical reality due to node-to-node thermal capacitance ($C_{\rm th}$). This single Cauer thermal network could be regard as the equivalent thermal circuit of the dual thermal paths network, but has no practical reality as well. According to the abovementioned theoretical analysis, the thermal capacitances dominate the $Z_{\rm th}$ during the initial phase. In addition, the top and bottom sides thermal capacitances close to junction have the same value, forming the same transient power flows of top and bottom sides during initial phase of $Z_{\rm th}$. The rear *RC* network has no influence on initial $Z_{\rm th}$ as mentioned. The front $R'_{\rm th}$ of the Cauer network in Fig. 4(b) could be split into two paralleled $2{\cdot}R'_{\rm th}$, as shown in Fig. 4(c). The thermal capacitances provide the short circuit between top and bottom nodes during the transient process. Therefore, the relationship between real $R_{\text{th-jc-top}}$ (or $R_{\text{th-jc-btm}}$) and measured $R'_{\text{th-jc-top}}$ (or $R'_{\text{th-jc-btm}}$) is (3). It could be concluded that the $R_{\text{th-jc-top}}$ or $R_{\text{th-jc-btm}}$ is twice the measured $R'_{\text{th-jc-top}}$ or $R'_{\text{th-jc-btm}}$ by TDIM, respectively, (2) shown at the bottom of the next page:

$$\begin{cases} R_{\rm th-jc-top} = 2 \cdot R'_{\rm th-jc-top} \\ R_{\rm th-jc-btm} = 2 \cdot R'_{\rm th-jc-btm} \end{cases} \tag{3}$$

where $R_{\text{th-jc-top}}$ and $R_{\text{th-jc-btm}}$ are the real $R_{\rm th}$ of top and bottom sides, respectively, and $R'_{\text{th-jc-top}}$ and $R'_{\text{th-jc-btm}}$ are the measured $R_{\rm th}$ of top and bottom sides, respectively.

III. Verification by Transient Simulations

To further study the influence of cooling conditions and packaging structures on $R_{\rm th}$ of the DSC module, the electrothermal coupling transient model based on the finite element (FE) method is built. The structure and boundary conditions are shown in Fig. 5. The material properties in the electrical and thermal models are given in Table I. In the Ansys solver of electrical model, the solid current excitation with 100 A flows through the SiC DSC module, as shown in Fig. 5. The induced "ohmic loss" is delivered into the transient thermal model. To

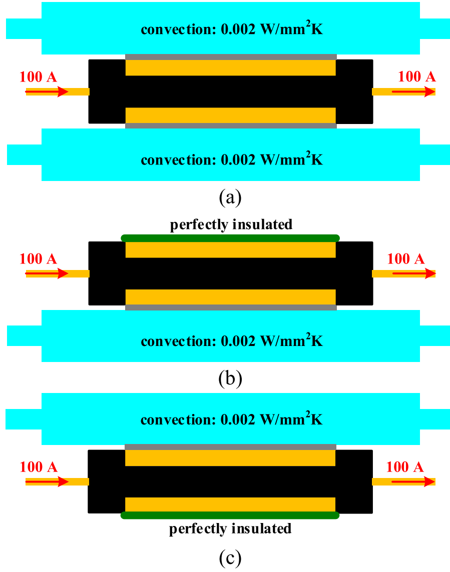

Fig. 5. Boundary conditions of FE simulation of DSC module under different cooling conditions. (a) DSC. (b) Bottom-side cooling. (c) Top-side cooling.

TABLE I
Electrical and Thermal Parameters of DSC Materials

Material	Electrical conductivity (S/m)	Thermal conductivity (W/m·K)	Specific heat (J/kg/K)
Al_2O_3	0	35	850
Al	3.8×10^7	238	951
Cu	5.8×10^7	400	385
SiC	277	370	800
Sinter layer	7×10^7	240	234
Wet TIM	0	6.5	2800
Dry TIM	0	0.65	1000

model the "wet" and "dry" conditions, the thermal conductivity of TIM layers between the DSC module and heatsinks is changed. Specifically, the thermal conductivity of wet and dry TIMs is given in Table I. The total simulation time is 100 s. The "heat generation" of conductive materials is imported from the electrical model. And, the convection coefficient with 0.02 W/mm^2·K is applied on top and bottom heatsinks. Since the junction temperature is highest in the whole module, the maximum temperature on the chip is extracted to analyze the Z_{th} of the SiC DSC model. The simulation results of Z_{th} curves are translated into structure function curves to determine the R_{th} of DSC module. The cooling conditions and packaging structures are changed to analyze their influences on the R_{th} values.

A. Influences of Cooling Conditions on Measured $R'_{th\text{-}jc}$

As mentioned above, various test conditions are performed in the $R_{\text{th-jc}}$ measurement. Therefore, DSC, bottom-side cooling,

TABLE II
Definition and Simulation Results of $R_{\text{TH-JC}}$

$R_{\text{th-jc}}$	Z_{th} curve	Cooling condition	Top TIM	Bottom TIM	Value (K/W)
$R_{\text{th-jc1}}$	Wet curve Dry curve	Double cooling Double cooling	Wet Dry	Wet Dry	0.327
$R_{\text{th-jc2}}$	Wet curve Dry curve	Double cooling Double cooling	Wet Wet	Wet Dry	0.313
$R_{\text{th-jc3}}$	Wet curve Dry curve	Bottom cooling Bottom cooling	/ /	Wet Dry	0.297
$R_{\text{th-jc4}}$	Wet curve Dry curve	Double cooling Double cooling	Wet Dry	Wet Wet	0.390
$R_{\text{th-jc5}}$	Wet curve Dry curve	Top cooling Top cooling	Wet Dry	/ /	0.379

and top-side cooling are modeled in the simulations, as shown in Fig. 5. The boundary condition of perfectly insulated is applied to achieve the thermal insulation. In each cooling conditions, the TIMs of top and bottom sides are changed to separate the structure function curves. Therefore, five types of $R_{\text{th-jc}}$ could be measured. The definitions of these $R_{\text{th-jc}}$ are given in Table II. The five conditions could explain the influences of cases in Fig. 2 on $R_{\text{th-jc}}$. The $R_{\text{th-jc1}}$, $R_{\text{th-jc2}}$, and $R_{\text{th-jc4}}$ represent the DSC condition in Fig. 2(a), while the $R_{\text{th-jc3}}$ and $R_{\text{th-jc5}}$ represent the SSC condition in Fig. 2(b).

By changing the cooling conditions and TIMs, the Z_{th} curves are calculated from the maximum temperature variations of the chips, as shown in Fig. 6. The legend denotes the cooling conditions and TIMs of top and bottom sides. The Z_{th} curves are translated into structure function curves, as shown in Fig. 7. According to [23], the separation point of wet and dry structure function curves is the "case" location. The cumulative ΣR_{thi} on x-axis is the corresponding $R_{\text{th-jc}}$. To find the exact separation point, the differences between wet and dry structure function curves ($\Delta\Sigma C_{\mathrm{thi}}$) are calculated, as shown in Fig. 8. The $R_{\text{th-jc}}$ is defined as the point where $\Delta\Sigma C_{\mathrm{thi}}$ clearly start to rise.

The point starting to rise is determined by the same baseline of $\Delta\Sigma C_{\mathrm{thi}}$ differential. The calculation results are given in Table II. There are two distinct $R_{\text{th-jc}}$ values, which are marked out in Fig. 8. The smaller $R_{\text{th-jc}}$ is derived from $R_{\text{th-jc1}}\sim R_{\text{th-jc3}}$, while the larger one is derived from $R_{\text{th-jc4}}\sim R_{\text{th-jc5}}$. The deviations among $R_{\text{th-jc1}}\sim R_{\text{th-jc3}}$ or $R_{\text{th-jc4}}\sim R_{\text{th-jc5}}$ result from the different slope of $\Delta\Sigma C_{\mathrm{thi}}$, as shown in Fig. 8. In addition, the smaller $R_{\text{th-jc}}$ is the $R'_{\text{th-jc-btm}}$ and the larger $R_{\text{th-jc}}$ is the $R'_{\text{th-jc-top}}$, according to the structure of DSC module in Fig. 1. It is means that the external cooling conditions of DSC module have no influence on $R'_{\text{th-jc-btm}}$ and $R'_{\text{th-jc-top}}$, which verifies the theory.

B. Influences of Packaging Structures on Measured $R'_{th\text{-}jc}$

According to the theoretical analysis, the $R_{\text{th-jc-top}}$ and $R_{\text{th-jc-btm}}$ determine the overall $R_{\text{th-jc}}$ distribution of the DSC

$$Z_{\mathrm{th}}(s) = \frac{1}{sC_{\mathrm{th-top1}} + \frac{1}{R_{\mathrm{th-top1}} + \frac{1}{sC_{\mathrm{th-top2}} + \frac{1}{R_{\mathrm{th-top2}} + \cdots}}} + sC_{\mathrm{th-btm1}} + \frac{1}{R_{\mathrm{th-btm1}} + \frac{1}{sC_{\mathrm{th-btm2}} + \frac{1}{R_{\mathrm{th-btm2}} + \cdots}}}} \quad (2)$$

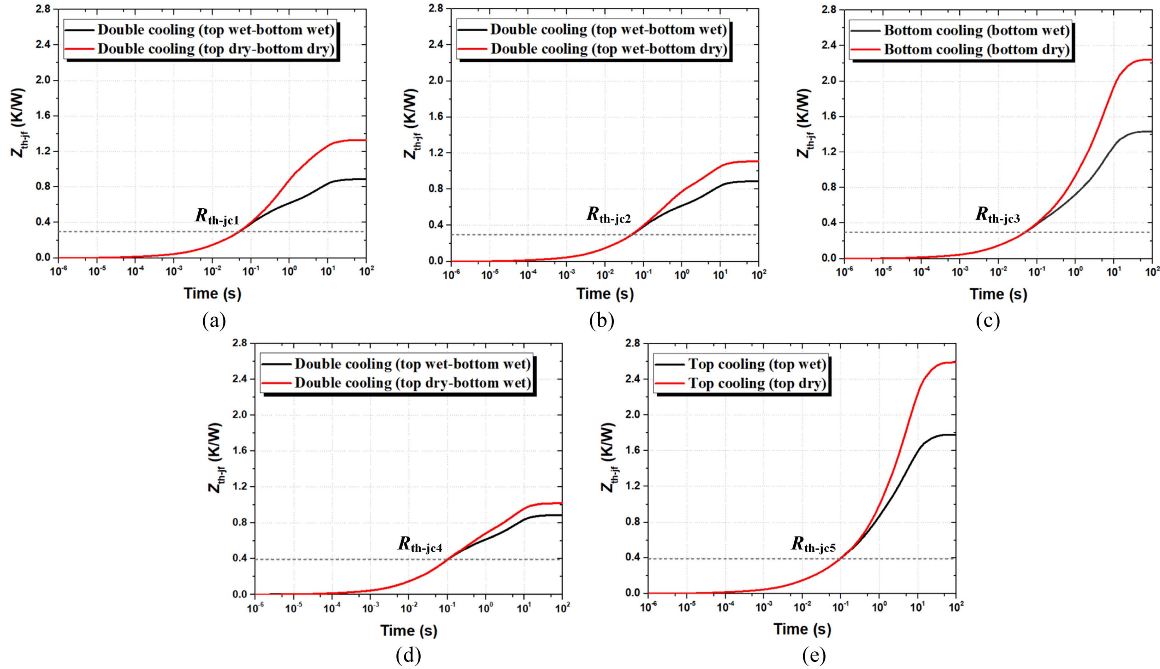

Fig. 6. Simulation results of $Z_{\rm th}$ under different cooling conditions and TIMs. (a) $R_{\rm th\text{-}jc1}$ determined by DSC with both top and bottom TIMs changed. (b) $R_{\rm th\text{-}jc2}$ determined by DSC with bottom TIM changed. (c) $R_{\rm th\text{-}jc3}$ determined by bottom-side cooling with bottom TIM changed. (d) $R_{\rm th\text{-}jc4}$ determined by DSC with top TIM changed. (e) $R_{\rm th\text{-}jc5}$ determined by top-side cooling with top TIM changed.

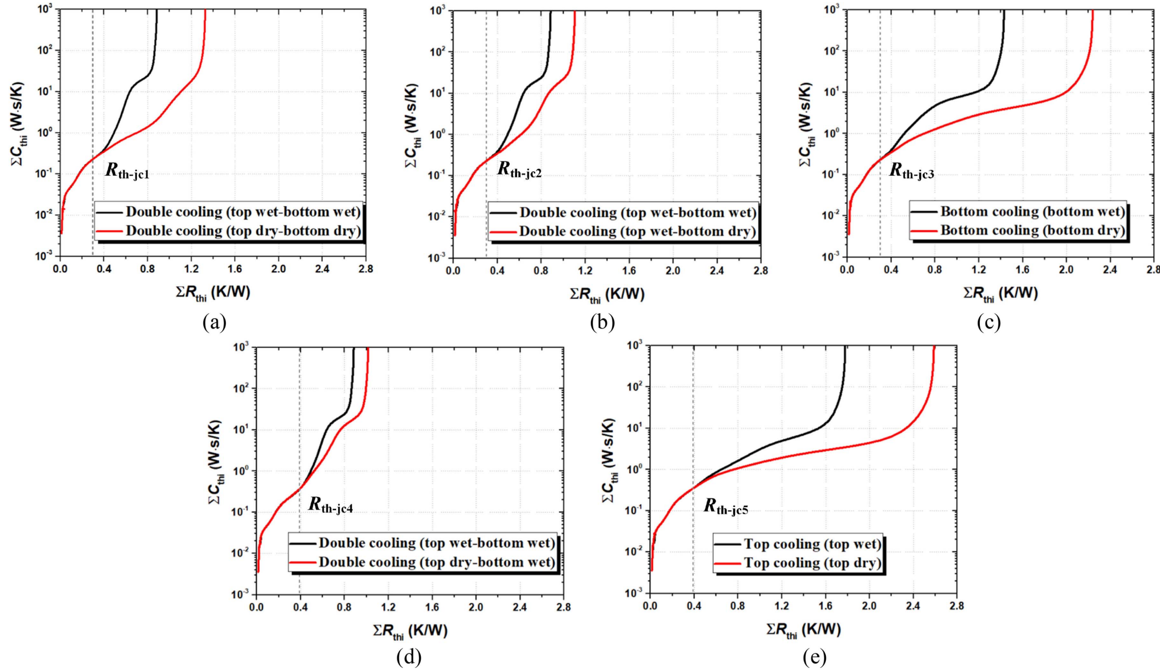

Fig. 7. Structure function curves calculated from simulated $Z_{\rm th}$ under different cooling conditions and TIMs. (a) DSC with both top and bottom TIMs changed. (b) DSC with bottom TIM changed. (c) Bottom-side cooling with bottom TIM changed. (d) DSC with top TIM changed. (e) Top-side cooling with top TIM changed.

module. Therefore, the structure of DSC module is changed in the simulations. Specifically, the layers from top heatsink to solder on the top side of chip are removed one by one until all eight layers are removed, as shown in Fig. 1. There are eight new structures. In each structure, bottom TIM is changed with TIM wet and TIM dry to study the influence on $R_{\rm th\text{-}jc\text{-}btm}$. The calculated $R_{\rm th\text{-}jc\text{-}btm}$ is labeled as $R_{\rm th\text{-}jc\text{-}btm1}$~$R_{\rm th\text{-}jc\text{-}btm8}$.

As the number of removed layers increases, the $Z_{\rm th}$ increases gradually, as shown in Fig. 9. This variation verifies the theory that the front *RC* network changes the $Z_{\rm th}$ curve early. Since the

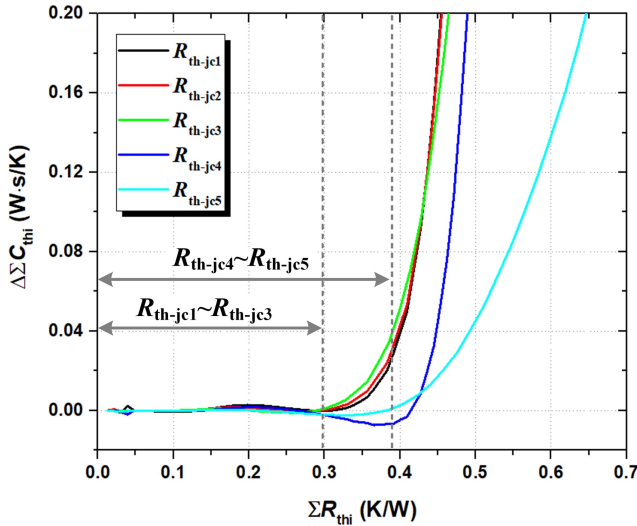

Fig. 8. Difference of wet and dry structure function curves under different cooling conditions in the simulations.

structure function describes the R_{th} distribution from junction to ambient, the top-side structure changes the shapes of Z_{th} curves and structure function, as shown in Fig. 10. Especially, the R_{th} near to junction changes greatly when the spacer in Fig. 1 is removed. The $R_{\text{th-jc-btm}}$ under eight structures is determined by calculating the $\Delta\Sigma C_{\text{thi}}$, which is marked out in Figs. 9–11. When the top-three layers: 1) heatsink; 2) TIM; and 3) copper, are removed, the $R_{\text{th-jc-btm1}}\sim R_{\text{th-jc-btm3}}$ are almost the same. The $R_{\text{th-jc-btm}}$ begins to increase when the number of removed layers is greater than 3, as shown in Fig. 11. It means that the $R_{\text{th-jc-btm}}$ is equivalent to the R_{th} from junction to somewhere of top ceramic. The $R_{\text{th-jc-btm8}}$ represents the $R_{\text{th-jc}}$ of SSC module with no layer on the top side. The values of $R_{\text{th-jc-btm1}}$ and $R_{\text{th-jc-btm8}}$ are 0.253 and 0.514 K/W, respectively. The $R_{\text{th-jc-btm8}}$ is approximately twice as high as $R_{\text{th-jc-btm1}}$. It could be concluded that the measured $R'_{\text{th-jc}}$ is just half of real $R_{\text{th-jc}}$, as explained in (3).

IV. Verification by Experiments

The device under test (DUT) is a customized SiC DSC module with half-bridge topology, as shown in Fig. 12. Three 1200V/98A SiC MOSFET chips are paralleled in high- and low-side bridge arm. The vertical structure is shown in Fig. 1. The detailed fabrication process and performance of the DUT have been revealed in [27]. In the test, only device of lower arm is evaluated to eliminate the influence of thermal coupling between high- and low-side devices.

Since the customized DSC module cannot be implemented in commercial R_{th} tester, the experimental platform is designed for R_{th} measurement, as shown in Figs. 13 and 14. The DUT is heated up to steady state by the current I_h. The value of I_h is adjusted to control the maximum junction temperature ($T_{j\max}$). The DUT is cooled by the water cooling system during the test. Since the auxiliary switch is used to control the current flow and protect the DUT, the rating current of the auxiliary switch should be much greater than that of the DUT to reduce the cooling requirement. The electric fan for cooling auxiliary switch is sufficient. Once the DUT achieves the steady state, the T_j measurement starts immediately. The gate signals and parameters sampled for Z_{th} calculation are controlled by micro-controller unit (MCU), DSP TMS320F28335. The detailed time sequence of MCU is shown in Fig. 14(b).

1) $t_1\sim t_2$*: Protection Delay:* During the turn-ON process, the turn-ON of DUT is 100 μs earlier than that of auxiliary switch to prevent DUT from high current stress.
2) $t_2\sim t_3$*: Heating Time:* The I_h flows through DUT until the electrical and thermal parameters achieve steady state, and 100 s is selected in the test. The voltage drop of DUT (V_{DS}) and I_h are sampled to calculate the power loss.
3) $t_3\sim t_4$*: Protection Delay:* During the turn-OFF process, the turn-OFF of DUT is 100 μs later than that of auxiliary switch to prevent DUT from high current stress.
4) $t_4\sim t_5$*: Cooling Time:* The I_h is removed. The DUT is cooled by the water cooling system. The temperature-sensitive electrical parameter (TSEP) method is used to capture the T_j variation.

Since the voltage drop of body diode of DUT under small current and $V_{GS} = -5$ V (V_{SD}) hardly degrades during the operation [28], [29], V_{SD} is used as TSEP. The sense current I_m with 15 mA is injected into body diode to generate the V_{SD}. The DUT is placed in heating chamber to calibrate the relationship between V_{SD} and T_j, which is shown in Fig. 15. The relationships of upper and lower devices between temperature and V_{SD} are almost the same and linear. There is recombination time with about 300 μs during transition from ON to OFF states. Therefore, the square root of time method is used to extrapolate the T_j during the recombination time [30], [31]. Considering the capacity and economy, the insulated gate bipolar transistor (IGBT) with 1200V/900A from Infineon is used as auxiliary switch.

In the test, the test conditions are changed, as given in Table II. To achieve thermal insulation, the nanoaerogel with thermal conductivity of 0.018 W/m·K and thickness of 10 mm is used. The "wet curve" is achieved by applying thermal grease with thermal conductivity of 6.2 W/m·K between module and heatsink. The air gap between module and heatsink is used as "TIM dry". The $R_{\text{th-jc}}$ is measured five times under each test conditions, to avoid the measurement errors.

Based on the measured results, the Z_{th} curves, structure function curves, and $\Delta\Sigma C_{\text{thi}}$ are calculated under different test conditions, as shown in Figs. 16–18. Compared with simulation results in Figs. 6–8, the steady-state $R_{\text{th-jf}}$ of practical module is lower due to the simulation simplification of fluid in water heatsink. However, the R_{th} distribution within module is similar with that of simulation results. Similar with simulation results, there are two distincts $R_{\text{th-jc}}$ that are marked out in Fig. 18. The test results verify the theory results and simulation results exactly. The external cooling conditions change the R_{th} far away from case, but have no influence on $R_{\text{th-jc}}$. The $R_{\text{th-jc}}$ deviations between test and simulation mainly result from the difference between ideal simulation parameters and immature packaging process.

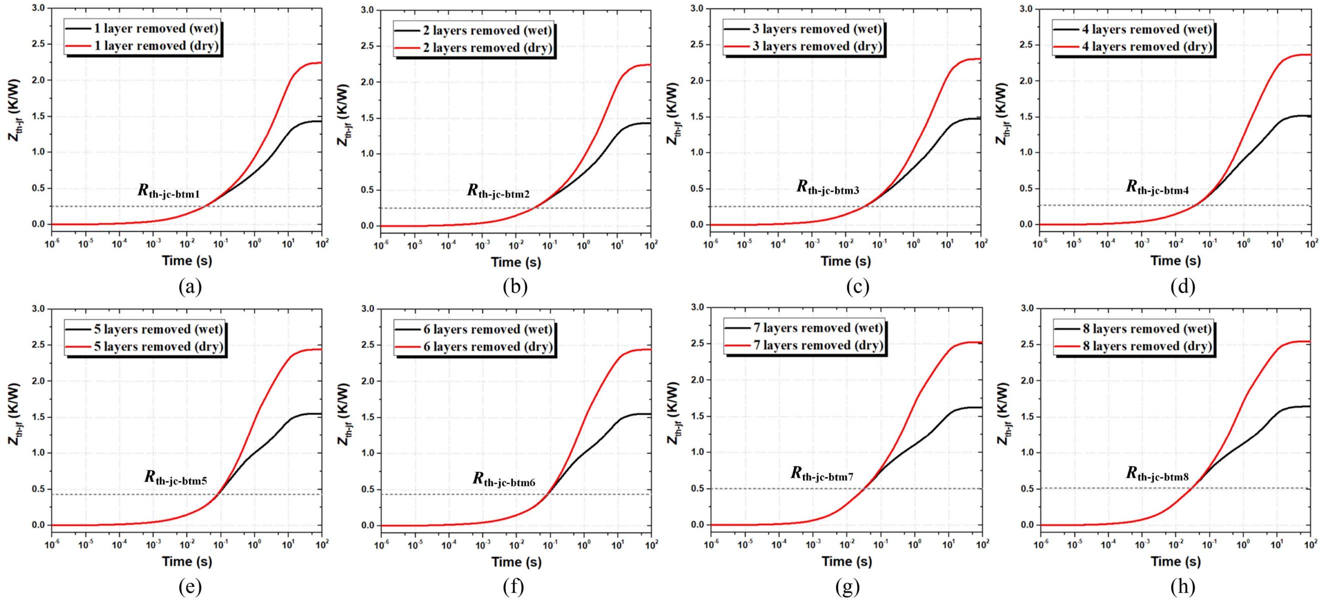

Fig. 9. Simulation results of $Z_{\rm th}$ under different top layer structures with bottom TIM changed. (a) One top layer removed. (b) Two top layers removed. (c) Three top layers removed. (d) Four top layers removed. (e) Five top layers removed. (f) Six top layers removed. (g) Seven top layers removed. (h) Eight top layers removed.

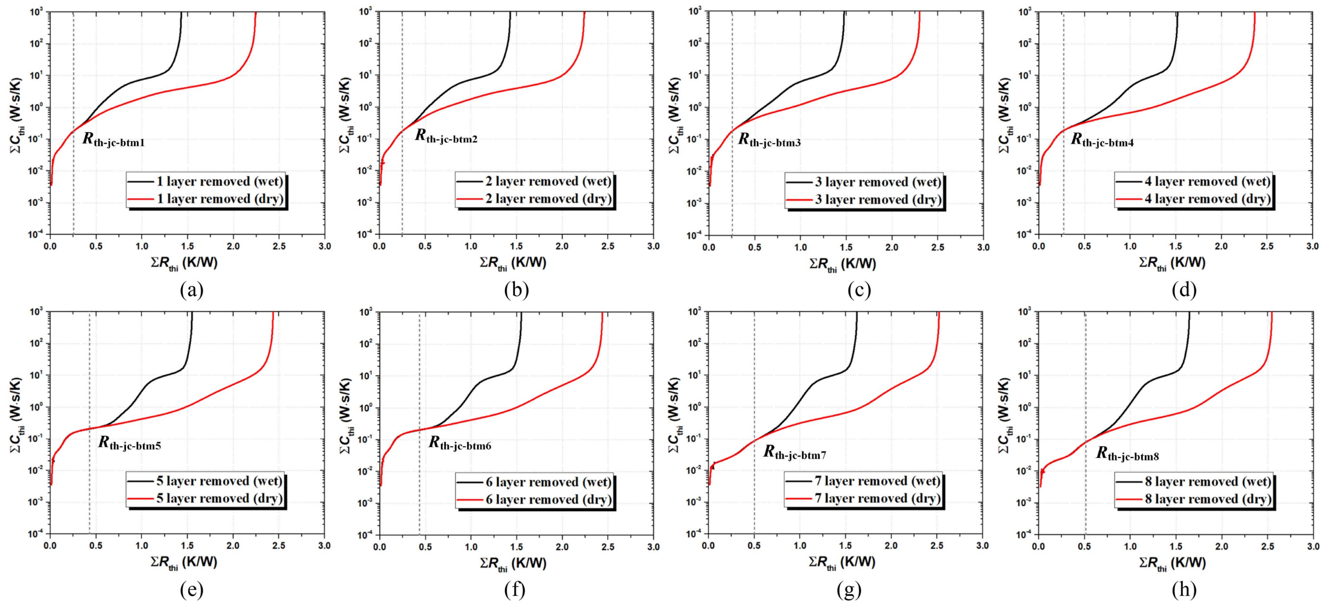

Fig. 10. Structure function curves calculated from simulated $Z_{\rm th}$ under different top layer structures with bottom TIM changed. (a) One top layer removed. (b) Two top layers removed. (c) Three top layers removed. (d) Four top layers removed. (e) Five top layers removed. (f) Six top layers removed. (g) Seven top layers removed. (h) Eight top layers removed.

From the abovementioned analysis, the $R_{\rm th\text{-}jc}$ of DSC module could be explained by Fig. 19.

1) When the $R_{\rm th\text{-}jc\text{-}btm}$ is smaller than $R_{\rm th\text{-}jc\text{-}top}$, the equivalent thermal circuit is Fig. 19(a). For $R_{\rm th\text{-}jc\text{-}btm}$, the changes of $R_{\rm th}$ from bottom case to fluid due to test conditions or structures cannot influence the value of $R_{\rm th\text{-}jc\text{-}btm}$. For $R_{\rm th\text{-}jc\text{-}top}$, the changes of $R_{\rm th}$ from top case to fluid cannot influence the value of $R_{\rm th\text{-}jc\text{-}top}$. The "Btm case" and "Top case" are the equivalent locations of cases. The "Btm case" is closer to the junction than the "Top case", due to $R_{\rm th\text{-}jc\text{-}btm} < R_{\rm th\text{-}jc\text{-}top}$.
2) The measured $R'_{\rm th\text{-}jc\text{-}btm}$ or $R'_{\rm th\text{-}jc\text{-}top}$ is half of real $R_{\rm th\text{-}jc\text{-}btm}$ or $R_{\rm th\text{-}jc\text{-}top}$, due to the paralleled $R_{\rm th}$.
3) When the $R_{\rm th\text{-}jc\text{-}top}$ is smaller than $R_{\rm th\text{-}jc\text{-}btm}$ (top layers are removed), the equivalent thermal circuit becomes Fig. 13(b). The "Top case" becomes the closest to the

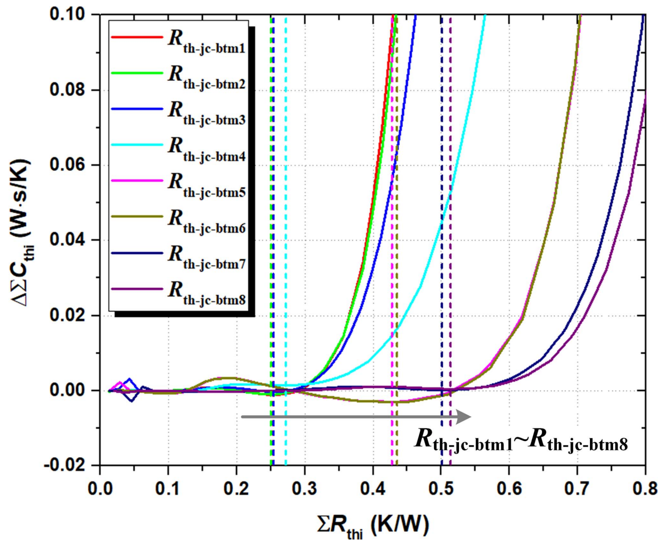

Fig. 11. Difference of wet and dry structure function curves under different top structures in the simulations.

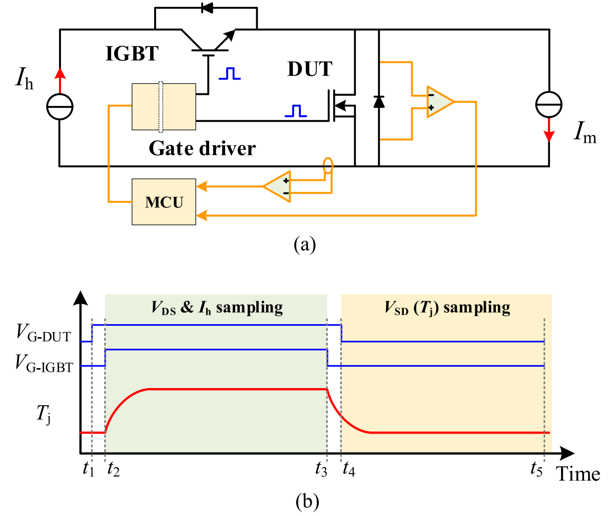

Fig. 14. Working principle of R_{th} measurement. (a) Equivalent circuit. (b) Time sequence of gate signals and T_j.

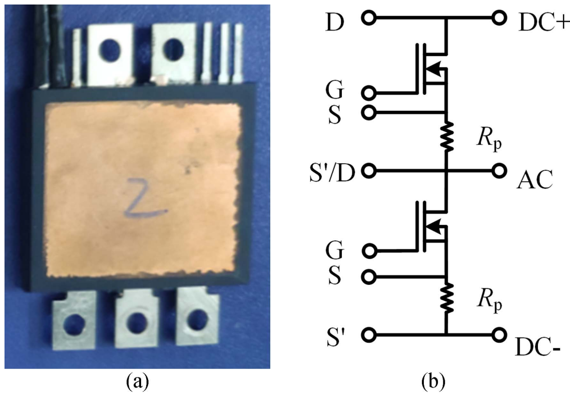

Fig. 12. SiC DSC module. (a) Top view. (b) Equivalent circuit.

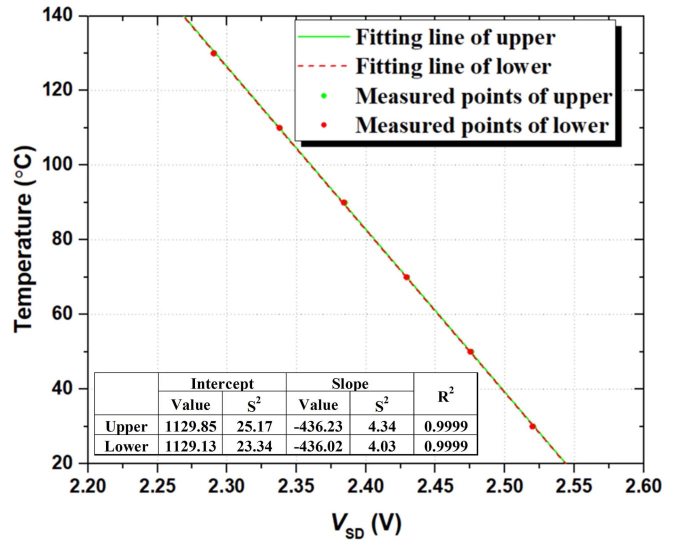

Fig. 15. Relationships of DUT between temperature and V_{SD}.

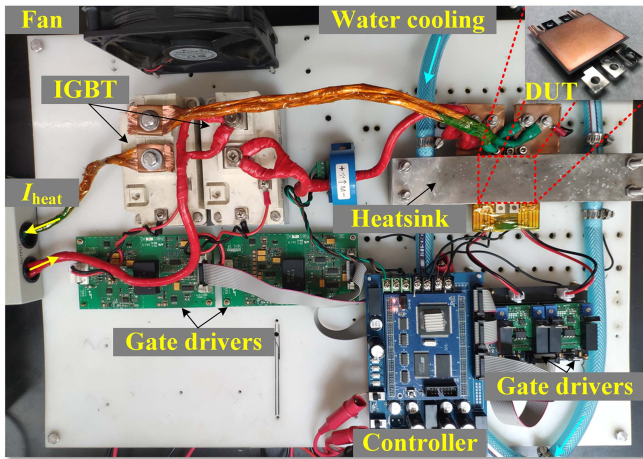

Fig. 13. Platform of R_{th} measurement.

junction instead of "Btm case". When all top layers are removed, $R_{th\text{-}jc\text{-}top}$ is zero. And, the $R_{th\text{-}jc\text{-}btm}$ becomes the $R_{th\text{-}jc}$ of SSC module.

4) The $R_{th\text{-}jc}$ near to junction ($R_{th\text{-}jc\text{-}N}$) and $R_{th\text{-}jc}$ far away from junction ($R_{th\text{-}jc\text{-}F}$) could be used as the definition of DSC module. The value of $R_{th\text{-}jc\text{-}N}$ is half of the smaller $R_{th\text{-}jc}$, while the value of $R_{th\text{-}jc\text{-}F}$ is the half of the difference between $R_{th\text{-}jc\text{-}top}$ and $R_{th\text{-}jc\text{-}btm}$. The new definition is critical in reliability evaluation. When the measured $R'_{th\text{-}jc\text{-}btm}$ increases during the aging test, it may be not necessarily the degradation of bottom materials. The R_{th} of top layer near to junction contributes to measured $R'_{th\text{-}jc\text{-}btm}$ as well, as shown in Fig. 10.

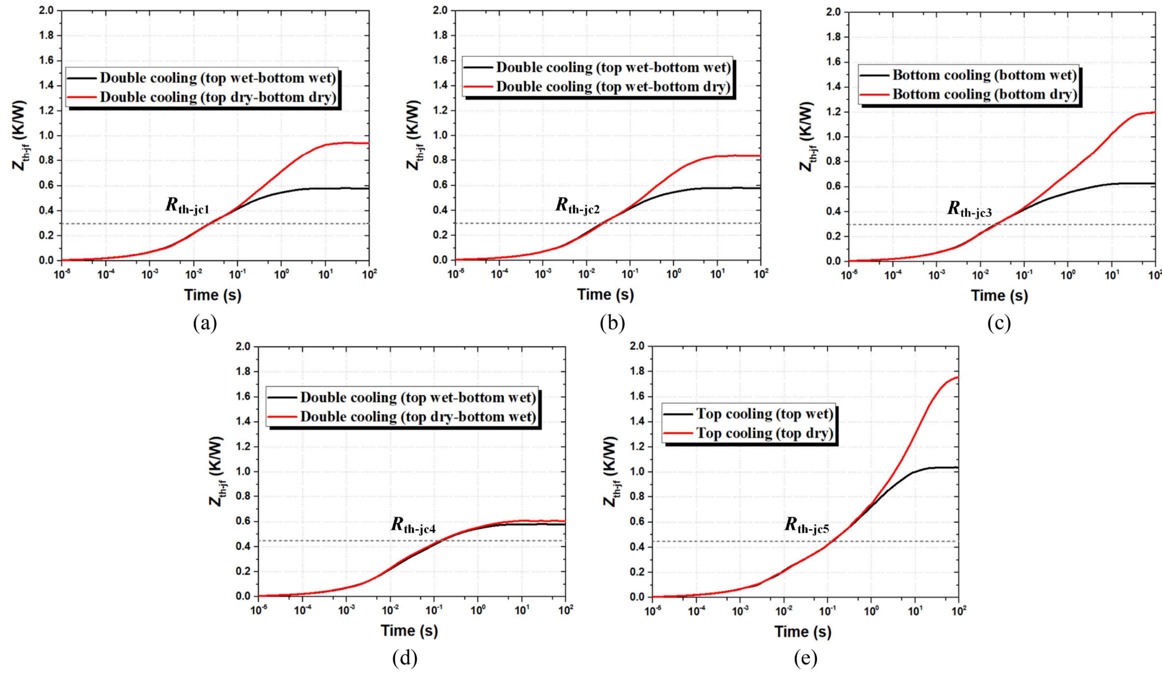

Fig. 16. Experimental results of Z_{th} under different cooling conditions and TIMs. (a) DSC with both top and bottom TIMs changed. (b) DSC with bottom TIM changed. (c) Bottom-side cooling with bottom TIM changed. (d) DSC with top TIM changed. (e) Top-side cooling with top TIM changed.

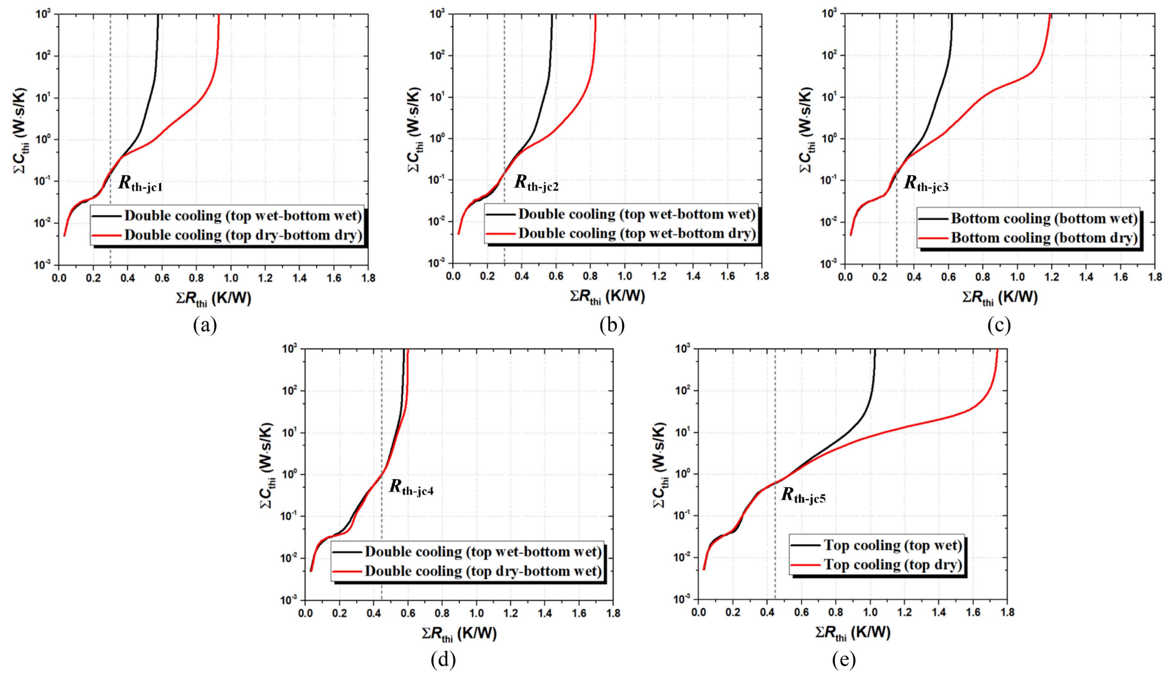

Fig. 17. Structure function curves calculated from measured Z_{th} under different cooling conditions and TIMs. (a) DSC with both top and bottom TIMs changed. (b) DSC with bottom TIM changed. (c) Bottom-side cooling with bottom TIM changed. (d) DSC with top TIM changed. (e) Top-side cooling with top TIM changed.

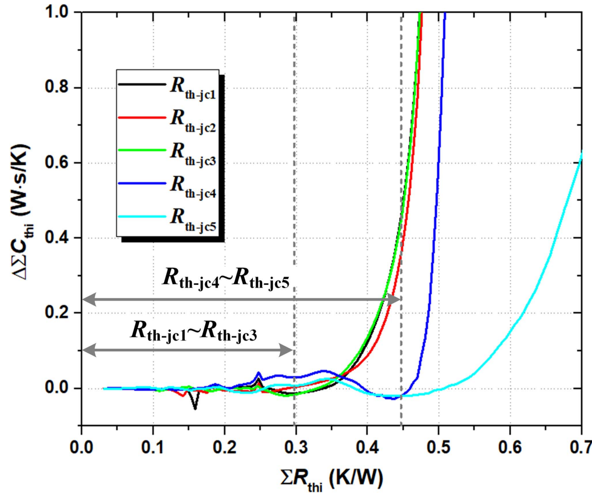

Fig. 18. Difference of wet and dry structure function curves under different cooling conditions in the experiments.

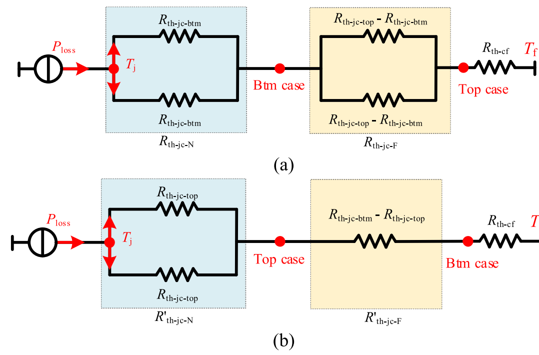

Fig. 19. Equivalent thermal circuit under different conditions. (a) $R_{\text{th-jc-btm}} < R_{\text{th-jc-top}}$. (b) $R_{\text{th-jc-btm}} > R_{\text{th-jc-Top}}$.

V. Conclusion

The asymmetric dual thermal paths of DSC module bring great uncertainty and challenge for thermal resistance evaluation. Through theoretical analysis and verification of simulations and experiments, the measurement mechanism of thermal resistance of DSC module through TDIM was analyzed comprehensively. The new discoveries and new definition about thermal resistance of DSC module are quite different from existing cognition.

The thermal insulator cannot block the power flow during the transient process due to the existence of thermal capacitance. It only affects the power loss and thermal impedance under steady state. Therefore, the external cooling conditions have no influence on thermal resistance from junction to bottom case and thermal resistance from junction to top case.

During the transient process of thermal impedance, the thermal capacitances dominate the thermal impedance. In addition, the top- and bottom-side thermal capacitances close to junction have the same value, forming the same transient power flows of top and bottom sides. Only single equivalent thermal path could be derived when TDIM is used. Therefore, the thermal resistances of top and bottom sides are paralleled from junction to case. In this case, the measured thermal resistance from junction to case is the half of the real value.

Since the measured thermal resistance includes the thermal resistance of top and bottom sides, the overall thermal resistance of DSC module could divided into thermal resistance near to junction and thermal resistance far away from junction. The new definition is more accurate for evaluating thermal resistance and reliability of DSC module.

In the future work, the new discoveries and definition method will be further verified in the reliability test, such as power cycling test.

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