Ultrafast Protection of Discrete SiC MOSFETs With PCB Coil-Based Current Sensors

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***Abstract*—Silicon carbide (SiC) MOSFETs offer significant advantages in terms of improved efficiency and reduced size of power electronic converters. However, they possess lesser short-circuit withstand time than silicon devices. An ultrafast short-circuit protection scheme for TO-247 packaged SiC MOSFETs is presented in this article. The protection scheme utilizes printed circuit board (PCB) coils to sense the rate of change of current through SiC MOSFETs in a half-bridge circuit. The PCB coils are fabricated near a single interconnect trace between the power device and the dc busbar. To ensure minimal intrusion inside the power-loop, the methodology of selecting the minimum trace length for a desired mutual inductance between the coil and the interconnect trace is presented through finite-element analysis. Experimental results for an SiC MOSFET subjected to a hard switched fault and a fault under load are presented, and the protection circuit response time under 25 ns is reported. Lastly, the peak current-mode control of a buck converter is implemented using the designed PCB coil-based sensor as current feedback sensor. Therefore, the PCB coil is demonstrated to be an effective alternative for Hall effect and magnetic core-based sensors in current control applications with dc/dc converters.**

***Index Terms*—Current sensor, finite element method (FEM), high frequency, power converter.**

I. Introduction

SILICON carbide (SiC) MOSFETs offer better performance than silicon insulated-gate bipolar transistor (IGBTs) owing to their excellent material properties. The ability to switch faster, operate at high junction temperature, and withstand high blocking voltage makes these devices suitable for a wide range of applications in electric vehicles and renewable energy technology [1], [2]. However, SiC MOSFETs possess lesser short-circuit withstand time than Si IGBTs, and consequently, their protection circuits should have lower response time than the state-of-the-art techniques for Si IGBTs [3].

Protection circuits based on high-bandwidth current sensors are effective for protecting SiC MOSFETs at ultrafast speeds [4]. Among several current sensing techniques [5], printed circuit board (PCB) Rogowski coil switch-current sensor (RSCS) is especially attractive owing to its high bandwidth, compact size, and ease of integration with power modules [6]. While many coil designs are proposed in the literature for protection of 62 mm and similar SiC MOSFET modules [7], [8], [9], [10], such a technique remains elusive for packages with a compact terminal pitch. Examples of these packages are discrete packages like TO-247-3 L, TO-247-4 L, TOLL, D2PAK, etc. Additionally, some module packages, e.g., EasyPack by Infineon [11], 45 mm and FM3 packages by Wolfspeed [12], [13], also have compact terminals leading to a small terminal pitch.

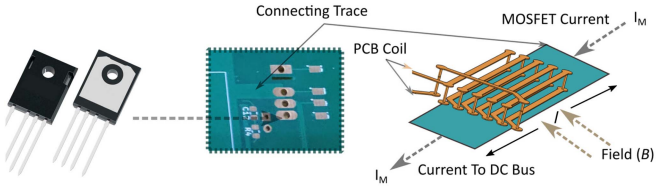

Fig. 1. A single interconnect trace-based PCB coil design. The region near the device terminals with the interconnect trace is shown zoomed. Magnetic field generated by the current flow in the trace causes flux linkages through the PCB coil.

For these devices, an equivalent method of sensing the device current is by placing PCB pickup coils on the power board to sense the field generated by PCB traces carrying the device current [14]. To create space for placement of the PCB coil, some solutions add external conducting elements to the power board [15], [16]. However, these solutions insert high inductance inside the power-loop, and their application is limited to characterization of the power device. A PCB coil design with a laminated busbar is presented in [17]. However, low current density on the busbars requires placement of a large-sized coil, which is detrimental to the power-loop inductance, sensor bandwidth, as well as the electromagnetic interference (EMI) performance of the PCB coil. PCB coils for small gallium nitride (GaN) packages are presented in the literature [18], [19], [20], [21]. However, such designs are not suitable for discrete SiC MOSFETs, where large-sized dc busbars are required.

A single interconnect trace-based PCB coil design is presented in this article with TO-247-4 L-packaged SiC MOSFETs. The interconnect, which connects the dc busbar with the SiC MOSFET terminal as shown in Fig. 1, produces the flux linkages with a PCB coil placed adjacent to the trace. Through this design, a mutual inductance of 0.175 nH per mm^3 of the PCB coil is achieved between the interconnect trace and the coil. This value, which is 44 times higher than the value with laminated busbar

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PCB coil design [17], signifies the efficacy of the presented design to extract high sensitivity with a compact coil size. The compact coil size not only minimizes intrusion inside the power-loop, but also results in a high natural frequency of 469 MHz. This frequency in turn facilitates high bandwidth capability of the designed current sensor, required for implementation of the ultrafast protection scheme.

In addition to the compact coil size, the coil design is directly linked to the length of the interconnect trace. Consequently, by controlling the trace length, two variables are controlled: 1) mutual inductance between the coil and the interconnect trace; and 2) the magnitude of power-loop stray inductance. These variables are mapped to the interconnect trace length through extensive three-dimensional finite-element method (3-D-FEM) simulations in COMSOL. Consequently, only the required interconnect trace length is selected based on the desired mutual inductance between the coil and the interconnect trace, thereby minimizing the power-loop stray inductance. Through the developed design methodology, a half-bridge circuit featuring PCB coils for current sensing of both the TO-packaged devices is demonstrated for the first time. The PCB coils are thereafter utilized for designing a protection circuit with a significant improvement in the response time from the existing state-of-the-art of 86 ns [7] to 25 ns.

The contributions in this article are summarized below.

1) A single interconnect-based PCB coil design is presented for discrete SiC MOSFETs. Power-loop stray inductance due to the interconnect trace and the mutual inductance between the trace and the PCB coil are mapped to a single design parameter, i.e., the trace length.
2) Ultrafast protection of discrete SiC MOSFETs is presented with the interconnect trace-based PCB coil design. Response time of the existing PCB Rogowski coil-based scheme is improved by 70% with the presented protection scheme. Error analysis of the fault adjustment circuit is carried out.
3) A dv/dt noise immunity test method for the PCB coil-based protection scheme is presented. Protection scheme is tested upto dv/dt of 120 V/ns for a discrete SiC MOSFET.
4) The peak current-mode control (PCMC) of a buck converter is implemented using the designed PCB coil-based sensor as current feedback sensor.

This article is organized as follows. Section II presents the PCB coil design on the half-bridge PCB. Section III presents design of the ultrafast protection circuit. The design of the integrator circuit is discussed, along with the methodology for selecting passive components in the protection circuit. Lastly, experimental results are given in Section IV. Section V concludes the article.

II. PCB Coil Design for a Half-Bridge Circuit

For a discrete device, a PCB coil design with dc busbars is presented in [17]. The design consists of embedding a coil inside the busbars of the power converter PCB to pick up the magnetic field produced by the device current flow. Large size of the dc busbars leads to low current density across it, necessitating placement of a large PCB coil inside the busbars to generate a coil output of sufficient sensitivity, as shown in Fig. 2. Further, the coil is placed near the dc bus away from the power device. For interfacing a PCB coil with the gate-driver circuit for implementation of an online overcurrent protection scheme, the coil should be placed near the power device [10].

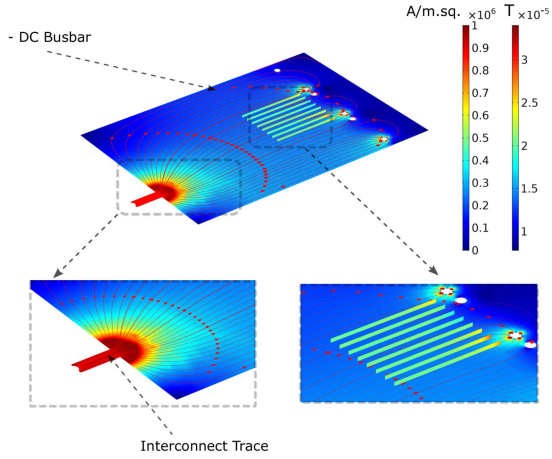

Fig. 2. Current distribution across the lower dc busbar and the device interconnect trace for a 1-A current flow through the power-loop. The streamlines corresponding to the current density vector are plotted in red.

These limitations are directly addressed with the single interconnect trace-based PCB coil design. Due to high current density on the interconnect trace as seen in Fig. 2, and hence the high magnetic field density surrounding it, size of the PCB coil required for a desired sensitivity is extremely small. The coil footprint for the design in [17] is $60 \times 30 \times 1.6$, while the size of the coil with a single interconnect trace is $8 \times 3.2 \times 0.7$, which is a reduction by a factor of 160.

Therefore, a miniaturized coil design is facilitated by selecting the interconnect trace for placement of the PCB coil. Owing to its miniaturized size and placement near the power device, coil output is directly interfaced with the gate-driver circuit and hence, facilitating the design of an ultrafast protection scheme for SiC MOSFETs. The direct interface shortens the connecting traces from the coil to the driver board, therefore, preserving the bandwidth and noise immunity of the sensor required for the ultrafast response of the protection scheme. The miniature size of the PCB coils facilitates their placement for both the devices in a half-bridge circuit. Hardware design of the PCB coils for the half-bridge circuit is now described.

The PCB coil design is demonstrated for the half-bridge circuit shown in Fig. 3(a). The PCB layout of the half-bridge circuit, on a four-layered PCB, is shown in Fig. 3(b). The MOSFETs are connected to dc busbars using two identical interconnect traces T_1 and T_2. Trace T_1 connects the positive dc bus (dc+) to the drain of top MOSFET (M_1) on the top-layer and trace T_2, shown zoomed in Fig. 3(c), connects the source terminal of bottom MOSFET (M_2) to the negative dc bus (dc$-$) on the bottom layer. Traces T_1 and T_2 carry the current through MOSFETs, M_1 and M_2, respectively. The embedded PCB coils pick up the magnetic field produced by current through these traces for sensing the device current. The design of the PCB coil is similar for both

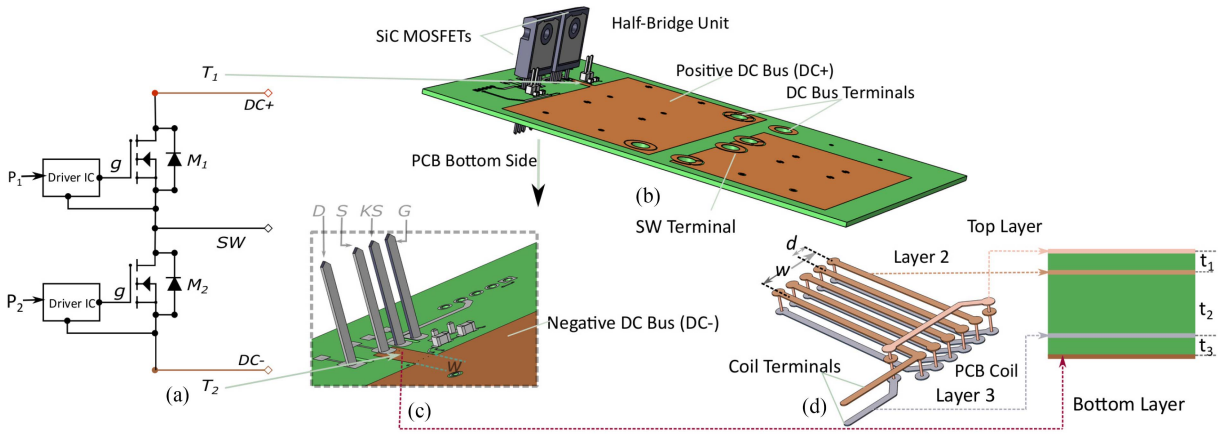

Fig. 3. SiC MOSFET-based half-bridge layout featuring embedded PCB coils. (a) Half-bridge schematic. (b) PCB layout. (c) Zoomed-in region near the source terminal of MOSFET M_2 on the bottom layer of PCB. (d) PCB coil implemented above trace T_2. Also shown is the PCB side view showing the arrangement of coil on the four-layered PCB. The dimensions are $t_1 = t_3 = 0.35$ mm, $t_2 = 0.7$ mm, $d = 0.8$ mm, and $w = 3.2$ mm.

the top and the bottom devices. Therefore, for simplicity, only the coil design for sensing current through M_2 is described.

Current from the source terminal of M_2 is routed through T_2 on the bottom layer of the half-bridge PCB, as shown in Fig. 3(c). The PCB coil is fabricated above T_2 with traces on the second and third layers of the half-bridge PCB. The traces are joined with buried vias to connect the turns forming the PCB coil, as shown in Fig. 3(d). The coil is, therefore, completely embedded within the half-bridge PCB. Further, the coil is placed such that its width overlaps trace T_2. In this way, the separation (t_3) between T_2 and the PCB coil is minimized, besides directly linking the placement of the coil to the interconnect trace. This separation is set by the PCB stack-up specification at 0.35 mm, which is significantly less than the minimum separation of 1.2 mm for the coil designed in [22]. Minimizing the separation between the PCB coil and T_2 increases the flux linkage per turn of the PCB coil. The buried coil facilitates placement of the coil near the power trace, resulting in an enhanced M, and therefore, coil sensitivity. However, the coil can be placed adjacent to the traces without the use of buried vias, resulting in a coil with lower sensitivity. While such a solution may be prudent for lowering the PCB cost, it will lead to higher stray inductance in the power-loop for obtaining a similar mutual inductance between the coil and the trace.

The lateral interturn separation between the coil turns, shown as d in Fig. 3(d), is limited by the PCB manufacturing technology. Consequently, the number of turns in the PCB coil, placed within the width (w) of T_2, is practically limited by d. While terminal dimensions of the TO-package constrain w, the length of the trace influences both the power-loop stray inductance and the mutual inductance between the PCB coil and the interconnect trace. Since these variables increase with the trace length, a minimum trace length is selected based on the desired mutual inductance between the PCB coil and the interconnect trace. Mapping of these variables to the interconnect trace length is carried out through FEM simulations. Description of the FEM model is given below.

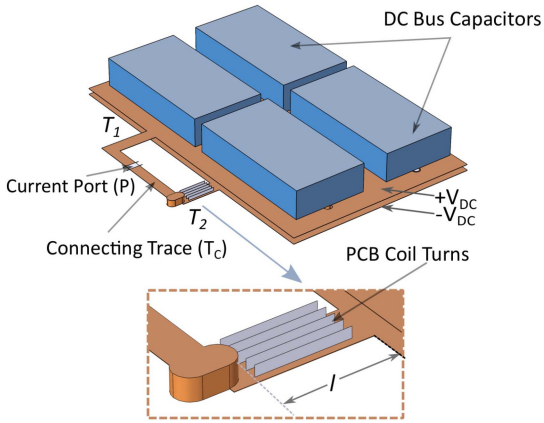

Fig. 4. FEM model of the half-bridge layout shown in Fig. 3.

Fig. 4 shows the FEM model of the half-bridge layout. To simplify the power-loop modeling, the current through the MOSFETs and the switching node trace, which connects the source of M_1 and the drain of M_2, is emulated via a single top-layer trace T_C as shown in Fig. 4. To complete the loop model, the dc bus capacitors shown in Fig. 4 are modeled as solid conductors for routing the current through dc busbars. In this manner, a continuous loop consisting of traces T_1, T_C, and T_2, and the dc busbars is formed. A current is injected through the loop by a current port (P) modeled inside the trace T_C. A magnetostatic FEM simulation is run to compute the magnetic field distribution (B) in the region of permeability μ surrounding the model due to the current flow (I_M) in the loop. The exterior boundary of this region, which spherically circumscribes the entire model shown in Fig. 4, is adjusted such that the magnetic field at the boundary has decayed substantially from its value near the loop. The loop inductance (L) is then estimated as

$$L = 2\left(\int_V \frac{B^2}{2\mu} dV\right) / {I_M}^2. \tag{1}$$

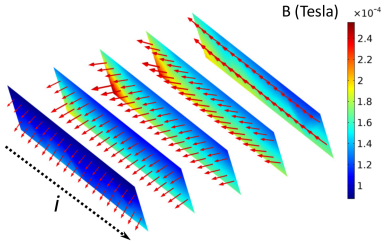

Fig. 5. Magnetic field distribution through the PCB coil with $I_M = 1$ A for $l = 8$ mm. Direction of magnetic field through the coil turns is indicated through arrows. Direction of current through the trace beneath the turns is also shown.

Furthermore, the magnetic field distribution (B) is used to compute the mutual inductance (M) between the trace T_2 and the PCB coil as

$$M = \frac{\lambda}{I_M} \tag{2}$$

where λ is the total flux linking the PCB coil. λ is computed through numerical integration of B over the surface area outlined by the traces forming the PCB coil. Each turn of the PCB coil is represented through an array of planar surfaces, as shown in Fig. 4. The elevation (t_3) of these surfaces above T_2, their lateral separation (d) and the height (t_2) are set according to the dimensions of the coil, as indicated in the caption of Fig. 3. As an illustration, the magnetic field distribution (B) through each turn of the PCB coil is shown in Fig. 5 for $I_M = 1$ A with the trace length set to 8 mm.

It can be observed that increasing the length (l) of T_2 can facilitate a coil design with larger turn area. A larger coil will have a higher mutual inductance with T_2 and hence higher sensitivity as well. However, increasing l also increases the inductance of the power-loop, which is detrimental toward high-speed operation of SiC MOSFETs. The loop inductance is estimated for $l = 2, 4, 8$, and 12 mm using (1). Both T_1 and T_2 are adjusted simultaneously to these lengths in the FEM model. Corresponding to each length, the mutual inductance is also estimated using (2).

For all the trace lengths, loop inductance (L) and the mutual-inductance (M) between the coil and T_2 are plotted in Fig. 6(a) and (b), respectively. L exhibits a slope of 1.58 nH/mm based on the linear fit through the data shown in Fig. 6(a). Since increase in L is purely due to the increased length of traces T_2 and T_2, the trace inductance ($L_T = 1.58\,l$) is estimated from this slope, as shown in Fig. 6(b). L_T includes the stray inductance contributed by both T_1 and T_2.

To minimize the power-loop inductance for designing a coil with any desired M, the minimum required length of the interconnect trace can be selected from Fig. 6(b). An approach for selecting an appropriate M for any intended application is now described. Such an approach removes the limitation of existing PCB coil designs [15], [16], [17], which is the arbitrary increase of stray inductance in the power-loop for designing a coil of desired sensitivity. Consider the error in the sensor output due to the op-amp input offset voltage (V_{OS}) [23]. As shown in the next section, the error in the sensor output due to V_{OS}, when

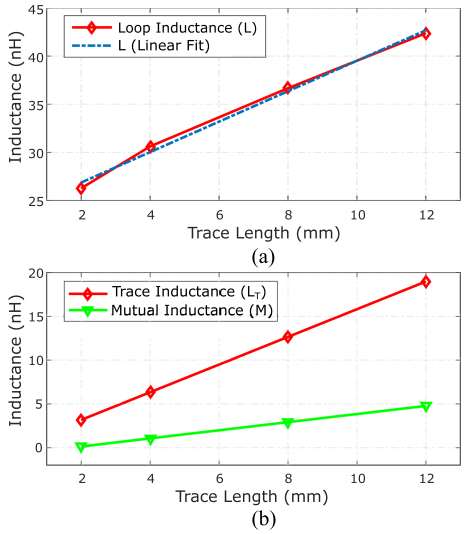

Fig. 6. (a) Variation of loop inductance (L) with trace length l. (b) Variation of mutual inductance (M) between the PCB coil and T_2 and trace inductance (L_T) with trace length l. All estimated parameters correspond to the trace width (w) of 3.2 mm.

measuring a steady-state device current I_M, is expressed as

$$E_{OS} = \frac{V_{OS} t}{M I_M} \tag{3}$$

where t is the duration from the instant when the power device is turned ON. The error increases once the device starts conducting and reaches its maximum value just before the device is turned OFF, after which the integrator is reset. For keeping the error below 5% when the device conducts a current of 20 A for 10 μs, for an op-amp with a typical offset voltage of 260 μV, the minimum M required is around 2.6 nH. Therefore, based on the intended application and the nature of components used in the analog circuitry, a base minimum value can be found for the mutual inductance. By selecting the minimum M needed, only the required length of interconnect trace is used, thereby minimizing the power-loop inductance. For the prototype presented in this article, the trace length is set at 8 mm, which gives a mutual inductance of 2.9668 nH between the trace and the PCB coil. The methodology for processing the designed PCB coil output for implementation of the ultrafast protection scheme is discussed in the next section.

III. Ultrafast Protection Circuit Design

The gate driver circuit featuring ultrafast protection is shown in Fig. 7(a). The circuit is fabricated as a PCB card, shown in Fig. 7(b). Once connected to the main half-bridge board, the gate driver card receives the PCB coil output for further processing. The voltage induced by the device current (I_M) across the PCB coil is expressed as

$$V_C(t) = M \frac{dI_M(t)}{dt}. \tag{4}$$

The coil output voltage (V_C) is integrated on the gate driver card to produce a voltage (V_S), which is proportional to I_M.

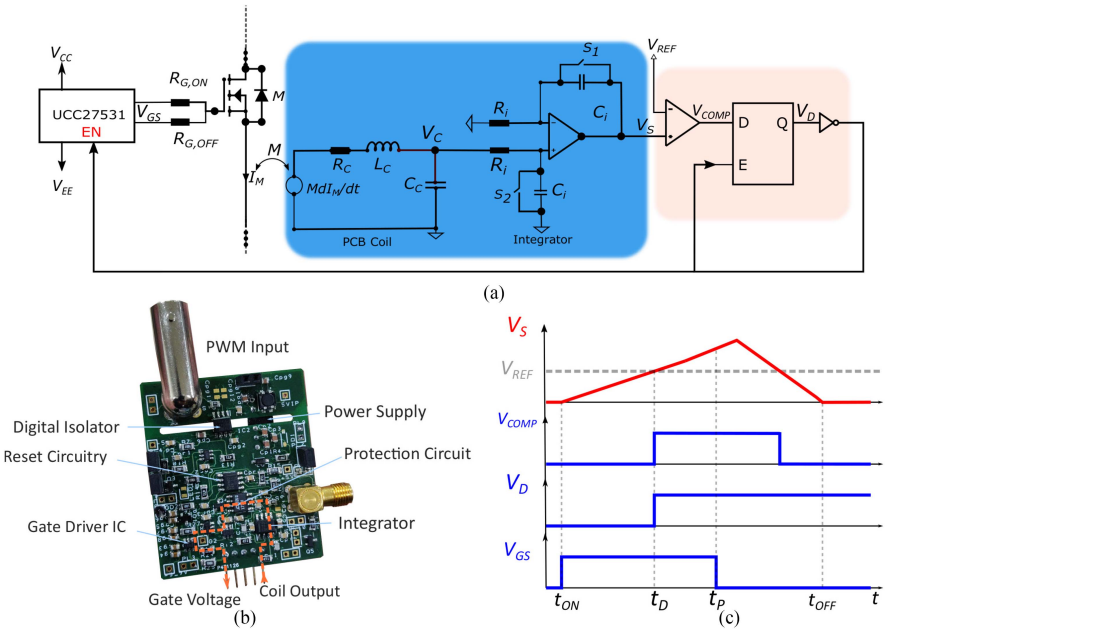

Fig. 7. (a) Gate driver schematic featuring the integrator and the protection circuitry. (b) PCB card implementing the gate driver schematic. (c) Simplified waveforms depicting the functioning of protection circuitry.

Integration is implemented using an analog integrator circuit configured in a noninverting topology [23], as shown in Fig. 7(a). A high-speed comparator compares V_S with a fault reference voltage V_{REF}. As will be discussed subsequently, V_{REF} can be set corresponding to any desired fault current level I_{REF}. Once the fault is detected, the comparator output goes high at the instant t_D shown in Fig. 7(c). This output is then latched and inverted before feeding it to the driver IC for disabling its output (V_{GS}), which occurs at the instant t_P shown in Fig. 7(c).

Having discussed the design of the PCB coil in the preceding section, the next step for implementation of the protection scheme is the design of the integrator and the logic circuit shown in Fig. 7(a). In this section, first, an expression for the current sensor frequency response is developed, which includes the influence of nonideal op-amp characteristics. The frequency response, validated through LTspice simulations, establishes the requisite high bandwidth current sensing capability of the PCB coil-based current sensor. Thereafter, fault level adjustment for the protection circuit is discussed.

A. Current Sensor Design

The current sensor, comprising the PCB coil as well as the integrator circuit, must have sufficient bandwidth for tracking switching current through an SiC MOSFET. The upper bandwidth limit (BW) [19] required to sense device current with a rise time t_r (us) is

$$\text{BW (MHz)} = \frac{0.35}{t_r}. \tag{5}$$

For commercially available SiC MOSFETs, di/dt as high as 5.79 A/ns is reported [24]. Therefore, the MOSFET current can rise quickly in the event of a short-circuit. From (5), sensing the device current with a typical rise time of 10 ns requires a current sensor bandwidth above 35 MHz. To determine the upper BW of the designed PCB coil based current sensor, the parameters in the lumped model of the PCB coil, shown in Fig. 7(a), are first extracted using a 3-D FEM simulation. A variable frequency current signal is injected through the terminals in the 3-D model of the designed PCB coil shown in Fig. 3(d), and the corresponding terminal voltage is computed. With the terminal current and voltage known, the impedance at the coil terminals is computed. The reactive part of that impedance is plotted in Fig. 8. The reactive impedance in the low-frequency region, shown zoomed in Fig. 8, is used to estimate the lumped inductance (L_C) of the PCB coil. Further, from the coil resonant frequency (f_r), the coil lumped capacitance (C_C) is estimated as

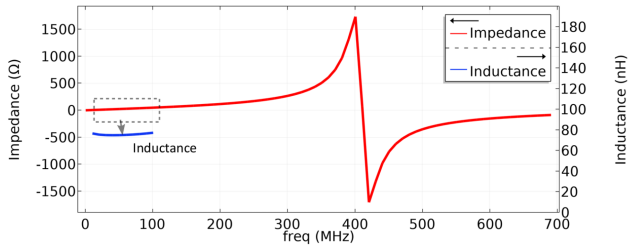

Fig. 8. Frequency response of the PCB coil. The response includes the influence of the connecting trace from the PCB coil to the integrator circuit.

$$C_C = \frac{1}{(2\pi f_r)^2 L_C}. \tag{6}$$

The extracted parameters of the PCB coil are listed in Table I. With these parameters, the transfer function for the coil ($C(s)$)

TABLE I
COIL PARAMETERS

Element	Magnitude
Inductance (L_C)	73.24 nH
Resistance (R_C)	0.31 Ω
Capacitance (C_C)	2.04 pF
Mutual inductance (M)	2.97 nH
Coil resonant frequency (f_r)	411.43 MHz

is expressed as

$$C(s) = \frac{V_C(s)}{I_M(s)} = \frac{Ms\,(1 + R_iC_is)}{Z(s)} \tag{7}$$

where

$$Z(s) = R_iC_iL_cC_cs^3 + (R_cC_cR_iC_i + L_cC_i + L_cC_c)s^2 + (R_iC_i + R_cC_c + R_cC_i)s + 1. \tag{8}$$

A practical integrator model ($I_P(s)$) [25], using an op-amp with finite open-loop gain (a_0) and a finite unity gain-bandwidth (ω_t), is expressed as

$$I_P(s) = \frac{V_S(s)}{V_C(s)} = \frac{a_0}{\left(1 + \frac{s}{\omega_0/a_0}\right)\left(1 + \frac{s}{\omega_t}\right)} \tag{9}$$

where

$$\omega_0 = \frac{1}{R_iC_i} \tag{10}$$

is the unity gain frequency. From (7) and (9), the sensor transfer function ($T(s)$) can be expressed as

$$T(s) = I_P(s)C(s) = \frac{a_0Ms\,(1 + R_iC_is)}{Z(s)\left(1 + \frac{s}{\omega_0/a_0}\right)\left(1 + \frac{s}{\omega_t}\right)}. \tag{11}$$

Using (11), the sensor frequency response ($T(j\omega)$) is plotted for $R_i = 470\,\Omega$ and $C_i = 0.1$ nF, as shown in Fig. 9(a). The model derived in (11) is derived using a lumped model of the Rogowski coil. Therefore, the model is valid only upto the first resonant frequency of the coil [26]. $T(j\omega)$ is plotted for a commercially available op-amp (THS4631) with a_0 and f_t as 80 dB and 325 MHz, respectively. $T(j\omega)$ is also plotted through an LTspice simulation using manufacturer-provided spice model of THS4631 in Fig. 9(b). The frequency response in Fig. 9(b) exhibits a larger gain roll-off at high frequency, which can be attributed to higher order poles included in the manufacturer spice model. Irrespective of the roll-off at high frequencies, it is observed that the measurement requirement of 35 MHz for a rise time of 10 ns is well within the flat response region of the frequency response.

B. Fault Level Adjustment

After ignoring the coil parasitic inductance and capacitance, the sensor output voltage (V_S) is simply expressed as

$$V_S(t) = \frac{Mi_M(t)}{R_iC_i}. \tag{12}$$

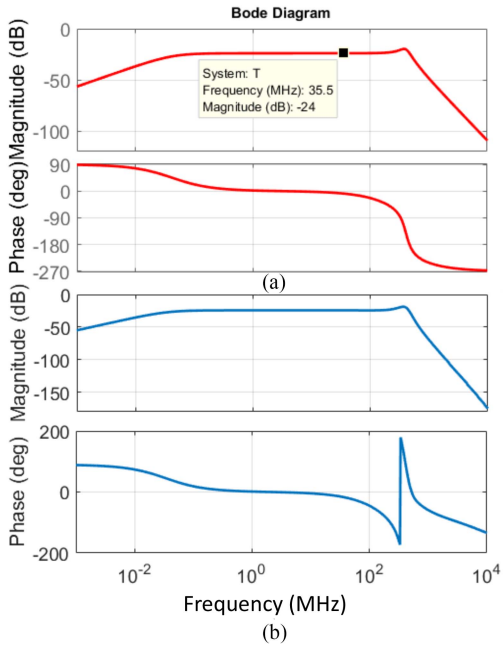

Fig. 9. Current sensor frequency response. (a) Sensor frequency response using the derived model ($T(j\omega)$). (b) Sensor frequency response generated through LTspice simulation.

Using the expression in (12) for adjustment of V_{REF} is justified since the frequency response ($T(j\omega)$) of the sensor ensures adequate bandwidth to track switching current transitions through the MOSFET. Therefore, the reference voltage (V_{REF}) for the comparator shown in Fig. 7(a), corresponding to fault current (I_{REF}), is adjusted as

$$V_{\text{REF}} = \frac{MI_{\text{REF}}}{R_iC_i}. \tag{13}$$

To avoid false triggering of the protection circuit, the error in the sensor output due to nonideal circuit components can be estimated beforehand. Generally, the error (dz) in $z = f(x_1, x_2, \ldots x_n)$ due to uncertainty in $x_1, x_2, \ldots x_n$ is expressed as

$$dz = \sqrt{\left(\frac{\partial F}{\partial x_1}\right)^2 dx_1^2 + \left(\frac{\partial F}{\partial x_2}\right)^2 dx_2^2 + \cdots \left(\frac{\partial F}{\partial x_n}\right)^2 dx_n^2}. \tag{14}$$

Using (14), the error in the sensor output (12) due to uncertainty in the value of R_i, C_i is expressed as

$$\frac{dV_S}{V_S} = \sqrt{\left(\frac{dR_i}{R_i}\right)^2 + \left(\frac{dC_i}{C_i}\right)^2}. \tag{15}$$

Since the component datasheets specify the uncertainty values, the expression in (15) can be used to set V_{REF} while accommodating any error in the sensor output. Another source of error for the integrator circuit is the op-amp input offset voltage (V_{OS}) [23]. Besides the expression in (12), the sensor output also contains an error term due to integration of V_{OS} and is

expressed as

$$V_S(t) = \frac{Mi_M(t)}{R_iC_i} + \frac{V_{OS}t}{R_iC_i} \tag{16}$$

where t is the duration from the instant when the power device is turned ON. The expression for the sensor error due to V_{OS} in (3), therefore, follows from (16). The error in the sensor output due to V_{OS} during hard switched fault (HSF) is negligible, as the fault occurs just after the device is turned ON and no significant accumulation of error has occurred. However, the error can be significant during FUL where the fault can occur during normal conduction of the device. Moreover, the error can be significant for high-inductance faults, where the fault current rises slowly after the device is turned ON. As such, V_{REF} can be adjusted appropriately based on V_{OS} of the op-amp and the inductance of the circuit.

Gate driver circuits with PCB Rogowski coil-based SC protection have been demonstrated to possess dv/dt immunity above 100 V/ns [7]. This immunity is facilitated by the absence of displacement currents due to diode junction capacitances, which exist with the DESAT-based protection circuits [27]. With only weak parasitic coupling between the PCB coil and the switch node, the PCB coil-based technique offers high immunity to dv/dt generated by fast-switching SiC MOSFETs [28]. The miniature size of PCB coil and its placement above the interconnect trace ensure adequate separation between the coil and the switch node, and hence minimizes the parasitic capacitance between them.

The noise immunity of the gate driver with RSCS-based protection is studied in [7] in terms of the common mode noise current injected through the isolation barrier via the gate driver power supply path. Moreover, the influence of high dv/dt on the gate driver power supply rail is investigated in [7]. In this article, a test method is presented to investigate the noise immunity of the protection scheme by measuring the component of sensor output (V_S) contributed exclusively by the switch node dv/dt. Therefore, when V_{REF} is adjusted to include this component in sensor output, at the highest dv/dt of 120 V/ns, false triggering of protection circuit is avoided. The test methodology is elaborated in the next section.

IV. Experimental Results

The developed half-bridge prototype is shown in Fig. 10. The half-bridge circuit employs two UnitedSiC SiC cascode devices (UF3C120080K4S). While the experimental results are demonstrated with a cascode device, the protection scheme possesses equal efficacy for any SiC MOSFET due to its current detection mechanism. The gate driver card, shown in Fig. 7(b), is shown connected to the half-bridge board in Fig. 10. The driver IC (TI UCC27531) used in the driver card is a simple nonisolated IC that provides sufficient peak current for driving a discrete SiC MOSFET. Isolation from the control ground is provided through a digital isolator (TI ISO7710) having high common-mode transient immunity. A high-speed comparator (LT1719) is used in the protection circuit to minimize propagation delay. Further, all the components on the driver card are powered by a single

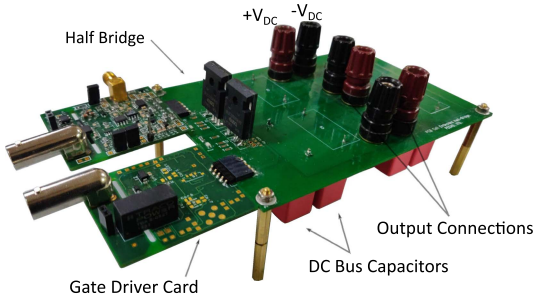

Fig. 10. Developed half-bridge prototype. The gate driver card is shown externally connected to the half-bridge board.

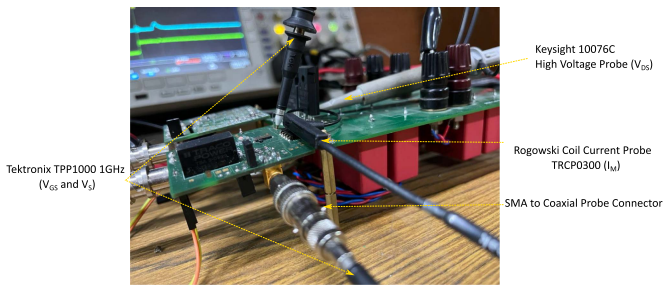

Fig. 11. Experimental setup. The probes used for measuring the current and voltage waveforms are marked along with their description.

2-W power supply (TBA 2-0522). Both the integrator op-amp (THS4631) and the comparator (LT1719) are powered with a bipolar voltage supply (± 5 V) generated on the driver card from the output of TBA 2-0522. The bipolar supply ensures that the sensor can track current of either polarity through the device, when it is turned ON. The experimental setup is shown in Fig. 11.

In this section, first, results from the experiments performed on the current sensor are presented. Second, results from HSF and fault under load (FUL) tests on the SiC MOSFET are presented. Lastly, results demonstrating cycle-by-cycle peak current limit for the power device in a buck converter are presented.

A. Current Sensor Evaluation

A 580-μH inductor is connected between dc+ and SW terminals shown in Fig. 3(a). Further, MOSFET M_2 is driven by four consecutive gating pulses, which results in four current pulses through the device. A TRCP0300 probe from Tektronix is used to evaluate the performance of the designed current sensor when measuring these current pulses, as shown in Fig. 12. Both the sensor measurement (V_S) and the Tektronix probe measurement (I_M) are shown in Fig. 12. From Fig. 12, it is observed that the sensor can track the rising and falling current transitions through the SiC MOSFET with the required bandwidth.

The mutual inductance between the trace T_2 and the PCB coil can be estimated from Fig. 12(b) at the instant when the device current reaches its steady state after it is turned ON. Device current of 15 A is seen to produce a sensor output voltage of 1 V. Consequently, for $R_i = 470\,\Omega$ and $C_i = 0.1$ nF, M is estimated to be 3.13 nH using (12), which is near the value

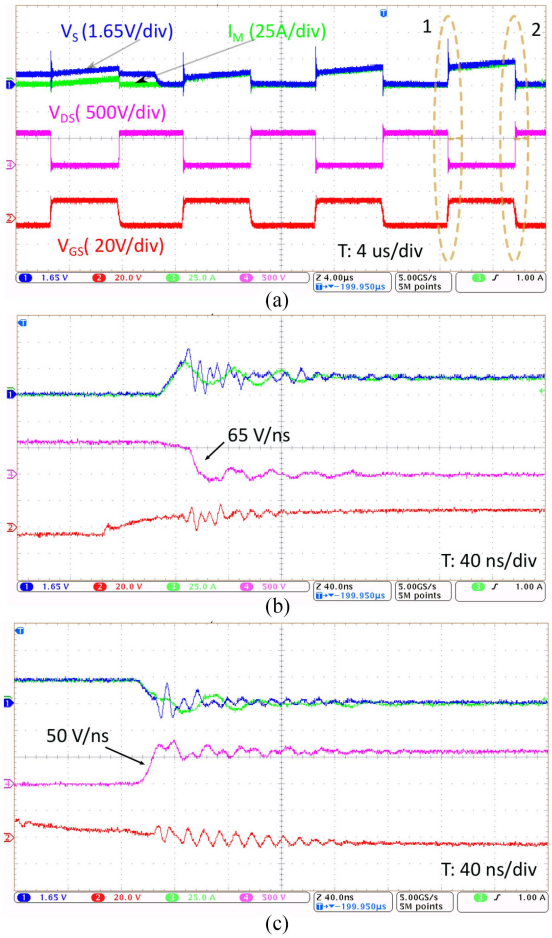

Fig. 12. (a) Pulse test results showing the device current measurement using the designed current sensor (V_S) as well as a commercial probe (I_M). (b) Turn-ON transition waveforms at the instant marked 1 in (a). (c) Turn-OFF transition waveforms at the instant marked 2 in (a).

(2.9668 nH) estimated from FEM simulations in Section II. This experimentally determined value of M is utilized for adjusting the reference fault level of the protection circuit. The resonant frequency of the coil is measured to be 469 MHz, which is higher than the simulated value (416 MHz). The difference can be attributed to the variation in the permittivity of the manufactured PCB and the permittivity considered for the FEM model.

Logic of the pulses which drive the MOSFET gate is utilized by an external reset circuit to remove any accumulated offset in the sensor output with switches S_1 and S_2 shown in Fig. 7(a). The reset occurs during the MOSFET turn-OFF period, as seen in Fig. 12(a) after the first gating pulse arrives. Thereafter, by periodically resetting the integrator capacitors, when the device is turned OFF, accumulation of offset in the sensor output is prevented.

B. Hard Switched Fault and Fault Under Load

Fig. 13 shows the half-bridge circuit and the gating pulse logic for conducting SC tests on the DUT, M_2. For conducting HSF, M_1 is first turned ON by issuing a single gate pulse and t_f interval afterwards, M_2 is switched ON as shown in Fig. 13(b).

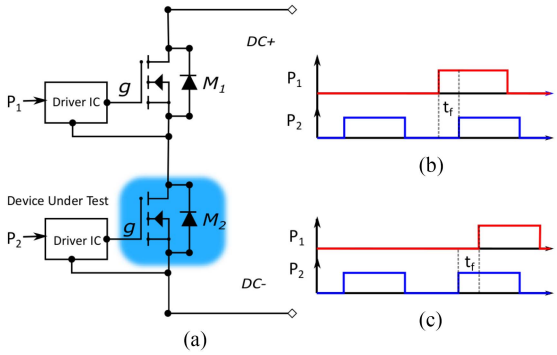

Fig. 13. (a) Half-bridge test setup showing the device under test (DUT) M_2. (b) Gate logic for conducting HSF test. (c) Gate logic for conducting FUL test.

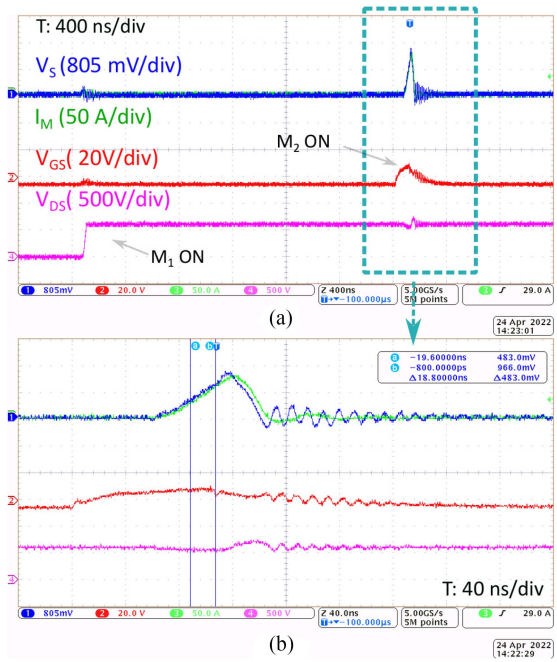

Fig. 14. (a) Experimental results demonstrating the protection of the device M_2 subjected to a HSF with $R_i = 2\,\text{k}\Omega$, $C_i = 0.1$ nF, $V_{\text{REF}} = 500$ mV, and $I_{\text{REF}} \approx 32$ A. (b) The indicated zoom region in (a) showing the approximate instant at which the protection circuit responds after detecting the fault.

For conducting FUL, M_2 is turned ON first. After an interval t_f, M_1 is turned ON. Furthermore, a continuous pulse train is fed to M_2 while a single fault-creating pulse P_1 is fed to M_1. Continuous pulse train to M_2 ensures that the integrator capacitors are being reset periodically.

Measurements for the sensor voltage (V_S) and the device current (I_M), when M_2 is hard switched into a fault state, are shown in Fig. 14. V_{DS} transitions from 0 to 600 V, for M_2, when M_1 is turned ON, as shown in Fig. 14(a). After some duration, M_2 is turned ON, hence short-circuiting the half-bridge leg. The protection circuit acts almost immediately to withdraw the gate pulse to M_2 after the fault reference level (V_{REF}) is detected by the protection circuit. After the fault is detected, the gate driver circuit withdraws gate pulse to M_2 within 25 ns, as seen in Fig. 14(b). Therefore, the protection scheme demonstrates an

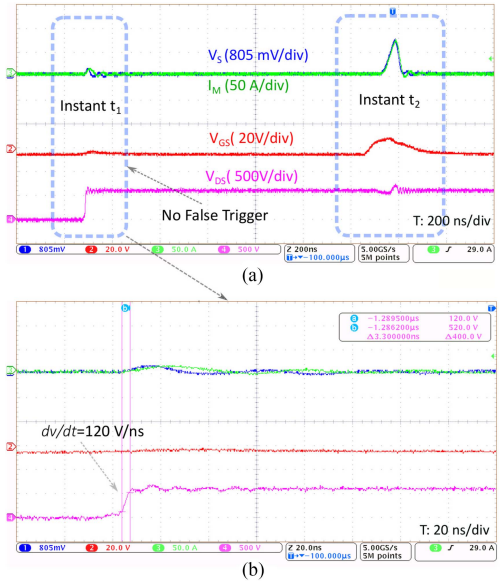

Fig. 15. HSF test results demonstrating the influence of switch node dv/dt (120 V/ns) on the protection scheme.

ultrafast response time. The dv/dt immunity of the protection scheme is also investigated with the following methodology.

A train of pulses is fed to the DUT M_2 in the test setup shown in Fig. 13. A HSF-creating pulse is generated by turning ON M_1 for a short period. It can be seen that the fault takes place at instant t_2 in Fig. 15. However at t_1, the voltage transition across the device occurs as M_1 is turned ON at that instant. While there is a slight perturbation in sensor output due to noise coupled by high dv/dt, the noise should be low enough to not trigger the protection scheme during normal operation of the power device. To investigate noise immunity of the protection scheme, the dv/dt-induced sensor output was monitored up to 120 V/ns. As can be observed in Fig. 15, the perturbation in the sensor output is significantly less than 500 mV threshold. Therefore, this sensor output can be useful for adjusting V_{REF} as this component will be present in the sensor output during normal operation of the power device when the SiC MOSFET is switching at high dv/dt.

As depicted in Fig. 13(c), FUL test is carried out by first turning ON M_2 and then subsequently turning ON M_1. Fig. 16 shows the measurement results for the sensor voltage (V_S) and the device current (I_M) when M_2 is subjected to a FUL. The driver IC (UCC27531) withdraws gate pulses to M_2 within 25 ns after detection of the fault, as can be observed from Fig. 16(b). Owing to the turn-OFF delay time of M_2, the device current increases to a peak value of around 170 A after the fault is detected. When the turn-OFF gate resistance is halved, the peak overshoot in the drain-source voltage of M_2 increased to 1.04 kV from 870 V while the total fault clearing time reduced from 140 to 80 ns, as shown in Fig. 16. Therefore, a trade-off between the fault clearing time and the peak overshoot exists based on the voltage rating of the power device. Additionally, soft turn-OFF functionality may be added to the driver circuit to lower the peak device drain-source voltage (V_{DS}) overshoot [29].

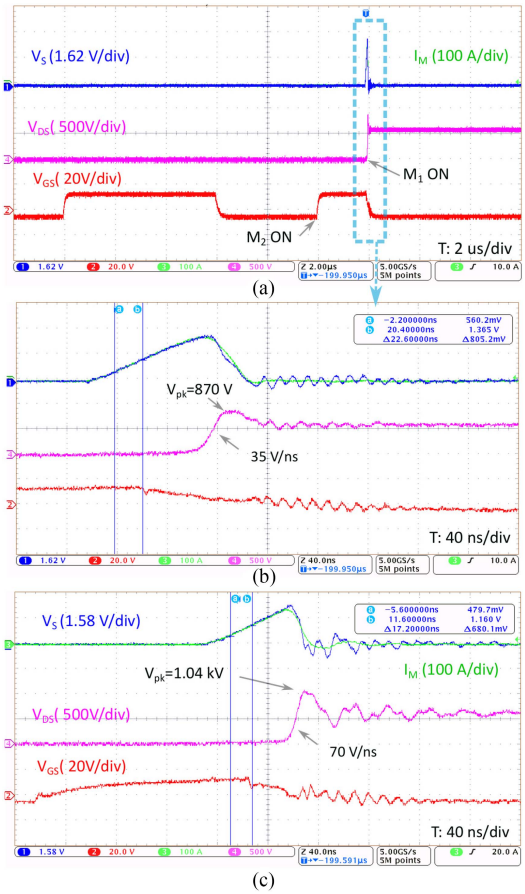

Fig. 16. (a) Experimental results demonstrating the protection of the device M_2 subjected to a FUL with $R_i = 2\,\text{k}\Omega$, $C_i = 0.1$ nF, $V_{\text{REF}} = 500$ mV, and $I_{\text{REF}} \approx 32$ A. (b) The indicated zoom region in (a) showing the approximate instant at which the protection circuit responds after detecting the fault. (c) FUL test results with the turn-OFF gate resistance halved.

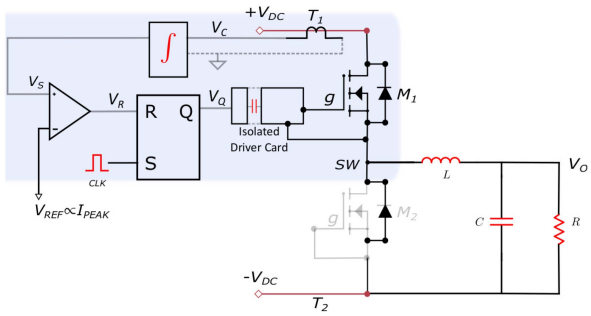

Fig. 17. Implementation of cycle-by-cycle current-limiting loop for the high-side SiC MOSFET M_1 in a buck converter.

C. Peak Current-Mode Control (PCMC) of a Buck Converter

PCB coil designed for the high-side SiC MOSFET M_1 in the half-bridge leg is now utilized to demonstrate the cycle-by-cycle limit of the peak current through the power device. The cycle-by-cycle current limit is inherent with the PCMC and is now demonstrated with the designed sensor. Fig. 17 shows the half-bridge circuit configured as a buck converter. The current through the high-side SiC MOSFET is sensed by processing the coil output

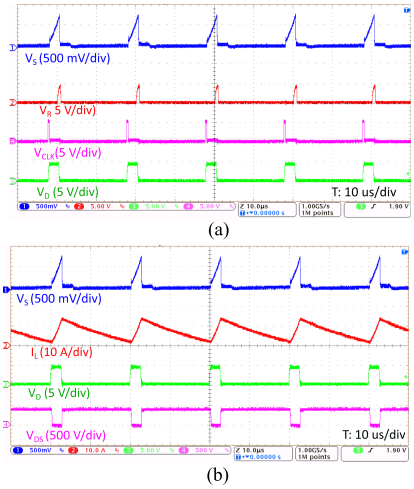

Fig. 18. Cycle-by-cycle peak current limit for the high-side MOSFET M_1. (a) Measurements for the sensor voltage with $R_i = 470\,\Omega$ and $C_i = 0.1$ nF, filtered with an *RC* filter, and the latch input/output signals. (b) The inductor current (I_L) and the MOSFET drain-source voltage (V_{DS}) waveforms. The peak current limit is adjusted to obtain a 400 to 48 V conversion with a 6.5-A load.

through an integrator circuit, which is now referenced to the signal ground. By comparing the current sensor output (V_S) with a peak current reference (V_{REF}) for resetting the *SR* latch, peak current limit through the MOSFET is set. The peak current reference is adjusted similarly as defined in (13). Experimental results demonstrating the peak-current limitation through M_1 are shown in Fig. 18. While the coil signal processing circuit is referenced to the local device ground for the HSF and FUL tests, the circuit is referenced to the controller ground in this test.

V. Conclusion

A simplified approach for designing PCB coils for discrete SiC MOSFETs is presented based on a single interconnect trace. The interconnect facilitates placement of miniature coils in the layout, therefore causing minimal intrusion inside the power-loop. With this coil design methodology, a half-bridge circuit is developed with embedded PCB coils for current sensing of both the devices in the circuit. Using the developed PCB coils, this article presents an ultrafast protection scheme with a swift response time, under 25 ns, suitable for integration with next-generation gate-driver circuits for discrete SiC MOSFETs. The immunity of the protection scheme is investigated up to dv/dt of 120 V/ns. Additionally, the PCB coil is also utilized for implementing peak current-mode control of a buck converter, which features inherent protection to the power device. As a direct replacement for CTs and Hall sensors, the PCB coils can facilitate more reliable converters with high power density.

Appendix

A. Influence of External Conductors

While there may be flux linkages through the PCB coil due to nearby current carrying conductors, any influence on the sensor output will be determined by the frequency of the current as well

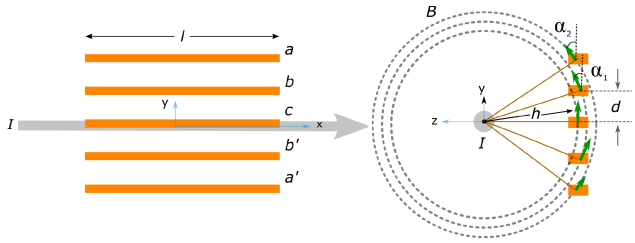

Fig. 19. PCB coil in the presence of flux linkages due to an external conductor.

as the proximity of the PCB from any nearby conductors. From the frequency response of the sensor shown in Fig. 9, it can be observed that the sensor possesses sensitivity only toward currents with their frequency spectrum lying within the bandwidth of the sensor. Consequently, the sensor is inherently immune toward external conductors carrying power-line frequency currents, which are of low frequency. For any external current (I_{EC}), with its frequency spectrum lying within the bandwidth of the sensor, the sensor output voltage ($V_S(t)$) when measuring device current ($I_M(t)$) is expressed as

$$V_S(t) = \frac{M}{R_i C_i} I_M(t) + \frac{M_{EC}}{R_i C_i} I_{EC}(t) \tag{17}$$

where M is the mutual inductance between the power-loop trace and the PCB coil as defined in manuscript, and M_{EC} is the mutual inductance between the external conductor and the PCB coil. An analytical expression of M_{EC} is now derived for a simplified geometry of an external conductor as a long straight conductor at a height h from the PCB coil, as shown in Fig. 19. To estimate the worst case flux linkages through the PCB coil, the conductor is oriented along the middle turn of the PCB coil. Since the length of this conductor can be considered to be much larger than the dimensions of the PCB coil, the magnetic field (B) at a distance h from the conductor can be estimated with Amperes law as

$$B = \frac{\mu_0 I}{2\pi h}. \tag{18}$$

Further, since the height of an external conductor above the PCB coil is much larger than the dimensions of the PCB coil, the variation of B across a single turn of PCB coil can be neglected. For the middle-turn (c) of the PCB coil, B is orthogonal to the plane of the turn. For the turns b, b' and a, a', the field is oriented to the plane of the turns at an angle α_1 and α_2, respectively, as shown in Fig. 19. The flux linkage through the PCB coil can, therefore, be expressed as

$$\lambda = \frac{\mu_0 l_c t}{2\pi}\left[\frac{1}{h} + \frac{2\cos(\alpha_1)}{\sqrt{h^2+d^2}} + \frac{2\cos(\alpha_2)}{\sqrt{h^2+(2\,d)^2}}\right] I_{EC}. \tag{19}$$

Therefore, M_{EC} is expressed as

$$M_{EC} = \frac{\mu_0 l_c t}{2\pi}\left[\frac{1}{h} + \frac{2\cos(\alpha_1)}{\sqrt{h^2+d^2}} + \frac{2\cos(\alpha_2)}{\sqrt{h^2+(2\,d)^2}}\right]. \tag{20}$$

Based on the expression for M_{EC} derived in (20), it can be inferred that an external conductor may cause some flux to link through the PCB coil, therefore, affecting immunity of the PCB

coil to the external fields. Thereafter, the influence of M_{EC} on the sensor output can be estimated with (17).

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