Smooth Pulse Number Transition Strategy Considering Time Delay in Synchronized SVPWM

Joon-Seok Kim, Do-Hyeon Kim, June-Hee Lee, *Member, IEEE*, and June-Seok Lee, *Senior Member, IEEE*

***Abstract*—In high power motor drive systems, synchronized space vector pulsewidth modulation (synchronized SVPWM) is widely used to guarantee stable control performance. Synchronized SVPWM has a characteristic that the switching frequency varies abruptly when the pulse number transitions. This article proposes a pulse number transition point at which the phase difference is minimized to remove the phase difference of the sampling point that appears during synchronized SVPWM control. In addition, for a smooth pulse number transition of synchronized SVPWM, a compensation method for the magnitude and phase error of the inverter output voltage due to the time delay and a method of removing the existing phase difference without using a phase-locked loop are proposed in consideration of the characteristic of changing switching frequency. The validity and the implementation of the proposed method are verified by experimental results using a high-power inverter driving 332 kW interior permanent magnet synchronous motor (IPMSM).**

***Index Terms*—High-power motor drives, low switching frequency, pulse number transition, synchronized space vector pulse width modulation (synchronized SVPWM), time delay.**

I. Introduction

CONTROLLING a voltage source inverter (VSI) using a high switching frequency in a high power motor drive system increases the ratio of the switching loss to the total power conversion loss due to the frequent switching operation of the power semiconductor. Therefore, the switching frequency of VSI is limited from a few hundred Hz to 1 kHz to reduce the switching loss, the temperature rise, and as a result, in the volume of the cooling system [1], [2], [3], [4], [5]. However, when conventional asynchronized pulsewidth modulation (PWM) is performed using a low switching frequency, harmonics, and subharmonics are generated [6], and these harmonics cause additional loss and oscillation. In addition, an output voltage imbalance occurs due to the asynchronization between the inverter output fundamental wave and the carrier wave [7]. In the high-speed region of the motor, the frequency of the inverter fundamental wave increases. Therefore, the number of switching pulses of the inverter decreases during one period of the fundamental wave, which increases the output voltage imbalance. To eliminate the disadvantages of asynchronized PWM with a low switching frequency, synchronized PWM is used.

Synchronized PWM determines the switching frequency with the product of the fundamental frequency of the inverter output voltage and a certain integer [4], [8]. High-power traction motors must be able to operate in the overmodulation region and six-step region to operate over a wide speed range while maximizing the utilization of the voltage source. Therefore, various studies have been conducted on synchronized space vector pulsewidth modulation (SVPWM) [2], [8], [9], [10] due to the advantages of increasing the linear modulation range between the output voltage and the voltage modulation index, having a small harmonic current in the steady state, and enabling the application of various overmodulation techniques. When synchronized PWM is used, it is possible to apply a switching angle to a desired part of the phase of the fundamental wave in the inverter output voltage. Therefore, research on algorithms such as specified harmonic elimination PWM (SHEPWM), which controls the switching angle that cancels specific harmonics [11], [12], [13], and synchronous optimal PWM (SOPWM), which calculates and controls a switching angle that minimizes total harmonic distortion (THD) is also steadily progressing [14], [15], [16]. However, both SHEPWM and SOPWM require a look up table of the optimal switching angle obtained through complex mathematical calculations. In addition, when applied to field-oriented-control (FOC) drives, since the average value of current cannot be sensed, complex control is additionally required to compensate for the resulting dynamic modulation error [1], [8], [9]. Synchronized SVPWM does not generate a dynamic modulation error when used with an existing FOC controller and has the characteristic that various pulse patterns are possible, such as the application of bus-clamping PWM strategies control [9], [18]. However, transitions between the various pulse patterns can degrade the performance and stability of the current controller. Therefore, studies for a smooth transition between various pulse patterns are being conducted. Wang et al. [19] proposed a pulse pattern transition point that maintains the continuity of the phase and the magnitude of the fundamental voltage while considering the effect of harmonic

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voltage for a smooth pulse pattern transition in a six-phase dual stator induction machine. Zhang et al. [20] proposed a method to match the ending vector angle of SVPWM and the starting vector angle of SHEPWM for a smooth transition from a three-level inverter to SVPWM and SHEPWM. Zhang et al. [3] analyzed the harmonic circuit and proposed a smooth pulse pattern transition point from SVPWM to SHEPWM in the sensorless drive. In [4], in the pulse number transition situation, the voltage vector was multiplied by the complex gain to match the end point of the flux trajectory before the transition with the start point of the flux trajectory after the transition. Therefore, there is a disadvantage that complex gains must be obtained in advance and used. In addition, although a method for compensating the control period has been proposed to compensate for the synchronization error, proper compensation is not possible because the time delay that appears in digital control unit implementation has been not considered.

In a generally used digital ac drive system, a time delay between the output voltage and the reference voltage of the synchronous frame current regulator exists due to digital implementation and SVPWM control characteristics [21]. When the ratio of the switching frequency to the fundamental frequency is sufficient, magnitude and phase errors are negligible. In a system such as a railway traction drive, the fundamental frequency of the output voltage increases by a few hundred Hz in the high-speed region. In addition, because the switching frequency is limited to about 1 kHz due to the size limitation of the cooling system, the switching frequency is controlled by a small integer product in the synchronized SVPWM. The ratio of the switching frequency to the fundamental frequency is not sufficient, and the error caused by the time delay thus cannot be ignored. The error in the magnitude and phase of the inverter output voltage can make the current regulator unstable at high speed and degrade dynamic performance [22], [23]. For this reason, appropriate compensation is required for the error caused by the time delay of the inverter output voltage, and in the transition of pulse patterns, the time delay is critical [8]. Therefore, studies have been conducted to compensate errors caused by time delay through calculation using the sampling period. In [8], a modified compensation method considering the synchronized SVPWM characteristic was applied only to the pulse pattern transition timing. However, in a transient state in which the fundamental frequency is changed, it is desirable to apply it not only to the transition timing but also to the entire control.

In synchronized SVPWM, current sampling is performed in the same phase of the fundamental wave of the inverter output voltage. However, in the process of controlling the sampling period, a synchronous phase error between the reference sampling point and the actual sampling point occurs due to a current and velocity sampling error, and variation of the d-axis and q-axis reference voltage in the synchronous reference frame in a transient state. Since this synchronous phase error deteriorates the dynamic characteristics of the sampling period control, a phase-locked loop (PLL) is used to eliminate the synchronous phase error and achieve a smooth pulse pattern transition [8], [25], [26]. However, if the PLL is used, the complexity of the control implementation increases, and a lot of time is required to select an appropriate gain value.

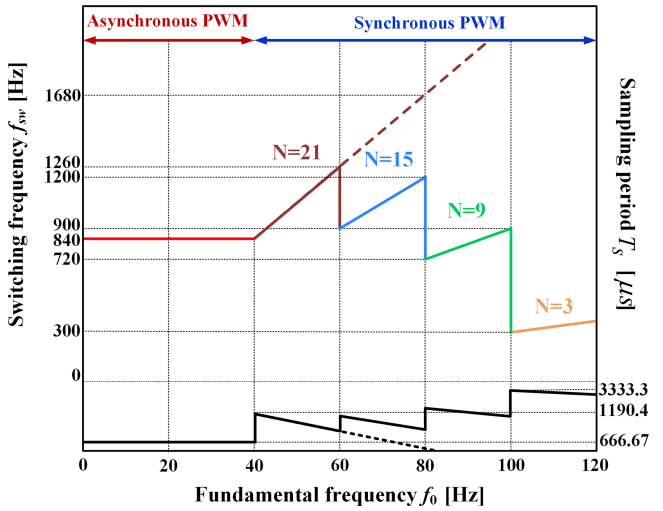


Fig. 1. Control of switching frequency according to pulse number and fundamental frequency.

The main contributions of this article are the proposal of a method for maintaining synchronization, for a smooth transition between different pulse numbers in synchronized SVPWM based on the carrier signal, and to explain the method in detail through analytical derivation. In addition, the proposed method does not use PLL to eliminate the synchronous phase error. The feasibility of the proposed method was verified through experimental results on a high-power inverter driving 332kW interior permanent magnet synchronous motor (IPMSM).

II. Smooth Pulse Number Transition Strategy

Synchronized SVPWM is a method of controlling the switching frequency by the product of the fundamental frequency and a specific integer as shown in Fig. 1. The number of pulses appearing in the output voltage during one cycle of the fundamental wave is equal to the integer controlling the switching frequency. To keep half-wave symmetry, quarter-wave symmetry, and three-phase symmetry, the number of pulses preferably should be multiples of three and odd multiples [3], [4]. Therefore, a desirable integer considered in this article, namely, the pulse number (N) is expressed as

$$N = 3 \cdot (2m - 1) \quad (m = 1, 2, 3 \ldots). \tag{1}$$

The switching frequency (f_{sw}) is determined through the following equation:

$$f_{sw} = N \cdot f_0, \tag{2}$$

where f_0 is the fundamental frequency of the inverter output voltage.

Fig. 1 is a case where f_{sw} is controlled by $N = 21$, 15, 9, and 3, and f_{sw} is proportionally changed according to each N and f_0. Because f_{sw} can be varied through N, it has the following characteristics. First, switching losses can be reduced through

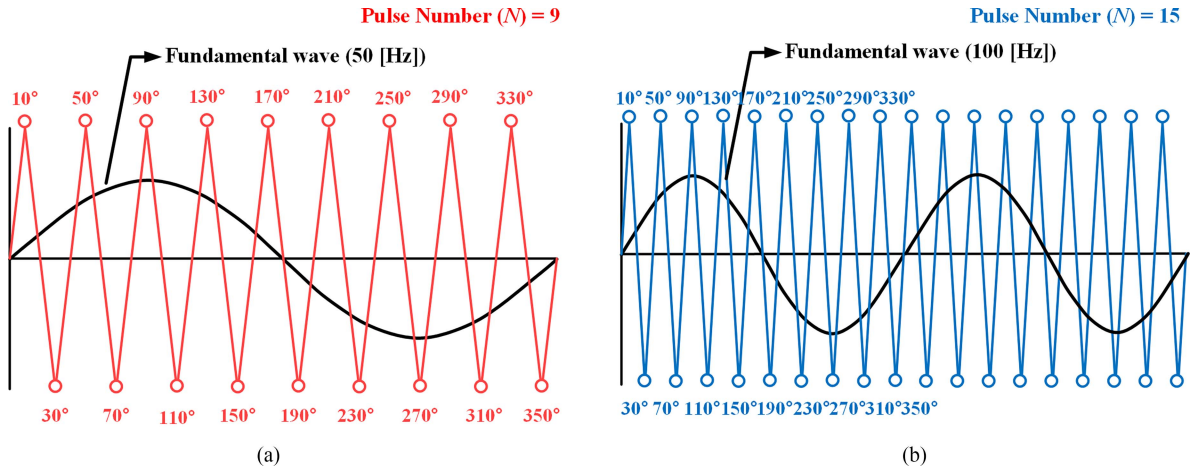


Fig. 2. Phase of reference sampling point according to phase of fundamental wave and pulse number in synchronous SVPWM. (a) When the fundamental frequency is 50 Hz. (b) When the fundamental frequency is 100 Hz.

pulse number transitions. For example, in Fig. 1, if $N = 21$ and no pulse number transition is performed at a f_0 of 60 Hz, the switching loss increases as the switching frequency increases as shown by the brown dashed line. Therefore, switching losses can be reduced by decreasing f_{sw} by transitioning N from $N = 21$ to 15. Second, it is possible to secure enough implementation time for control. Carrier-based SVPWM performs current sensing when the carrier reaches the maximum and minimum values, and as a result, the average value of the current is sensed. Therefore, the sampling period (T_s) (the so called control period) and the switching frequency have the following relationship:

$$T_s = \frac{1}{f_{sw}} = \frac{1}{N \cdot f_0}. \tag{3}$$

If pulse number transitioning is not performed as shown by the black dashed line, T_s becomes shorter in inverse proportion to the increase of f_{sw}. In addition, T_s may be insufficient if the amount of computation is large. Therefore, it is possible to secure implementation time by reducing f_{sw} through the pulse number transition.

A. *Pulse Transition Point That Minimizes Phase Error*

For a smooth pulse pattern transition, the pulse pattern transition should be made at a sampling point that minimizes the synchronous phase error (φ_{err}), which means the phase difference between the reference sampling point and the actual sampling point. In an ideally controlled synchronized SVPWM, sampling occurs at a fixed phases of the fundamental wave of the inverter output voltage, and these fixed phases become the reference sampling points. Therefore, φ_{err} should be minimized as it affects the performance of the current controller and consequently increases the current and torque ripple that induces oscillations in speed [4]. In addition, it interferes with the synchronization of the switching frequency and the fundamental frequency.

Fig. 2(a) and (b) show the reference sampling points according to $N = 9$ when sampling is performed twice in one switching period. When double sampling is performed, the number of pulses in one fundamental cycle is N. However, the number of samplings performed during one fundamental cycle is $2N$. The double sampling method reduces the current sampling error because the average value of current is measured. Therefore, more accurate control is possible [27], [28]. In addition, the space vector approach to PWM offers certain flexibilities in the design of PWM strategies [17]. In the case of double sampling, the sampling period (T_s) is derived as follows:

$$T_s = \frac{1}{2 \cdot N \cdot f_0} = \frac{1}{2 \cdot f_{sw}}. \tag{4}$$

For the convenience of understanding in this section, a steady state where there is no change in f_0 is assumed, and in this case, T_s is changed only by the pulse number transition. Since the control period of the synchronous SVPWM is determined as in (4), the number of samplings performed during one period of the fundamental wave is constant as $2N$. Accordingly, the phase of the point at which sampling is performed based on the phase of the fundamental wave is also constant. Fig. 2(a) and (b) show that the number of samplings within one period of the fundamental wave is the same regardless of the frequency of the fundamental wave. As shown in Fig. 3(a), (b), and (c), if the number of sampling points (k) is counted from the sampling point with the smallest angle between the V_{ds} axis and the sampling point, the phase of the reference sampling point ($\varphi^*_{N,k}$) is defined as follows:

$$\varphi^*_{N,k} = \frac{2\pi}{2 \cdot N} \cdot (k - 0.5), \ (k = 1, 2, 3 \ldots 2N). \tag{5}$$

Therefore, the phase of the next sampling point can be expressed as follows using T_s, T_s:

$$\varphi^*_{N,k+1} = \varphi^*_{N,k} + 2 \cdot \pi \cdot f_0 \cdot T_s \cdot 2 = \varphi^*_{N,k} + \frac{\pi}{N}. \tag{6}$$

For a smooth pulse number transition, it should be made at a sampling point that minimizes the φ_{err} and φ_{err} can be

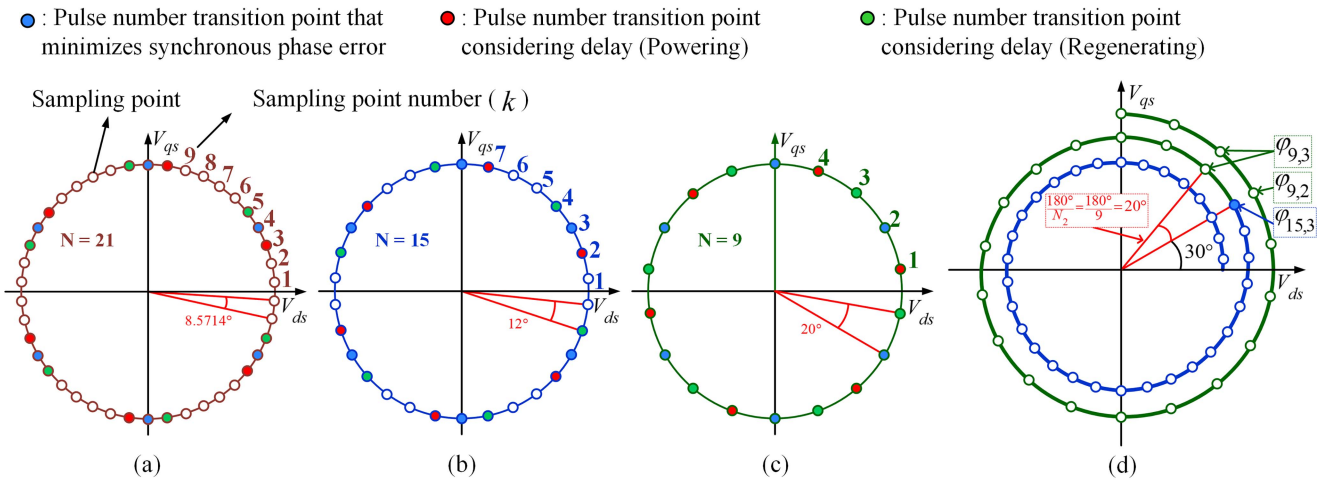


Fig. 3. Proposed synchronous phase error minimization pulse number transition point. (a) Reference sampling point when $N = 21$. (b) Reference sampling point when $N = 15$. (c) Reference sampling point when $N = 9$. (d) The sampling point when the pulse number transition $N = 15$ to 9 at the proposed point.

expressed as

$$\varphi_{\text{err}} = \varphi^*_{N,k} - \varphi_{N,k} = \varphi^*_{N,k} - \left(\varphi_{N,k-1} + \frac{\pi}{N}\right) \tag{7}$$

to eliminate φ_{err}, $\varphi^*_{N,k}$ and the phase of the actual sampling point ($\varphi_{N,k}$) must coincide. In terms of the pulse transition timing, assuming that the number of pulses before the transition is N_x and the number of pulses after the transition is N_{x+1}, the following conditions must be satisfied for φ_{err} to become zero:

$$\varphi^*_{N_{x+1},k_2} = \varphi_{N_{x+1},k_2} = \varphi_{N_x,k_1} + \frac{\pi}{N_{x+1}} \tag{8}$$

as in Fig. 3(d). When sampling number transition from $N_{\text{x}} = 15$ to $N_{x+1} = 9$ occurs in the sampling point at $\varphi_{15,3}$, the next actual sampling point $\varphi_{9,3}$ coincides with $\varphi^*_{9,3}$ due to $\pi/N_{x+1} = 20°$. The pulse number transition point that minimizes φ_{err} corresponds to the point represented by the blue circle at each N in Fig. 3(a), (b), and (c).

However, T_s calculated through the transition pulse number is applied to the next sampling point because of time delay due to the digital control unit. Therefore, to apply T_s calculated by the transition pulse number at the overlapping point, the T_s calculation through the transition pulse number must be performed at one sampling point before the overlap point. When the motor operates in powering, the point before one sampling period from the overlap point corresponds to the red point in Fig. 3(a), (b), and (c), and when the motor operates in regenerating, it corresponds to the green point. Such sampling points that minimize the proposed phase error are defined as a switchable sampling point.

B. Compensation Method for Problem Caused by Time Delays

In SVPWM, the reference voltage vector (V^*) of the 3-phase inverter can be expressed as

$$V^* = V_{ref} \cdot e^{j(\omega_e t + \theta_v)} \tag{9}$$

as shown in Fig. 4, where ω_e is the angular velocity of synchronous reference frame, θ_v is the angle between the reference

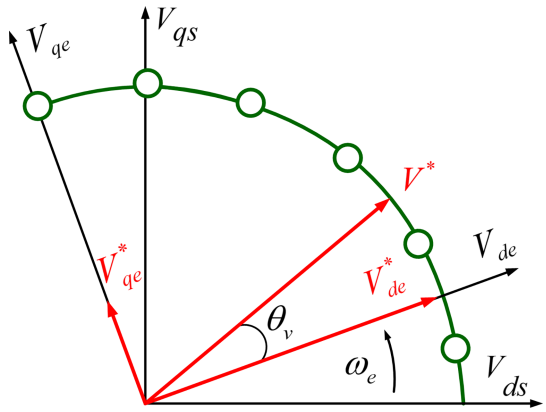


Fig. 4. Synchronous reference frame representation of voltage vector.

voltage vector and the synchronous reference frame, and V_{ref} is the magnitude of V^*.

In most motor driving devices and power conversion devices in the industry, current controllers and PWM generators are implemented on a digital unit [23], [24]. Therefore, the digital control leads the time delay [22]. In asynchronized SVPWM with a constant T_s, the calculated output voltage has a time delay of 1 T_s, as shown in Fig. 5. In addition, a delay of 0.5 T_s is additionally generated due to the characteristic of SVPWM where the reference voltage vector is located at the midpoint of the sampling period [21]. This means that a total time delay of 1.5 T_s occurs at the output voltage. In [21], assuming that ω_e is constant in asynchronized SVPWM, the magnitude and phase of the output voltage were compensated by multiplying the output of the current controller by the compensation function (K_{Async}) below,

$$K_{\text{Async}} = \frac{2}{\omega_e T_s} \sin\left(\frac{\omega_e T_s}{2}\right) e^{j(1.5 T_s \omega_e)}. \tag{10}$$

In synchronized SVPWM control where f_{sw} is synchronized by N times f_0 of the inverter output voltage, f_{sw} changes at

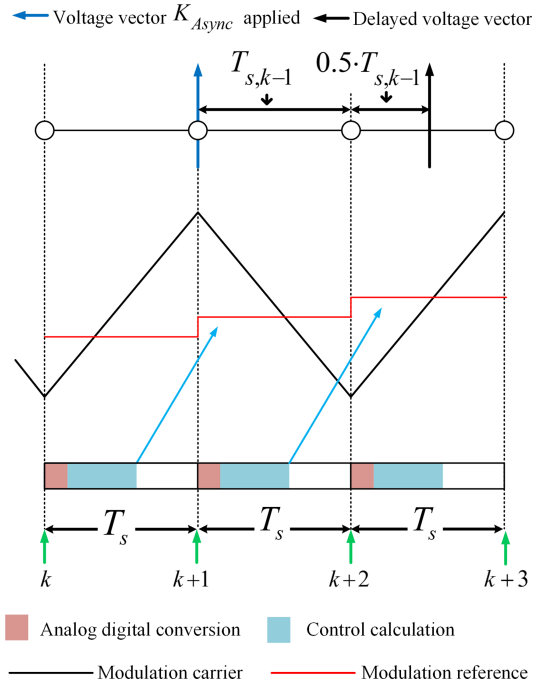


Fig. 5. Time delay problem in inverter output voltage in asynchronized SVPWM.

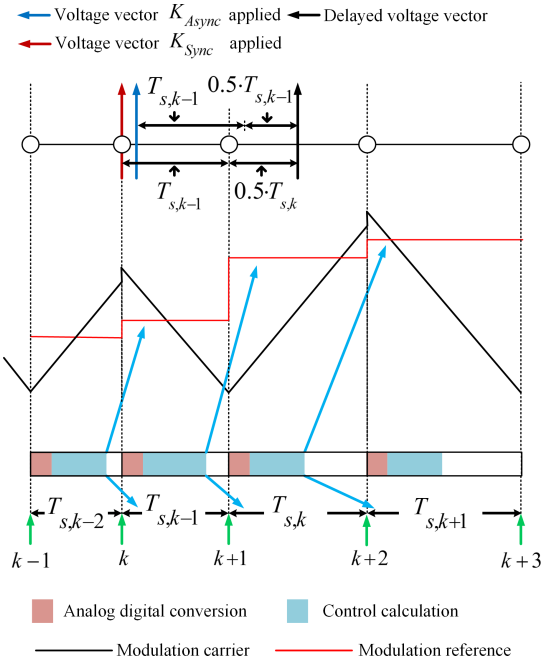


Fig. 6. Time delay problem in inverter output voltage in synchronized SVPWM.

every sampling point. Therefore, T_s is not constant, unlike in the case of asynchronized SVPWM. Namely, in synchronized SVPWM, if K_{Async} is applied, the phase of the output voltage vector is not properly compensated. As shown in Fig. 6, it can be seen better that the output voltage vector represented by the blue arrow compensated by K_{Async} is not properly compensated at the time of the pulse number transition point where the sampling period changes rapidly. When sampling is performed at sampling point k, the output voltage is delayed by the control period $T_{s,k-1}$ used for control at sampling point k. According to the characteristics of SVPWM, since the reference voltage vector is in the middle of the next sampling period $T_{s,k}$, a half delay of the next sampling period $0.5T_{s,k}$ occurs. Namely, the time delay by the digital control unit is as much as the sampling period at the time of sampling, and the time delay by the SVPWM characteristic is half of the sampling period to be applied at the next sampling point. The sampling period at the next sampling point corresponds with a control period calculated at the present sampling point. Therefore, the compensation function K_{Sync} can be expressed as follows, assuming ω_e is constant

$$K_{\text{Sync}} = \frac{2}{\omega_e T_{s,k-1}} \sin\left(\frac{\omega_e T_{s,k-1}}{2}\right) e^{j(1T_{s,k-1}\omega_e + 0.5T_{s,k}\omega_e)}. \tag{11}$$

As in the case of asynchronized SVPWM, the magnitude and phase of the output voltage can be compensated by multiplying the output of the current controller by the compensation function K_{Sync}.

C. Synchronous Phase Error Compensation Method Without Using PLL

Synchronous phase error (φ_{err}) occurs not only at the pulse number transition point, but also at all sampling points because of changes of θ_v due to variation in the d-axis and q-axis reference voltage in the synchronous reference frame in the transient state. To eliminate φ_{err}, a method of compensating the phase error using a PLL is widely used [8], [25], [26]. In this article, the synchronous phase error is compensated without using a PLL to avoid the difficulties of PLL parameter design and to facilitate digital implementation.

The phase of the sampling point ($\varphi_{N,k}$) can be calculated by the following equation through the current controller output voltages expressed in the stationary reference frame V_{ds} and V_{qs}

$$\varphi_{N,k} = \tan^{-1}\left(\frac{V_{qs}}{V_{ds}}\right). \tag{12}$$

Therefore, φ_{err} can be derived from (7) and (12).

As shown in Fig. 7, in the ideal case with no synchronous phase errors (φ_{err}), the reference sampling point coincides with the actual sampling point, and the phase difference between each sampling point is constant at 20°. In addition, Fig. 7 shows the other case of actual control with synchronous phase errors (φ_{err}). φ_{err} occurs at k and the compensation sampling period corresponding to φ_{err} is calculated at $k+1$. It is applied to the sampling period to remove φ_{err} at $k+2$ because of the time delay owing to the digital control unit. The compensation sampling period ($T_{comp,k}$) can be expressed as the following formula:

$$T_{comp,k} = \varphi_{\text{err}} \cdot \frac{1}{\omega_e} = \frac{\varphi_{\text{err}}}{2\pi \cdot f_0}. \tag{13}$$

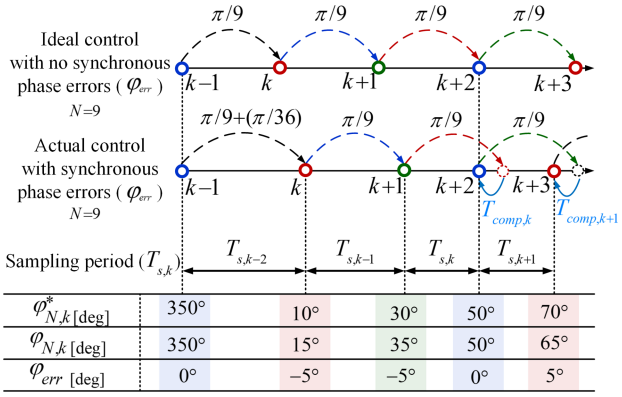


Fig. 7. Principle of the proposed synchronous phase error compensation method.

Therefore, the control period where φ_{err} is compensated can be summarized as follows:

$$T_{s,k} = \frac{1}{2 \cdot N \cdot f_0} + T_{comp,k}. \tag{14}$$

In [4], φ_{err} is eliminated by compensating the time corresponding to the phase difference of the voltage vector at the reference sampling point in the same manner as the method proposed in this article. However, since the time delay appearing in the output sampling period is compensated without considering the time delay, the error will not be removed properly. Namely, as shown in Fig. 7, if the sampling period corresponding to the phase error is compensated as it is, the phase error does not disappear since the $T_{comp,k}$ is compensated for the next sampling period. The principle that the phase error is compensated in a case in which the time delay is considered is expressed as an equation as follows:

$$\varphi_{\text{err},k+2} = \varphi_{\text{err},k+1} - \alpha \cdot \varphi_{\text{err},k} \tag{15}$$

where α is the coefficient that adjusts the size of the compensation component in consideration of the time delay. Fig. 8 shows a state where φ_{err} is compensated according to the magnitude of α. It is assumed that 10° and -10° occur continuously, which are extreme phase errors that can occur in the case of $N = 9$. In case of compensation as in Fig. 6 and (14), it can be seen that φ_{err} does not disappear because $\alpha = 1$. In addition, it can be confirmed through simulation that the best response characteristic is obtained when $\alpha = 0.3$. In the same principle, as shown in Fig. 9, when the maximum possible synchronization error is assumed when $N = 21$, it shows that $\alpha = 0.3$ has the best response and that the phase error converges to 0 as in the case of $N = 9$.

Finally, the sampling period for which the phase error is compensated in consideration of the time delay is calculated using the following equation:

$$T_{s,k} = T_{s,cal} + T_{comp,k} = \frac{1}{2 \cdot N \cdot f_0} + 0.3 \cdot \frac{\varphi_{\text{err}}}{2\pi \cdot f_0} \tag{16}$$

where $T_{s,cal}$ denotes the calculated sampling period to which the $T_{comp,k}$ has not yet been added.

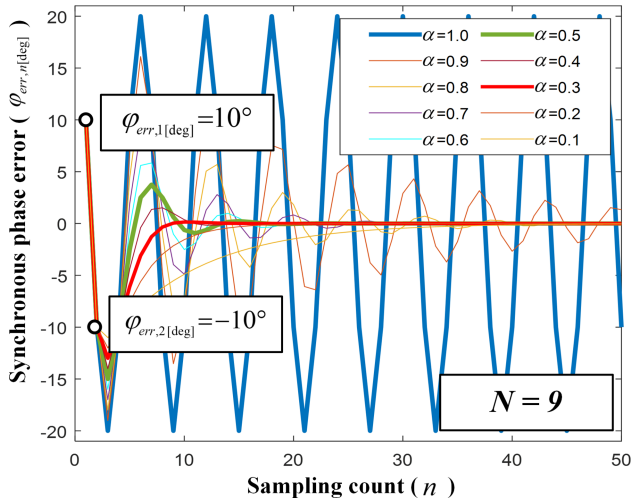


Fig. 8. Synchronous phase error response characteristics according to α in the proposed compensation method when $N = 9$.

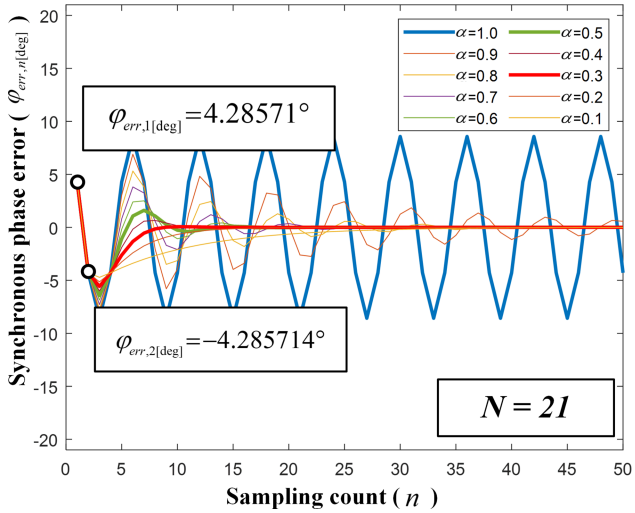


Fig. 9. Synchronous phase error response characteristics according to α in the proposed compensation method when $N = 21$.

D. Implementation of the Proposed Synchronized SVPWM

Fig. 10 shows a block diagram for IPMSM control using the method proposed in this article. The synchronous reference frame voltage, which is the output of the PI current controller, is used to determine the phase of present the sampling point by (12). Pulse number selector block selects N based on motor speed and uses $\varphi_{N,k}$ to perform the pulse number transition at the switchable sampling point that minimizes φ_{err} considering the time delay, as described in part A. $T_{s,cal}$ is calculated then through the determined pulse number and f_0. To compensate for φ_{err}, $T_{comp,k}$ is computed using f_0 by (16) in part C. In conclusion, the compensated sampling period $T_{s,k}$ is determined through $T_{s,cal}$ and $T_{comp,k}$. Using the obtained $T_{s,k}$ and $T_{s,k-1}$, the magnitude and phase errors appearing in the inverter output voltage due to 1.5 T_s time delay are compensated by multiplying the inverter output voltage by K_{Sync} expressed in (11) of part B.

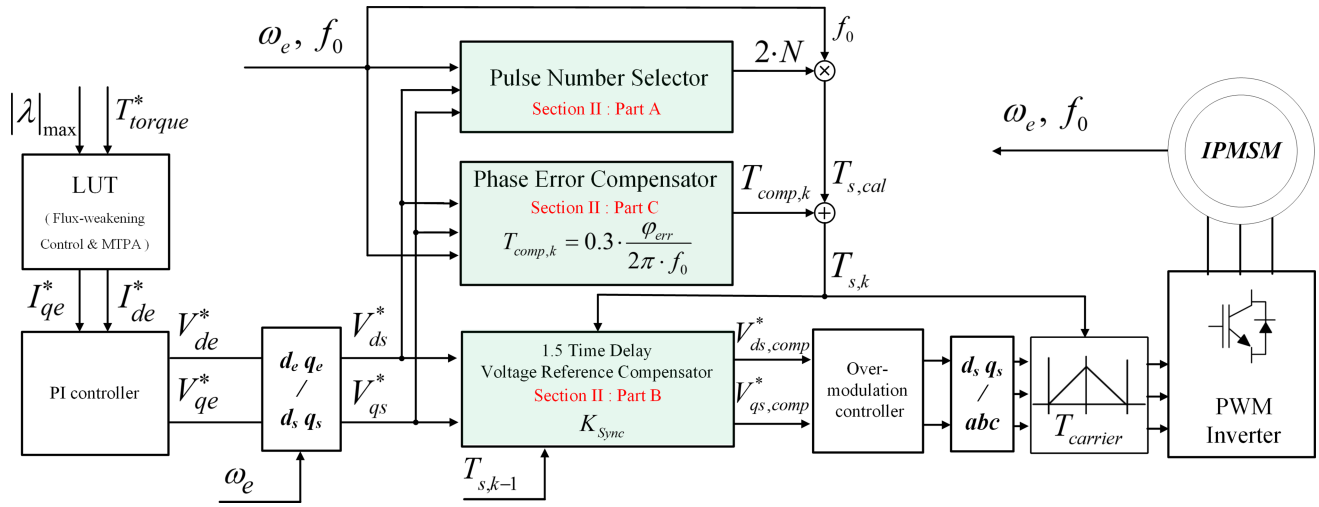


Fig. 10. IPMSM's synchronized SVPWM control block diagram with the proposed compensation method.

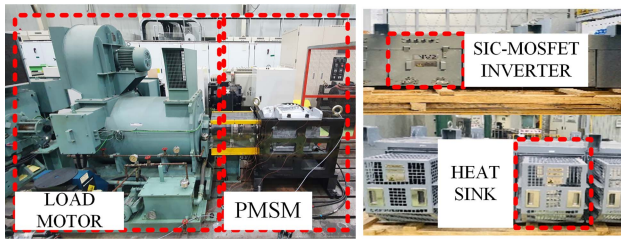


Fig. 11. Motor and inverter setup configured for the experiment on the proposed method.

TABLE I
MACHINE PARAMETERS

Parameter	Symbol	332 kW PM Machine
dc voltage	V_{dc}	1500 V
Rated power	P_N	332 kW
Rated current	I_N	350 A
Rated frequency	f_N	125 Hz
Number of pole pairs	P	6
Stator phase resistance	R_s	0.039 Ω
Stator d-axis inductance	L_s	1.833 mH
Stator q-axis inductance	L_s	5.335 mH

Finally, the compensated reference voltage is compared with the carrier generated by $T_{s,k}$ to output a PWM signal.

III. EXPERIMENT

To demonstrate the validity of the proposed strategy, an experimental set as shown in Fig. 11, was constructed using a permanent magnet synchronous motor with the parameters listed in Table I, and an inverter using a 3,300V/750A SIC MOSFET. The control method was implemented using a ARM STM32F407IG microcontroller unit. Dead time was performed by applying 12 μs. To identify the value of φ_{err}, the phase error ratio (R_{err}) occupied by φ_{err} within one sampling period is defined and is expressed as follows:

$$R_{\text{err}} = \frac{\varphi_{\text{err}} \cdot 2N}{360} . \frac{180}{\pi} \quad (-0.5 \le R_{\text{err}} \le 0.5) \tag{17}$$

by using R_{err}, the relative value of φ_{err} can be known regardless of the pulse number.

A. Comparison With and Without Application of the Proposed Strategy

In this section, the case in which the proposed strategy is applied and the case in which it is not applied as shown in Fig. 12, are compared. It can be confirmed that an increase in current ripple due to φ_{err} does not occur at the pulse number transition point when the proposed strategy is applied. The point at which the pulse number transition occurs can be confirmed through the sampling point number of each experimental result.

Fig. 12(a) shows the experimental result without applying methods of parts A, B, and C proposed in this article. Since no method is applied, significant R_{err} occurs, increasing the current ripple.

Fig. 12(b) shows the result that the pulse number transition was performed at the switchable sampling point in part A. In addition, the compensation method of part B was applied, but the asynchronous compensation function K_{Async} was applied instead of the synchronous compensation function K_{Sync}, which was proposed in this article. The current ripple does not increase at the time of pulse number transition because the transition is performed at the switchable sampling point. Therefore, current ripple of Fig. 12(a) is larger than that of Fig. 12(b) at the pulse number transition. However, since Fig. 12(b) is a case in which the compensation method proposed in part C is not applied, it can be confirmed that a large R_{err} still exists as large as Fig. 12(a).

Fig. 12(c) and (d) show two cases of pulse number transition ($N = 15 \rightarrow 9, N = 9 \rightarrow 15$) when all compensation methods

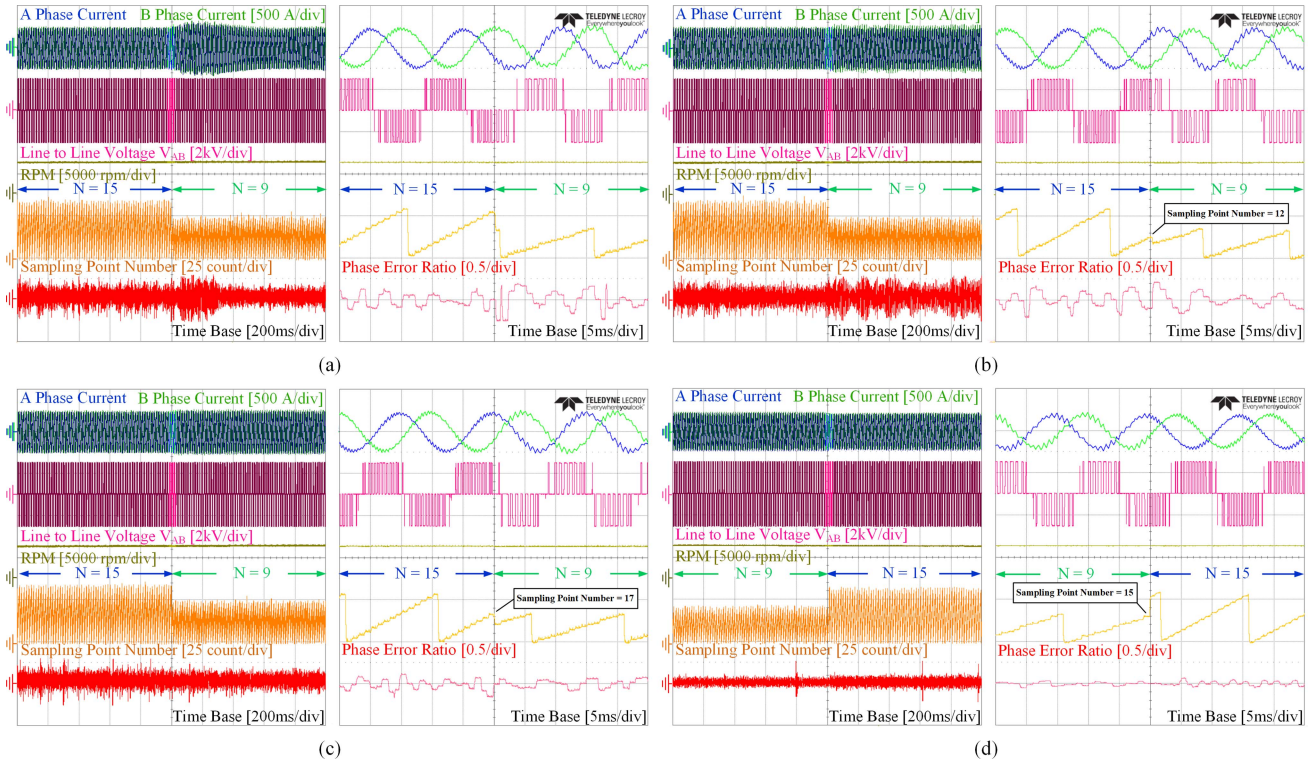


Fig. 12. Experimental results on current voltage output waveform and synchronous phase. (a) Without any compensation. (b) When only the compensation method in part A is applied. (c) When all compensation methods proposed in parts A, B, and C are applied. (d) When applying the compensation method as in (c) and operating in regenerating.

proposed in parts A, B, and C are applied. Since φ_{err} compensation and pulse number transition at the switchable sampling point are performed well, it can be confirmed that the current ripple does not increase because R_{err} hardly occurs at the pulse number transition point compared to the cases in Fig. 10(a) and (b).

In addition, through Fig. 12(b), (c), and (d), it is possible to identify whether the pulse number has been changed at the switchable sampling point suggested in part A or not. At $N = 15$, the switchable sampling point numbers in powering are 2, 7, 12, 17, 22, and 27. Therefore, in Fig. 12(b), the pulse number transition from $N = 15$ to 9 is performed when the sampling points number is 12. At $N = 9$, the switchable sampling point numbers in regenerating are 3, 6, 9, 12, 15, and 18. Therefore, in Fig. 12(d), the pulse number transition from $N = 9$ to 15 is performed when the sampling point's number is 15.

B. Pulse Number Transition in Various Situations

In this section, experiments are carried out to identify whether the pulse number transition is performed smoothly by the proposed method even in a situation where the magnitude of the reference current changes through the LUT according to change of the reference torque. In addition, an experiment is performed to identify whether the pulse number transition is smoothly performed even in the overmodulation region. In Fig. 13, the IPMSM is controlled with rated torque from powering to

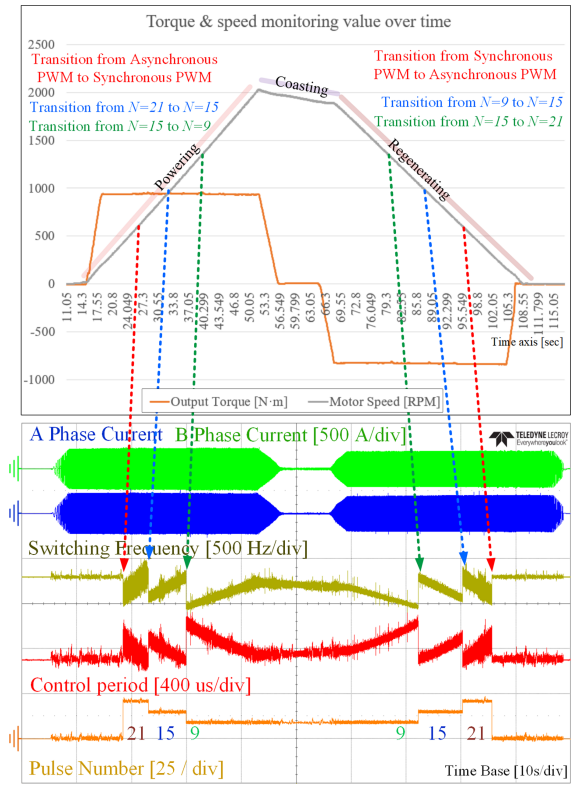


Fig. 13. Full experimental results applying all compensation methods under simple torque profile.

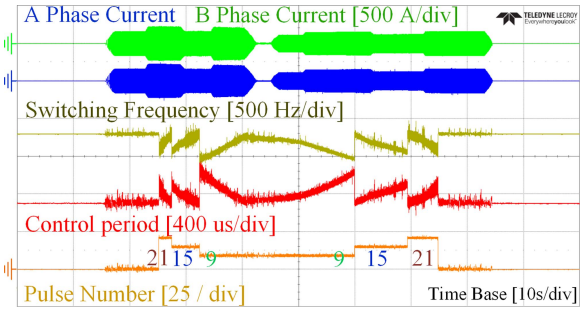
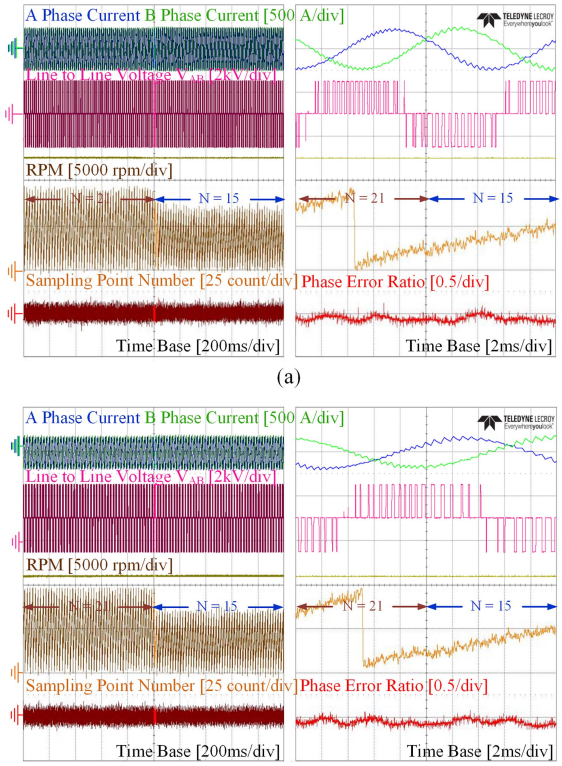


Fig. 14. Full experimental results applying all compensation methods under complex torque profile.



(a)

(b)

Fig. 15. Results of applying all compensation methods in parts A, B, and C at the pulse number transition point ($N = 21 \rightarrow 15$). (a) When controlling the rated current. (b) When controlling at half the rated current.

regenerating. The pulse number selection is based on the speed of the motor. During powering operation, transition speed from asynchronous SVPWM to synchronous SVPWM is 700 r/min, transition speed from $N = 21$ to 15 is 950 r/min, and the transition speed from $N = 15$ to 9 in synchronous SVPWM is set at 1300 r/min. The regenerating operation means the opposite case to the powering operation. The pulse number transition based on speed can be confirmed by comparing the experimental waveform shown in Fig. 13, with the speed and torque monitoring profile, and it can be confirmed that the pulse number transition is properly performed in a wide speed range. The current ripple does not increase at any of the pulse number transition points in the powering as well as in regenerating, and the sampling period

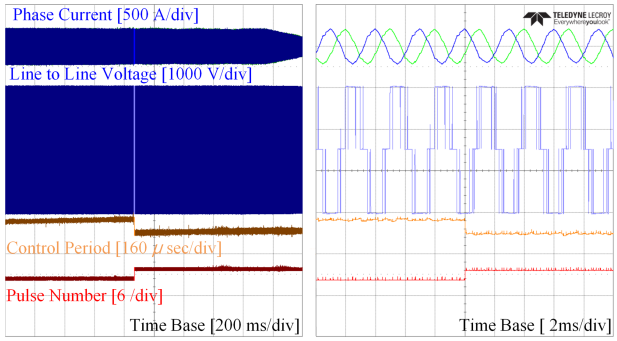


Fig. 16. Pulse number transition experimental result in overmodulation region point ($N = 9 \rightarrow 15$).

is also accurately controlled according to the pulse number. In addition, through the waveform of Fig. 14, which is a situation where the magnitude of the current is varied by changing the torque command, it can be confirmed that the current ripple does not increase at any of the pulse transition points regardless of the situation in which the magnitude of the current varies. In Fig. 15(a) and (b), the magnitude of the current at the pulse number transition point ($N = 21 \rightarrow 15$) was controlled to be the rated current and half of the rated current. In both cases, the current ripple does not increase due to R_{err} being controlled at a small value.

Fig. 16 shows a experimental waveform where the proposed algorithm operates properly in the overmodulation region. The dynamic overmodulation technique outputs a feasible new voltage vector by correcting the phase of vector. As shown in Fig. 10, the algorithm proposed in this article is located before the overmodulation controller. Therefore, the overmodulation technique does not affect the proposed methods. As a result, it can be confirmed that the proposed algorithm operates properly, and the control period and fundamental frequency are well synchronized even in the overmodulation region.

IV. Conclusion

In this article, a compensation method for the magnitude and phase error of the output voltage caused by time delay in synchronized SVPWM and a pulse number transition point to minimize the synchronous phase error were proposed. In addition, a method for compensating the synchronous phase error without using a PLL was proposed to eliminate the disadvantages of using PLL. The validity of the proposed methods was verified through experimental results, which showed that the magnitude of the synchronous phase error decreased with application of the proposed methods.

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