Medium Frequency Output Impedance Limits of Switched-Capacitor Circuits

Dengke Zheng, Yuhang Yang, Shiming Hu, and Yan Deng

***Abstract*—As an intrinsic power loss of switched-capacitor circuits (SCCs), capacitor charge-sharing loss reduces the system efficiency. In this article, the approach based on q-u curves of capacitors is proposed to calculate capacitor charge-sharing loss precisely. By considering both capacitor charge-sharing loss and conduction loss, the output impedance of an SCC with a finite output capacitance can be modeled accurately in medium switching frequency. Compared with the previous modeling techniques, the proposed modeling method called $R_{\rm LSL}$ not only counts the output capacitor effect but also applies to a wide range of well-posed switched capacitor circuits. Several high-order SCCs are taken as examples to validate the accuracy of $R_{\rm LSL}$ via simulations and experiments and it could be corroborated that $R_{\rm LSL}$ can predict the output impedance precisely with the change of switching frequency, output capacitor, and duty cycle in the mid-band.**

***Index Terms*—Mid-band, modeling, switched capacitor (SC).**

NOMENCLATURE

C_i	*i*th flying capacitor.
$C_{\rm out}$	Output capacitor.
C_{ph}^n	Total equivalent capacitance of phase *n*.
R_c	Equivalent series resistance (ESR) of flying capacitors.
R_s	Parasitic resistance of the switch.
R_o	ESR of output capacitors.
S_j	*j*th switch.
V_i	Initial voltage of C_i.
V_{ti}	Final voltage of C_i.
V_{sti}	Steady-state voltage of C_i.
E_i	Energy loss in energy dissipation equivalent circuit (EDEC) of C_i.
Δu_i	Difference between V_{ti} and V_{sti}.
Δu_{C_i}	Difference between V_i and V_{ti}.
$I_{l\_c}^n$	Current of branch *l* in the constant stage of phase *n*.
$I_{C_i\_c}^n$, $I_{S_j\_c}^n$	Current through C_i, S_j in the constant stage of phase *n*.
f_l , f_u	Lower, the upper boundary of mid-band.
$a_{C_i}^n$	Total charge multiplier to C_i in the *n*th phase.
$a_{C_i\_c}^n$, $a_{S_j\_c}^n$	Charge multiplier to C_i, S_j in the constant stage of phase *n*.
$a_{C_i\_p}^n$	Charge multiplier to C_i in the pulse stage of phase *n*.
$a_{C_{\rm out}\_c}^n$	Charge multiplier to $C_{\rm out}$ in the constant stage of phase *n*.
$a_{C_{\rm out}\_p}^n$	Charge multiplier to $C_{\rm out}$ in the pulse stage of phase *n*.
$E_{\rm LSL}$	Calculated energy loss in the LSL model.
$R_{\rm LSL}$	Output impedance corresponding to $E_{\rm LSL}$.
$E_{{\rm LSL}\_R_o}$	Additional energy loss considering the effect of R_o.
$R_{{\rm LSL}(M)}$	Modified output impedance considering the effect of R_o.

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I. INTRODUCTION

DUE TO the merits of small size, high power density, and high efficiency, switched-capacitor circuits (SCCs) have been extensively used, such as power harvesting applications, the power supply for electric vehicles, and so forth [1], [2], [3], [4]. Nonetheless, intrinsic power loss, also known as capacitor charge-sharing loss, exists in SCCs, which restricts their high-power applications [5]. Calculating the capacitor charge-sharing loss precisely is important to predict and improve the performance of SCCs.

A generic SCC model has been proposed in [6]. As shown in Fig. 1, it contains an ideal dc–dc transformer and a serial resistive output impedance. The conversion ratio, completely depending on the topology, represents the ideal voltage gain of an SCC, and the equivalent output impedance, reflecting the power loss directly [7], has been used to evaluate the performance of SCCs [8], [9]. In recent years, many modeling methods have been developed to calculate the equivalent output impedance [1], [2], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22]. The concepts of slow-switching limit (SSL) and fast-switching limit (FSL) presented in [17] are widely applied. However, the SSL is only applicable within a relatively low-frequency band and the FSL is for high frequency, i.e., both the SSL and FSL are not suitable in a wide medium frequency range [19].

To resolve this question, the method proposed in [18] combines the SSL and FSL into one curve to estimate output impedance. In [1], the voltage-gap modeling method has been

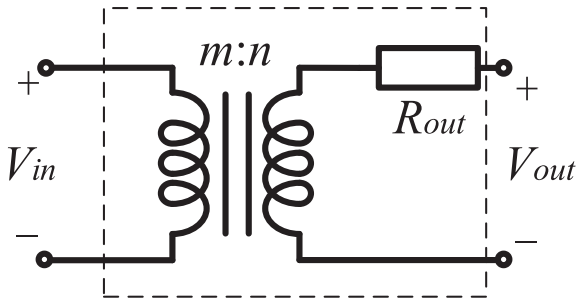

Fig. 1. Generic model of an SCC.

introduced for single-stage SCCs. Based on the average current of flying capacitors, a mathematical expression of output impedance has been demonstrated in [2]. As outlined in [19], these modeling methods neglect the output capacitor effect and are precise only under the huge output capacitor condition. However, in some applications especially when the circuit size is limited, a large output capacitor is unfit and the modeling methods mentioned previously are all incompetent.

The transient calculation-based modeling technique proposed in [19] takes the output capacitor effect into account for the first time but it is only suitable for three types of simple dual-phase SCCs without coupling loops. In [20], although the output capacitor effect is not included, the curvature-based average modeling method, which relates the SSL and FSL impedances to the total output impedance can be applied to the SCC with a finite output capacitance as well. However, it is for the topology in which the equivalent circuits of each phase are first-order as the time constants of the equivalent circuits of each phase are necessary to obtain the output impedance. In [21], a modeling method considers the finite terminal capacitances, input and output capacitances, for a two-to-one SC converter. It could be found that there scarcely exist modeling techniques fitting more sophisticated converters, which have more components and interconnections under the restricted output capacitor condition, e.g., the multistage Dickson topology, the high-order Ladder topology, and so forth.

Previous researches almost based modeling upon the analysis of currents and voltages directly or indirectly but neither the current nor voltage can paint the model and nature of the nonlinear circuit comprehensively [23]. The essential character of switching circuits is the stored energy and its flowing alongside the translation of the circuit configuration [23] and the energy redistribution of the SCCs always accompanies the charge transfer. Therefore, aiming to model the SCC precisely, this article studies the relationship between the energy loss and the charge transfer of the SCC with a limited output capacitor in the mid-band.

In this article, the capacitor charge-sharing loss can be calculated accurately from the perspective of stored electric potential energy (EPE) and a general expression can be derived, which is elaborated in Section II. Based on the conclusion drawn in Section II, the simplified phase equivalent circuit of the SCC is analyzed and the lower switching limit (LSL) is introduced in Section III. In Section IV, the four-to-one Dickson topology [24] is taken as an example to calculate the R_{LSL}. Subsequently, the accuracy of the proposed modeling method is confirmed by the digital simulation in Section V and the experiment in Section VI. Finally, Section VII concludes this article.

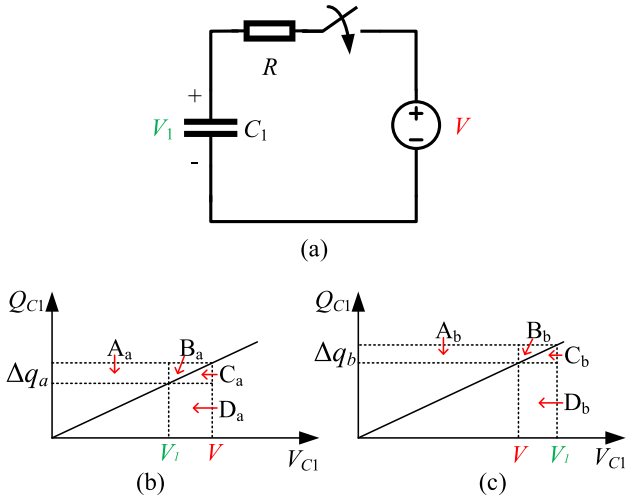

Fig. 2. Capacitor is charged or discharged by a voltage source. (a) Circuit. (b) Q-u curve of C_1 when $V_1 < V$. (c) Q-u curve of C_1 when $V_1 > V$.

II. Loss Analysis With Q-U Curves

The capacitor charge-sharing loss happens when a capacitor is charged or discharged by another capacitor or a voltage source and it could be calculated by state equations. For example, Fig. 2(a) shows a capacitor with initial voltage V_1, which is charged or discharged by a voltage source. The current and the voltage across the resistance R can be obtained easily by solving a differential equation; then the power loss could be computed. However, when evaluating the power loss of complex SCCs, which usually are high-order circuits, this traditional approach based on current and voltage usually cannot derive a generalized expression of output impedance, which means difficulties in optimizing circuits. In fact, the energy loss of the circuit in Fig. 2(a) can be analyzed in the view of EPE, which is directly revealed in the q-u curve of C_1.

As plotted in Fig. 2(b), the capacitor C_1 is charged by the voltage source V, from $V_{C1} = V_1$ to $V_{C1} = V$, and the charge flowing into C_1 is represented by Δq_a. $\mathrm{A_a}$, $\mathrm{B_a}$, $\mathrm{C_a}$, and $\mathrm{D_a}$ represent the geometry they point to, respectively. The increment of EPE in C_1 is the area of the trapezoid $\mathrm{C_a}$+$\mathrm{D_a}$, and meanwhile, the decrement of EPE in the voltage source is the area of the rectangle $\mathrm{A_a}$+$\mathrm{B_a}$+$\mathrm{C_a}$. Energy loss can then be easily obtained by the difference between two areas. Owing to the geometrical symmetry, the area of $\mathrm{A_a}$ is equal to the area of $\mathrm{D_a}$, and therefore, the energy loss of this circuit is indicated by the area of $\mathrm{B_a}$ or $\mathrm{C_a}$. This analytical method can be applied to the discharge process of C_1 displayed in Fig. 2(c).

To derive a generic expression of capacitor charge-sharing loss, a complex circuit shown in Fig. 3 only containing capacitors and voltage sources as the energy storage elements is analyzed, in which C_1, C_2 are discharging-capacitors and

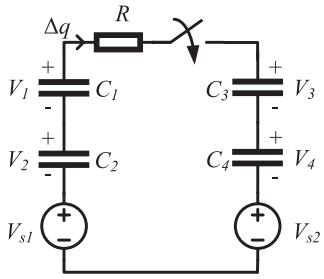

Fig. 3. Circuit using capacitors and voltage sources to store energy.

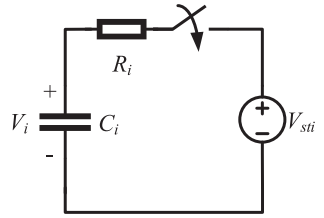

Fig. 4. Energy dissipation equivalent circuit of C_i.

C_3, C_4 are charging-capacitors. It is clear that the reduction in stored electric potential energy in the circuit equals the energy dissipated in the loop lumped resistance R. Then, the energy dissipation equivalent circuit (EDEC) of each capacitor could be defined and illustrated in Fig. 4, where the amount of charge transfer in EDEC and the original circuit is equivalent.

The capacitance C_i and initial voltage V_i of capacitor C_i in EDEC are equal to their counterparts in the original circuit, where the index i refers to the ith capacitor; the V_{sti} is the steady-state voltage of C_i in the original circuit, but R_i is irrelevant to R as the energy loss is independent of circuit resistance in this scenario. E_i can be defined as the energy loss associated with C_i, which is the energy loss in EDEC of C_i. It is distinct that the q-u curve of capacitor C_i in the original circuit and EDEC are the same, for the capacitance C_i, initial voltage V_i, and the amount of charge transfer are equal. The q-u curves of all capacitors in Fig. 3 or their EDECs could be plotted in Fig. 5(a) and (b), both in full-charging and partial-charging patterns, where V_{ti} refers to the final voltage of C_i when the switch turns OFF. In the full-charging pattern V_{ti} is equivalent to V_{sti} and in the partial-charging pattern V_{ti} and V_{sti} are not equal. Moreover, a represents the initial state and b represents the final state in the q-u plane.

A. Derivation of Energy Loss

In the steady state, the relationship among the voltages of each energy storage element could be derived as

$$V_{st1} + V_{st2} + V_{s1} = V_{st3} + V_{st4} + V_{s2} \tag{1}$$

and the energy loss could be defined as the difference between the initial total energy and the final total energy, which can be calculated as

$$E_{\text{loss}} = \sum_i \Delta E_{C_i} + \sum_j \Delta E_{V_{sj}} \tag{2}$$

where ΔE_{Ci} is the energy loss of C_i and ΔE_{Vsj} is the energy loss of the voltage source V_{sj}. Via the q-u curve, ΔE_{Ci} of discharging capacitor can be expressed as

$$\Delta E_{Ci} = E_i + V_{sti} \cdot \Delta q, (i = 1, 2) \tag{3}$$

and ΔE_{Ci} of charging capacitor can be expressed as

$$\Delta E_{Ci} = E_i - V_{sti} \cdot \Delta q, (i = 3, 4) \tag{4}$$

where Δq is the charge flowing into/out of capacitors or voltage sources during each charging/discharging stage. Furthermore, the Δq of all voltage sources and capacitors is equal as all of them are series in one close loop. According to (1)–(4), the total energy loss can be yielded as

$$E_{\text{loss}} = \sum_{i=1}^{4} E_i. \tag{5}$$

Theorem 1: The energy loss of the circuit, which only utilizes capacitors and voltage sources to store energy is equivalent to adding up the energy loss of all capacitors' EDEC.

Based on (5), Theorem 1 can be deduced and the confirmation is presented in Appendix A. Through the q-u curves, E_i can be expressed as follows:

$$E_i = \Delta q \cdot \Delta u_i + \frac{\Delta q^2}{2C_i}, (i = 1, 2, 3, 4) \tag{6}$$

where the Δu_i is the difference between the final voltage and the steady-state voltage of C_i, and it is non-negative. The remarkable thing is that the Δu_i equals 0 only in the full-charging pattern. By substituting (6) into (5), the energy loss can be reduced to

$$E_{\text{loss}} = \sum_{i=1}^{4} \left(\Delta q \cdot \Delta u_i + \frac{\Delta q^2}{2C_i} \right) \tag{7}$$

where the Δq can be expressed by the component of the charge multiplier vector [17] but the Δu_i needs to be derived in the partial-charging pattern.

B. Derivation of Δu_i

The circuit presented in Fig. 6 contains a discharging capacitor C_1, a charging capacitor C_2, and a voltage source V_s. The voltage across the switch is denoted as ΔV before it is closed. Apparently

$$\Delta V = V_1 - V_2 - V_s. \tag{8}$$

After the switch is closed, the current i and the voltage across the capacitor C_1 can be easily derived as

$$i = \frac{\Delta V}{R} e^{-\frac{t}{\tau}} \tag{9}$$

$$u_{C_1} = \left(V_1 - \frac{\Delta V \tau}{RC_1} \right) + \frac{\Delta V \tau}{RC_1} e^{-\frac{t}{\tau}} \tag{10}$$

where τ is the time constant. Then, Δu_1 can be computed as

$$\Delta u_1 = u_{C_1}(t_{\text{on}}) - u_{C_1}(\infty) = \frac{\Delta V \tau}{RC_1} e^{-\frac{t_{\text{on}}}{\tau}} \tag{11}$$

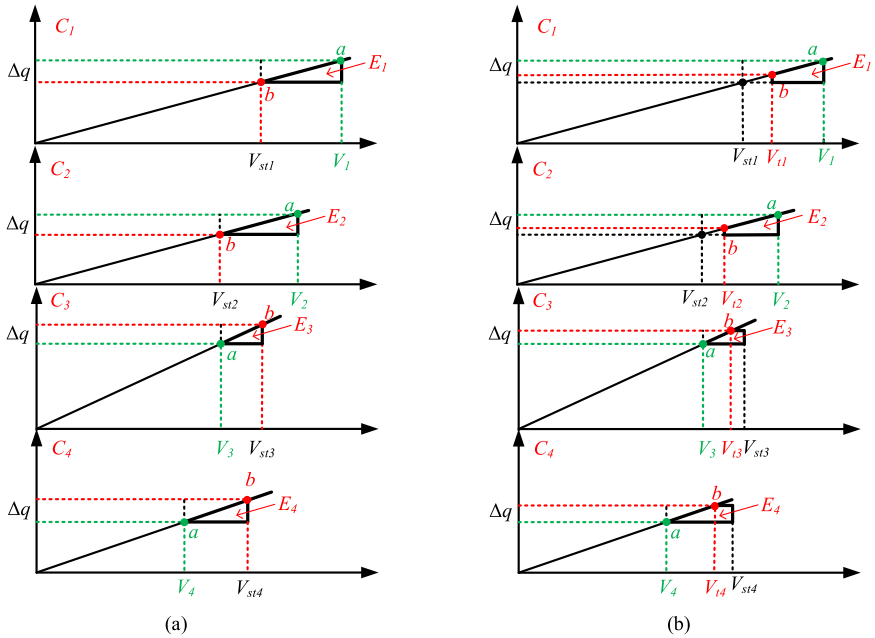

Fig. 5. Q-u curves of all capacitors in Fig. 3. (a) In full-charging pattern. (b) In partial-charging pattern.

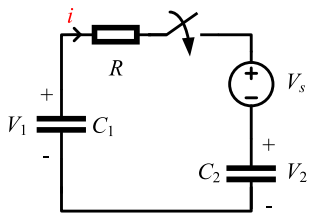

Fig. 6. Capacitor is charged or discharged by another capacitor.

where $t_{\rm on}$ is the duration of circuit conduction and ΔV can be procured via

$$\Delta q = \int_0^{t_{\rm on}} i dt. \tag{12}$$

According to (12), ΔV is calculated to be

$$\Delta V = \frac{\Delta q}{(1 - e^{-\frac{t_{\rm on}}{\tau}})C_{eq}} \tag{13}$$

where C_{eq} is the equivalent capacitor of the circuit in Fig. 6. Substituting (13) into (11) yields

$$\Delta u_1 = \Delta u_{C_1} \frac{e^{-\frac{t_{\rm on}}{\tau}}}{1 - e^{-\frac{t_{\rm on}}{\tau}}} \tag{14}$$

whereΔu_{C_i} is the voltage change of C_i during the switch is closed and it is equal to the difference between the final voltage and the initial voltage; clearly, it is positive. Similarly, for the charging capacitor C_2, Δu_2 is computed to be

$$\Delta u_2 = \Delta u_{C_2} \frac{e^{-\frac{t_{\rm on}}{\tau}}}{1 - e^{-\frac{t_{\rm on}}{\tau}}}. \tag{15}$$

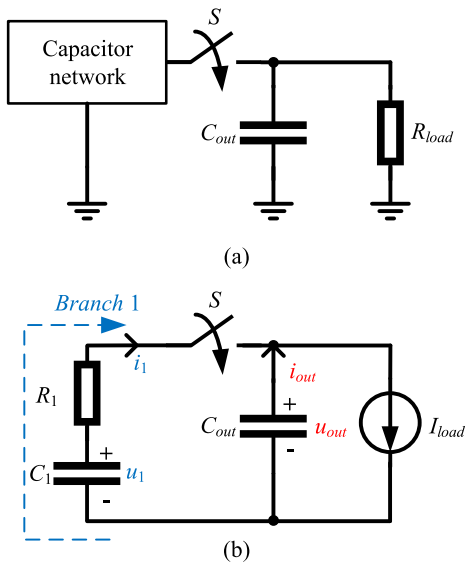

Fig. 7. Circuit of each phase in a SCC. (a) Equivalent circuit. (b) Simplified circuit.

III. Analysis of Energy Loss on Phase Circuit

The equivalent circuit of each phase in an SCC is shown in Fig. 7(a). The capacitor network contains the voltage sources, switches, and flying capacitors. It is clear that the circuit configuration of the capacitor network changes with the phase shifting. In some phases when the switch S is OFF, the output capacitor effect does not exist and the energy loss can be obtained without error via (7) as the equivalent circuit only utilizes capacitors and voltage sources to store energy. However, in other phases that the switch S is ON, the output capacitor effect exists and should be considered. Hence, the analysis under the case that the switch S is ON is necessary to get the energy loss of an SCC in a period.

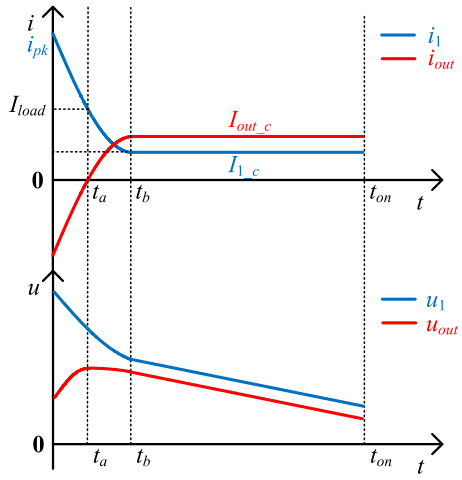

Fig. 8. Waveforms of variables in simplified phase circuit.

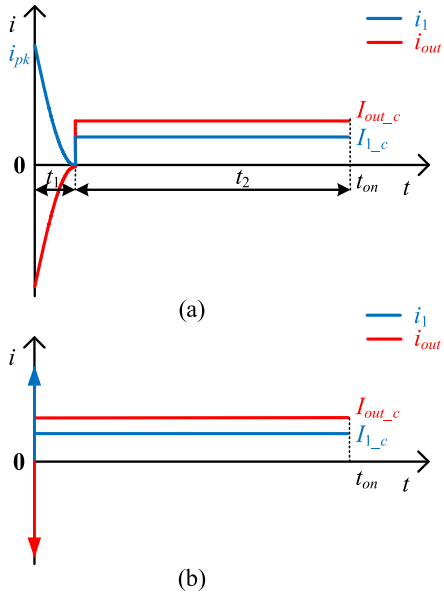

Fig. 9. Schematic diagram of current waveform. (a) In two-stage model. (b) In LSL model.

As Fig. 7(b) displays, the capacitor network in Fig. 7(a) is substituted by branch 1 for the convenience of analysis. Branch 1 consists of a flying capacitor C_1 and a lumped parasitic resistance R_1. Furthermore, given that the load resistance is usually much larger than the parasitic one and the current of any branch is continuous in mid-band, the load resistance is replaced by a current source.

The ensuing circuit analysis is based on the simplified phase circuit plotted in Fig. 7(b). Given the character of SCCs, the circuit analysis has the following two restrictions.

1) The switch S closes at $t = 0$, then the capacitor C_1 discharges, and the output capacitor C_{out} is charged.
2) The switch S opens at $t = t_{\text{ON}}$ again and the voltage polarity of C_1 and C_{out} remains the same in the interim.

The waveforms of u_1, i_1, u_{out}, and i_{out} can be plotted and illustrated in Fig. 8 under these restrictions.

A. Simplified Phase Circuit Analysis

1) Stage 1. [0, T_a]: After the switch S is closed, due to the voltage mismatch between C_1 and C_{out}, there will be a surge of pulse current as the parasitic resistance is usually small. Using Kirchhoff's Voltage Law and Kirchhoff's Current Law (KCL) yields

$$i_1 = \frac{u_1 - u_{\text{out}}}{R_1} \tag{16}$$

$$i_{\text{out}} = I_{\text{load}} - i_1. \tag{17}$$

With the capacitor C_1 discharging and the output capacitor C_{out} charging, u_1 decreases, and u_{out} increases. According to (16) and (17), i_1 and -i_{out} decrease rapidly. When $t = t_a$, i_{out} equals 0 and i_1 equals I_{load}. At the same time, the output voltage u_{out} reaches the peak value. It is distinct that the peak value of the charging/discharging current is extremely large when the SCC works in mid-band, namely $i_{pk} >> I_{\text{load}}$.

In this stage, the flying capacitor not only charges the output capacitor C_{out} but supplies power to the load as well.

2) Stage 2. [t_a, T_b]: When $t = t_a$, the output capacitor turns to discharge and the output voltage starts to decrease. In this stage, i_1 and -i_{out} proceed to decrease until $t = t_b$ when they both reach the steady state. Owing to $i_{pk} >> I_{\text{load}}$, $t_a \approx t_b$ can be inferred in mid-band. The energy dissipation of stage 2 is only produced by conduction loss.

3) Stage 3. [t_b, T_{on}]: In this stage, the current of any branch keeps constant and its value is determined by the proportion of the capacitance of each branch and the load current. The voltage of C_1 and C_{out} drops synchronously and has a constant gap because of R_1. The energy dissipation of stage 3 is only produced by conduction loss.

B. Two-Stage Model

From Fig. 8, the simplified phase circuit can be divided into three stages according to the branch current but it can be approximated in two stages for analysis as $t_a \approx t_b$ in mid-band, which is shown in Fig. 9(a).

1) Pulse Stage: Owing to the tiny parasitic resistance R_1, the process of charging/discharging between the flying capacitor C_1 and the output capacitor C_{out} reaches the steady state quickly, and the current through capacitors has a steep change, which lasts a short time t_1. Therefore, the effect of the load is neglected and the energy flow is considered to happen only between capacitors, i.e., the energy loss in this stage can be obtained by (7) directly.

2) Constant Stage: In this stage, the equivalent capacitors of each branch discharge simultaneously and supply energy to the load together, which leads to a constant current in each branch lasting a long time t_2.

C. LSL Model

Bearing in mind that t_1 is much smaller than t_2 in mid-band, the two-stage model could be further simplified to the LSL model, as presented in Fig. 9(b). In fact, the LSL model is exactly

the real model under the conditions of neglecting parasitic resistance and using the current source load.

1) Pulse Stage: In the LSL model, the current through capacitors is deemed as the current impulse. Denote the total charge that flows from C_1 during the time interval $[0, t_{\rm ON}]$ as Δq. The charge transfer Δq_p of the flying capacitor in this stage is the difference between Δq and the charge transfer in the constant stage, which can be expressed as

$$\Delta q_p = \Delta q - I_{1\_c} t_{\rm on}. \tag{18}$$

Via (7), the energy loss in this stage can be computed to be

$$E_{\rm LSL\_p} = \frac{\Delta q_p^2}{2C_{eq}} \tag{19}$$

where $\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_{\rm out}}$.

2) Constant Stage: In the constant stage, the current of any branch keeps constant and its value is determined by the proportion of the capacitance of each branch and the load current. We obtain

$$I_{1\_c} = \frac{C_1}{C_1 + C_{\rm out}} I_{\rm load}. \tag{20}$$

Subsequently, the energy loss in this stage can be calculated to be

$$E_{\rm LSL\_c} = I_{1\_c}^2 \cdot R_1 \cdot t_{\rm on}. \tag{21}$$

According to (19) and (21), the energy loss during simplified-phase-circuit conduction can be obtained

$$E_{\rm LSL} = E_{\rm LSL\_p} + E_{\rm LSL\_c} \tag{22}$$

where $E_{\rm LSL\_p}$ represents the energy loss caused by the capacitor charge-sharing loss and $E_{\rm LSL\_c}$ refers to the energy loss generated by the conduction loss.

D. Generalization to SCCs

For a multiphase SCC, as shown in [25], which switches between more than two configurations in turn, the energy loss of each phase can be computed via the LSL model and the total energy loss in a period can be obtained by accumulation.

The abovementioned analysis is based on the simplified phase circuit presented in Fig. 7(b). The other cases are discussed below, based on the equivalent phase circuit demonstrated in Fig. 7(a).

1) Cases that S is Open: It is clear that the LSL model is still applicable in this case but the current of each capacitor is 0 in the constant stage.

2) Cases that S is Closed but With a Sophisticated Capacitor Network: No matter how sophisticated the capacitor network is, as long as the parasitic resistance of every branch is much smaller than load resistance, the branch current could be approximately divided into two stages and the LSL model is suitable in mid-band.

For an SCC with N phases, its energy loss in a switching cycle can be derived approximately using the LSL model

$$E_{\rm LSL} = \sum_{n=1}^{N} E_{\rm LSL}^n \tag{23}$$

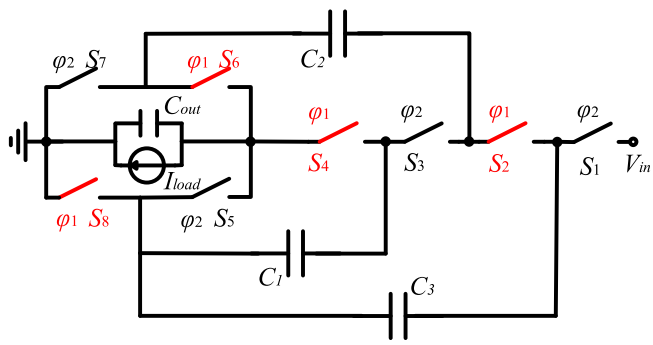

Fig. 10. Four-to-one Dickson topology.

where $E_{\rm LSL}^n$ is the energy loss in the nth phase. Then, the average output impedance for the LSL model can be obtained

$$R_{\rm LSL} = \frac{E_{\rm loss} \cdot f_s}{I_{\rm load}^2} \tag{24}$$

where f_s is the switching frequency.

Theorem 2: $R_{\rm LSL}$ *is the lower limit of output impedance in the mid-band.*

The corroboration of Theorem 2 is elaborated in Appendix B.

E. Summarization

In this section, three simplifications are taken to calculate the energy loss of the equivalent phase circuit.

1) *Circuit Simplification:* The load is deemed as a current source, which means we use the average output current to calculate.
2) *Model Simplification:* The real model is simplified to the two-stage model as $t_a \approx t_b$ in mid-band.
3) *Analysis Simplification:* The two-stage model is simplified to the LSL model to facilitate the calculation, due to $t_1 << t_2$ in the mid-band.

All the abovementioned simplifications are exactly based on the condition that the parasitic resistance of any branch is much smaller than load resistance, which is satisfied naturally in practical SCCs. Thus, these simplifications are sensible and do not introduce large errors.

IV. Modeling of the Switched Capacitor Circuit

The four-to-one Dickson topology presented in Fig. 10 is taken as an example to explain the process of calculating the $R_{\rm LSL}$ of an SCC. The calculation is under the following assumptions.

1) Each of the flying capacitors is deemed as an ideal capacitor with an equal equivalent series resistance (ESR) R_c.
2) All the switches have an equal ON-state resistance R_s.
3) The circuit operates in two phases demonstrated in Fig. 11(a) and (b), where R_l and C_{eql} are the lumped resistance and equivalent capacitor of branch l, respectively.

Because the charge transfer in the constant stage is necessary to compute the energy loss in the pulse stage, the constant stage is analyzed at first.

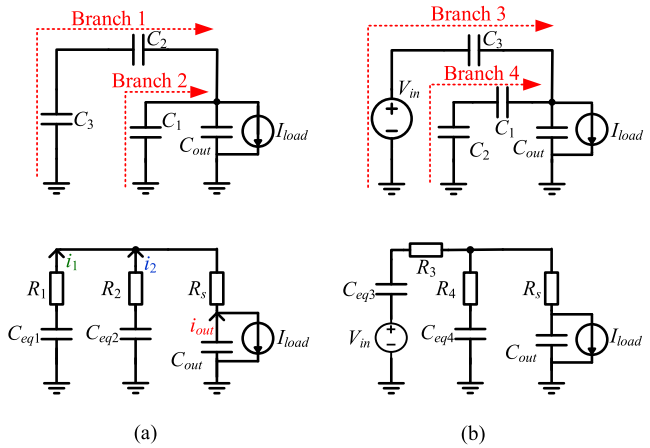

Fig. 11. Four-to-one Dickson topology in each phase. (a) Phase 1. (b) Phase 2.

A. Constant Stage

Before the constant stage, the current of each branch has reached the steady state. In the constant stage, the voltage and the voltage attenuation rate of the parallel-connected branches are the same. Hence, the current in parallel connected branches is proportional to their equivalent capacitance. For the four-to-one Dickson topology, the relationship among the current of different branches can be procured. In the constant stage of phase 1, we obtain

$$I^1_{1\_c} : I^1_{2\_c} : I^1_{\text{out}\_c} = C_{eq1} : C_{eq2} : C_{\text{out}} \tag{25}$$

where $I^n_{l\_c}$ is the current of branch l in the constant stage of phase n. Via KCL, it can be found that

$$I^1_{1\_c} + I^1_{2\_c} + I^1_{\text{out}\_c} = I_{\text{load}}. \tag{26}$$

From (25) and (26), the current of each branch in the constant stage can be expressed by I_{load}. For an SCC with N phases, considering the same dead-time in each phase, its energy loss in the constant stage of a switching cycle can be derived as

$$E_{\text{LSL}\_c} = \sum_{l}\sum_{n=1}^{N} {I^n_{l\_c}}^2 \cdot R_l \cdot \frac{d}{f_s} \tag{27}$$

where d is the duty cycle and f_s is the switching frequency. Dividing the energy loss on R_c and R_s yields

$$E_{\text{LSL}\_c} = \sum_{j}\sum_{n=1}^{N} {I^n_{S_{j\_c}}}^2 \cdot R_s \cdot \frac{d}{f_s} + \sum_{i}\sum_{n=1}^{N} {I^n_{C_{i\_c}}}^2 \cdot R_c \cdot \frac{d}{f_s} \tag{28}$$

where $I^n_{S_{j\_c}}$ is the current through the switch S_j in the constant stage of phase n and $I^n_{C_{i\_c}}$ refers to the current through the flying capacitor C_i in the constant stage of phase n.

The charge flowing into C_i in the constant stage of phase n is denoted as $\Delta q^n_{C_{i\_c}}$. Analogously to the concept of charge multiplier in [17] and [26], the charge multiplier to C_i in the constant stage of phase n can be defined as

$$a^n_{C_{i\_c}} = \frac{\Delta q^n_{C_{i\_c}}}{q_{\text{out}}} \tag{29}$$

where q_{out} is the charge delivered to the load during a period. It is distinct that $a^n_{C_{i\_c}}$ is positive if the charge flows into C_i, negative otherwise. Similarly, the charge multiplier to S_j in the constant stage of phase n can be defined as well, which is denoted as $a^n_{S_{j\_c}}$. It can be specified that $a^n_{S_{j\_c}}$ is positive when the current flows from the drain to the source, and vice versa.

For the four-to-one Dickson circuit, its flying capacitor charge multiplier vector in the constant stage of phase n $\mathbf{a^n_{C\_c}}$ can be given by

$$\begin{aligned}\mathbf{a^1_{C\_c}} &= \begin{bmatrix} a^1_{C_{1\_c}} & a^1_{C_{2\_c}} & a^1_{C_{3\_c}} \end{bmatrix}^T \\ &= \begin{bmatrix} -\frac{d\cdot C_{eq2}}{C^1_{ph}} & \frac{d\cdot C_{eq1}}{C^1_{ph}} & -\frac{d\cdot C_{eq1}}{C^1_{ph}} \end{bmatrix}^T \end{aligned} \tag{30}$$

$$\mathbf{a^2_{C\_c}} = \begin{bmatrix} \frac{d\cdot C_{eq4}}{C^2_{ph}} & -\frac{d\cdot C_{eq4}}{C^2_{ph}} & \frac{d\cdot C_{eq3}}{C^2_{ph}} \end{bmatrix}^T \tag{31}$$

where C^1_{ph} and C^2_{ph} are the total equivalent capacitance of phase 1 and phase 2, respectively, which can be expressed as

$$C^1_{ph} = C_{eq1} + C_{eq2} + C_{\text{out}} \tag{32}$$

$$C^2_{ph} = C_{eq3} + C_{eq4} + C_{\text{out}}. \tag{33}$$

For the four-to-one Dickson circuit, the switch charge multiplier vector in the constant stage of phase n $\mathbf{a^n_{S\_c}}$ can be obtained moreover

$$\mathbf{a^1_{S\_c}} = \begin{bmatrix} 0 & \frac{d\cdot C_{eq1}}{C^1_{ph}} & 0 & \frac{d\cdot C_{eq2}}{C^1_{ph}} & 0 & -\frac{d\cdot C_{eq1}}{C^1_{ph}} & 0 & -\frac{d\cdot (C_{eq1}+C_{eq2})}{C^1_{ph}} \end{bmatrix}^T \tag{34}$$

$$\mathbf{a^2_{S\_c}} = \begin{bmatrix} \frac{d\cdot C_{eq3}}{C^2_{ph}} & 0 & \frac{d\cdot C_{eq4}}{C^2_{ph}} & 0 & -\frac{d\cdot (C_{eq3}+C_{eq4})}{C^2_{ph}} & 0 & -\frac{d\cdot C_{eq4}}{C^2_{ph}} & 0 \end{bmatrix}^T. \tag{35}$$

The relationship between $I^n_{C_{i\_c}}$ and $\Delta q^n_{C_{i\_c}}$ can be written easily as

$$\Delta q^n_{C_{i\_c}} = I^n_{C_{i\_c}} \cdot \frac{d}{f_s}. \tag{36}$$

From (29) and (36), we obtain

$$I^n_{C_{i\_c}} = \frac{a^n_{C_{i\_c}}}{d} I_{\text{load}}. \tag{37}$$

Analogously

$$I^n_{S_{j\_c}} = \frac{a^n_{S_{j\_c}}}{d} I_{\text{load}}. \tag{38}$$

According to (24), (28), (37), and (38), the output impedance corresponding to the total energy loss of the constant stage in the LSL model can be derived as

$$R_{\text{LSL}\_c} = \frac{1}{d} \cdot \left(\sum_{j}\sum_{n=1}^{N} {a^n_{S_{j\_c}}}^2 \cdot R_s + \sum_{i}\sum_{n=1}^{N} {a^n_{C_{i\_c}}}^2 \cdot R_c \right). \tag{39}$$

B. Pulse Stage

The charge flowing into C_i in the pulse stage of phase n is denoted as $\Delta q^n_{C_{i\_p}}$. According to (18), we obtain

$$\Delta q^n_{C_{i\_p}} = a^n_{C_i} q_{\text{out}} - \Delta q^n_{C_{i\_c}} \tag{40}$$

where $a^n_{C_i}$ is the total charge multiplier to the flying capacitor C_i in the nth phase. As described in [17], $a^n_{C_i}$ is positive when the charge flows into C_i in phase n. The charge flowing into the output capacitor in the pulse stage of phase n can be determined by KCL and $\Delta q^n_{C_{i\_p}}$, which is denoted as $\Delta q^n_{C_{\text{out}\_p}}$. Clearly, $\Delta q^n_{C_{\text{out}\_p}}$ is always positive as the output capacitor charges in the pulse stage and discharges in the constant stage.

The energy loss in the pulse stage can be obtained via (7)

$$E_{\text{LSL}\_p} = \sum_i \sum_{n=1}^{N} \frac{\Delta q^n_{C_{i\_p}}{}^2}{2 \cdot C_i} + \sum_{n=1}^{N} \frac{\Delta q^n_{C_{\text{out}\_p}}{}^2}{2 \cdot C_{\text{out}}}. \tag{41}$$

Analogously to $a^n_{C_{i\_c}}$, the charge multiplier to C_i and C_{out} in the pulse stage of phase n can be defined, respectively, as

$$a^n_{C_{i\_p}} = \frac{\Delta q^n_{C_{i\_p}}}{q_{\text{out}}} \tag{42}$$

$$a^n_{C_{\text{out}\_p}} = \frac{\Delta q^n_{C_{\text{out}\_p}}}{q_{\text{out}}}. \tag{43}$$

Comparing (29), (40), and (42) yields

$$a^n_{C_i} = a^n_{C_{i\_c}} + a^n_{C_{i\_p}}. \tag{44}$$

It can be found that the concept of the charge multiplier defined in [17] is divided into two parts with different meanings in this article. $a^n_{C_{i\_c}}$ represents the charge related to the conduction loss and $a^n_{C_{i\_p}}$ symbolizes the charge concerning the capacitor charge-sharing loss.

For the four-to-one Dickson circuit, its total flying capacitor charge multiplier vector in phase n $\mathbf{a^n_C}$ can be written as

$$\mathbf{a^1_C} = \left[\begin{array}{ccc} a^1_{C_1} & a^1_{C_2} & a^1_{C_3} \end{array}\right]^T = \left[\begin{array}{ccc} -\frac{1}{4} & \frac{1}{4} & -\frac{1}{4} \end{array}\right]^T \tag{45}$$

$$\mathbf{a^2_C} = \left[\begin{array}{ccc} \frac{1}{4} & -\frac{1}{4} & \frac{1}{4} \end{array}\right]^T. \tag{46}$$

Then, the flying capacitor charge multiplier vector in the pulse stage of phase n can be got by substituting (30), (31) and (45), (46) into (44).

Introducing (41)–(43) into (24) yields

$$R_{\text{LSL}\_p} = \sum_i \sum_{n=1}^{N} \frac{\left(a^n_{C_{i\_p}}\right)^2}{2 \cdot C_i \cdot f_s} + \sum_{n=1}^{N} \frac{\left(a^n_{C_{\text{out}\_p}}\right)^2}{2 \cdot C_{\text{out}} \cdot f_s}. \tag{47}$$

Finally, the total output impedance in the LSL model can be computed to be

$$R_{\text{LSL}} = R_{\text{LSL}\_c} + R_{\text{LSL}\_p}. \tag{48}$$

C. Relationship Between R_{LSL} and R_{SSL}

As outlined in [17], the R_{SSL} is derived under the condition of output voltage source, which can be regarded as a capacitor with an infinite capacitance.

From (25) and (26), it could be inferred that

$$\lim_{C_{\text{out}} \to \infty} I^n_{C_{i\_c}} = 0. \tag{49}$$

Therefore,

$$\lim_{C_{\text{out}} \to \infty} a^n_{C_{i\_c}} = 0 \tag{50}$$

$$\lim_{C_{\text{out}} \to \infty} a^n_{S_{j\_c}} = 0. \tag{51}$$

According to (39), (50), and (51), we get

$$\lim_{C_{\text{out}} \to \infty} R_{\text{LSL}\_c} = 0. \tag{52}$$

Because $a^n_{C_{\text{out}\_p}}$ is finite, introducing (44) and (50) into (47) yields

$$\lim_{C_{\text{out}} \to \infty} R_{\text{LSL}\_p} = \sum_i \sum_{n=1}^{N} \frac{\left(a^n_{C_i}\right)^2}{2 \cdot C_i \cdot f_s}. \tag{53}$$

According to [27], we know

$$R_{\text{SSL}} = \sum_i \sum_{n=1}^{N} \frac{\left(a^n_{C_i}\right)^2}{2 \cdot C_i \cdot f_s}. \tag{54}$$

Comparing (48) and (52)–(54) results in

$$\lim_{C_{\text{out}} \to \infty} R_{\text{LSL}} = R_{\text{SSL}}. \tag{55}$$

To some extent, R_{SSL} can be seen as a special case of R_{LSL} under the condition that the capacitance of C_{out} is infinite.

D. Definition of Mid-Band

The mid-band is defined as the frequency range of switching frequency that $f_s \in (f_l,\ f_u)$.

1) Lower Boundary f_l: In practical SCC, the current of any branch decays exponentially in the constant stage. To ensure the accuracy of modeling, the f_l is given as the minimum frequency at which the current of any branch decreases no more than 1/e. So, the following inequality holds at least:

$$\tau_a > \frac{d}{f_s} \tag{56}$$

where τ_a is the overall time constant, which is the weighted average of the individual time constants of each phase according to the duty ratio. Bearing in mind that the parasitic resistance is much smaller than the R_{load}, the parasitic resistance is not included when calculating the time constant. Via (56), we obtain

$$f_l = \frac{d}{\tau_a}. \tag{57}$$

For the four-to-one Dickson circuit, f_l can be computed to be

$$f_l = \frac{2d}{(C^1_{ph} + C^2_{ph}) \cdot R_{\text{load}}}. \tag{58}$$

2) Upper Boundary f_u: The premise of the analysis simplification from the two-stage model to the LSL model is $t_1 << t_2$. Hence, (59) should be satisfied

$$\frac{d}{f_s} >> \tau_p \tag{59}$$

where τ_p is the maximum time constant of all loops, which are composed of different branches and the output capacitor. For the high-order loops, some approximations are needed. The load

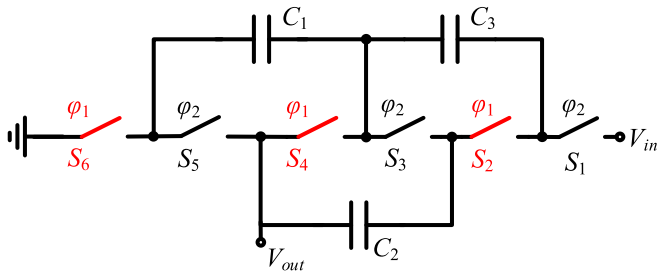

Fig. 12. Three-to-one Ladder topology.

TABLE I
PARAMETER LIST FOR SIMULATION VERIFICATION

Parameter	Value
V_{in}	20 V
C_1=C_2=C_3	22 μF
R_c	2 mΩ
R_s	0.9 mΩ
R_{load}	300 mΩ

resistance is not considered as the effect of the load is neglected in the pulse stage. By (59), f_u can be set as

$$f_u = \frac{d}{10\tau_p}. \tag{60}$$

E. ESR of Output Capacitor Effect

The ESR of C_{out} is denoted as R_o. The additional energy loss when considering the effect of R_o can be expressed as

$$E_{\text{LSL\_}R_o} = \sum_{n=1}^{N} {I^n_{C_{\text{out}}\_c}}^2 \cdot R_o \cdot \frac{d}{f_s} + I^2_{\text{load}} \cdot R_o \cdot \frac{1-dN}{f_s} \tag{61}$$

where $I^n_{C_{\text{out}}\_c}$ is the current through C_{out} in the constant stage of phase n. Analogously to (39), the additional output impedance can be expressed using the output capacitor charge multiplier in the constant stage of phase n

$$R_{\text{LSL\_}R_o} = \frac{1}{d} \cdot \sum_{n=1}^{N} {a^n_{C_{\text{out}}\_c}}^2 \cdot R_o + (1-dN) \cdot R_o \tag{62}$$

where $a^n_{C_{\text{out}}\_c}$ is given by

$$a^n_{C_{\text{out}}\_c} = -d \cdot \frac{C_{\text{out}}}{C^n_{ph}}. \tag{63}$$

When the effect of R_o is considered, the modified output impedance in the LSL model can be derived as

$$R_{\text{LSL}(M)} = R_{\text{LSL}} + R_{\text{LSL\_}R_o}. \tag{64}$$

V. VERIFICATION BY SIMULATION

A. R_{out} Versus F_s With Fixed d and C_{out}

The four-to-one Dickson circuit and the three-to-one Ladder topology presented in Fig. 12 are built in MATLAB with the parameters shown in Table I, respectively. The duty cycle is set to 50% and the output capacitor has a capacitance of 33 μF

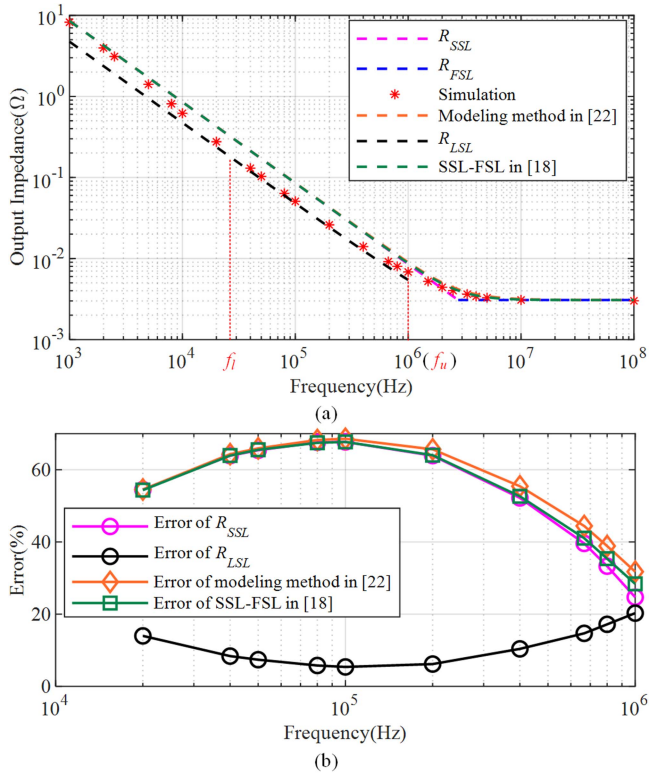

Fig. 13. Comparison between simulation and calculation for 4:1 Dickson circuit. (a) Results. (b) Error.

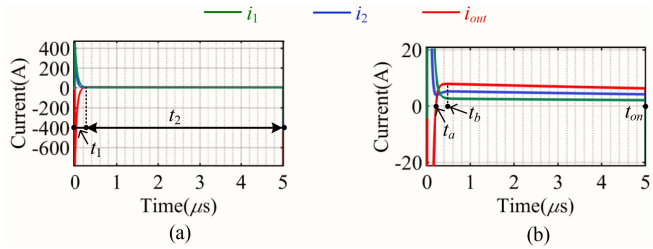

Fig. 14. Current waveforms of each branch in phase 1 of four-to-one Dickson circuit. (a) Zoom out. (b) Zoom in.

for both. For the four-to-one Dickson circuit, its f_l is calculated to be 25 kHz and the f_u is derived close to 1 MHz in the abovementioned conditions. For the three-to-one Ladder circuit, its f_l and f_u are computed approximately to be 33 kHz and 1 MHz, respectively.

A comparison between R_{SSL}, R_{FSL}, R_{LSL}, simulations and the modeling methods in [18] and [22] can be made based on the four-to-one Dickson circuit in Fig. 13(a) and errors at some frequencies in the mid-band are plotted in Fig. 13(b). Taking the current direction in Fig. 11(a) as positive, the current waveforms of each branch in phase 1 at 100 kHz are presented in Fig. 14. A comparison between R_{SSL}, R_{FSL}, R_{LSL}, and simulations for the three-to-one Ladder circuit is shown in Fig 15.

According to Figs. 13(a) and Fig. 15(a), R_{SSL}, R_{FSL}, and the modeling methods in [18] and [22] show a great match with simulation results at low-band or high-band. In Fig. 14, it could be found that the peak value of branch current is much larger

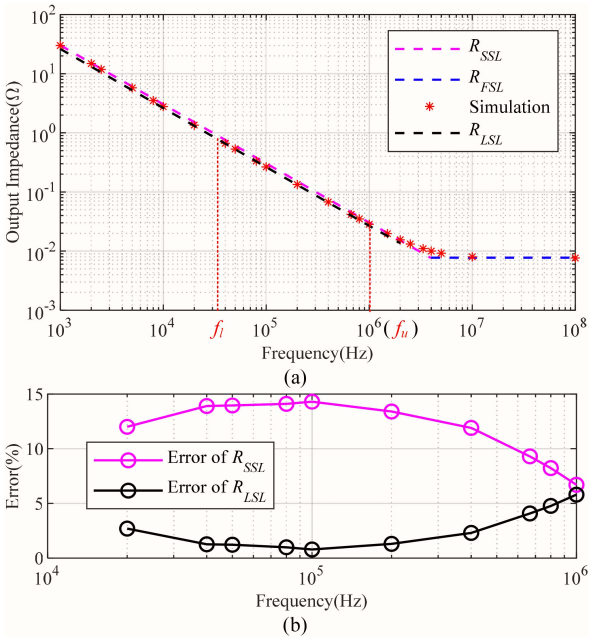

Fig. 15. Comparison between simulation and calculation for 3:1 Ladder circuit. (a) Results. (b) Error.

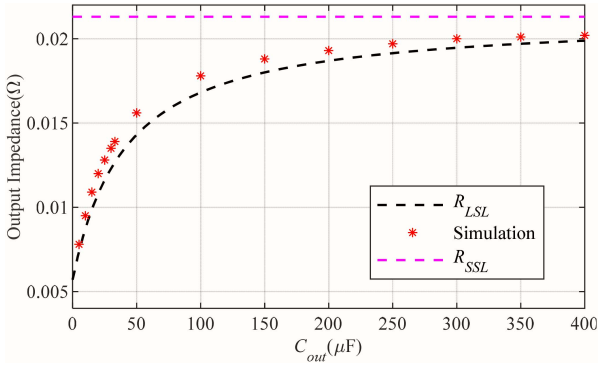

Fig. 16. Output impedance of 4:1 Dickson circuit versus output capacitor.

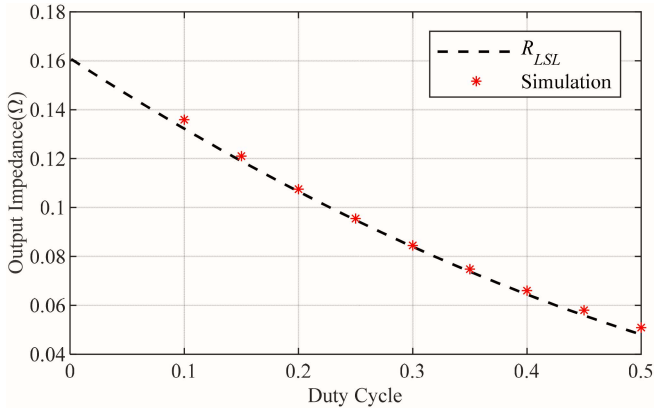

Fig. 17. Output impedance of 4:1 Dickson circuit versus duty cycle.

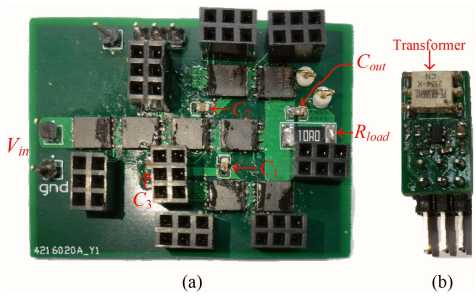

Fig. 18. Photograph of the four-to-one Dickson circuit prototype. (a) Main circuit board. (b) Drive circuit board.

TABLE II
COMPONENT LIST OF THE PROTOTYPE

Component	Value
$C_1 = C_2 = C_3$	Multilayer Ceramic Capacitor: 0.47 μF, ESR: 20 mΩ
C_{out}	Multilayer Ceramic Capacitor: 1 μF, ESR: 10 mΩ
S_1–S_8	BSC009NE2LS5, $R_{ds(on)}$: 0.9 mΩ
Transformer	PE-68386NL, operating frequency: 50 kHz and up

than its steady-state value and the duration of the pulse stage is much smaller than the constant stage. Therefore, the LSL model is sensible and in terms of accuracy, $R_{\rm LSL}$ has an absolute advantage over $R_{\rm SSL}$ and the method in [18] and [22] at mid-band via Figs. 13 and 15.

B. $R_{\rm out}$ Versus $C_{\rm out}$ With Fixed d and $F_{\rm s}$

Under the parameters presented in Table I, the simulation results of the four-to-one Dickson circuit are compared with the calculation results of $R_{\rm SSL}$ and $R_{\rm LSL}$ in the output capacitor range 5 μF–400 μF, in which the duty cycle d is still 50% and the switching frequency f_s is set to 400 kHz.

As plotted in Fig. 16, $R_{\rm LSL}$ is always accurate and lower than the simulated value as the output capacitor changes. The larger the output capacitor is, the larger the output impedance is, which is the same as has been found in [21]. The larger the output capacitor is, the closer output impedance and $R_{\rm LSL}$ are to $R_{\rm SSL}$, i.e., (55) is verified.

C. R_{out} Versus d With Fixed C_{out} and F_s

When the switching frequency is set to 100 kHz and the output capacitor has a capacitance of 33 μF, the four-to-one Dickson circuit with parameters shown in Table I is simulated in MATLAB in the duty cycle range 0.1–0.5 as well.

The simulation results and $R_{\rm LSL}$ are compared in Fig. 17. Clearly, $R_{\rm LSL}$ shows great accuracy at different duty cycles.

VI. VERIFICATION BY EXPERIMENT

Utilizing the 4:1 Dickson circuit, the accuracy of the LSL model is validated via the experiment. The prototype is shown in Fig. 18 and the component list is shown in Table II.

To reduce the effect of stray inductances, the main circuit board (5×3.7 cm^2) shown in Fig. 18(a) is made compact and the drive circuit is integrated on a small drive circuit board presented in Fig. 18(b), which could be plugged into the main circuit board.

The first set of experiments is carried out with experimental parameters given in Tables II and III, which are fixed frequency

TABLE III
PARAMETER LIST FOR EXPERIMENT VERIFICATION 1

Parameter	Value
V_{in}	15 V
R_{load}	10 Ω
d	[0, 0.5]
f_s	100 kHz

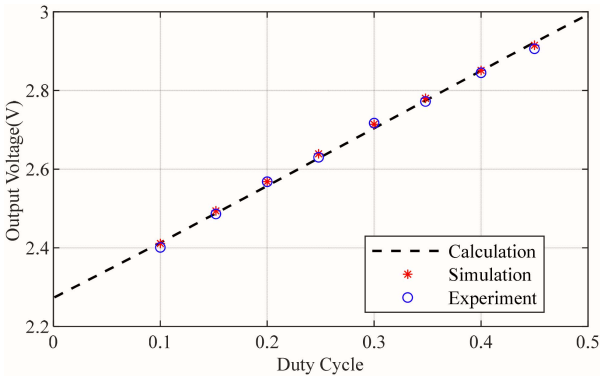

Fig. 19. Calculation, simulation, and experimental results comparison for four-to-one Dickson circuit at different duty cycles.

Fig. 20. Waveforms of $V_{\rm in}$, $V_{\rm out}$, PWM 1 and PWM 2 at $d = 0.45$ and $f_s = 100$ kHz.

and output capacitor. The results of calculation and simulation with the same circuit parameters are compared with the experimental results in Fig. 19. The waveforms at $d = 0.45$ and $f_s = 100$ kHz are displayed in Fig. 20.

The second group of experiments is conducted with a fixed duty cycle and output capacitor and the concrete parameters are shown in Tables II and IV. The output voltage calculated by the LSL model, simulations, and experiments are compared in Fig. 21. From Figs. 19 and 21, it could be found that the LSL model shows good matches with the simulation and experimental results.

TABLE IV
PARAMETER LIST FOR EXPERIMENT VERIFICATION 2

Parameter	Value
V_{in}	15 V
R_{load}	10 Ω
d	0.2
f_s	100 k-500 kHz

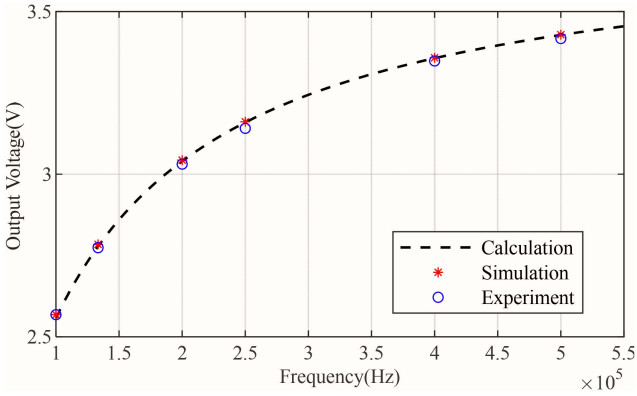

Fig. 21. Calculation, simulation, and experimental results comparison for four-to-one Dickson circuit at different frequencies.

VII. CONCLUSION

By taking both capacitor charge-sharing loss and conduction loss into account, the LSL is proposed in this article. Thanks to considering the output capacitor effect, the LSL model is applicable to the SCC with a limited output capacitor. Since the charge transfer is used to analyze energy loss rather than the voltage and current, the LSL model can be applied to high-order SCCs conveniently. Based on the charge multiplier analysis, the LSL model is suitable for the well-posed SCCs.

Different from the SSL and FSL, which are applicable at low or high frequencies, LSL has great accuracy in the mid-band at which most practical SCCs work. In [2], SCCs have been divided into three operating modes according to the charge/discharge instantaneous current waveforms. SSL corresponds to the complete charge mode, FSL corresponds to the no charge mode, and LSL proposed in this article accords with the partial charge mode.

Through the simulation and experiment, it could be corroborated that LSL can predict the output impedance precisely with the change of switching frequency, output capacitor, and duty cycle. Therefore, the proposed modeling method could be used to guide circuit design and parameter optimization.

APPENDIX A

Proof of Theorem 1

The circuit illustrated in Fig. 22 is used to prove Theorem 1. The circuit contains L branches and there are any number of capacitors, any number of voltage sources, and a resistance in series in each branch. Adjacent branches are connected by a switch. The reference voltage direction is marked on the

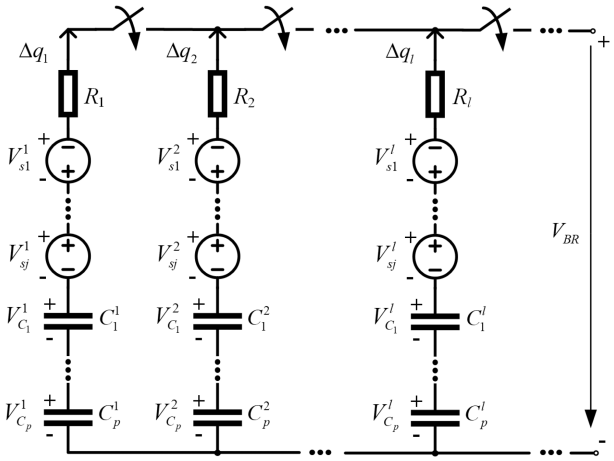

Fig. 22. Circuit to verify Theorem 1.

diagram and the current reference direction is taken as the nonassociated reference direction. All the switches close and open simultaneously. During the circuit conduction, according to KCL, we obtain

$$\sum_l \Delta q_l = 0 \tag{65}$$

where Δq_l is the charge flowing through the branch *l*. In the steady state, the voltage in each branch has the following relationship:

$$\sum_j V_{sj}^l + \sum_p V_{st\_C_p}^l = V_{ST\_BR} \tag{66}$$

where V_{sj}^l is the voltage of the *j*th voltage source in the branch *l*, $V_{st\_C_p}^l$ is the steady-state voltage of the capacitor C_p^l, and V_{ST_BR} is the steady-state value of the total branch voltage V_{BR}.

From (2), the total energy loss can be derived as

$$E_{\text{loss}} = \sum_l \sum_p \Delta E_{C_p}^l + \sum_l \sum_j \Delta E_{V_{sj}}^l \tag{67}$$

where $\Delta E_{C_p}^l$ is the energy loss of C_p^l and$\Delta E_{V_{sj}}^l$is the energy loss of V_{sj}^l. According to (3), we get

$$\Delta E_{C_p}^l = E_p^l + \Delta q_l \cdot V_{st\_C_p}^l \tag{68}$$

$$\Delta E_{V_{sj}}^l = \Delta q_l \cdot V_{sj}^l \tag{69}$$

where E_p^l is the energy loss in EDEC of C_p^l. Substituting (68) and (69) into (67) and (A5) into (A3) yields

$$\begin{aligned} E_{\text{loss}} &= \sum_l \sum_p E_p^l + \sum_l \Delta q_l \cdot \Big(\sum_j V_{sj}^l + \sum_p V_{st\_C_p}^l\Big) \\ &= \sum_l \sum_p E_p^l. \end{aligned} \tag{70}$$

It is clear that if there is a parallel connection of capacitors in the branch, the same conclusion can be drawn, which will not be repeated here.

Appendix B

Proof of Theorem 2

In the LSL model, the energy loss of SCCs contains two parts. In the pulse stage, only capacitor charge-sharing loss is considered, and in the constant stage, only conduction loss is considered. If we could prove that these two losses in the LSL model are not greater than the actual situation in any phase, R_{LSL} is the lower limit of output impedance in the mid-band.

1) Capacitor Charge-Sharing Loss in the Pulse Stage: In the LSL model, the current through capacitors is deemed as the current impulse. The charge transfer$\Delta q_{C_i_p}$ of the flying capacitor C_i in this stage is the difference between the total charge transfer in a phase Δq_{C_i} and the charge transfer in the constant stage

$$\Delta q_{C_i\_p} = \Delta q_{C_i} - I_{C_i\_c} \cdot t_{\text{on}} \tag{71}$$

where $I_{C_i\_c}$ is the average current through C_i in constant stage, and t_{on} is the time the circuit is on in a phase. In the actual situation, the duration of the constant stage is no more than t_{on} due to parasitic resistance, so, $\Delta q_{C_i\_p}$ is the smallest in all circumstances, which is not greater than the actual situation. Via (19), we know

$$E_{\text{LSL\_}p} = \sum_i \frac{\Delta q_{C_i\_p}^2}{2C_i}. \tag{72}$$

It could be said that the capacitor charge-sharing loss in the LSL model is not greater than the actual situation.

2) Conduction Loss in the Constant Stage: It could be proved that charges with the total amount of Q pass through a resistor R in any way within the time T, where the energy consumption is the smallest in the form of constant current.

The current through *R* is denoted as *i*(t) and the current in constant form is denoted as *I*, we obtain

$$\int_0^T i(t)dt = I \cdot T. \tag{73}$$

According to the integral version of Cauchy–Schwarz inequality, we obtain

$$\int_0^T i^2(t)dt \cdot \int_0^T 1dt \geq \left[\int_0^T i(t)dt\right]^2. \tag{74}$$

From (73) and (74), we could get

$$\int_0^T i^2(t)dt \geq I^2 T. \tag{75}$$

In the LSL model, the load is considered as a current source. In other words, we use the average output current to calculate. However, in the actual situation, the branch current is not constant. According to (75), it could be said that the conduction loss in the LSL model is not greater than the actual situation.

So, R_{LSL} is the lower limit of output impedance in the mid-band.

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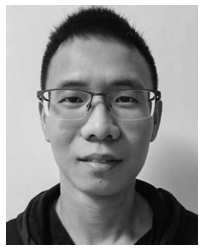

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