Layout-Dominated Dynamic Current Balancing Analysis of Multichip SiC Power Modules Based on Coupled Parasitic Network Model

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***Abstract*—Multichip silicon carbide (SiC) power modules with Kelvin-source connections are commonly used in applications requiring large capacity. As a result of the parasitic effect induced by the interconnections in module packaging, the dynamic current mismatch among paralleled dies limits the available capacity of power modules. This article presents a general analysis on the mechanism of layout-dominated dynamic current balancing in multichip SiC power modules, utilizing a coupled parasitic network model. Focusing on the interrelation of parasitic parameters in the power module, a coupled parasitic network model is developed specially for switching transients, and the dynamic current balancing equations are derived. For the multichip power modules with two different layouts, the parasitic parameters pertaining to the proposed model are extracted by the finite-element analysis (FEA). The acquired parasitic parameters considering magnetic coupling are utilized to calculate and verify the dynamic current balancing equations. Moreover, based on these parasitic parameters, the electromagnetic coupling simulation is performed to evaluate the dynamic current sharing. Furthermore, for the validation of the proposed model and equations, experiments are conducted with the fabricated power module prototypes.**

***Index Terms*—Coupled parasitic network model, dynamic current balancing, multichip SiC power modules, package layout.**

I. Introduction

With the rapid development of electrified vehicles such as electric vehicles and more electrical aircraft, the high-capacity power electronic converters is becoming increasingly prominent [1], [2], [3]. As a basic switching unit for power electronic converters, the power semiconductor module is extensively adopted in these fields due to its high-density integration and easy-to-use interface [4], [5]. Particularly, silicon carbide (SiC) bare dies can theoretically achieve faster switching speed, lower switching losses, and higher switching frequency than the corresponding silicon (Si) bare dies, making them more promising for high-capacity applications. Despite these features, attributed to the low yield rate in the wafer and high thermal-mechanical stress in the device, the imperfect manufacturing technique for SiC metal-oxide-semiconductor field-effect transistor (MOSFET) limits the active area of the single die [6]. Therefore, the maximum current rating of SiC MOSFET bare die designed for a commercial purpose is typically restricted to 100 A at a voltage rating of 1.2 kV, which is inadequate to meet the needs of high-capacity applications [7]. For the purpose of increasing the current rating of power modules, the multichip parallel operation is generally regarded as a feasible and practical approach [8]. However, the parasitic effect induced by the interconnections in module packaging, especially parasitic inductance, can cause a considerable adverse impact on the dynamic current sharing among paralleled dies. Imbalanced current sharing generates uneven power losses and nonuniform junction temperature, resulting in the degradation of reliability and lifetime for power modules [9], [10]. In order to prevent irreversible damage to the multichip power modules from imbalanced current, current derating of the modules is normally adopted in practical applications [11]. Therefore, for the maximal capacity of each paralleled die, it is crucial to analyze the layout-dominated dynamic current balancing characteristics and investigate how to improve the balancing performance during the design of the multichip power modules.

A comprehensive understanding of the mechanism for dynamic current balancing is essential to mitigate the mismatched dynamic current effectively. Wang et al. [12] designed a double-end sourced layout by incorporating an additional pair of dc-bus terminals to improve the dynamic current sharing. Through symmetric direct bonded copper (DBC) layout, the discrepancies in parasitic parameters attributed to the unequal loop length and area of individual bare dies are reduced. In [13], the mechanism of transient current imbalance is elaborated through a case study of a commercial half-bridge multichip power module. It is indicated that the common source stray inductance mismatch and the applied di/dt account for the transient current imbalance between paralleled devices. Moreover, in [14], the power source parasitic parameter matrix and the common

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branch impedance coupling matrix are presented to assess the dynamic current sharing level. Similarly, based on the matrices of parasitic impedances, common coefficients are proposed to evaluate the current sharing characteristics in [15]. It is stated that symmetric nondiagonal elements of the above-mentioned parasitic impedance matrices are capable of balancing the dynamic current among paralleled dies. Additionally, a method to balance dynamic current by adjusting the connection points of bonding wires and copper traces is adopted in [16] and [17]. In this method, the power loop and drive loop are assumed to be fully decoupled to simplify the analysis of the magnetic coupling.

In the previous research, only the parasitics of the power loops, drive loops, and their shared current paths are taken into account. The parasitics of the drive loops affecting the power loops through magnetic coupling are overlooked. This, however, serves the same way as the shared current path and can induce the mutual inductance between these two loops [18]. An inappropriate layout of the drive and power loops may potentially introduce the nonnegligible mutual inductance derived from the magnetic coupling effect [19]. As a typical representative, common source inductance generally serves as negative feedback from the power loop to the drive loop. During the switching transients, the voltage drop across common source inductance counteracts the variation of gate-source voltage and consequently mitigates the overshoot of the drain current [20], [21]. Due to the magnetic coupling, the Kelvin connection may not eliminate the effect of the common source inductance. Therefore, their discrepancies can create the dynamic current imbalance among paralleled dies in the power module. Consequently, the conventional mechanistic analysis exclusively based on the shared current paths lacks universality in cases where the magnetic coupling has a notable impact.

In this article, a coupled parasitic network model and dynamic current balancing equations are proposed for the analysis of dynamic current balancing in multichip SiC power modules. For relatively high accuracy of the current sharing prediction, the impact of the self and mutual partial inductances among multiple current segments in switching transients is discussed. In addition, the parasitics extraction and electromagnetic coupling analysis are conducted to assess the switching performance of paralleled SiC MOSFETs. Experimental tests are performed on a fabricated power module with two different layouts, to verify the proposed model and equations.

The rest of this article is presented as follows. Section II illustrates the configuration and DBC layout of the studied multichip SiC power modules. Based on this, the mechanism of layout-dominated dynamic current balancing based on coupled parasitic network model is analyzed. In Section III, the parasitic parameters considering magnetic coupling are extracted to verify the derived dynamic current balancing equations via electromagnetic coupling simulation. Section IV provides the experimental verifications of the parasitics extraction and the dynamic current sharing prediction. Finally, Section V concludes this article.

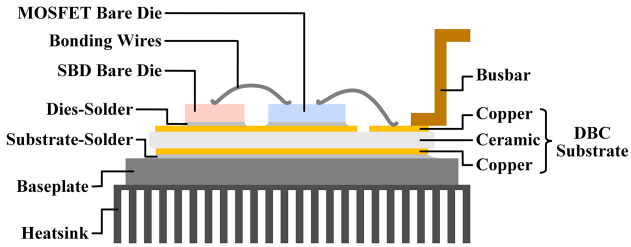

Fig. 1. Internal layer structure of wire-bonded packaging module.

II. Proposed Coupled Parasitic Network Model for Dynamic Current Balancing Analysis

Taking the multichip power modules with common layouts for instance, a coupled parasitic network model is established according to the concept of partial inductance. Based on the proposed model, the dynamic current balancing equations are presented as optimization guidelines for the layout designing.

A. Studied Multichip SiC Power Modules: Configuration and DBC Layout

The internal layer structure of the conventional wire-bonded packaging module is revealed in Fig. 1. Overall, DBC substrate, dies-solder, busbars, and bonding wires are involved in the interconnections of module packaging. The parasitic effect is generated from these sections in a multichip power module, which varies the distribution of the dynamic current among paralleled dies.

For dynamic current balancing analysis, multichip SiC phase-leg power modules with two commonly used DBC substrate layouts are investigated in this work, as shown in Fig. 2(a) and (b). The configurations of the studied modules are depicted in Fig. 3(a) and (b), which share an identical structure. Each switch consists of three SiC MOSFET dies (CREE CPM312000075A) with Kelvin-source connections and three antiparallel SiC Schottky barrier diode dies (CREE CPW41200S010B). The MOSFETs and Schottky barrier diodes (SBDs) at the high side switch are denoted as M_1-M_3 and D_1-D_3, while those at the low side are denoted as M_4-M_6 and D_4-D_6, successively. The gate and Kelvin-source busbars for the high and low side switches are marked as G_H, KS_H, G_L, and KS_L, respectively. The dc busbars of layout A are recorded as DC+, DC_1-, and DC_2-, while those of layout B are recorded as DC+ and DC-. In addition, ac represents the output busbar for both layouts A and B. For a fair comparison, the two layouts of the studied modules are designed with the same DBC substrate size. The detailed physical dimensions and materials of the multichip phase-leg power modules are listed in Table I.

B. Mechanism of Layout-Dominated Dynamic Current Balancing Based on Coupled Parasitic Network Model

As to a multichip power module, the layout-dominated parasitic parameters are primarily composed of partial inductance and equivalent series resistance (ESR). Particularly, the partial

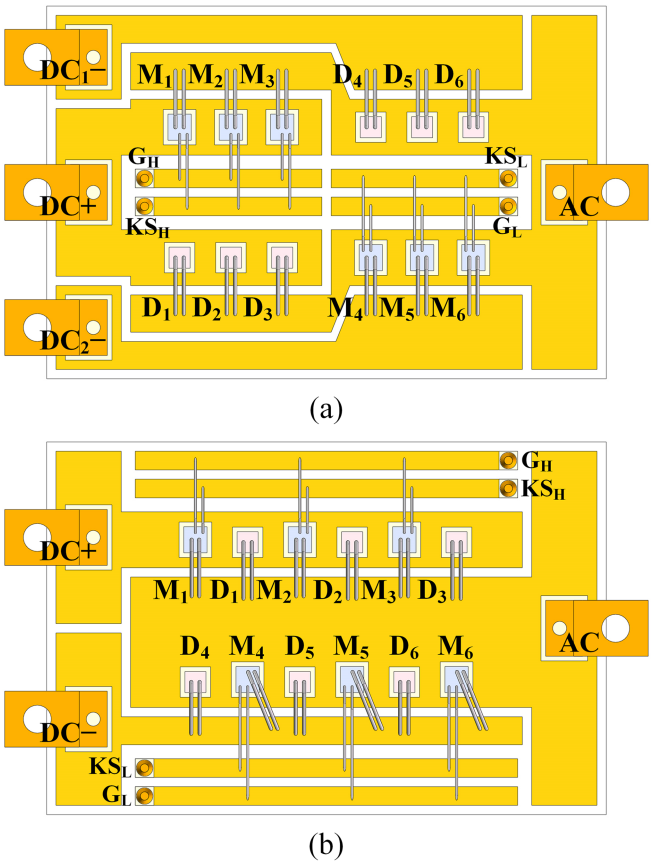

Fig. 2. Multichip SiC power modules with (a) layout A and (b) layout B.

TABLE I
PHYSICAL DIMENSIONS AND MATERIALS OF THE POWER MODULES

	Layout A	Layout B
DBC Size (mm)	60.0 × 40.0	60.0 × 40.0
DBC Thickness (mm)	0.2 (Cu) 1.0 (AlN)	0.2 (Cu) 1.0 (AlN)
SiC MOSFET Size (mm)	2.50 × 2.80	2.50 × 2.80
SiC SBD Size (mm)	2.26 × 2.26	2.26 × 2.26
SiC MOSFET Bonding Wires Diameter (mil)	15 (Power Loop) 10 (Drive Loop)	15 (Power Loop) 10 (Drive Loop)
SiC SBD Bonding Wires Diameter (mil)	15	15

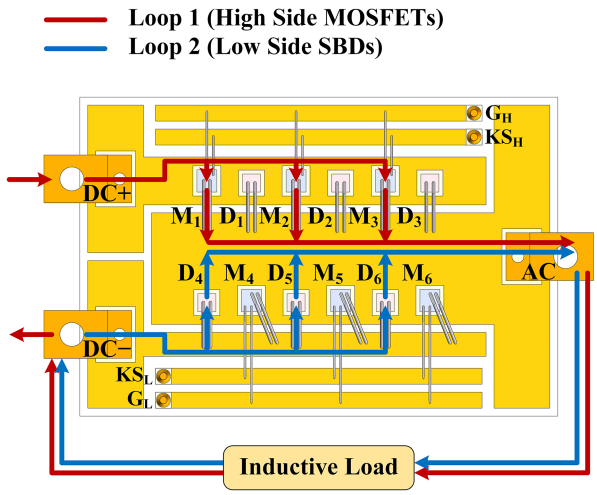

Fig. 4. Commutation loops of paralleled dies with layout B.

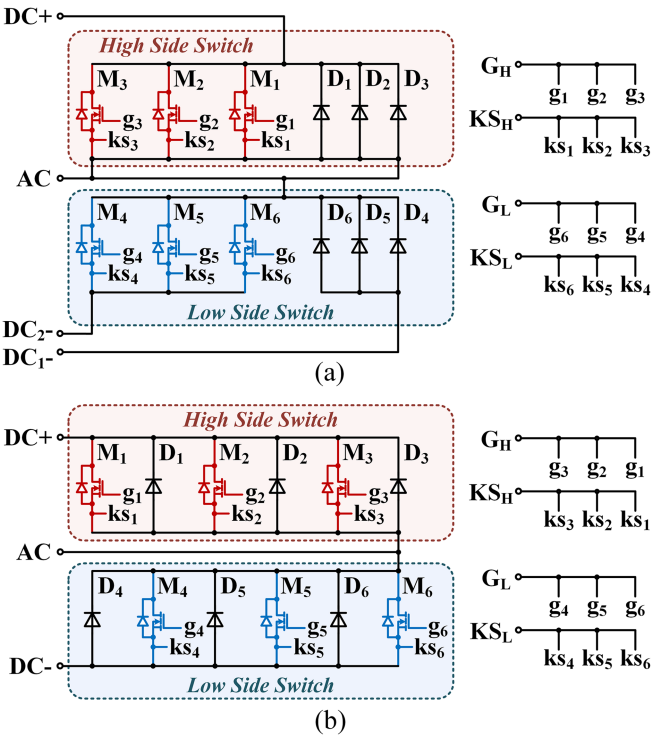

Fig. 3. Configurations of the phase-leg power modules with (a) layout A and (b) layout B.

inductance is divided into self-partial inductance and mutual partial inductance [22]. Within a current loop, the self-partial inductance of each segment is the ratio of the magnetic flux (between the targeted segment and infinity) to the current of that segment. Between two segments of the same or different current loops, the mutual partial inductance is the ratio of the magnetic flux (penetrating the surface between the second segment and infinity) to the current of the first segment. Accordingly, it is feasible to develop a lumped-circuit model of a closed current loop, where the segments of the loop perimeter are denoted by self-partial inductances and mutual partial inductances between every two segments.

Under inductive load, the commutation loops of paralleled dies with layout B are shown in Fig. 4. Depending on the direction of the load current, the current commutation occurs between the high side MOSFETs (M_1-M_3) and low side SBDs (D_4-D_6) or between the low side MOSFETs (M_4-M_6) and high side SBDs (D_1-D_3). In the former case, loop 1 for the high side MOSFETs is referred to as the power loop, which covers the segments before commutation. Loop 2 for the low side SBDs covers the segments after commutation. Thus, focusing on the dynamic current sharing among paralleled MOSFETs, the partial inductances relevant to the segments of the power loop and the gate drive loop are followed with interest.

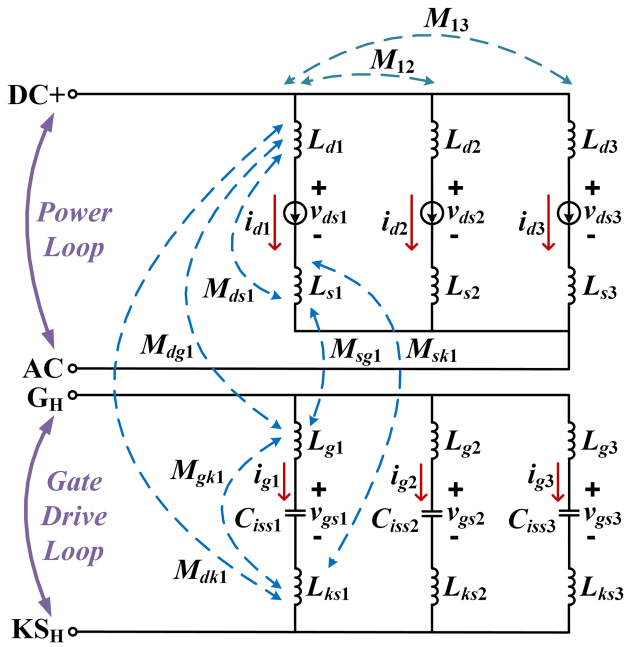

Fig. 5. Coupled parasitic network model for high side paralleled MOSFETs at switching transients.

With the consideration of magnetic coupling among each current segment, a coupled parasitic network model at switching transients is presented in Fig. 5. This proposed model describes the interrelation of parasitic parameters inside the multichip power module. Since the high side switch shares similar characteristics with the low side switch in a phase-leg module, the proposed model is illustrated by the paralleled SiC MOSFETs of only the high side switch. The coupled parasitic network model consists of a power loop and a gate drive loop, which are closely coupled through mutual inductance. For these two loops, L_x and M_x indicate self-partial inductance and mutual partial inductance of correlative current segments. For instance, L_{d1} is the self-partial inductance between DC+ busbar and the drain of bare die M_1, and L_{s1} is the self-partial inductance between ac busbar and the source of the bare die M_1. Likewise, L_{g1} is the self-partial inductance between G_H busbar and the gate of bare die M_1, and L_{ks1} is the self-partial inductance between KS_H busbar and the Kelvin-source of bare die M_1. In addition, M_{ds1}, M_{dg1}, M_{dk1}, M_{sg1}, M_{sk1}, and M_{gk1} are the mutual partial inductances between the corresponding two segments of the current loop. For simplicity, only the mutual partial inductances between two segments pertaining to the same die are labeled in detail. While those concerned with the different dies are summarized by symbols with only numeric subscripts, e.g., M_{12} and M_{13} refer to the mutual partial inductances related to the bare die M_1. Specifically, M_{12} includes M_{d1d2}, M_{d1s2}, M_{d1g2}, M_{d1k2}, M_{s1d2}, M_{s1s2}, M_{s1g2}, and M_{s1k2}. Similarly, M_{13} contains M_{d1d3}, M_{d1s3}, M_{d1g3}, M_{d1k3}, M_{s1d3}, M_{s1s3}, M_{s1g3}, and M_{s1k3}. The mutual partial inductances within the gate drive loop are not considered, due to their slight impact on the dynamic current sharing. Besides, compared with the partial inductances, the ESRs have negligible effect during turn-ON and turn-OFF periods, and thus they will be neglected during the following analysis for simplicity [23].

Dynamic current imbalance primarily occurs during the switching transients when MOSFETs operate in the saturation region [24]. Accordingly, the drain-source parasitic capacitance (C_{ds}) can be neglected [15]. The gate-source capacitance (C_{gs}) is dynamically connected in parallel with the gate-drain capacitance (C_{gd}), which together form the equivalent input capacitance (C_{iss}). Thus, each SiC MOSFET die is modeled as a current source (i_d) controlled by its gate-source voltage (v_{gs}) in the power loop and input capacitance (C_{iss}) in the gate drive loop. To focus on the layout-dominated dynamic current balancing issue, the device parameters of the paralleled SiC MOSFETs are regarded to be basically identical, which can be achieved by preselection for dies before module manufacturing.

In the coupled parasitic network model, $L_{d1,23}$ and $L_{s1,23}$ can be regarded as two-port coupled inductors, whose port voltage is derived from both the self and mutual inductances. According to the definition of inductance and the Law of Electromagnetic Induction, the port voltage v_{d1} of L_{d1}, v_{d2} of L_{d2}, v_{d3} of L_{d3}, v_{s1} of L_{s1}, v_{s2} of L_{s2}, and v_{s3} of L_{s3} can be expressed as

$$\begin{cases} v_{d1}=L_{d1}\frac{di_{d1}}{dt}+M_{ds1}\frac{di_{d1}}{dt}+M_{dg1}\frac{di_{g1}}{dt}+M_{dk1}\frac{di_{g1}}{dt} \\ +M_{d1d2}\frac{di_{d2}}{dt}+M_{d1s2}\frac{di_{d2}}{dt}+M_{d1g2}\frac{di_{g2}}{dt}+M_{d1k2}\frac{di_{g2}}{dt} \\ +M_{d1d3}\frac{di_{d3}}{dt}+M_{d1s3}\frac{di_{d3}}{dt}+M_{d1g3}\frac{di_{g3}}{dt}+M_{d1k3}\frac{di_{g3}}{dt} \\ v_{d2}=L_{d2}\frac{di_{d2}}{dt}+M_{ds2}\frac{di_{d2}}{dt}+M_{dg2}\frac{di_{g2}}{dt}+M_{dk2}\frac{di_{g2}}{dt} \\ +M_{d2d1}\frac{di_{d1}}{dt}+M_{d2s1}\frac{di_{d1}}{dt}+M_{d2g1}\frac{di_{g1}}{dt}+M_{d2k1}\frac{di_{g1}}{dt} \\ +M_{d2d3}\frac{di_{d3}}{dt}+M_{d2s3}\frac{di_{d3}}{dt}+M_{d2g3}\frac{di_{g3}}{dt}+M_{d2k3}\frac{di_{g3}}{dt} \\ v_{d3}=L_{d3}\frac{di_{d3}}{dt}+M_{ds3}\frac{di_{d3}}{dt}+M_{dg3}\frac{di_{g3}}{dt}+M_{dk3}\frac{di_{g3}}{dt} \\ +M_{d3d1}\frac{di_{d1}}{dt}+M_{d3s1}\frac{di_{d1}}{dt}+M_{d3g1}\frac{di_{g1}}{dt}+M_{d3k1}\frac{di_{g1}}{dt} \\ +M_{d3d2}\frac{di_{d2}}{dt}+M_{d3s2}\frac{di_{d2}}{dt}+M_{d3g2}\frac{di_{g2}}{dt}+M_{d3k2}\frac{di_{g2}}{dt} \end{cases} \tag{1}$$

$$\begin{cases} v_{s1}=L_{s1}\frac{di_{d1}}{dt}+M_{ds1}\frac{di_{d1}}{dt}+M_{sg1}\frac{di_{g1}}{dt}+M_{sk1}\frac{di_{g1}}{dt} \\ +M_{s1d2}\frac{di_{d2}}{dt}+M_{s1s2}\frac{di_{d2}}{dt}+M_{s1g2}\frac{di_{g2}}{dt}+M_{s1k2}\frac{di_{g2}}{dt} \\ +M_{s1d3}\frac{di_{d3}}{dt}+M_{s1s3}\frac{di_{d3}}{dt}+M_{s1g3}\frac{di_{g3}}{dt}+M_{s1k3}\frac{di_{g3}}{dt} \\ v_{s2}=L_{s2}\frac{di_{d2}}{dt}+M_{ds2}\frac{di_{d2}}{dt}+M_{sg2}\frac{di_{g2}}{dt}+M_{sk2}\frac{di_{g2}}{dt} \\ +M_{s2d1}\frac{di_{d1}}{dt}+M_{s2s1}\frac{di_{d1}}{dt}+M_{s2g1}\frac{di_{g1}}{dt}+M_{s2k1}\frac{di_{g1}}{dt} \\ +M_{s2d3}\frac{di_{d3}}{dt}+M_{s2s3}\frac{di_{d3}}{dt}+M_{s2g3}\frac{di_{g3}}{dt}+M_{s2k3}\frac{di_{g3}}{dt} \\ v_{s3}=L_{s3}\frac{di_{d3}}{dt}+M_{ds3}\frac{di_{d3}}{dt}+M_{sg3}\frac{di_{g3}}{dt}+M_{sk3}\frac{di_{g3}}{dt} \\ +M_{s3d1}\frac{di_{d1}}{dt}+M_{s3s1}\frac{di_{d1}}{dt}+M_{s3g1}\frac{di_{g1}}{dt}+M_{s3k1}\frac{di_{g1}}{dt} \\ +M_{s3d2}\frac{di_{d2}}{dt}+M_{s3s2}\frac{di_{d2}}{dt}+M_{s3g2}\frac{di_{g2}}{dt}+M_{s3k2}\frac{di_{g2}}{dt}. \end{cases} \tag{2}$$

Due to the compact arrangement of the paralleled dies, the discrepancy of the mutual partial inductances concerning the same kind and different dies can be ignored. Specifically, the same letter subscripts of M_x denote the same kind, and the different number subscripts of M_x represent different dies. The validity of this assumption is illustrated in Section III-C. Based

on this assumption, there are

$$\begin{cases} M_{d1d2}=M_{d1d3}=M_{d2d1}=M_{d2d3}=M_{d3d1} \\ =M_{d3d2}=M_{dd} \\ M_{d1s2}=M_{d1s3}=M_{d2s1}=M_{d2s3}=M_{d3s1} \\ =M_{d3s2}=M_{ds} \\ M_{d1g2}=M_{d1g3}=M_{d2g1}=M_{d2g3}=M_{d3g1} \\ =M_{d3g2}=M_{dg} \\ M_{d1k2}=M_{d1k3}=M_{d2k1}=M_{d2k3}=M_{d3k1} \\ =M_{d3k2}=M_{dk} \end{cases} \tag{3}$$

$$\begin{cases} M_{s1d2}=M_{s1d3}=M_{s2d1}=M_{s2d3}=M_{s3d1} \\ =M_{s3d2}=M_{sd} \\ M_{s1s2}=M_{s1s3}=M_{s2s1}=M_{s2s3}=M_{s3s1} \\ =M_{s3s2}=M_{ss} \\ M_{s1g2}=M_{s1g3}=M_{s2g1}=M_{s2g3}=M_{s3g1} \\ =M_{s3g2}=M_{sg} \\ M_{s1k2}=M_{s1k3}=M_{s2k1}=M_{s2k3}=M_{s3k1} \\ =M_{s3k2}=M_{sk}. \end{cases} \tag{4}$$

Based on (1), (2), (3), and (4), the following equations hold:

$$\begin{cases} v_{d1}=(L_{d1}+M_{ds1})\frac{di_{d1}}{dt}+(M_{dg1}+M_{dk1})\frac{di_{g1}}{dt} \\ +(M_{dd}+M_{ds})\frac{d(i_{d2}+i_{d3})}{dt}+(M_{dg}+M_{dk})\frac{d(i_{g2}+i_{g3})}{dt} \\ v_{d2}=(L_{d2}+M_{ds2})\frac{di_{d2}}{dt}+(M_{dg2}+M_{dk2})\frac{di_{g2}}{dt} \\ +(M_dd+M_{ds})\frac{d(i_{d1}+i_{d3})}{dt}+(M_{dg}+M_{dk})\frac{d(i_{g1}+i_{g3})}{dt} \\ v_{d3}=(L_{d3}+M_{ds3})\frac{di_{d3}}{dt}+(M_{dg3}+M_{dk3})\frac{di_{g3}}{dt} \\ +(M_{dd}+M_{ds})\frac{d(i_{d1}+i_{d2})}{dt}+(M_{dg}+M_{dk})\frac{d(i_{g1}+i_{g2})}{dt} \end{cases} \tag{5}$$

$$\begin{cases} v_{s1}=(L_{s1}+M_{ds1})\frac{di_{d1}}{dt}+(M_{sg1}+M_{sk1})\frac{di_{g1}}{dt} \\ +(M_{sd}+M_{ss})\frac{d(i_{d2}+i_{d3})}{dt}+(M_{sg}+M_{sk})\frac{d(i_{g2}+i_{g3})}{dt} \\ v_{s2}=(L_{s2}+M_{ds2})\frac{di_{d2}}{dt}+(M_{sg2}+M_{sk2})\frac{di_{g2}}{dt} \\ +(M_{sd}+M_{ss})\frac{d(i_{d1}+i_{d3})}{dt}+(M_{sg}+M_{sk})\frac{d(i_{g1}+i_{g3})}{dt} \\ v_{s3}=(L_{s3}+M_{ds3})\frac{di_{d3}}{dt}+(M_{sg3}+M_{sk3})\frac{di_{g3}}{dt} \\ +(M_{sd}+M_{ss})\frac{d(i_{d1}+i_{d2})}{dt}+(M_{sg}+M_{sk})\frac{d(i_{g1}+i_{g2})}{dt}. \end{cases} \tag{6}$$

In the saturation region of SiC MOSFETs, the correlation between the drain current and gate-source voltage of the paralleled dies is expressed as

$$\begin{cases} i_{d1}=g(v_{gs1}-V_{th})^2 \\ i_{d2}=g(v_{gs2}-V_{th})^2 \\ i_{d3}=g(v_{gs3}-V_{th})^2 \end{cases} \tag{7}$$

where g and V_{th} represent the transconductance and threshold voltage of the SiC MOSFET dies separately. Both parameters are determined only by the device material and manufacturing process [7]. As previously mentioned, these device parameters of the paralleled dies are considered to be equal.

To derive the conditions for dynamic current balancing, the drain current of the paralleled SiC MOSFET dies need to be assumed as

$$i_{d1}=i_{d2}=i_{d3}=i_d. \tag{8}$$

Combining (7) and (8) yields

$$v_{gs1}=v_{gs2}=v_{gs3}=v_{gs}. \tag{9}$$

Provided that (8) and (9) are satisfied concurrently, the drain-source voltage of the three paralleled SiC MOSFETs can be deduced as

$$v_{ds1}=v_{ds2}=v_{ds3}=v_{ds}. \tag{10}$$

In addition, the relevance between the gate current and gate-source voltage in the gate drive loop can be denoted as

$$\begin{cases} i_{g1}=C_{iss1}\frac{dv_{gs1}}{dt} \\ i_{g2}=C_{iss2}\frac{dv_{gs2}}{dt} \\ i_{g3}=C_{iss3}\frac{dv_{gs3}}{dt}. \end{cases} \tag{11}$$

Although the junction capacitance of each SiC MOSFET may vary during the switching transients [25], the input capacitance can be fitted as

$$\begin{cases} C_{iss1}=\frac{C_{0iss}-C_{hiss}}{1+(v_{ds1}/V_b)^r}+C_{hiss} \\ C_{iss2}=\frac{C_{0iss}-C_{hiss}}{1+(v_{ds2}/V_b)^r}+C_{hiss} \\ C_{iss3}=\frac{C_{0iss}-C_{hiss}}{1+(v_{ds3}/V_b)^r}+C_{hiss} \end{cases} \tag{12}$$

where C_{0iss} and C_{hiss} are values of the input capacitance provided from the datasheet in zero voltage and high voltage, respectively. In addition, V_b and r are the fitting parameters determined by the device selection [26]. Accordingly, once the device is specified, the input capacitance during the switching transients is determined only by the drain-source voltage of the paralleled dies.

Based on (10) and (12), there is

$$C_{iss1}=C_{iss2}=C_{iss3}. \tag{13}$$

Combining (9), (11), and (13) yields

$$i_{g1}=i_{g2}=i_{g3}=i_g. \tag{14}$$

Substituting (8) and (14) into (5) and (6), the following equations hold for the dynamic current balancing:

$$\begin{cases} v_{d1}=(L_{d1}+M_{ds1}+2M_{dd}+2M_{ds})\frac{di_d}{dt} \\ +(M_{dg1}+M_{dk1}+2M_{dg}+2M_{dk})\frac{di_g}{dt} \\ v_{d2}=(L_{d2}+M_{ds2}+2M_{dd}+2M_{ds})\frac{di_d}{dt} \\ +(M_{dg2}+M_{dk2}+2M_{dg}+2M_{dk})\frac{di_g}{dt} \\ v_{d3}=(L_{d3}+M_{ds3}+2M_{dd}+2M_{ds})\frac{di_d}{dt} \\ +(M_{dg3}+M_{dk3}+2M_{dg}+2M_{dk})\frac{di_g}{dt} \end{cases} \tag{15}$$

$$\begin{cases} v_{s1} = (L_{s1} + M_{ds1} + 2M_{sd} + 2M_{ss})\frac{di_d}{dt} \\ \quad + (M_{sg1} + M_{sk1} + 2M_{sg} + 2M_{sk})\frac{di_g}{dt} \\ v_{s2} = (L_{s2} + M_{ds2} + 2M_{sd} + 2M_{ss})\frac{di_d}{dt} \\ \quad + (M_{sg2} + M_{sk2} + 2M_{sg} + 2M_{sk})\frac{di_g}{dt} \\ v_{s3} = (L_{s3} + M_{ds3} + 2M_{sd} + 2M_{ss})\frac{di_d}{dt} \\ \quad + (M_{sg3} + M_{sk3} + 2M_{sg} + 2M_{sk})\frac{di_g}{dt}. \end{cases} \tag{16}$$

Applying the Kirchhoff Voltage Law (KVL) to every parallel branch of the power loop gives

$$v_{d1} + v_{ds1} + v_{s1} = v_{d2} + v_{ds2} + v_{s2} = v_{d3} + v_{ds3} + v_{s3}. \tag{17}$$

Substituting (10), (15), and (16) into (17) yields

$$\begin{aligned} &(L_{d1} + L_{s1} + 2M_{ds1})\frac{di_d}{dt} \\ &\quad + (M_{dg1} + M_{dk1} + M_{sg1} + M_{sk1})\frac{di_g}{dt} \\ &= (L_{d2} + L_{s2} + 2M_{ds2})\frac{di_d}{dt} \\ &\quad + (M_{dg2} + M_{dk2} + M_{sg2} + M_{sk2})\frac{di_g}{dt} \\ &= (L_{d3} + L_{s3} + 2M_{ds3})\frac{di_d}{dt} \\ &\quad + (M_{dg3} + M_{dk3} + M_{sg3} + M_{sk3})\frac{di_g}{dt}. \end{aligned} \tag{18}$$

Based on (18), the dynamic current balancing among all paralleled dies can be achieved when the following two equations hold simultaneously, i.e.,

$$\begin{cases} L_{d1} + L_{s1} + 2M_{ds1} = L_{d2} + L_{s2} + 2M_{ds2} \\ L_{d2} + L_{s2} + 2M_{ds2} = L_{d3} + L_{s3} + 2M_{ds3} \end{cases} \tag{19}$$

$$\begin{cases} M_{dg1} + M_{dk1} + M_{sg1} + M_{sk1} = M_{dg2} + M_{dk2} \\ \quad + M_{sg2} + M_{sk2} \\ M_{dg2} + M_{dk2} + M_{sg2} + M_{sk2} = M_{dg3} + M_{dk3} \\ \quad + M_{sg3} + M_{sk3}. \end{cases} \tag{20}$$

Accordingly, (19) and (20) are jointly regarded as the dynamic current balancing equations. They can serve as the current balancing optimization guidelines for designing the layout of the multichip power modules.

III. Parasitics Extraction and Electromagnetic Coupling Analysis for Studied Power Modules

The parasitic parameters involved in the coupled parasitic network model are extracted by ANSYS Q3D and then are utilized to calculate the dynamic current balancing equations. Additionally, based on the state space frequency-dependent model derived from the extracted parasitic parameters, the electromagnetic coupling simulation is conducted using ANSYS SIMPLORER to evaluate the switching performance of the paralleled SiC MOSFETs. The close match between the calculated values of the proposed equations and the simulation results verifies the effectiveness of the derived dynamic current balancing analysis.

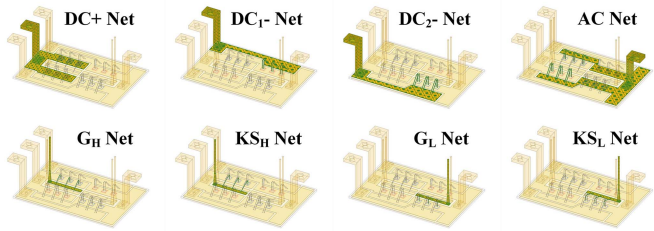

Fig. 6. Current conducting nets for layout A in ANSYS Q3D.

A. Parasitics Extraction

In the studied case, ANSYS Q3D is used as a finite-element analysis (FEA) tool to acquire the parasitic parameters related to the dynamic current balancing analysis. To establish a more accurate switching current in the subsequent electromagnetic coupling simulation, not only the partial inductances, but also the ESRs ignored in the coupled parasitic network model are extracted. Based on the proposed model, the power module geometry is arranged in multiple current conducting nets. These nets are further divided into several segments pertaining to the power loop and the gate drive loop. Each segment can be extracted with a self-partial inductance and an ESR.

Accordingly, the studied power module with layout A is separated into eight nets, as shown in Fig. 6. Likewise, the power module with layout B can be separated into seven nets. Inside the current conducting nets, Source and Sink are the measuring points of each segment, which specify the current reference direction. Any net included in the inductance or resistance matrix must have a single Sink defined, along with at least one Source [27]. Based on this, the top surface of dc, ac, gate, and Kelvin-source busbars are set as Sink. The solder layers at the bottom pads of dies are set as Source, and the ends of bonding wires connected with the top pads of dies are also set as Source. The current reference direction is defined from Source to Sink, which is inconsistent with the actual current direction of several segments. Hence, the positive and negative polarities of the extracted mutual partial inductances are corrected according to the actual current direction.

Using the Q3D electromagnetic field simulation, the proximity and skin effects are all considered, and the partial inductances and ESRs can be recorded as a function of frequency. Through a frequency sweep from 0 to 100 MHz, the frequency-dependent parasitic parameters of the power modules with two different layouts are extracted. Taking the layout A for instance, the partial inductances and ESRs are illustrated in Fig. 7(a) and (b). Among these solutions, the negative parameters contain some mutual partial inductances and ESRs between every two segments, indicating their actual current direction is opposite to the reference direction. It is clear that the partial inductances enter the region with the complete skin effect at a frequency around 10 MHz. In this region, the extractive solutions of partial inductances remain basically constant. Therefore, for layouts

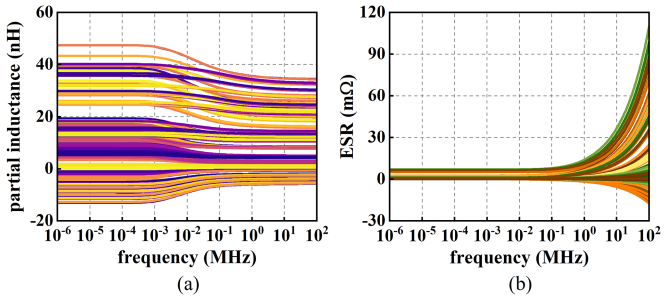

Fig. 7. Frequency-dependent parasitic parameters of the power module with layout A. (a) Self and mutual partial inductances. (b) ESRs.

TABLE II
PARTIAL INDUCTANCE EXTRACTED FOR LAYOUT A

Layout A f = 10 MHz		High side switch			Low side switch		
		M_1	M_2	M_3	M_4	M_5	M_6
Partial inductance (nH)	L_d	13.20	13.51	13.79	14.02	13.72	13.40
	L_s	24.48	23.13	21.78	31.62	33.56	35.74
	M_{ds}	0.17	-0.01	-0.12	0.22	0.33	0.51
	M_{dg}	4.68	4.88	5.08	5.38	5.18	4.97
	M_{dk}	-4.65	-4.74	-4.86	-5.16	-5.04	-4.95
	M_{sg}	-0.98	-0.87	-0.82	-0.57	-0.68	-0.84
	M_{sk}	0.90	0.83	0.81	0.48	0.59	0.72

TABLE III
PARTIAL INDUCTANCE EXTRACTED FOR LAYOUT B

Layout B f = 10 MHz		High side switch			Low side switch		
		M_1	M_2	M_3	M_4	M_5	M_6
Partial inductance (nH)	L_d	13.20	13.86	14.47	14.30	13.70	13.07
	L_s	19.98	18.95	17.92	21.67	26.91	32.19
	M_{ds}	-0.23	-0.31	-0.30	0.00	0.12	0.38
	M_{dg}	0.12	0.46	0.68	0.55	0.28	-0.07
	M_{dk}	-0.28	-0.57	-0.74	-0.61	-0.38	-0.05
	M_{sg}	-3.43	-3.16	-2.85	-6.66	-8.94	-11.44
	M_{sk}	3.61	3.37	3.09	7.54	10.47	13.57

A and B, the partial inductances used in the dynamic current balancing equations at 10 MHz are listed in Tables II and III.

B. Electromagnetic Coupling Analysis

As demonstrated in Section II, the dynamic current sharing relies heavily on the frequency-dependent parasitic parameters in module packaging. In the frequency sweep mode of Q3D, each frequency point contains a matrix solution, whose elements consist of the extracted partial inductances and ESRs. These matrix solutions can be reorganized into the state space frequency-dependent model in ANSYS SIMPLORER, as shown in Fig. 8. The model implements bidirectional dynamic data transmission with an application circuit through a multipin connection. Furthermore, the partial inductances and ESRs are fit as functions of the instantaneous switching frequency. As to the state space frequency-dependent model, each pin corresponds to a measuring point designated in Q3D, i.e., Source or Sink. Therefore, as an interface circuit between Q3D and

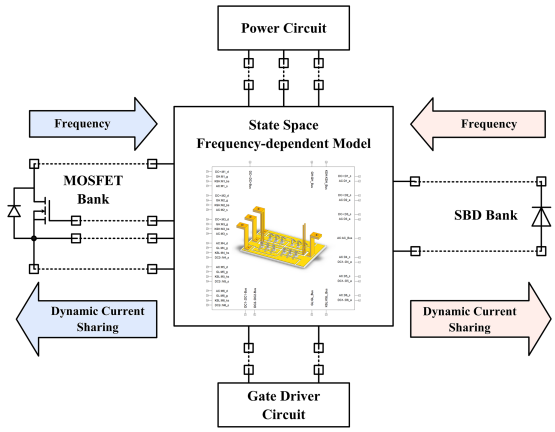

Fig. 8. State space frequency-dependent model derived from the extracted parasitic parameters.

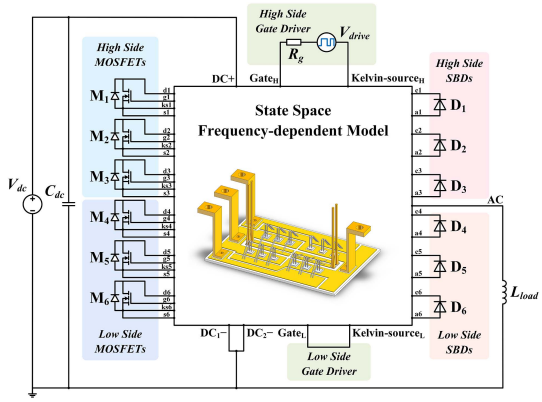

Fig. 9. Electromagnetic coupling simulation topology for high side MOSFETs of layout A as the active switch.

SIMPLORER, the state space frequency-dependent model can be utilized to evaluate the dynamic current sharing.

The electromagnetic coupling simulation is performed using SIMPLORER, as illustrated in Fig. 9. In the state space frequency-dependent model, pins d1-d6 refer to the solder layers at the bottom drain pads of the MOSFET dies. Pins g1-g6 represent the ends of bonding wires connected to the top gate pads, while pins ks1-ks6 and s1-s6 indicate those connected to the top source pads of MOSFET dies. Moreover, pins a1-a6 describe the ends of bonding wires connected to the top anode pads of SBD dies. Pins c1-c6 denote the solder layers at the bottom cathode pads of SBD dies. When the high side MOSFETs are set active, the high side gate driver connected to the Gate_H and $\text{Kelvin-source}_\text{H}$ pins is enabled. Meanwhile, the low side gate driver linked to the Gate_L and $\text{Kelvin-source}_\text{L}$ pins is shorted. DC+, DC_1-, and DC_2- are pins connected to the dc busbar voltage source. DC_1- and DC_2- pins refer to the paralleled double-end negative busbars of the power module with layout A. Pin AC is the output busbar serving a load of the application circuit.

C. Simulation Verification

As illustrated in Section II, dynamic current sharing among paralleled dies depends on whether (19) and (20) are met simultaneously in a multichip power module. Comparing the calculated values of these two equations with the transient switching

TABLE IV
CALCULATED VALUES OF DYNAMIC CURRENT BALANCING EQUATIONS

Layout A $f=10$ MHz		High side switch			Low side switch		
		M_1	M_2	M_3	M_4	M_5	M_6
Calculated values (nH)	E_{19}	38.02	36.62	35.33	46.08	47.94	50.16
	E_{20}	-0.05	0.10	0.21	0.13	0.05	-0.10
Layout B $f=10$ MHz		High side switch			Low side switch		
		M_1	M_2	M_3	M_4	M_5	M_6
Calculated values (nH)	E_{19}	32.72	32.19	31.79	35.97	40.85	46.02
	E_{20}	0.02	0.10	0.18	0.82	1.43	2.01

waveform, the effectiveness of the dynamic current balancing analysis can be verified.

For comparison among paralleled MOSFET dies, the calculated values of the dynamic current balancing (19) and (20) are denoted as E_{19} and E_{20}, respectively, i.e.,

$$\begin{cases} E_{19} = L_{dj} + L_{sj} + 2M_{dsj} \\ E_{20} = M_{dgj} + M_{dkj} + M_{sgj} + M_{skj} \end{cases} \quad j = 1, 2, 3, 4, 5, 6 \tag{21}$$

where L_{dj} and L_{sj} are the self-partial inductances extracted in Section III-A for each paralleled MOSFET die. Similarly, M_{dsj}, M_{dgj}, M_{dkj}, M_{sgj}, and M_{skj} are the mutual partial inductances extracted in the same manner. Besides, all of these partial inductances mentioned in (21) are listed in Table II for layout A and Table III for layout B.

Based on the partial inductances from Tables II and III, the calculated values E_{19} and E_{20} for the paralleled MOSFET dies of layouts A and B are listed in Table IV. Taking the die M_1 of layout A for instance, $L_{d1}=13.20$ nH, $L_{s1}=24.48$ nH, and $M_{ds1}=0.17$ nH can be collected from Table II. According to (21), E_{19} for die M_1 of layout A can be calculated as 38.02 nH. A total of 24 calculated values are obtained in a similar way. The calculation results are divided into four sets representing the high or low side switches for the layout A or B. These four sets of results essentially demonstrate four different cases of the dynamic current sharing. Specifically, the high side switch of layout B presents the slightest difference among the three paralleled MOSFETs, indicating potentially the best dynamic current sharing performance. On the other hand, the low side switch of layout B presents the most significant discrepancy among the three paralleled MOSFETs in (19) and (20), indicating potentially the worst performance.

Additionally, the mutual partial inductances mentioned in (3) and (4) are listed in Table V for layout A and Table VI for layout B, which are extracted from Q3D utilizing the same approach as in Section III-A. The results indicate that the discrepancy of the mutual partial inductances concerning the same kind and different dies can be ignored. Thus, the effectiveness of the assumption in (3) and (4) is verified.

In ANSYS SIMPLORER, a double pulse test circuit is established to assess the switching performance of the three paralleled MOSFETs. This test circuit mainly contains the dc busbar voltage source, energy storage capacitors, decoupling capacitors, load inductor, gate driver, devices under test, and the developed state space frequency-dependent model, as shown in Fig. 9. The gate driver is modeled as a programable voltage source in series with an external gate resistor. Depending on whether the active switch is located on the high or low side, one end of the load inductor is connected to the negative or positive polarity of the dc busbar voltage source. The device models of SiC MOSFETs and SBDs are established using SIMPLORER's inbuilt device characterization tool. Under the operating condition with a 600-V busbar voltage and a 135.6-μH load inductance, the comparison of the simulated switching current at turn-ON and turn-OFF transients are presented in Figs. 10 and 11 separately. Based on the comparison, the high side and low side switches of layout B have the best and worst dynamic current sharing performance, respectively, which is consistent with the calculation results in Table IV.

TABLE V
ASSUMPTION VERIFICATION OF PARTIAL INDUCTANCE FOR LAYOUT A

Layout A $f=10$ MHz	Mutual partial inductance with the same kind and different dies (nH)					
Equation (3) of the assumption	M_{d1d2}	M_{d1d3}	M_{d2d1}	M_{d2d3}	M_{d3d1}	M_{d3d2}
	13.23	13.26	13.23	13.30	13.26	13.30
	M_{d1s2}	M_{d1s3}	M_{d2s1}	M_{d2s3}	M_{d3s1}	M_{d3s2}
	0.11	0.08	0.05	-0.02	-0.06	-0.08
	M_{d1g2}	M_{d1g3}	M_{d2g1}	M_{d2g3}	M_{d3g1}	M_{d3g2}
	4.76	4.80	4.85	4.92	4.97	5.00
	M_{d1k2}	M_{d1k3}	M_{d2k1}	M_{d2k3}	M_{d3k1}	M_{d3k2}
	-4.68	-4.70	-4.73	-4.76	-4.79	-4.82
Equation (4) of the assumption	M_{s1d2}	M_{s1d3}	M_{s2d1}	M_{s2d3}	M_{s3d1}	M_{s3d2}
	0.05	-0.06	0.11	-0.08	0.08	-0.02
	M_{s1s2}	M_{s1s3}	M_{s2s1}	M_{s2s3}	M_{s3s1}	M_{s3s2}
	16.88	16.75	16.88	16.82	16.75	16.82
	M_{s1g2}	M_{s1g3}	M_{s2g1}	M_{s2g3}	M_{s3g1}	M_{s3g2}
	-0.95	-0.93	-0.90	-0.86	-0.84	-0.83
	M_{s1k2}	M_{s1k3}	M_{s2k1}	M_{s2k3}	M_{s3k1}	M_{s3k2}
	0.88	0.87	0.85	0.83	0.82	0.81

TABLE VI
ASSUMPTION VERIFICATION OF PARTIAL INDUCTANCE FOR LAYOUT B

Layout B $f=10$ MHz	Mutual partial inductance with the same kind and different dies (nH)					
Equation (3) of the assumption	M_{d1d2}	M_{d1d3}	M_{d2d1}	M_{d2d3}	M_{d3d1}	M_{d3d2}
	13.26	13.28	13.26	13.34	13.28	13.34
	M_{d1s2}	M_{d1s3}	M_{d2s1}	M_{d2s3}	M_{d3s1}	M_{d3s2}
	-0.24	-0.25	-0.26	-0.26	-0.28	-0.29
	M_{d1g2}	M_{d1g3}	M_{d2g1}	M_{d2g3}	M_{d3g1}	M_{d3g2}
	0.31	0.36	0.42	0.47	0.48	0.49
	M_{d1k2}	M_{d1k3}	M_{d2k1}	M_{d2k3}	M_{d3k1}	M_{d3k2}
	-0.49	-0.53	-0.56	-0.61	-0.64	-0.65
Equation (4) of the assumption	M_{s1d2}	M_{s1d3}	M_{s2d1}	M_{s2d3}	M_{s3d1}	M_{s3d2}
	-0.26	-0.28	-0.24	-0.29	-0.25	-0.26
	M_{s1s2}	M_{s1s3}	M_{s2s1}	M_{s2s3}	M_{s3s1}	M_{s3s2}
	12.55	12.40	12.55	12.47	12.40	12.47
	M_{s1g2}	M_{s1g3}	M_{s2g1}	M_{s2g3}	M_{s3g1}	M_{s3g2}
	-3.26	-3.22	-3.18	-3.13	-3.10	-3.08
	M_{s1k2}	M_{s1k3}	M_{s2k1}	M_{s2k3}	M_{s3k1}	M_{s3k2}
	3.46	3.42	3.39	3.35	3.32	3.30

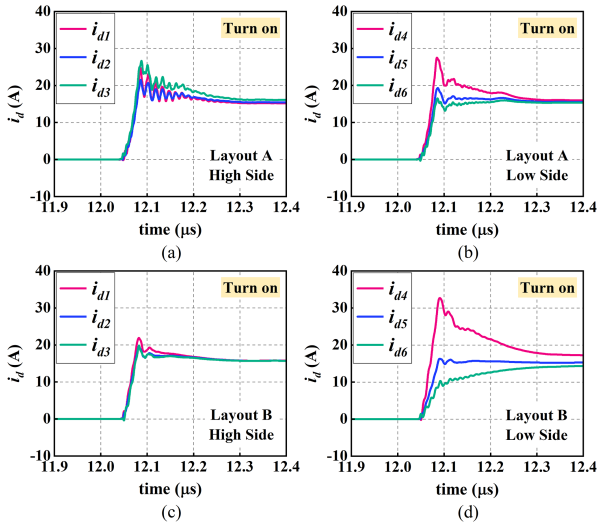

Fig. 10. Simulated switching current at turn-ON transient. (a) High side MOSFETs of layout A. (b) Low side MOSFETs of layout A. (c) High side MOSFETs of layout B. (d) Low side MOSFETs of layout B.

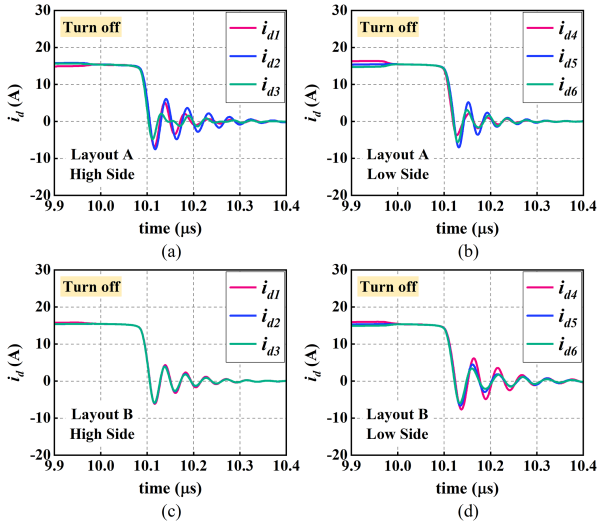

Fig. 11. Simulated switching current at turn-OFF transient. (a) High side MOSFETs of layout A. (b) Low side MOSFETs of layout A. (c) High side MOSFETs of layout B. (d) Low side MOSFETs of layout B.

IV. Experimental Verification on Dynamic Current Balancing in Multichip Power Modules

To further verify the coupled parasitic network model and the dynamic current balancing equations, experiments have been performed on the developed power module prototypes and the results of partial inductances and dynamic switching current are recorded.

A. Experimental Verification of Parasitics Extraction

To verify the extracted parameters of partial inductances, the multichip SiC phase-leg power module prototypes with layouts A and B are developed and measured, as shown in Fig. 12(a).

The measurement of impedance involves applying a current to the device under test and measuring its terminal voltage. Due

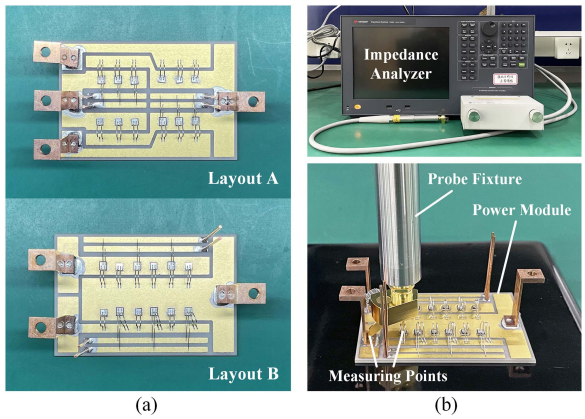

Fig. 12. (a) Fabricated power module prototypes with layouts A and B. (b) Impedance analyzer and probe fixture in the experimental test.

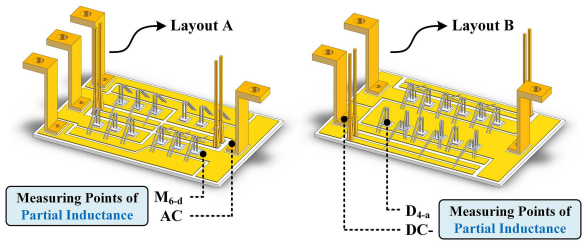

Fig. 13. Measuring points of partial inductances for parasitics verification.

to the relatively small inductance of the device, adopting a high-frequency current injection for a measurable voltage is necessary. As a solution, a KEYSIGHT impedance analyzer E4990A with the frequency ranging from 20 Hz to 120 MHz is utilized to measure the partial inductances. It is worth mentioning that the probe of the impedance analyzer (alligator probe) is excluded due to the nonnegligible inductance of its connecting wires. Compared to the device under test, the wires of the alligator probe introduce parasitics with the same order of magnitude. Therefore, a pin probe is employed instead to more accurately measure the partial inductances with relatively small values, as illustrated in Fig. 12(b). Through careful calibration, the small parasitics of the probe can be well compensated.

On account of the fixed shape, the distance between the two pins of the probe can be adjusted to a limited extent. As a consequence, when the distance between the measuring points exceeds the maximum range that the pins can adjust, the inductances cannot be measured. Accordingly, two partial inductances matching conditions are illustrated in Fig. 13 for experiment verification. However, there are some differences between these two inductances and the partial inductances extracted in Section III. The inductances measured from Fig. 13 are smaller than that extracted in Section III, as one of the measuring points for the former inductances is located on the bottom surface of the busbar. In other words, the parasitic inductances of the busbars are not included in these two inductances. Fig. 14 shows the experimental results of these two partial inductances with a frequency sweep from 100 kHz to 10 MHz. Same as in Section III, the inductances at 10 MHz are recorded. Moreover,

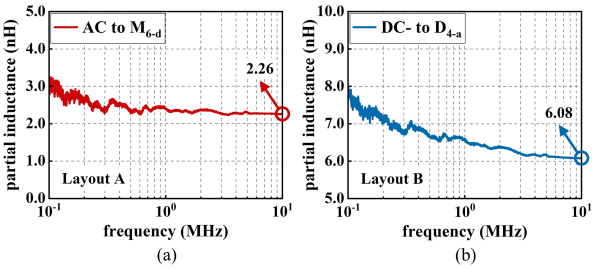

Fig. 14. Experimental results of partial inductances. (a) Measuring points AC to $M_{6\text{-}d}$ for layout A. (b) Measuring points DC- to $D_{4\text{-}a}$ for layout B.

Fig. 15. Double pulse test platform for the studied power modules.

TABLE VII
COMPARISON OF SIMULATION AND EXPERIMENT

f =10 MHz	Partial inductance (nH)		Error
	Simulation	Experiment	
Layout A: AC to $M_{6\text{-}d}$	2.45	2.26	7.76 %
Layout B: DC- to $D_{4\text{-}a}$	6.73	6.08	9.66 %

the comparison of simulation and experiment for these two inductances is listed in Table VII.

B. Experimental Verification of Dynamic Current Sharing

A double pulse test platform is built to assess the switching performance of paralleled SiC MOSFETs for layouts A and B, as shown in Fig. 15. To obtain the current of each MOSFET die in the power module, a PEM Rogowski coil (30 MHz/60 A) is adopted as the current sensor. Due to the small intervals between every two dies, the drain currents of the paralleled SiC MOSFETs are measured one after another. The same Rogowski coil and identical test conditions are applied to each MOSFET die. For ease of the coil passing through the bonding wires, the power modules are submerged in the insulating oil instead of encapsulated by silica gel. In addition, a solid-state circuit

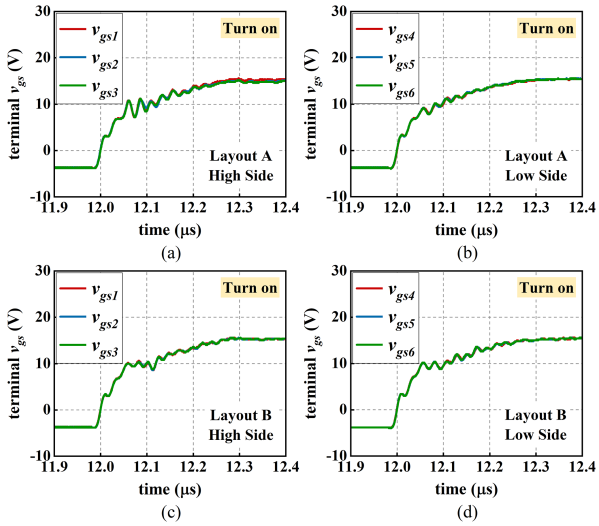

Fig. 16. Experimental turn-ON terminal v_{gs}. (a) High side for layout A. (b) Low side for layout A. (c) High side for layout B. (d) Low side for layout B.

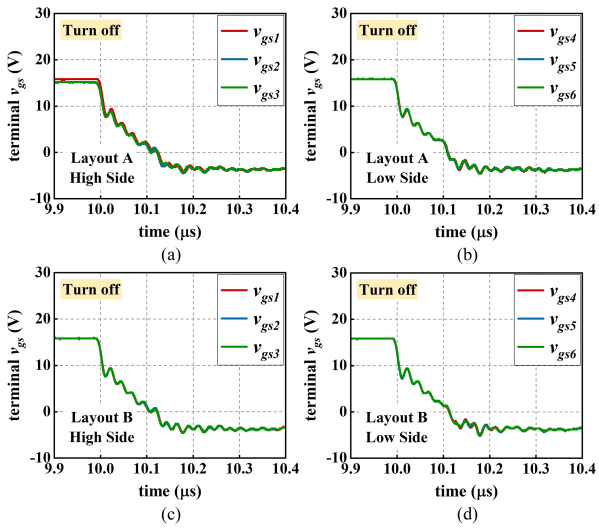

Fig. 17. Experimental turn-OFF terminal v_{gs}. (a) High side for layout A. (b) Low side for layout A. (c) High side for layout B. (d) Low side for layout B.

breaker (SSCB) is equipped to the double pulse test platform for overcurrent protection.

The experiment tests are performed by four groups, i.e., high or low side switches for the layout A or B. The busbar voltage is set to 600 V, while the 135.6-μH load inductance is selected. With regard to the drive board, R_{gon} and R_{goff} are both 6.8 Ω. The drive voltage applied to the gate and Kelvin-source busbars is -4/+16 V. Additionally, the gate-source voltages of these two busbar terminals are recorded in Figs. 16 and 17. The results indicate that the test conditions are set uniformly for each paralleled MOSFET die, allowing for a fair comparison of the dynamic current sharing. The experimental switching current at the turn-ON and turn-OFF transients are depicted in Figs. 18 and 19. Due to the lack of preselection for the paralleled dies before fabricating the studied power module prototypes, the mismatches of device parameters induce errors between the simulation and experiment. Overall, since the dynamic current

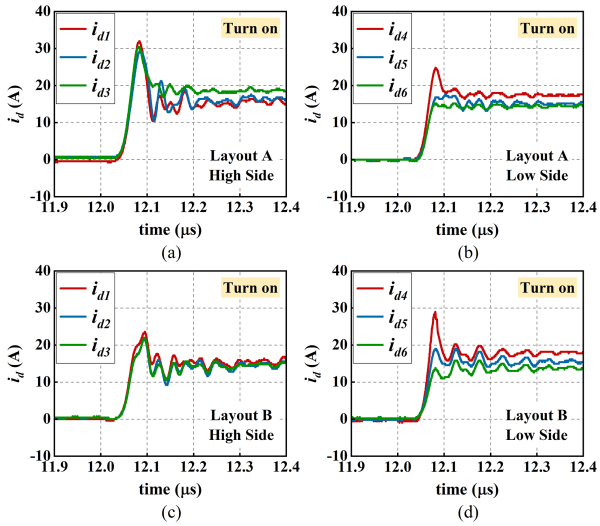

Fig. 18. Experimental switching current at turn-ON transient. (a) High side MOSFETs of layout A. (b) Low side MOSFETs of layout A. (c) High side MOSFETs of layout B. (d) Low side MOSFETs of layout B.

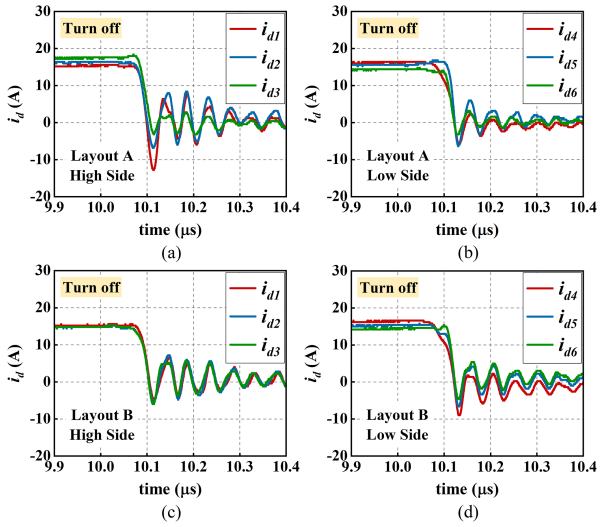

Fig. 19. Experimental switching current at turn-OFF transient. (a) High side MOSFETs of layout A. (b) Low side MOSFETs of layout A. (c) High side MOSFETs of layout B. (d) Low side MOSFETs of layout B.

balancing equations are basically satisfied, the high side MOSFETs of layout B achieve desirable dynamic current balancing.

V. Conclusion

This article presents a coupled parasitic network model to analyze the mechanism of the layout-dominated dynamic current balancing in multichip SiC power modules. Particularly, the impact of self and mutual partial inductances among several current segments involved in the switching transients is taken into consideration. Based on the proposed model, two dynamic current balancing equations are identified, which can serve as current balancing optimization guidelines for designing the layout of multichip power modules. By comparing the power modules with two commonly used layouts, both simulation and experiment verify the effectiveness of the proposed model and equations with high accuracy. As for the application in the layout designing, to satisfy the dynamic current balancing equations, the relevant partial inductances can be varied by adjusting the shape of the copper trace, the arrangement of the paralleled dies, and the connection points of the bonding wires on the copper trace.

References

[1] K. Rajashekara, "Present status and future trends in electric vehicle propulsion technologies," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 1, pp. 3–10, Mar. 2013.

[2] S. Yin, K. J. Tseng, R. Simanjorang, Y. Liu, and J. Pou, "A 50-kW high-frequency and high-efficiency SiC voltage source inverter for more electric aircraft," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9124–9134, Nov. 2017.

[3] X. Du, F. Diao, Z. Zhao, and Y. Zhao, "A 25kW silicon carbide 3kV/540V series-resonant converter for electric aircraft systems," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 1183–1188.

[4] B. Mouawad, J. Espina, J. Li, L. Empringham, and C. M. Johnson, "Novel silicon carbide integrated power module for EV application," in *Proc. 1st Workshop Wide Bandgap Power Devices Appl. Asia*, 2018, pp. 176–180.

[5] M. Guacci, D. Bortis, I. F. Kovačević-Badstübner, U. Grossner, and J. W. Kolar, "Analysis and design of a 1200 V all-SiC planar interconnection power module for next generation more electrical aircraft power electronic building blocks," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 4, pp. 320–330, Dec. 2017.

[6] L. Zhang, X. Yuan, X. Wu, C. Shi, J. Zhang, and Y. Zhang, "Performance evaluation of high-power SiC MOSFET modules in comparison to si IGBT modules," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1181–1196, Feb. 2019.

[7] Z. Zeng, X. Zhang, and Z. Zhang, "Imbalance current analysis and its suppression methodology for parallel SiC MOSFETs with aid of a differential mode choke," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1508–1519, Feb. 2020.

[8] Z. Wang, M. Chinthavali, S. L. Campbell, T. Wu, and B. Ozpineci, "A 50-kW air-cooled SiC inverter with 3-D printing enabled power module packaging structure and genetic algorithm optimized heatsinks," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 6256–6265, Nov./Dec. 2019.

[9] H. Li et al., "Influences of device and circuit mismatches on paralleling silicon carbide MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 621–634, Jan. 2016.

[10] X. Li et al., "EM-electrothermal analysis of semiconductor power modules," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 9, no. 8, pp. 1495–1503, Aug. 2019.

[11] U. Scheuermann, "Paralleling of chips—From worst-case scenario to a statistical approach," *EngineerIT*, pp. 39–41, 2008.

[12] M. Wang, F. Luo, and L. Xu, "A double-end sourced wire-bonded multichip SiC MOSFET power module with improved dynamic current sharing," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1828–1836, Dec. 2017.

[13] H. Li, S. Munk-Nielsen, S. Bęczkowski, and X. Wang, "A novel DBC layout for current imbalance mitigation in SiC MOSFET multichip power modules," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8042–8045, Dec. 2016.

[14] B. Zhao, P. Sun, Q. Yu, Y. Cai, and Z. Zhao, "Layout-dominated dynamic imbalanced current analysis and its suppression strategy of parallel SiC MOSFETs," *IEEE Trans. Device Mater. Rel.*, vol. 21, no. 3, pp. 394–404, Sep. 2021.

[15] Z. Zeng, X. Zhang, and X. Li, "Layout-dominated dynamic current imbalance in multichip power module: Mechanism modeling and comparative evaluation," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11199–11214, Nov. 2019.

[16] C. Zhao, L. Wang, F. Zhang, and F. Yang, "A method to balance dynamic current of paralleled SiC MOSFETs with Kelvin connection based on response surface model and nonlinear optimization," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2068–2079, Feb. 2021.

[17] S. Bęczkowski, A. B. Jørgensen, H. Li, C. Uhrenfeldt, X. Dai, and S. Munk-Nielsen, "Switching current imbalance mitigation in power modules with parallel connected SiC MOSFETs," in *Proc. 19th Eur. Conf. Power Electron. Appl.*, 2017, pp. 1–8.

[18] Z. Chen, "Electrical integration of SiC power devices for high-power-density applications," Ph.D. dissertation, Dept. Elect. Eng., Virginia Polytechnic Inst. State Univ., Blacksburg, VA, USA, 2013.
[19] A. Dutta, "A low temperature co-fired ceramic (LTCC) interposer based three-dimensional stacked wire bondless power module," Ph.D. dissertation, Dept. Elect. Eng., Univ. Arkansas, Fayetteville, AR, USA, 2017.
[20] B. Yang and J. Zhang, "Effect and utilization of common source inductance in synchronous rectification," in *Proc. 20th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2005, pp. 1407–1411.
[21] F. Merienne, J. Roudet, and J. L. Schanen, "Switching disturbance due to source inductance for a power MOSFET: Analysis and solutions," in *Proc. 27th Annu. IEEE Power Electron. Specialists Conf.*, 1996, pp. 1743–1747.
[22] C. R. Paul, *Inductance: Loop and Partial.* Hoboken, NJ, USA: Wiley, 2010, pp. 195–205.
[23] H. Daou, M. Ameziani, D. Lhotellier, F. Costa, M. Petit, and E. Labouré, "Dynamic electric model for IGBT power module based on Q3D and simplorer: 3D layout design, stray inductance estimation, experimental verifications," in *Proc. Int. Conf. Elect. Syst. for Aircr., Railway, Ship Propulsion Road Veh. Int. Transp. Electrific. Conf.*, 2016, pp. 1–6.
[24] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET multichip phase-leg module for high-temperature, high-frequency applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2307–2320, May 2014.
[25] C. Qian, Z. Wang, G. Xin, and X. Shi, "Datasheet driven switching loss, turn-on/off overvoltage, di/dt, and dv/dt prediction method for SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9551–9570, Aug. 2022.
[26] J. Sun, L. Yuan, R. Duan, Z. Lu, and Z. Zhao, "A semiphysical semibehavioral analytical model for switching transient process of SiC MOSFET module," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 2258–2270, Apr. 2021.
[27] *ANSYS Electronics Desktop Online Help*, ANSYS Inc., Canonsburg, PA, USA, 2015.

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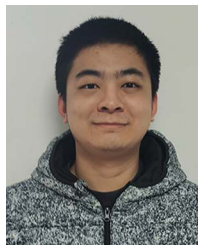

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