Isolated 3-Level DC–DC Converter With Complete ZVS Using Magnetizing Inductors

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***Abstract*—An isolated dc–dc converter with dedicated 3-level modulation is proposed to achieve a 4:1 output voltage range, and complete zero-voltage-switching (ZVS) of all active switches using the magnetizing inductors. The single input 3-level modulation scheme coordinates the phase-shift, duty cycle, and switching frequency to ensure 1) the magnetizing currents are independent of load voltage and current; 2) the output voltage is proportional to the modulation input. As a result, the dual half- and full-bridge modes of the switching network are unified and modeled as a voltage-controlled voltage source, with the same control parameters for both modes of operation. In addition, the magnetizing-to-series inductance ratios of the leading and lagging transformers are increased to 100 and 25 times, respectively. Therefore, the circulating current is low, and the series inductors can be integrated into the transformers. The proposed topology is intended for high-power applications with a wide output voltage range but less input voltage variation. A 30 kW prototype with a power density of 7.2 kW/L and an output voltage of 165 V-680 V was built and tested to verify the characteristics and feasibility of the proposed H8 topology plus modulation scheme.**

***Index Terms*—Battery chargers, dc/dc converters, electric vehicle (EV), isolated 3-level, magnetizing inductor, modulation, zero-voltage-switching.**

I. Introduction

A HIGH-POWER off-board dc charger with a 4:1 (the highest: the lowest output voltage) range and very high overall efficiency is critical to accommodate the different battery voltages of various electric vehicles (EVs). Although LLC and phase-shift full-bridge (PSFB) converters are widely used, they have inherent disadvantages in applications with wide output voltage ranges.

As shown in Fig. 1(a), the LLC converter could achieve complete ZVS with magnetizing inductor [1], [2], [3]. However, in order to obtain a 4:1 output range, the LLC converter requires a more wide operating frequency range (3:1) and a lower L_m/L_k (magnetizing to series inductance) ratio (less than 0.7), which results in a higher circulating current and lower overall efficiency [4], [5]. Moreover, large ac resonant inductors have high core losses and copper losses.

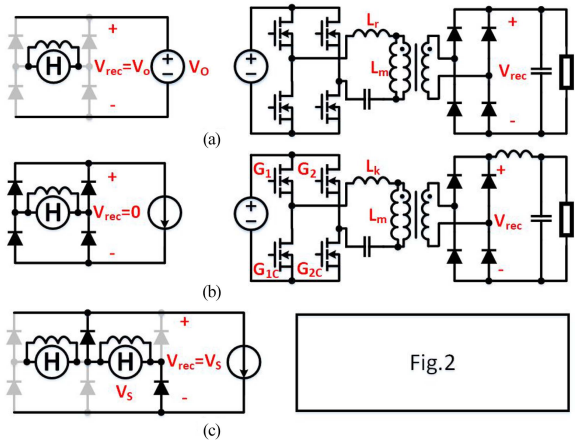

Fig. 1. Utilization of magnetizing inductor L_m for ZVS transition. (a) Load-independent ZVS enabled by L_m in LLC (voltage-type output); (b) Ineffective L_m in PSFB (current-type output); (c) Adaptive ZVS enabled by L_m in the proposed circuit (current-type output).

Several works exploit topology morphing to narrow the optimization range of LLC resonant converters [6], [7], [8]. In [6], the L_m/L_k ratio increased to 5.65. However, the additional RMS current on the active switches due to magnetizing current is still high. Besides, the modulation and control parameters need to be customized for the different operating modes. Topology morphing with more operational modes is employed in [9], [10], [11], [12] to further narrow the optimization scope for applications with wider gain ranges. However, the controls and modulations are more complicated and harder to manage. Besides, for high power wide output voltage range applications, the total circulating current is still high due to the large variation of the magnetizing current.

The buck-type PSFB converter suffers considerable circulating current when the phase shift is large. Besides, the ZVS of the lagging leg is lost under light load conditions [13], [14], [15], [16], [17], [18], [19]. The PSFB cannot effectively use the magnetizing current to help ZVS because L_m is shorted during the lagging leg transition, and the magnetizing current amplitude decreases proportionally when the phase-shift increases, as shown in Fig. 1(b).

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A straightforward way to extend the ZVS range is to proportionally increase the magnetizing current as the phase-shift increases [20]. Nonetheless, the magnetizing inductor remains shorted during the lagging leg transition, and ZVS is lost at low phase-shift and light load conditions during the passive-to-active transition. Another approach is to add the constant magnetizing current of another converter to the current of the series inductor to extend the ZVS range of the lagging leg [21]. But in the free-wheeling stage, since the two transformers on the secondary side are connected in series, a circulating current will be generated. As a result, excessive conduction loss is caused. The circulation problem is alleviated in [22], but the circulation current still exists. The voltage stress on the secondary-side diodes is much higher due to the small resetting capacitor. Additionally, single full-bridge operation mode suffers from the same issue as traditional PSFBs.

Another approach is combining the ZVS principle of the LLC with a buck-type PSFB. The idea is that the output is clamped and supported by a voltage source during the transition to force the L_m in series with L_k and then charge/discharge C_{oss} together. The solution in [23] and [24] exploits this principle to achieve a full-range ZVS for the leading leg. But the lagging leg can only achieve zero-current-switching (ZCS). The solution in [25] achieves the full-range ZVS for the lagging leg, but the leading leg loses ZVS at very light load conditions. Besides, the output voltage range is limited to 2:1 because of the 2-level operation. There are dc–dc converters with 3-level modulation and a wide gain range in [26], [27], [28]. However, they suffer from passive-to-active transition problems like conventional PSFB. For phase-shifted converters with current-mode outputs, and a wide gain range (4:1 or more), achieving full-range ZVS from no load to full load is challenging.

The main goal of this article is to achieve an isolated dc–dc converter with a 4:1 output voltage range and a full-range ZVS from no-load to full-load using independent magnetizing currents. In particular, the main contributions of this work can be summarized as follows: 1) Isolated H8 dc–dc converter with 3-level modulation scheme integrates the dual full-bridge (FB) and dual half-bridge (HB) modes with only one control variable, for phase, duty cycle, and frequency coordination; 2) The two operating modes of the switching network are unified and modeled as a voltage-controlled voltage source, and the control parameters of the two operating modes are the same; 3) The magnetizing to leakage inductance ratios of the leading and lagging transformers are improved to 100 and 25 times, respectively. Therefore, the circulating current is low, and the series inductors can be integrated into transformers; 4) Experimental evaluation of the performance of the proposed isolated H8 topology and 3-level modulation based on a 30 kW prototype with a 4:1 output voltage range.

II. Operating Principle and Average Model of the Proposed Isolated H8 DC–DC Converter

A. Circuit Topology and Switching States

The circuit configuration of the proposed converter is shown in Fig. 2. The two active H-bridges on the primary side and the asymmetric 3-phase diode bridge on the secondary side provide the degrees of freedom to achieve full-range ZVS enabled by independent magnetizing currents and 3-level operation by integrating the FB and HB modes. The isolated H8 topology has 36 valid switching states shown in Table I and eight are selected to enable a 4:1 wide voltage gain range with a 3-level operation and the independent peak current of two magnetizing inductors.

All voltages in this section are normalized to per-unit values. The bases for the primary and secondary sides are E and E/n,

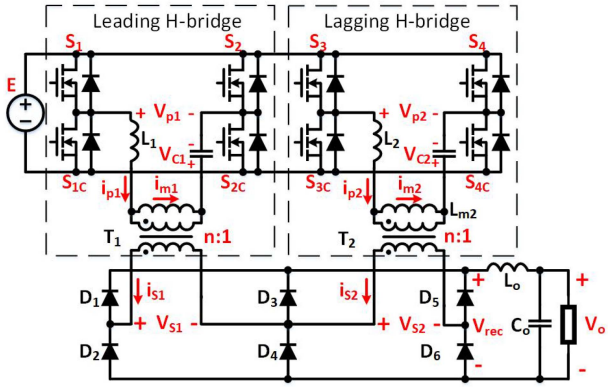

Fig. 2. Circuit configuration of isolated H8 DC–DC converter.

TABLE I
Switching States and Associated Outputs for the Proposed H8 Isolated DC–DC Converter

State	Input variables						Intermediate		Output
	S_1	S_2	V_{C1}	S_3	S_4	V_{C2}	V_{S1}	V_{S2}	V_{rec}
1	1	0	0	1	0	0	1	1	2
2	0	1	0	0	1	0	-1	-1	2
3	1	0	0	1	0	0.5	1	0.5	1.5
4	0	1	0	0	0	0.5	-1	-0.5	1.5
5	1	0	0.5	1	0	0	0.5	1	1.5
6	0	0	0.5	0	1	0	-0.5	-1	1.5
7	1	0	0	0	1	0	1	-1	1
8	0	1	0	1	0	0	-1	1	1
9	1	0	0	0	0	0.5	1	-0.5	1
10	0	1	0	1	0	0.5	-1	0.5	1
11	1	0	0	0	0	0	1	0	1
12	1	0	0	1	1	0	1	0	1
13	0	1	0	0	0	0	-1	0	1
14	0	1	0	1	1	0	-1	0	1
15	1	0	0.5	0	1	0	0.5	-1	1
16	0	0	0.5	1	0	0	-0.5	1	1
17	1	0	0.5	1	0	0.5	0.5	0.5	1
18	0	0	0.5	0	0	0.5	-0.5	-0.5	1
19	0	0	0	1	0	0	0	1	1
20	1	1	0	1	0	0	0	1	1
21	0	0	0	0	1	0	0	-1	1
22	1	1	0	0	1	0	0	-1	1
23	1	0	0.5	0	0	0.5	0.5	-0.5	0.5
24	0	0	0.5	1	0	0.5	-0.5	0.5	0.5
25	1	0	0.5	0	0	0	0.5	0	0.5
26	1	0	0.5	1	1	0	0.5	0	0.5
27	0	0	0.5	0	0	0	-0.5	0	0.5
28	0	0	0.5	1	1	0	-0.5	0	0.5
29	0	0	0	1	0	0.5	0	0.5	0.5
30	1	1	0	1	0	0.5	0	0.5	0.5
31	0	0	0	0	0	0.5	0	-0.5	0.5
32	1	1	0	0	0	0.5	0	-0.5	0.5
33	0	0	0	0	0	0	0	0	0
34	0	0	0	1	1	0	0	0	0
35	1	1	0	0	0	0	0	0	0
36	1	1	0	1	1	0	0	0	0

respectively, where E is the input voltage, and n is the primary to secondary transformer turns ratio shown in Fig. 2.

The active switches in the same HB are complementary and defined as S_k and S_{kc} $(k = 1, 2, 3, 4)$. S_1 to S_4 are four independent control variables and are defined in (1).

$$S_{k(c)} = \begin{cases} 1, & S_{k(c)} \text{ is on} \\ 0, & S_{k(c)} \text{ is off} \end{cases} \quad (k = 1, 2, 3, 4). \tag{1}$$

The two H-bridges could work in FB mode or HB mode to extend the output voltage range. In the FB mode, the output voltages of the two H-bridges are symmetrical, and the dc blocking capacitor voltage $V_{c(p.u.)}$ is 0. In the HB mode, $S_2(S_4)$ is always 0 (or 1). Therefore, the corresponding $V_{c(p.u.)}$ is 0.5 (or -0.5). Without loss of generality, only consider $V_{c(p.u.)} = 0.5$ case in the design, as shown as follows:

$$V_{Cn(p.u.)} = \begin{cases} 0.5, & \text{half-bridge mode} \\ 0, & \text{full-bridge mode} \end{cases} \quad (n = 1, 2). \tag{2}$$

The voltages across series inductors L_1 and L_2 are neglected for simplicity. The series inductors L_1 and L_2 are in series with the output filter inductor and the load except for dead time, and the latter two have much higher impedance. As for the deadtime, it is less than 3% of the switching cycle in this article. Therefore, ignoring the voltages across series inductors L_1 and L_2 does not significantly affect the main characteristics of the converter. Based on the Kirchhoff's Voltage Law, the output voltages V_{S1} and V_{S2} of the two H-bridges are derived

$$\begin{cases} V_{S1(p.u.)} = S_1 - S_2 - V_{C1(p.u.)} \\ V_{S2(p.u.)} = S_3 - S_4 - V_{C2(p.u.)}. \end{cases} \tag{3}$$

For the leading H-bridge, there are six possible combinations of input variables S_1, S_2, V_{C1}, and corresponding output V_{S1} after removing the symmetric $V_{c(p.u.)} = -0.5$ cases. Similarly, the lagging H-bridge also has six cases. Therefore, there are $6 \times 6 = 36$ inputs combinations in Table I.

An asymmetric three-phase diode rectifier connects the two H-bridges' outputs through isolation transformers. $|V_{S1}|$ is the rectified voltage of diode bridge formed by D_1, D_2, D_3, and D_4. $|V_{S2}|$ is the rectified voltage of diode bridge formed by D_3, D_4, D_5, and D_6. $|V_{S1} + V_{S2}|$ is the rectified voltage of diode bridge formed by D_1, D_2, D_5, and D_6. The output of the three parallel diode bridges is the highest value among $|V_{S1}|$, $|V_{S2}|$, and $|V_{S1} + V_{S2}|$. Therefore, the relationship between inputs V_{S1} and V_{S2} and rectified output V_{rec} can be described in (4). Table I is built based on (1)–(4)

$$V_{\text{rec}} = \max\{|V_{S1}|, |V_{S2}|, |V_{S1} + V_{S2}|\}. \tag{4}$$

To make sure the two H-bridges could serve as a voltage source for each other, eliminate the free-wheeling current, and make magnetizing current always triangular shape, the switching states with zero intermediate voltage V_{S1} and V_{S2} are eliminated. The combination of states (3,4,9,10) and (5,6,15,16) with 1–1.5 normalized output voltage range are removed because they overlap with the 1–2 range of switching states combination (1,2,7,8). The remaining eight switching states 1, 2, 7, 8, 17, 18, 23, and 24 in Table I are selected to implement the 3-level operation and 4:1 output voltage range, which is verified by the last column in Table I.

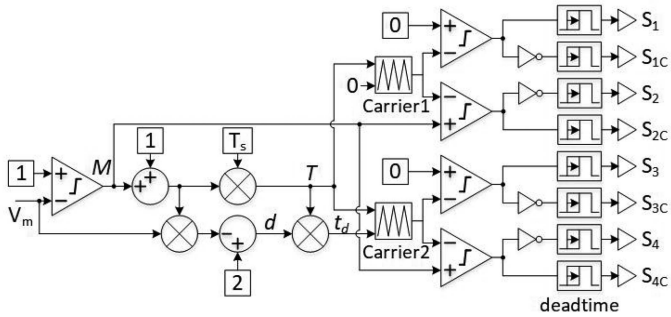

Fig. 3. Function blocks of the proposed 3-level modulation to realize 1) the magnetizing currents are independent of load voltage and current; 2) the output voltage is proportional to the modulation input.

B. 3-Level Modulator for H8 DC–DC Converter

The modulation targets to achieve a 3-level operation with a proportional output voltage to the modulation input, and independent peak magnetizing currents using one unified modulation input V_m. The existing 3-level modulations use interleaved or cascaded carriers with fixed frequency and phase-shift [29], [30], [31], [32]. While in the proposed modulation, one unified control variable V_m coordinates variable phase-shift t_d between carriers 1 and 2, switching period T, and 3-level operation altogether. The functional blocks of the proposed modulator use only one input, V_m, to generate gating signals for all eight switches in dual half-bridge and full-bridge modes, as shown in Fig. 3. The two carriers are symmetrical triangular waveforms with a minimum value of -1 and a maximum value of 1. V_m controls the operation mode. When $V_m \geq 1$, the comparator output M is 0, resulting in a 50% duty cycle for both leading and lagging H-bridges. When $V_m < 1$, comparator output M is 1, and it result in a 100% duty cycle for S_{2C} and S_{4C} and a 0% duty cycle for S_2 and S_4. T controls the switching period. It is $2T_s$ in dual half-bridge mode and T_s in dual full-bridge mode, which will be proved in (11). The phase-shift between the leading and lagging H-bridges is controlled by t_d, which is the multiplication of d in (5) and T_s in (11). d is the phase-shift ratio for one switching cycle, as shown in Fig. 4. The deadtime is generated by turn-ON delays.

The time-domain waveforms of 3-level modulation is shown in Fig. 4 and the proposed modulation function is shown in (5) and Fig. 5. d is defined as the ratio of the time duration of state 23 (or 7) and half of switching period $T_{S1}/2$ (or $T_{S2}/2$)

$$d = \begin{cases} 2 - 2V_m, & \frac{1}{2} \leq V_m < 1 \\ 2 - V_m, & 1 \leq V_m \leq 2. \end{cases} \tag{5}$$

The output voltage of the proposed circuit is equal to the average rectification voltage V_{rec}, as shown as follows:

$$V_{o(p.u.)} = \overline{V}_{rec(p.u.)} \tag{6}$$

If the normalized output voltage is between 0.5 and 1, switching states 17, 18, 23, and 24 are selected and combined in the way shown in the left part of Fig. 4. Since both H-bridges work

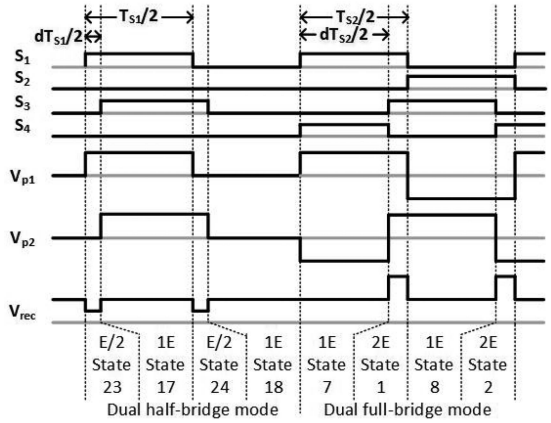

Fig. 4. Time-domain waveforms of the 3-level modulation.

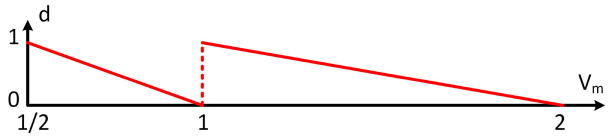

Fig. 5. Modulation function for isolated H8 DC–DC converter.

as HB, this mode is defined as dual HB mode. In this case, the switching period is T_{S1}. The output voltage is calculated as follows:

$$\overline{V}_{\mathrm{rec}(p.u.)} = (1-d)\cdot 1 + d\cdot\frac{1}{2} = \frac{1}{2}(2-d). \tag{7}$$

The magnetizing current peak in this case is shown as follows:

$$I_{m_{pk1}} = \frac{1}{2}\cdot\frac{E}{2}\cdot\frac{T_{S1}}{2}\cdot\frac{1}{L_m} = \frac{E\cdot T_{S1}}{8L_m}. \tag{8}$$

Similarly, if the normalized output voltage is between 1 and 2, switching states 1, 2, 7, and 8 are selected and combined in the way shown in the right part of Fig. 4. This mode is defined as dual FB mode. In this case, the switching period is T_{S2}. The output voltage is calculated as follows:

$$\overline{V}_{\mathrm{rec}(p.u.)} = (1-d)\cdot 2 + d = 2-d. \tag{9}$$

The magnetizing current peak, in this case, is shown as follows:

$$I_{mpk2} = \frac{1}{2}\cdot E\cdot\frac{T_{S2}}{2}\cdot\frac{1}{L_m} = \frac{E\cdot T_{S2}}{4L_m}. \tag{10}$$

To fully utilize the magnetic cores and improve the overall efficiency, the volt–second of transformers and output inductor, which are proportional to the peaks of the magnetizing currents, are designed to be the same for the dual HB and FB modes. Therefore, the relationship between T_{S1} and T_{S2} is derived in (11).

$$T_{S1} = 2\cdot T_{S2} \triangleq 2\cdot T_S. \tag{11}$$

From (8), (10), and (11), the amplitude of the magnetizing current depends on the volt–second and the magnetizing inductance, which are designed to be the same. Therefore, the magnetizing current is independent of output voltage, current, and phase variations in the proposed modulation scheme.

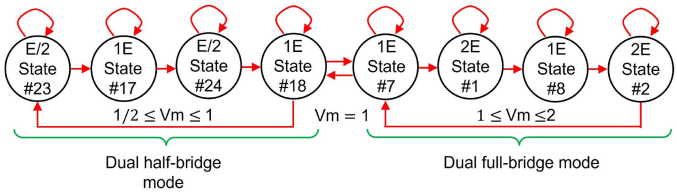

Fig. 6. State transition diagram of the proposed modulation.

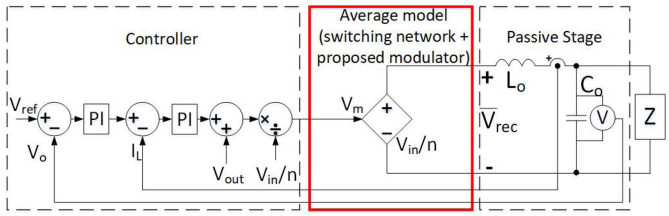

Fig. 7. Control blocks based on the average model of the switching network and the proposed modulator.

According to the time-domain modulation shown in Fig. 4 and the proposed modulation function (5), the state transition diagram is obtained and shown in Fig. 6.

Substituting (5) into (7) and (9), the relationship between modulation input V_m and the average of rectification voltage $\overline{V}_{\mathrm{rec}}$ is derived in (12). $\frac{V_{in}}{n}$ is the voltage base of the secondary side

$$\overline{V}_{\mathrm{rec}} = V_m * \frac{V_{\mathrm{in}}}{n}. \tag{12}$$

Combining (6) and (12), the normalized output voltage $V_{o(p.u.)}$ is equal to the modulation input V_m for the whole 4:1 output voltage range. Therefore, it is mathematically verified that the proposed 3-level modulation scheme, which uses only one control variable, ensures two targets at the same time: 1) the peak magnetizing currents of the two transformers are independent of load voltage, current; 2) the output voltage is proportional to the modulation input V_m.

C. Average Model of the Switching Network Plus the Proposed Modulator

The state-of-the-art modulation for the dc–dc converter with topology morphing is a simple combination of case-by-case modes [7], [9]. Moreover, the control parameter must be customized for each operating mode. However, in this article, the two operation modes of the switching network and the proposed modulator are unified and modeled as a voltage-controlled voltage source, and the control parameters are the same for both cases. The proposed converter system is controlled just like a classic buck converter.

Based on (12), the proposed modulator in Fig. 3 and the switching network with two operation modes are unified and modeled as a voltage-controlled voltage source in Fig. 7. The input, gain, and output of the voltage-controlled voltage source are the modulation index V_m, secondary-side voltage base V_{in}/n, and the average of the rectified voltage $\overline{V}_{\mathrm{rec}}$.

As a result, the control parameters are the same whether in the dual full-bridge mode or the dual half-bridge mode, and

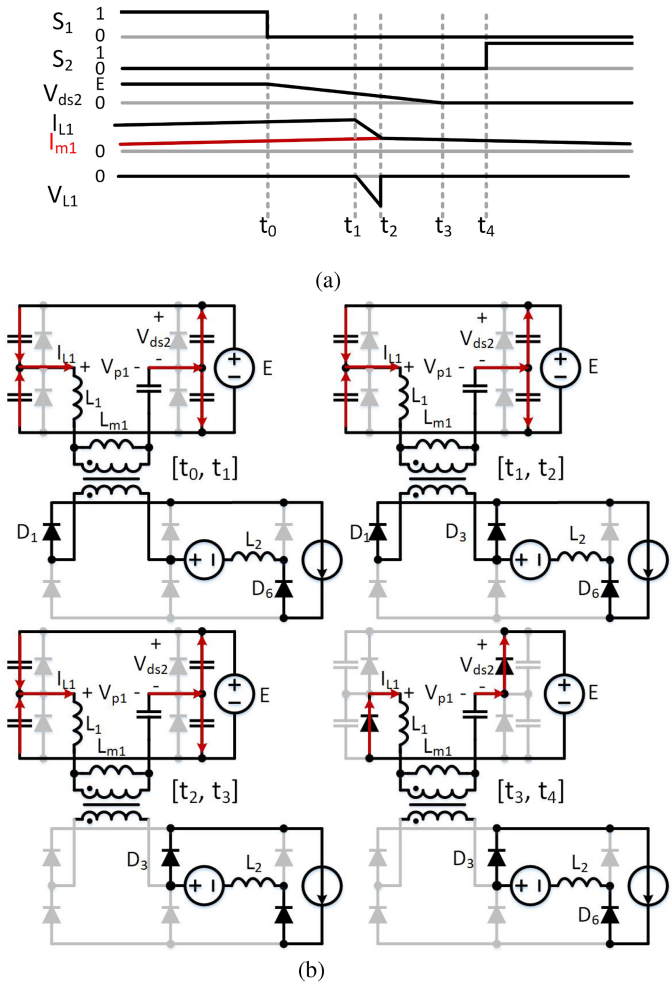

Fig. 8. Full-range ZVS in the leading H-bridge. (a) Time domain waveforms. (b) Mode analysis.

the control of the proposed converter can be the same as a buck circuit. This article adopts a classic dual-loop control for the proposed topology, as shown in Fig. 7. It also has the output voltage feedforwad and the input voltage feedforward to counteract the disturbance caused by the input and output voltage variations.

D. Full-Range ZVS for the Leading H-Bridge

As discussed in Section II, the ZVS of the leading H-bridge is enabled by the independent magnetizing current. Moreover, the magnetizing inductor is released in mode (t_2, t_3), which makes the ZVS condition independent of the series inductance. The leading H-bridge time-domain ZVS transitions and mode analysis are shown in Fig. 8. The full load-range ZVS energy and the timing requirements are also presented.

$Mode\,[t_0, t_1]$: S_1 is turned OFFat t_0 but series inductor current i_{L1} is almost constant before V_{ds2} drops to $V_{in}/2$ ($V_{P1} = 0$ at this point). i_{L1} and V_{ds2} can be expressed as (13) and (14). I_{Lo} is the load current, n is the transformer turns ratio, and C_{oss} is the output capacitance of a single active switch at the primary side.

$$i_{L1} = I_{mpk} + \frac{I_{Lo}}{n_1} = -2C_{\text{oss}}\frac{dv_{ds2}}{dt} \tag{13}$$

$$v_{ds2} = V_{in} - \frac{I_{mpk} + I_{Lo}/n_1}{2C_{\text{oss}}}t. \tag{14}$$

The time duration of V_{ds2} dropping from E to $E/2$ is derived as follows:

$$\Delta t_{01} = \frac{V_{\text{in}}C_{\text{oss}}}{I_{mpk} + I_{Lo}/n_1}. \tag{15}$$

$Mode\,[t_1, t_2]$: at t_1, V_{ds2} equals $E/2$ and i_{L1} begins to drop until reaches magnetizing current i_{m1} at t_2. v_{ds2}, i_{L1}, and time duration of this mode Δt_{12} are described in (16)–(18), where $Z_0 = \sqrt{\frac{L_1}{C_{\text{oss}}}}$, $\omega_0 = \frac{1}{\sqrt{L_1 C_{\text{oss}}}}$, and $i_{L1} = I_{mpk} + I_{Lo}/n$.

$$v_{ds2} = \frac{V_{in}}{2} - \frac{i_{L1}(t_1)Z_0}{2}\sin\omega_0(t - t_1) \tag{16}$$

$$i_{L1} = i_{L1}(t_1)\cos\omega_0(t - t_1) \tag{17}$$

$$\Delta t_{12} = \frac{1}{\omega_0}\arccos\frac{I_{mpk}}{i_{L1}(t_1)}. \tag{18}$$

$Mode\,[t_2, t_3]$: the output of the leading H-bridge is blocked and clamped by the output of the lagging H-bridge. Therefore, L_{m1} is released to be in series with L_1 and charge/discharge the C_{oss} together. v_{ds2} and i_{L1} are described in (19) and (20), where $Z_1 = \sqrt{\frac{L_1 + L_{m1}}{C_{\text{oss}}}}$ and $\omega_1 = \frac{1}{\sqrt{(L_1 + L_{m1})C_{\text{oss}}}}$. The equations could be simplified given that L_{m1} is much larger than L_1 and the resonant period of $(L_1 + L_{ms})$ and C_{oss} is much longer than the deadtime

$$v_{ds2} = \frac{V_{\text{in}}}{2} + \left(V_{ds2}(t_2) - \frac{V_{\text{in}}}{2}\right)\cos\omega_1(t - t_2) - \frac{I_{mpk}Z_1}{2}\sin\omega_2(t - t_2) \approx V_{ds2}(t_2) - \frac{I_{mpk}}{2C_{\text{oss}}}(t - t_2) \tag{19}$$

$$i_{L1} = \frac{2V_{ds}(t_2) - V_{\text{in}}}{Z_1}\sin\omega_1(t - t_2) + I_{mpk}\cos\omega_1(t - t_2). \tag{20}$$

This mode ends when V_{ds2} drops to zero. The time duration of this mode is derived in (21). As a result, the soft-switching energy could be mainly provided by the magnetizing inductor, and the full-range ZVS is independent of L_1

$$\Delta t_{23} = \frac{2V_{ds2}(t_2)C_{\text{oss}}}{I_{mpk}}. \tag{21}$$

$Mode\,[t_3, t_4]$: at t_3, V_{ds2} remains at 0 and the body diodes of S_2 and S_{1C} conduct. S_2 and S_{1C} are turned ON at t_4, and the soft-switching process for the leading H-bridge is done. The voltage on L_1 is still close to 0, and the voltage drop is mainly on L_{m1}. It is worthwhile to point out that active switches' low turn-ON current (equals magnetizing current) is true under all conditions because of the low series inductance.

Similar to LLC, the full-range ZVS of the leading H-bridge is enabled by the magnetizing inductor under any output voltage

and current and phase variations. Moreover, the ZVS condition is independent of the value of L_1.

Based on the analysis above, the worst case for ZVS energy requirement is at no-load condition. It can be satisfied if

$$\frac{1}{2}L_{m1}I_{mpk}^2 \geq 4 * \frac{1}{2}C_{\text{oss}}V_{\text{in}}^2. \tag{22}$$

Substituting (10), (11) into (22), the maximum magnetizing inductance is

$$L_{m1} \leq \frac{T_s^2}{64\text{Coss}}. \tag{23}$$

Based on (15), (18), (21), the ZVS timing requirement is satisfied over the full load-range if the deadtime is longer than the maximum value of Δt_{03}

$$t_{d1} \geq \Delta t_{03}\text{max} = \frac{2V_{in}C_{\text{oss}}}{I_{mpk}}. \tag{24}$$

The magnetizing inductance design also ensures that the active switches' RMS current is increased by less than 2.5% compared to the RMS current without magnetizing current. The currents through the active switches are a pulsating waveform with linear ripples. Based on the RMS current value presented in the [33, appendix A.1], the circulating magnetizing current limitation equation is shown as follows:

$$\sqrt{1+\frac{1}{3}\left(\frac{nI_{mpk}}{I_o}\right)^2} < 1.025. \tag{25}$$

Inserting (10) and (11) into (24) and (25), and combining the energy requirement in (22), the requirement for the magnetizing inductance is derived as follows:

$$\frac{nET_s}{1.56I_o} \leq L_{m1} \leq \min\left(\frac{T_s t_{dt}}{8C_{\text{oss}}}, \frac{T_s^2}{64\text{Coss}}\right). \tag{26}$$

If the output capacitance C_{oss} is 350 pF, the switching frequency is 140 kHz, and the deadtime is less than 1% of the switching period, the reasonable range for the magnetizing inductance is 107–127 μH to achieve full load-range ZVS. In the prototype, L_{m1} is 110 μH.

For the leading H-bridge, series inductor L_1 is designed as small as possible because: 1) the ZVS is independent of L_1; 2) lower series inductance could reduce the magnetic loss, duty cycle loss, and the stress on the snubber circuit; 3) the small series inductance creates the low current turn-ON condition for active switches, and the turn-ON current is the amplitude of the magnetizing current. In the prototype, the primary and secondary windings are interleaved to get the minimum leakage inductance, which is 1.1 μH.

E. Full-Range ZVS for the Lagging H-Bridge

The full-range ZVS from no-load to full-load could be achieved if the energy and timing requirements given in this section are met. The required series inductance is reduced compared to PSFB because the independent peak magnetizing current guarantees the minimum current through the series inductor. The lagging H-bridge time-domain waveforms and mode analysis are shown in Fig. 9.

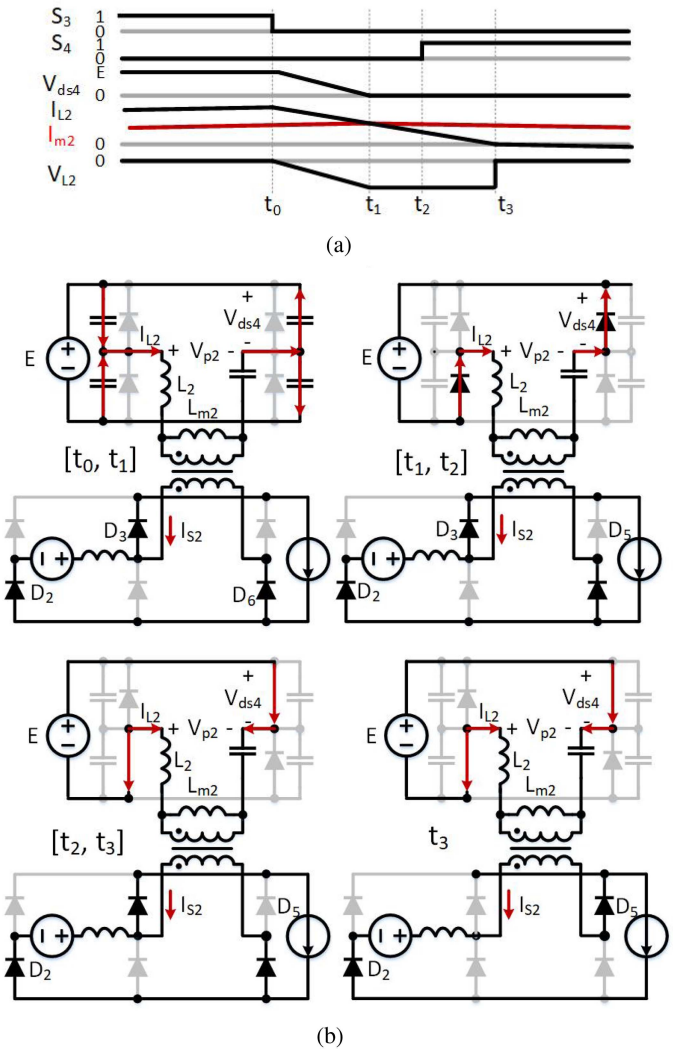

Fig. 9. Full-range ZVS in the lagging H-bridge. (a) Time domain waveforms. (b) Mode analysis at light load condition.

Mode[t_0, t_1]: S_3 and S_{4C} are turned OFFat t_0. The minimum initial value of i_{L2} is guaranteed by the peak magnetizing current I_{mpk}. This mode ends when V_{ds4} drops to zero at t_1. The voltage v_{ds4} and series inductor current i_{L2} are described in (27) and (28), where $Z_2 = \sqrt{\frac{L_1+L_2}{C_{\text{oss}}}}$, $\omega_2 = \frac{1}{\sqrt{(L_1+L_2)C_{\text{oss}}}}$, and $i_{L_2}(t_0) = I_{mpk} + I_{Lo}/n$.

$$v_{ds4} = V_{\text{in}} - \frac{i_{L_2}(t_0)Z_2}{2}\sin\omega_2(t-t_0) \tag{27}$$

$$i_{L2} = I_{mpk} + (I_{L_o}/n)\cos\omega_2(t-t_0). \tag{28}$$

The minimum value for $i_{L2}(t_0)$ is the peak magnetizing current I_{mpk}. To make sure V_{ds4} could drop to zero in this mode, V_{in} needs to be smaller than $0.5I_{mpk}Z_2$ in (27). This is equivalent to the energy requirement to achieve ZVS described in (32).

The time duration for this mode is derived as follows:

$$\Delta t_{01} = \frac{1}{\omega_2}\arcsin\frac{2V_{\text{in}}}{(I_{L_o}/n + I_{mpk})Z_2}. \tag{29}$$

Mode[t_1, t_2]: At t_1, the body diodes of S_4 and S_{3C} conduct. The current through L_2 linearly drops as described in (30). Turn ON S_4 and S_{3C} before i_{L2} drops to zero, and finish the ZVS process for the lagging H-bridge

$$i_{L2} = i_{L2}(t_1) - \frac{2V_{\text{in}}}{L_1 + L_2}(t - t_3). \tag{30}$$

The time duration for this mode needs to meet the requirement in (31) to make sure i_{L2} is still positive when turning on S_4 and S_{3C}

$$\Delta t_{12} \le \frac{i_{L2}(t_3)(L_1 + L_2)}{2V_{\text{in}}}. \tag{31}$$

The ZVS energy requirement is shown as follows:

$$\frac{1}{2}(L_1 + L_2)I_{mpk}^2 \ge \frac{1}{2}(4C_{\text{oss}})V_{\text{in}}^2. \tag{32}$$

Substituting (10) into (32), get (33)

$$L_2 > \frac{64C_{\text{oss}}L_{m2}^2}{T_s^2} - L_1. \tag{33}$$

The magnetizing inductance is also designed to ensure the active switches' RMS current is increased by less than 2.5% compared to the RMS current without magnetizing current, as shown in (25).

Therefore, the maximum magnetizing current peak is 12 A. Based on (10), considering 700 V input voltage and 140 kHz switching frequency, the minimum L_{m2} is 107 μH. The magnetizing inductor L_{m2} is 110 μH in this design.

Based on the energy limitation described in (33), considering 350 pF C_{oss}, 700 V V_{in}, 11.5 A I_{mpk}, 110 μH L_{m2}, 1.1 μH L_1, the minimum L_2 is 4.2 μH. In this article, L_2 is 4.4 μH.

Based on (29), (31), the timing constrain for the deadtime t_{d2} in the worst case is derived in (34). All the coefficients are constant values. Using the parameters presented above, the range for the deadtime is 69–113 ns. This article adopts 110 ns.

$$\frac{1}{\omega_2}a\sin\frac{2V_{\text{in}}}{I_{mpk}Z_2} < t_{d2} < \frac{1}{\omega_2}a\sin\frac{2V_{\text{in}}}{I_{mpk}Z_2} + \frac{I_{mpk}(L_1 + L_2)}{2V_{\text{in}}}. \tag{34}$$

III. Design Considerations

The volt–seconds of the transformers and output inductor are kept the same in the dual FB/HB mode by adjusting the switching frequency in (11). Therefore, the transformer and output inductor designs for the two modes are the same. The dc blocking capacitor and the output capacitor are designed at the dual half-bridge mode, in which the voltage ripple is more significant because of the lower switching frequency.

A. Transformers Turns Ratio

Assume the turns ratio for the leading and lagging transformers are $n_1 : 1$ and $n_2 : 1$, respectively. Based on (4), the minimum output voltage for the dual FB mode is (35) and the maximum output voltage for the dual HB mode is (36). The equality happens when $n_1 = n_2$. Therefore, the transformers' turns ratio needs to be the same to make the output voltage consecutive. The turns ratio is redefined as n.

$$V_{o-\min-FB} = \max\left\{\frac{E}{n_1}, \frac{E}{n_2}\right\} \tag{35}$$

$$V_{o-\max-HB} = \frac{E}{2n_1} + \frac{E}{2n_2} \le \max\left\{\frac{E}{n_1}, \frac{E}{n_2}\right\}. \tag{36}$$

The turns ratio n is determined by the maximum output voltage and minimum input voltage, as shown as follows:

$$n = \frac{2V_{in-\min}}{V_{o-\max}}. \tag{37}$$

B. Design of DC Blocking Capacitor

The voltage rating of the dc blocking capacitors is half of the input voltage rating considering the dual half-bridge mode shown in (2).

The dc blocking capacitors C_1 and C_2 are designed based on (38) to make the voltage ripple at the maximum load current in the dual half-bridge mode within a reasonable range

$$C_1 = C_2 \ge \frac{I_o T_{s1}}{2n\Delta V}. \tag{38}$$

Considering 10% voltage ripple, $650 - 750$ V input voltage, 60 A load current, 70 kHz switching frequency at dual half-bridge mode, and 2:1 turns ratio, ceramic capacitors with 700 V voltage rating and 3μF capacitance are adopted.

C. Output LC Filter Design

For the dual full-bridge mode, the peak-to-peak current ripple is designed less than 20% of the rated current, as shown in (39). The dual half-bridge mode follows the same rule:

$$\Delta i_{pk-pk} = \frac{(V_o - V_{in}/n)dT_s/2}{L_o}. \tag{39}$$

Substituting (9) into (39), get

$$L_o \ge \frac{d(1-d)V_{\text{in}}T_s}{2n\Delta i_{pk-pk}}. \tag{40}$$

The relationship among the required output capacitance, filter inductor current ripple, output voltage ripple, and switching period is derived as follows:

$$C_o \ge \frac{\Delta i_{pk-pk}T_{s1}}{8\Delta v_{pk-pk}}. \tag{41}$$

Given 700 V input voltage, 70/140 kHz switching frequency at the dual half/full-bridge mode, 2:1 turns ratio, 60 A maximum load current, and 20% current ripple, 1 V voltage ripple, the minimum filter inductance and capacitance are 26 μH and 10.7 μF, respectively.

D. Voltage Stress, Current Stress, and RMS Current of All Passive Components and Semiconductor Devices

The voltage stress, current stress, and RMS current of all passive components are summarized in Table II, in which $V_{\text{in}} = 750$ V (maximum input voltage), $I_o = 60$ A (Maximum load current), $I_{mpk} = 11.5$ A (magnetizing current peak), $n = 2$ (turns ratio), and $\Delta i_{pk-pk} = 12$ A.

TABLE II
VOLTAGE AND CURRENT STRESS OF THE ACTIVE AND PASSIVE COMPONENTS IN THE PROPOSED CONVERTER

	Parameters	Equation	Value
Active Switches	Voltage stress	V_{in}	$750V$
	Current stress	$I_o/n + I_{mpk}$	$41A$
	RMS current	$\frac{\sqrt{2}I_o}{2n}\sqrt{1+\frac{1}{3}(\frac{nI_{mpk}}{I_o})^2}$	$22.7A$
Diodes	Voltage stress	$D_3, D_4 : V_o/(2D); Others : V_o/D$	$D_3, D_4 : 355V; Others : 710V$
	Current stress	I_o	$60A$
	RMS current	$\sqrt{2}I_o/2$	$42.4A$
Transformers with integrated inductor	Voltage Stress(primary)	V_{in}	$750V$
	Current Stress(primary)	$I_o/n + I_{mpk}$	$41A$
	RMS current(primary)	$\frac{I_o}{n}\sqrt{1+\frac{1}{3}(\frac{nI_{mpk}}{I_o})^2}$	$32A$
DC blocking capacitor	Voltage Stress	$V_{in}/2$	$375V$
	RMS Current	$\frac{I_o}{n}\sqrt{1+\frac{1}{3}(\frac{nI_{mpk}}{I_o})^2}$	$32A$
Output inductor	Voltage Stress	$2V_{in}/n$	$750V$
	RMS Current	I_o	$60A$
Output capacitor	Voltage Stress	V_o	$682V$
	RMS Current	$\Delta i_{pk-pk}/2\sqrt{3}$	$3.5A$

TABLE III
TOPOLOGY COMPARISONS FOR HIGH-POWER WIDE OUTPUT VOLTAGE RANGE APPLICATIONS

	LLC [5]	Ref [6]	PSFB [13]	Ref [21]	Ref [25]	This paper
Gain range	5:1	4:1	>4:1	2:1	2:1	4:1
free-wheeling current	Zero	Zero	Large	Medium	Zero	Zero
Additional conduction loss due to I_m	16.6%	14.75%	0%	5.8%/0%	4.6%/0.1%	2.4%/2.4%
Full-range ZVS from no-load to full-load	Yes	Yes	No	No	No	Yes
Voltage/Current-type filter	Voltage-type	Voltage-type	Current-type	Current-type	Current-type	Current-type
RMS Current on output capacitor	$0.482I_o$	$0.482I_o$	$\frac{\Delta i_{opk-pk}}{2\sqrt{3}}$	$\frac{\Delta i_{opk-pk}}{2\sqrt{3}}$	$\frac{\Delta i_{opk-pk}}{2\sqrt{3}}$	$\frac{\Delta i_{opk-pk}}{2\sqrt{3}}$
External AC inductor	Very Large	Large	Medium	No	Medium	No
Output inductor voltage level	N/A	N/A	2-level	3-level	3-level	3-level
Duty cycle loss	N/A	N/A	High(9.7%)	Low(No data)	Medium (7.5%)	Low (3.7%)
Suitable power level	$0.2-20kW$	$0.2-20kW$	$0.2-20kW$	$0.2-20kW$	$0.2-20kW$	$20-200kW$

Compared to the LLC converter, the RMS current of the active switches and diodes are reduced more than 10% and the conduction loss is reduced more than 20% because of the low magnetizing current and the square current shape. The transformer VA rating of the LLC converter is also more than 10% larger than the proposed converter.

Compared to the PSFB converter, the RMS current of the active switches and diodes is increased 2.5% and the conduction loss is increased 5% because of the additional magnetizing current. However, the active switches in the proposed converter could achieve full-range ZVS from no-load to full-load conditions. The existence of magnetizing currents reduces the required series inductance, duty cycle loss, stress on the snubber circuit, magnetic loss, and the volume of magnetic material significantly.

E. Topology Comparisons for the High-Power Wide Output Voltage Range Applications

The comparisons among the state-of-the-art topologies for the high-power wide output voltage range applications are summarized in Table III and explained below.

Compared to the normal LLC converter [5] and the LLC converter with topology morphing [6], the proposed converter prevails in high-power EV charger applications with a 4:1 gain range or above because 1) a much lower additional conduction loss due to the magnetizing current to achieve ZVS from no-load to full-load, 2) no need for extra LC filters for battery charger applications, 3) more than eight times RMS current reduction on the output capacitor, which is one of the bottom legs of the converter's lifetime, 4) no bulky external ac inductors.

Compared to the PSFB converter and other phase-shifted converters with an extended ZVS range utilizing magnetizing inductor, the proposed converter is the most suitable option in high-power applications with a wide output voltage range because 1) the capability to achieve full-range ZVS from no-load to full-load with zero free-wheeling current and low additional conduction loss due to the magnetizing current, 2) extremely low duty cycle loss and no need for external AC inductors due to the small series inductance. 3) Three-level operation and more than 50% size reduction on the output inductor compared to the PSFB converter with the 2-level operation.

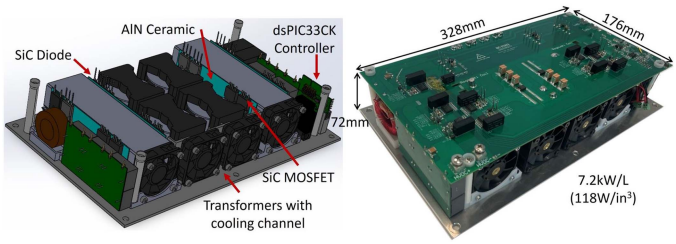

Fig. 10. 30 kW Prototype with 7.2 kW/L power density.

TABLE IV
PARAMETERS OF THE PROTOTYPE

Paras	Specifications	Parameters	$T_{X1/2}$ Specs
V_{in}	$650V-750V$	T_1: $L_{k1}:1.1\mu H$ $L_{m1}:110\mu H$ $2*T_{X1}$ (primary winding in series, secondary winding in parallel)	Core: PC95PQ65/54-Z air gap: 0.6mm winding:7:7 fully interleaved
V_{out}	$165V-682V$		
I_{out}	$60A$		
f_{sw}	$140/70kHz$		
$S_{1-4(c)}$	$1200V/25m\Omega$		
D_{1-6}	$1200V/100A$		
C_o	$1200V/12\mu F$		
$C_{1/2}$	$700V/3\mu F$		
L_o	Core: 2 sets of E42/21/20 airgap:2.5mm	T_2: $L_{k2}:4.4\mu H$ $L_{m2}:110\mu H$ $2*T_{X2}$ (primary winding in series, secondary winding in parallel)	Core: PC95PQ65/54-Z air gap:0.6mm winding:7:7 pri/shunt/sec magnetic shunt: 2mm*7mm $180\mu_0$
	Winding: 14 turns litz wire with 4000 strands of AWG44		

The proposed converter is only suitable for the high-power (>20 kW) applications.

IV. EXPERIMENTAL VERIFICATION

A 30 kW hardware prototype with 7.2 kW/L power density shown in Fig. 10 has been designed, fabricated, and tested to verify the circuit operation. The virtual prototyping design on the left shows the inner structure of the prototype. The power module consists of power devices with TO-247 package, low-cost AlN ceramic, and heatsink [34]. The transformers with integrated series inductors are enclosed within the cooling channel. Microchip fixed-point DSC dsPIC33CK256MP508 is used to implement the modulation and close-loop control [35].

The specifications of the prototype are listed in Table IV. Based on the voltage and current rating listed in Table II, the semiconductors and passive components are selected considering a certain amount of margin. The SiC MOSFET $MSC025SMA120B4$ and SiC Schottky diodes $MSC050DA120BCT$ from Microchip serve as the power semiconductors. Both leading and lagging transformers consist of two sets of ferrite cores PC95PQ65/54-Z with a 0.6 mm air gap to fully utilize the height and improve the power density. The windings are in series at the primary side and in parallel at the secondary side to make the current sharing balanced. The primary and secondary windings of the leading transformer are fully interleaved to minimize the leakage inductance. For the lagging transformer, the 7-turn windings at the primary and secondary sides are separated as inner and outer layers, respectively. A magnetic shunt with 180 relative permeability, 2 mm thickness and 7 mm height is placed between the primary and secondary side windings to get the required series inductance. The output inductor also adopts ferrite core and Litz wire considering the size limitation and high-frequency current ripple(12 A 280 kHz).

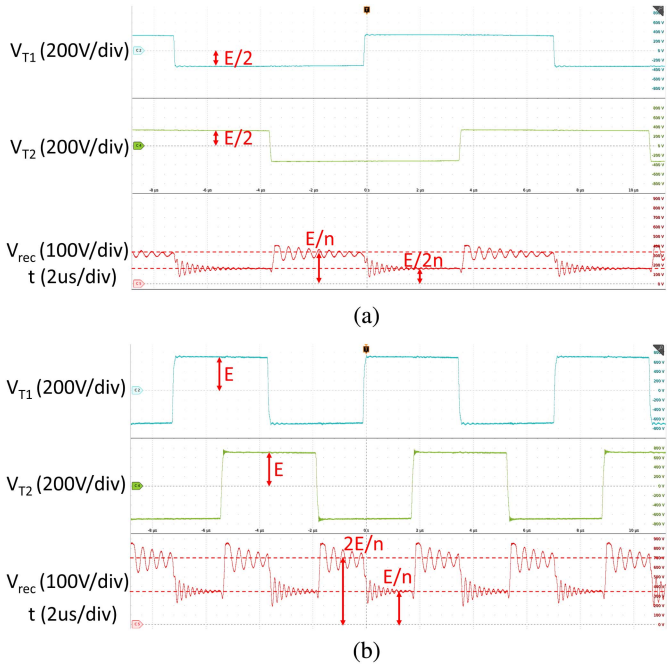

Fig. 11. Verification of 3-level modulation with unified modulation input V_m. (a) $V_m = 0.75$ (dual HB mode, 70 kHz). (b) $V_m = 1.5$ (dual FB mode, 140 kHz).

To validate the 3-level modulation using one unified modulation input V_m, two cases are shown in Fig. 11. V_{T1} and V_{T2} are the voltages across the primary side of the two transformers, including the leakage inductors. The outputs of the two transformers are in series when the polarities are the same and in parallel when the polarities are opposite. As a result, the rectification voltage V_{rec} operates between E/n and $E/2n$ when $V_m = 0.75$ and between E/n and $2E/n$ when $V_m = 1.5$, where E is 700 V and n equals 2.

Fig. 12 verifies that the volt–seconds applied on the primary side of transformers remain the same whatever the modulation index, operational mode, and switching frequencies. Combining the unchanged volt-seconds with (8), (10), the magnetizing currents of the two transformers are always triangular, and the amplitudes are kept the same under all conditions.

Fig. 13 shows the experimental verification of the active switches' ZVS operation under no load conditions, which is the worst case. By observing that V_{ds1} and V_{ds3} drop to zero before S_1 and S_3 turn ON at different V_m, both figures indicate that full-range ZVS is achieved.

The ZVS of the lagging H-bridge is always maintained during the load step transition, as shown in Fig. 14. The load steps from 1 to 8 kW with 400 V output voltage. The ZVS of the leading H-bridge is not shown here because it has a much better ZVS condition.

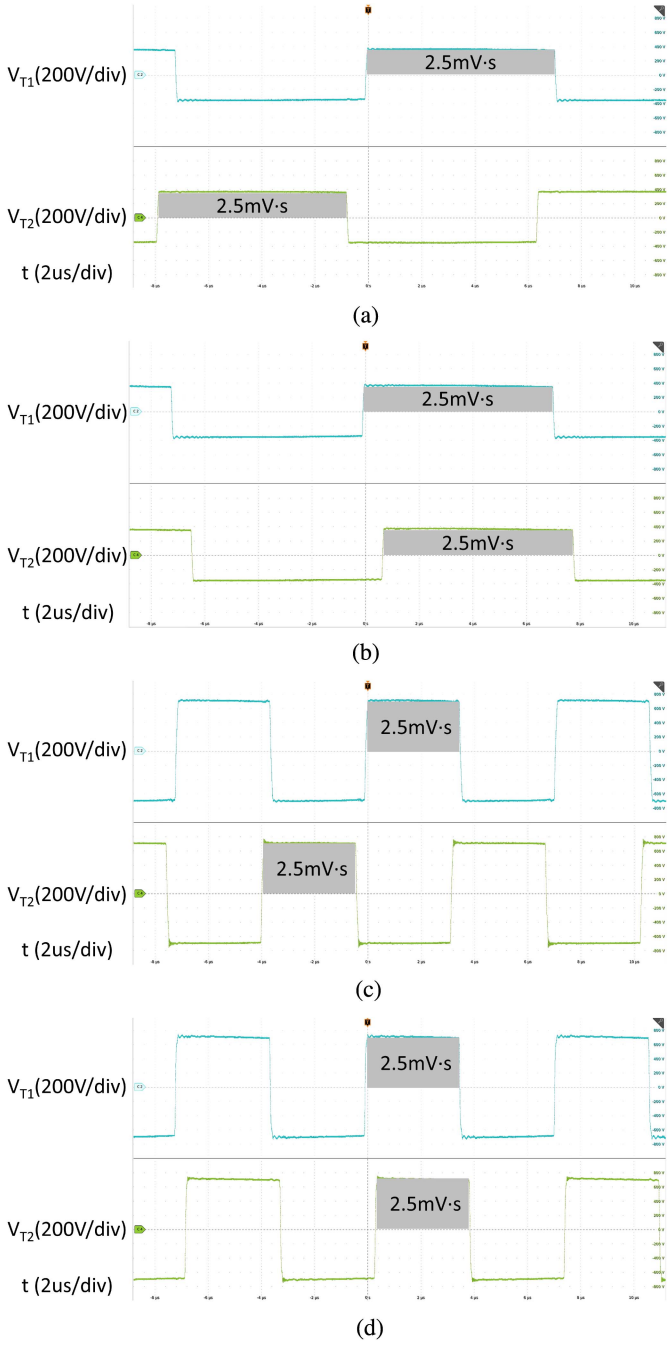

Fig. 12. Constant volt–second and peak magnetizing current at different modulation input V_m and operational modes. (a) $V_m = 0.55$ (dual HB mode, 70 kHz). (b) $V_m = 0.95$ (dual HB mode, 70 kHz). (c) $V_m = 1.1$ (dual FB mode, 140 kHz). (d) $V_m = 1.9$ (dual FB mode, 140 kHz).

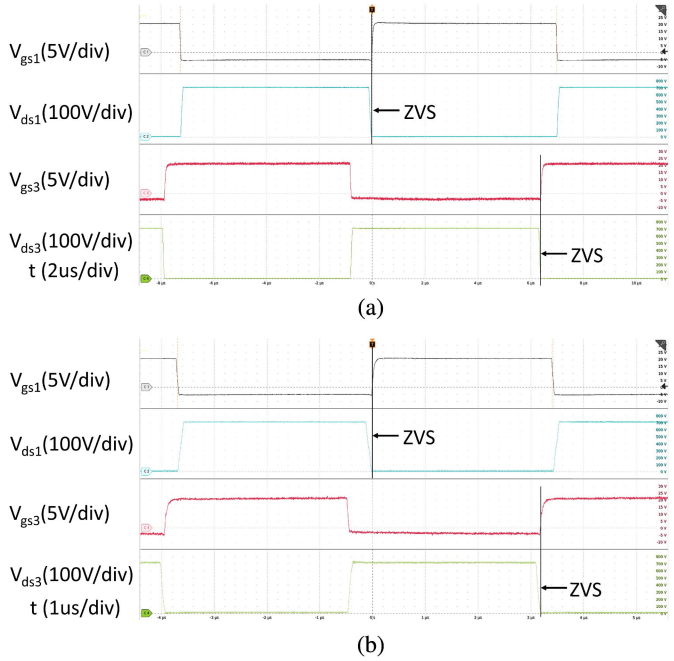

Fig. 13. Verification of the full-range ZVS. (a) $V_m = 0.55$ (dual HB mode, 70 kHz). (b) $V_m = 1.1$ (dual FB mode, 140 kHz).

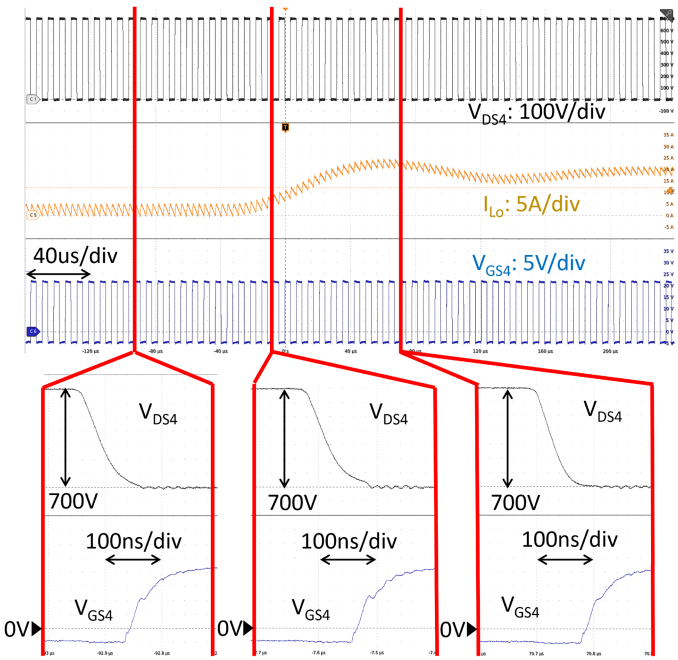

Fig. 14. ZVS of the lagging H-bridge during load step from 1 to 8 kW.

The ZVS of the lagging H-bridge is also maintained during the input step transition, as shown in Fig. 15. The input voltage steps from 750 to 650 V within 400 μs.

Fig. 16 shows the load step response. The input voltage is 700 V, and the output voltage target is 500 V. The load resistance steps from 23 to 17 Ω using a 2-pole mechanical switch gear. As a result, the output power steps from 11 to 15 kW. The output voltage dip is 20 V, and the time duration is within 12 ms. In the EV charger application, the load would not have such a sudden change, and the output voltage variation would be much smaller.

The input voltage step response is shown in Fig. 17. The input voltage drops from 700 to 650 V within 500 μs. Output voltage variation is less than 5 V. The output is not affected much due to the feedforward of the input voltage.

The efficiency contour map and 3D map in Figs. 18 and 19 are drawn based on 102 experimental points evenly distributed within the operational area. A 300 kW adjustable load bank is

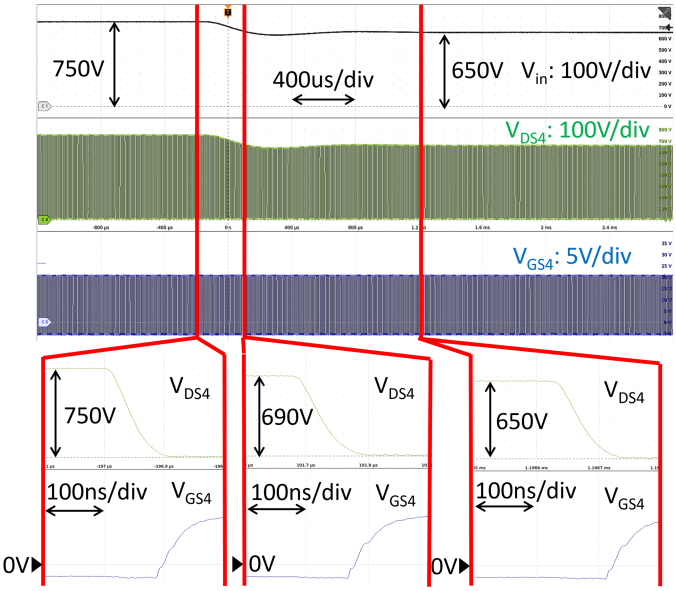

Fig. 15. ZVS of the lagging H-bridge during input voltage step from 750 to 650 V.

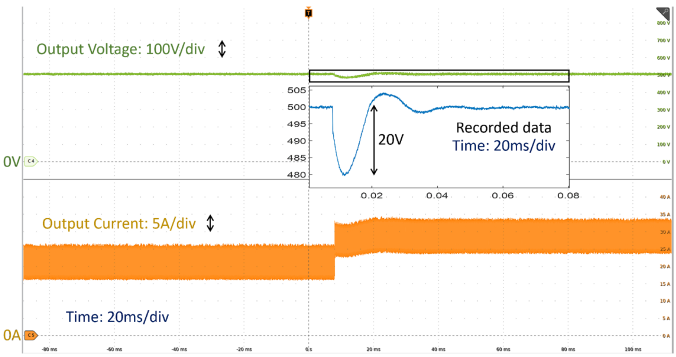

Fig. 16. Load step response from 11 to 15 kW at 500 V output voltage.

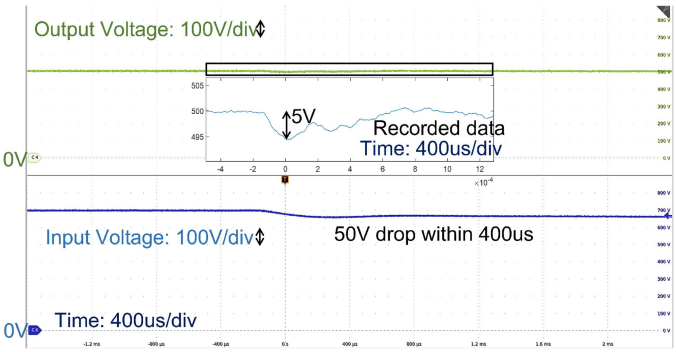

Fig. 17. Input voltage step response at 500 V output voltage and 11 kW output power.

configured under different output voltage and current to get the efficiency contour map. The phase-shift is adjusted within the operational region to regulate the output voltage under different load conditions. While on the boundaries, the phase-shift is kept constant at the minimum/maximum value, and the output voltage drops when the load gets heavier because of the duty cycle loss and voltage drop on the ESR.

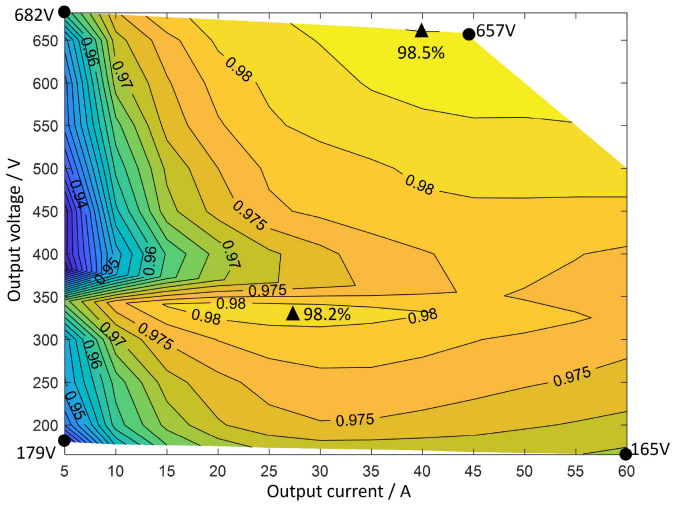

Fig. 18. Efficiency contour map and output boundaries based on experiment results.

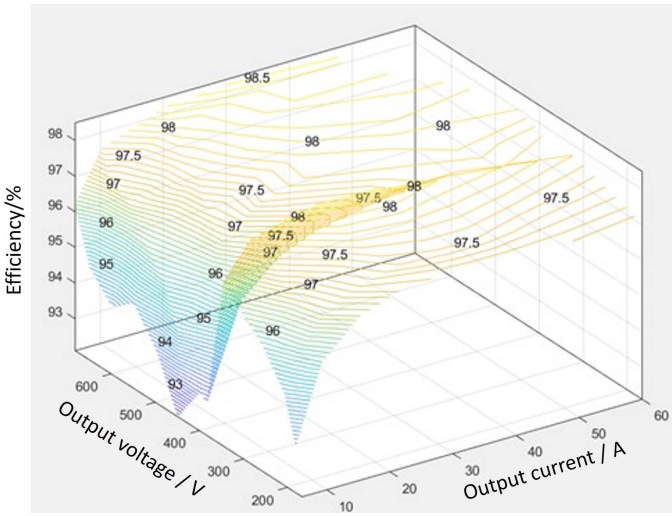

Fig. 19. Efficiency 3-D map and output boundaries based on experiment results.

The peak efficiency is 98.5% for the dual FB mode and 98.2% for the dual HB mode. The efficiency remains around 97% for output current higher than 30% of the rated output current. Besides, the highest and the lowest output voltage boundaries verify the low duty cycle loss of the proposed converter.

The transition between dual HB mode and dual FB mode is realized by topology morphing [6]. For the transition from dual FB (HB) mode to dual HB (FB) mode, when the voltage is below (above) the threshold, the duty cycle linearly decrease (increase) from 50% (0%) to 0% (50%), the switching frequency linearly decrease (increase) from 140 kHz (70 kHz) to 70 kHz (140 kHz). The phase-shift between the leading and lagging legs is used to regulate to the output voltage. Fig. 20 shows the transition from dual HB mode to the dual FB modes. The output inductor current targets at constant 14 A, and the load resistance steps from 16Ω to 35 Ω at t_0. As a result, the output voltage steps from 220 V at dual HB mode to 490 V at dual FB mode. The transition between t_1 and t_2 is finished within 20 ms.

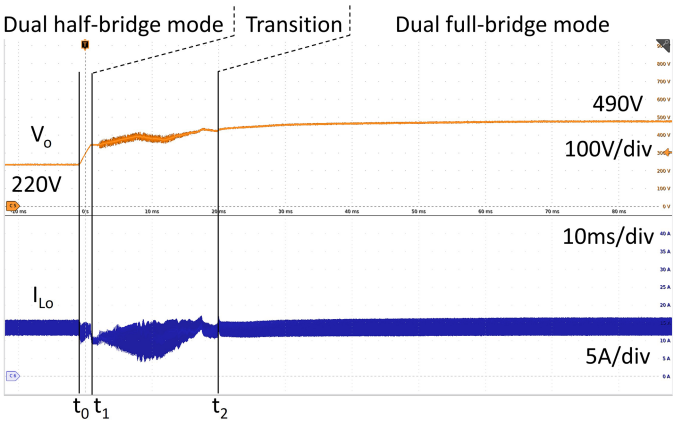

Fig. 20. Load step transition from dual HB mode at 220 V to dual FB mode at 490 V.

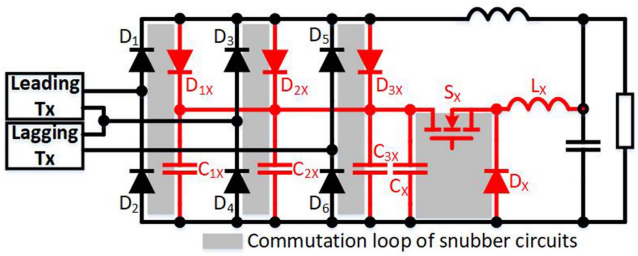

Fig. 21. Active snubber circuits with minimized commutation loop.

TABLE V
PARAMETERS OF THE SNUBBER CIRCUIT

Parameters	Specifications	Parameters	Specifications
V_{in}	$800V/400V$	S_X	$1.2kV\ 520m\Omega$
f_X	$25kHz$	D_X	$1.2kV\ 10A$
D_{1X-3X}	$1.2kV\ 2A$	C_{1X-3X}	0.1μF
C_X	$1.2kV\ 1.1\mu F$	L_X	$610\mu H$

All power diodes at the secondary side share an active snubber circuit to recycle the energy in the simplest way, as shown in the red part in Fig. 21. It is a buck circuit with a regulated input voltage. The switching frequency is much lower than the main switches. Each diode half-bridge has a small ceramic snubber capacitor (0.1 μF) and a small clamping diode (Only 2 A) with minimal commutation loops to minimize the voltage spikes across the diodes, as shown in Fig. 21. The input voltage is regulated at around 20% higher than the rectified voltage amplitude in the ideal case. They are 800 V at dual full-bridge mode and 400 V at dual half-bridge mode. All the parameters of the snubber circuit are summarized in Table V. The volume of the active snubber circuit is only 3% of the 30 kW prototype. No design procedure is provided as it is beyond the scope of this article.

The voltage across diodes D_2, D_4, and D_6 are shown in Fig. 22. The highest voltage spikes of D_2 and D_6 are 800 V, same as design. The ringing frequency when two H-bridges are connected in parallel is around twice the ringing frequency when two H-bridges are connected in series due to the different

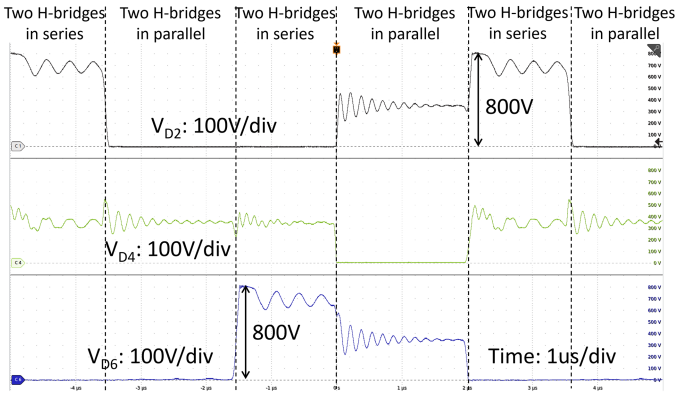

Fig. 22. Diode voltage waveforms with peak voltage clamped by active snubber.

equivalent resonant inductances (L_1 and L_2 in parallel versus L_1 and L_2 in series).

V. CONCLUSION

This article presents an isolated dc–dc converter with a 4:1 output voltage range and full-range ZVS from no-load to full-load utilizing independent magnetizing currents. The key features are summarized below: 1) an isolated H8 dc–dc topology with a 3-level modulation scheme integrates the dual full-bridge and dual half-bridge mode by one control variable and achieves phase, duty cycle, and frequency control all together; 2) the two operation modes are unified and modeled as a simple voltage-controlled voltage source, and the control parameters are the same for the two operation modes; 3) low circulating magnetizing current and integrated transformers with small leakage inductors improve the power density and the overall efficiency significantly; 4) A 30 kW prototype with 7.2 kW/L power density (cooling inclusive), 165–680 V output voltage range verifies the features and feasibility of the proposed topology and modulation scheme.

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