High Efficiency and High Power Density Partial Power Regulation Topology With Wide Input Range

Zongheng Wu, Zhiwei Wang, Teng Liu, Wenzhe Xu, Cai Chen, and Yong Kang

***Abstract*—Data centers require high efficiency and high power-density dc–dc converter with wide input range and galvanic isolation. To overcome the drawbacks of traditional single-stage *LLC* and two-stage solutions, a novel partial power regulation topology with wide input range is proposed in this article. The proposed topology delivers the load power through a three-ports *LLC*-based dc transformer regulated DCX (DCX). A pulsewidth modulation (PWM) converter is cascaded with one of the input ports of the DCX and then in series with the other input port to regulate the output voltage. Since a single transformer and a partial power PWM converter are employed, high power density can be achieved. Furthermore, only a portion of the load power is transferred by the PWM converter, the efficiency sacrifice is reduced. By introducing an appropriate negative current, the zero voltage switching of the PWM is also achieved. Furthermore, when the input voltage approaches the lower or the upper limit, the switching frequency of the PWM regulator can be ultralow. As a result, switching losses and core losses are further reduced. Finally, a prototype with 190—475 V input and 12 V/500 W output is demonstrated, which achieves a peak efficiency of up to 97.2% and a power density of 153 W/in^3.**

***Index Terms*—Dc transformer (DCX), high efficiency, high power density, partial power regulation, wide input range.**

I. Introduction

INFORMATION technology is booming in recent decades. The ever-increasing demand for large-scale information storage and computation pushing the size of data centers increases dramatically. And this results in huge energy consumption and electricity cost [1]. It is been reported that Google and Microsoft consume more than 1120 GWh and 600 GWh annually, having to pay 67 million dollars and 36 million dollars, respectively [2]. The electricity consumption of data centers is about 1% of all electricity consumed in the world [3]. The emission of a large amount of carbon dioxide due to the burning of fossil fuels for electricity causes environmental issues. Hence, it is significant to improve the energy utilization efficiency of the data center.

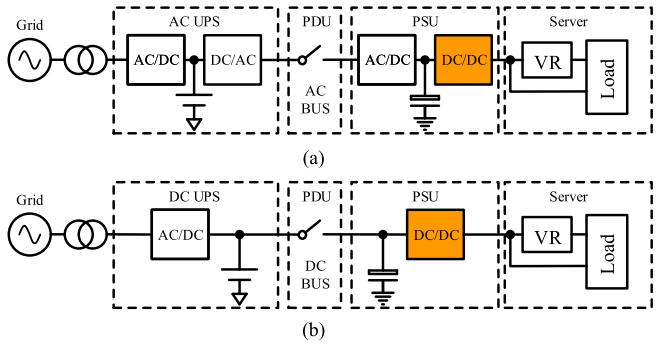

Fig. 1 Power distribution structure of data center. (a) Ac bus. (b) High voltage dc bus.

The two mainstream power distribution architectures of data centers are shown in Fig. 1. Fig. 1(a) shows the ac bus power distribution structure. An ac uninterrupted power supply (UPS) is powered by the grid and the output port of the UPS is connected with all the rank power supplies by the ac power distribution unit (PDU). The rank power supply consists of a power factor correction (PFC) stage and an isolated dc–dc stage. The PFC stage converts the ac bus to a high voltage dc bus and the cascaded dc–dc converter steps the dc bus down to 12 V [4]. To suppress the double-line-frequency voltage ripple caused by the PFC stage and to meet the requirement of the hold-up time, the wide input range capability of the dc–dc is needed. To improve the total efficiency, the high voltage dc bus structure is used to replace the ac bus system [4]. In dc bus system, as shown in Fig. 1(b), the grid is connected to the energy storage unit with a PFC converter. The high voltage dc bus is connected to the rank power supply by the dc PDU. The dc–dc converter in the rank steps the high voltage down to 12 V. Here, a dc transformer regulated DCX (DCX) can be employed to achieve high-efficiency isolation and a high step-down ratio [4], [5]. However, once the grid is disconnected, the voltage of the energy storage battery is floating within a wide range due to the discharging. The output voltage of the DCX will not maintains a constant value anymore. Hence, whichever the power distribution system is, a high efficiency isolated dc–dc converter with a wide input range is needed.

On the other hand, high frequency and high power density are also the tendencies. However, traditional hard switching pulse

Manuscript received 26 March 2022; revised 7 June 2022 and 3 August 2022; accepted 8 September 2022. Date of publication 19 September 2022; date of current version 18 November 2022. This work was supported in part by the National Natural Science Foundation of China under Grant 52077094. Recommended for publication by Associate Editor L. Corradini. *(Corresponding author: Cai Chen.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3207526.

Digital Object Identifier 10.1109/TPEL.2022.3207526

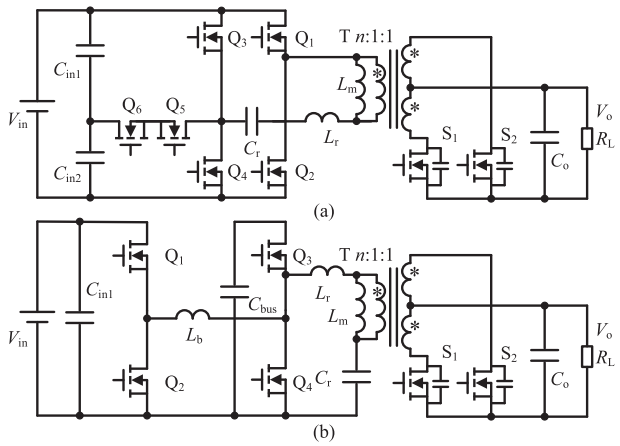

Fig. 2. (a) Circuit structure of dual-bridge *LLC*. (b) Circuit structure of BB*LLC*.

width modulation converter cannot provide high efficiency due to the large switching loss [6], [7]. The pulsewidth modulation (PWM) zero voltage switching (ZVS) topologies such as phase-shift full-bridge converter and dual-active-bridge converter is also hard to obtain high efficiency due to the large turn-OFF current of primary-side switches, nonzero current switching (ZCS) of rectifiers, and large circulating current [8], [9], [10], [11], [12], [13].

Among all kinds of ZVS converters, *LLC* converter, which provides ZVS switching at the primary side and zero current switching (ZCS) at the rectifiers, is broadly adopted in applications that need both electrical isolation and high efficiency [14], [15], [16]. However, the *LLC* converter regulated the output by adjusting the phase-shifting angle, switching frequency, or duty cycle. A large resonant inductor is needed for output regulation and it not only occupies large volume but also induces large loss. On the other hand, it is difficult to get available control strategies for a high frequency regulated *LLC* converter with phase-shifting modulation or frequency modulation [17], [18], [19]. And the synchronous rectifier logic is also difficult to implement [20], [21], [22], [23], [24]. It is worse for an *LLC* with a wide input range.

To extend the gain range of the *LLC* converter, different methods are previously proposed. A dual-bridge *LLC* resonant converter with fixed-frequency PWM control is proposed in [25], as shown in Fig. 2(a). In this converter, Q_1 and Q_2 operate with a 50% duty cycle. Q_3 and Q_4 have an identical duty cycle with a 180° phase shift angle. Q_3 and Q_5, and Q_4 and Q_6, are, respectively, turned ON alternatively. Once the duty cycle of Q3 varies from 0% to 50%, the circuit changes from a half bridge to a full bridge. However, as the output voltage is regulated by adjusting the duty cycle, there is still difficulty in the implementation of synchronous rectifier logic under high switching.

LLC converter provides optimal performance at the series resonant frequency. The ZVS turn ON, low current turn OFF of primary devices, and ZCS turn OFF of rectifiers can be obtained, which are helpful to obtain the high efficiency and high power density. And the synchronous rectifier logic is also simplified [4], [5], [14]. However, auxiliary circuit is needed for output regulation due to the fixed voltage ratio of the DCX. The conventional solution employs a cascaded nonisolated PWM regulator for output regulation suffers from high switching loss due to the PWM converter bears full input or output voltage and current [26], [27]. Liu et al. [28] proposed a buck–boost integrated *LLC* converter, as shown in Fig. 2(b). In this topology, a four-switch noninverting buck–boost converter is merged with the *LLC* resonant converter. The *LLC* stage works as a DCX and the output voltage is regulated by adjusting the duty cycle of the buck–boost bridge. Meanwhile, by adjusting the phase-shift angle between the buck–boost bridge and the *LLC* bridge, the ZVS turn ON of the buck–boost bridge can be also obtained. However, the full load regulator occupies a large volume, which decreases the power density.

In [29] and [32], a sigma converter is proposed and demonstrated. In this topology, a high efficiency unregulated DCX is used to deliver most of the load power to achieve high step-down ratio. And a buck converter is adopted to regulate the output voltage. The sigma converter can achieve both high efficiency and high power density. However, the sigma converter cannot provide galvanic isolation. In [30], a partial power regulation RDC is proposed. In this topology, DCX with two transformers is adopted and only a small part of the load power is transferred to the load by the two-stage structure. Hence, the efficiency sacrifice is minimized. However, both two transformers in this topology need a large power rating when applied to wide input range applications. It will suffer from worse efficiency and power density. A partial-power preregulated dc transformer (P^3DCT) is proposed in [31], as shown in Fig. 3(c). The full bridge FB_1, FB_3, and the half bridge HB_1 are working at the same frequency with the duty cycle of 50%. FB_1 and FB_3 operate synchronously. The switching frequency of FB_3 is several times of the switching frequency of FB_1 and the output voltage of FB_3, a high frequency square waveform, is directly superposed on the dc input to power FB_1. By adjusting the duty cycle of FB_3 and the phase-shift angle between FB_1 and HB_1, the output voltage can be regulated. However, since the high frequency square waveform is directly superposed on the

Dc input, large volume *LC* filter is needed at the output port and FB_3 is working with hard switching. Hence, it is not suitable for wide input range applications.

In this article, a novel partial power regulation topology is proposed. A single transformer with a tertiary winding is adopted to form a DCX with two input ports and one output port. A PWM converter is cascaded with one of the input ports and in series with the other input port. The output voltage is regulated by the PWM converter. The triangular current mode (TCM) operation is implemented in the PWM regulator. Since the PWM regulator only bears part of the bus voltage and the ZVS turn ON of TCM operation, the efficiency sacrifice caused by the PWM regulator is minimized.

The rest of this article is organized as follows. Section II introduces the circuit structure of the proposed partial power regulation topology and its operating principle. The ZVS operation is also analyzed to further improve efficiency. In Section III, the design guidelines are given to obtain an optimal efficiency.

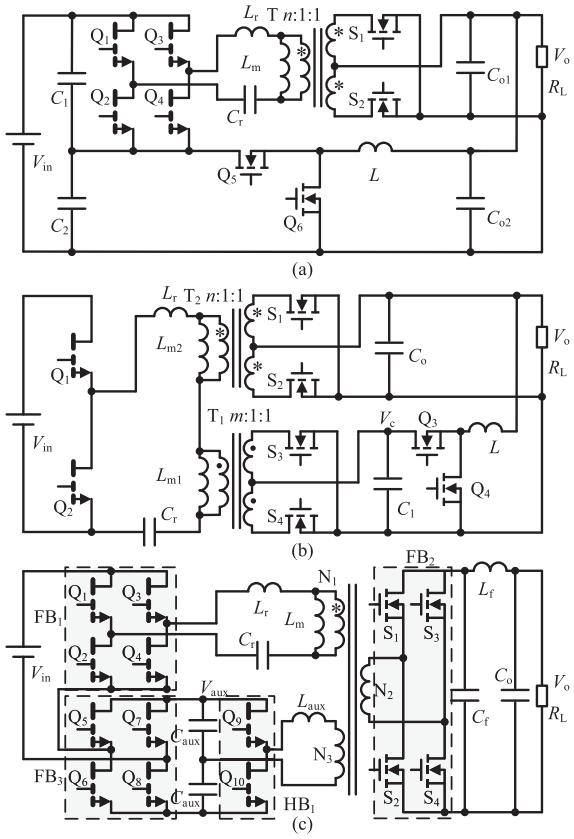

Fig. 3. (a) Sigma converter [29]. (b) Regulated DCX structure [30]. (c) P^{3}DCT converter [31].

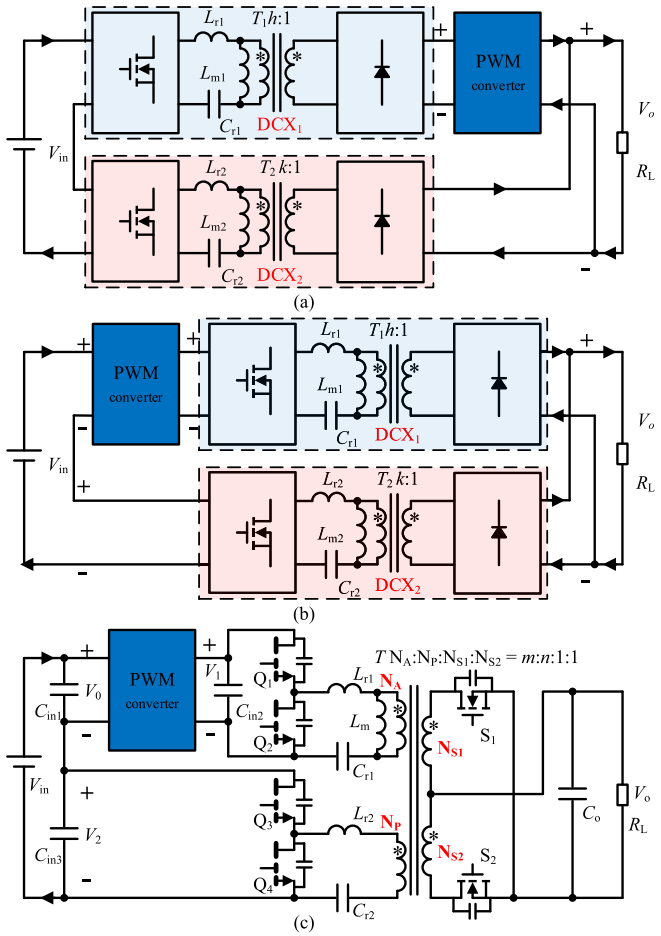

Fig. 4. Circuit schematic of ISOP structure. (a) Type I. (b) Type II. (c) Simplified circuit structure of the proposed topology.

Section IV gives the experimental results to verify the theoretical analysis and comparisons with others solutions to show the exact benefit of the proposed converter. Finally, Section V concludes this article.

II. Circuit Configuration and Operating Principle

A. Circuit Configuration of Proposed Topology

As mentioned previously, the *LLC* converter provides optimal performance due to the ZVS and ZCS switching and simplified synchronous rectifier logic at the series resonant frequency, but it provides a fixed voltage ratio. Considering the concept of the sigma converter in [33], a dual-channel converter system based on DCX with input-series and output-parallel (ISOP) connected is presented. In this converter system, the main channel is a DCX and the auxiliary channel is a two-stage structure consist of a DCX and a PWM converter. Since only part of the load power is delivered to the load by the two-stage structure, the power loss induced by the PWM converter is reduced compared to the conventional two-stage structures and the regulation function is also achieved. This converter system has two circuit structures, as shown in Fig. 4(a) and (b). Fig. 4(a) shows the circuit structure in which the PWM converter is cascaded with the auxiliary DCX at the secondary side. Because the two DCXs are in series at the input port, the primary side switches and resonant tanks can be merged into one bridge and one resonant tank. Using two transformers with center-tapped secondary windings and adopting two synchronous rectifiers, the circuit topology of [30] can be obtained, as shown in Fig. 3(b). This topology is suitable for DCX with a narrow input range and output regulation. Once this topology is applied to wide input range applications, T_2 and its rectifier deliver nearly the whole load power under minimum input voltage, and T_1 and its rectifier deliver most of the load power under the maximum input voltage. Since the two transformers are connected in series, it is hard to integrate these two transformers into one. Hence, both the two transformers need a large power rating, and both the synchronous rectifiers require a high current rating. Furthermore, the primary side switches bear high current stress under low input voltage and high voltage stress under high input voltage as the input voltage has a wide range. All of these increase the cost and limit the improvement of power density.

The circuit topology proposed in this paper is based on the circuit structure shown in Fig. 4(b). In this structure, the PWM converter of the auxiliary is cascaded with the DCX at the primary side. The two DCXs are connected in parallel at the output port. Setting the two resonant frequencies the same, the rectifiers of two DCX can be merged into one. And then, the secondary windings of the two transformers are connected in

parallel. Hence, the two transformers can be integrated into one transformer. The circuit configuration of the proposed topology is shown in Fig. 4(c). The transformer of the DCX has three windings. N_P and N_A are the primary windings and $N_{S1\&S2}$ is the center tapped secondary winding. And the input voltage V_{in} is split into two V_0 and V_2. V_2 is applied to a half-bridge and then applied to winding N_P through a resonant tank. V_0 is applied to the input port of a nonisolated PWM converter. The output voltage of the nonisolated PWM converter (V_1) is applied to the other half-bridge and then applied to winding N_A through a resonant tank. The tertiary winding is a center-tapped winding for high current output and the synchronous rectifier is also adopted to reduce the conduction loss. In the proposed topology, the output voltage is regulated by the nonisolated PWM converter and the *LLC*-based DCX is only for isolation and step down. Hence, the synchronous logic is simplified and it is suitable for wide input range applications. Furthermore, the partial power regulation structure helps reduce the power loss and the single transformer helps improve the power density.

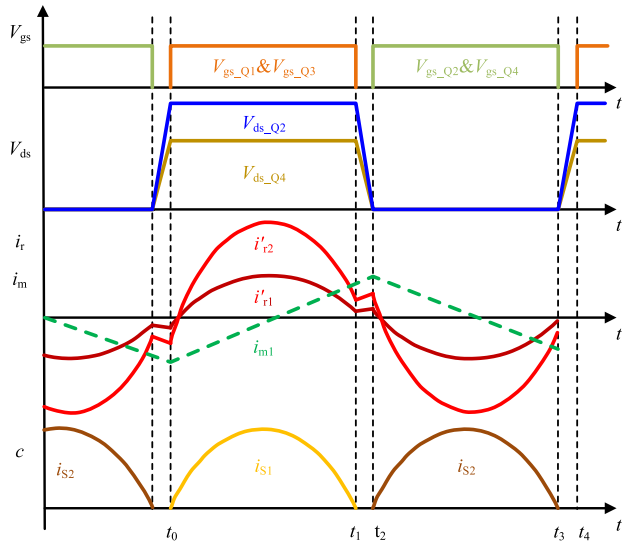

Fig. 5. Key waveforms of the three-ports DCX.

B. Brief Operating Principle

To give a simplified analysis of the main circuit the operating principle of the three-ports DCX is given first. Assumptions are made here for the next step's analysis. In the proposed topology, the resonant frequencies of the two resonant tanks are the same and both equal to the switching frequency. The losses of the windings and core of the transformer are neglected here. Furthermore, all the inductors and capacitors are regarded as ideal components. The ON-state resistance of the primary switches and rectifier devices is ignored. The output capacitor of the switches presented here is for ZVS analysis. And the synchronous rectifiers are treated as ideal diodes. Because a three-port transformer is used in the proposed topology, the equivalent magnetizing inductor is present at the N_A port for the sake of simplicity.

According to the first harmonic approximation analysis, the resonant tanks provide unity gain as the proposed converter operates at the series resonant frequency. Hence, it can be easily obtained that the dc voltage of the three ports of the DCX is in proportion to its turns under steady-state operation. Hence, the voltage at the dc port of the DCX is determined by the turn ratio of the transformer. Moreover, a half-bridge has a voltage gain of 0.5. As depicted in Fig. 4(c), the transformer has three windings N_A, N_P, and $N_{S1\&S2}$. The turns ratio of the windings is m: n: 1. The input voltage V_{in} is split into V_0 and V_2. V_2 refers to the input voltage of the half-bridge connected to N_P and V_0 is the input voltage of the PWM converter. V_1 is the output voltage of the PWM converter and also the input voltage of the bridge leg connected to N_A. V_o is the output voltage of the proposed converter. The output voltage is adjusted by the duty cycle of the PWM converter. The voltage gain of the PWM converter is defined as

$$f(d) = \frac{V_1}{V_0}. \tag{1}$$

According to the turns ratio of the transformer, the following relations are obtained:

$$\begin{cases} V_1 = 2m \cdot V_o \\ V_2 = 2n \cdot V_o. \end{cases} \tag{2}$$

Combining (1) and (2) and replacing the sum of V_0 and V_1 with V_{in}, the steady-state voltage gain can be obtained

$$G(d) = \frac{V_o}{V_{in}} = \frac{f(d)}{f(d) \cdot 2n + 2m}. \tag{3}$$

Once m and n are selected, the output voltage is determined by $f(d)$. Hence, the output voltage can be regulated at a fixed value with an appropriate control loop.

The main waveforms under steady-state operation of the proposed topology are given in Fig. 5. And one switches period can be split into 4 intervals. The equivalent circuits of each interval are depicted in Fig. 6.

Stage I (t_0-t_1): The equivalent circuit of this stage is shown in Fig. 6(a). The primary side switches Q_1, Q_3 and the synchronous rectifier device S_1 turns ON at t_0 moment. The transformer is clamped by the equivalent output voltage $m \cdot V_o$. Hence, the magnetizing current increase linearly. The dc voltage V_1 and V_2 are applied to the two resonant tanks, respectively. Under steady-state, there is half of V_1 and V_2 dc bias on the two resonant capacitors, respectively. Then, the sinusoidal current of the two resonant tanks deviate from the magnetizing current, and energy is transferred to the load by Q_1, Q_3, and S_1. The amplitudes of the two resonant currents are determined by the power ratio, which is adjusted by the PWM converter.

Stage II (t_1-t_2): As the switching frequency equals the series resonant frequency of the resonant tank, the sum of i_{r1} and $i_{r2} \cdot n/m$ meet the magnetizing current at t_1 moment. The equivalent circuit of this stage is illustrated in Fig. 6(b). Q_1 and Q_3 turn OFF at t_1 moment. Meanwhile, the current flows through S_1 equals zero and S_1 ZCS turns OFF simultaneously. After t_1 moment, all the switches keep OFF-state until t_2. There is no energy is delivered from input to load and the load is powered

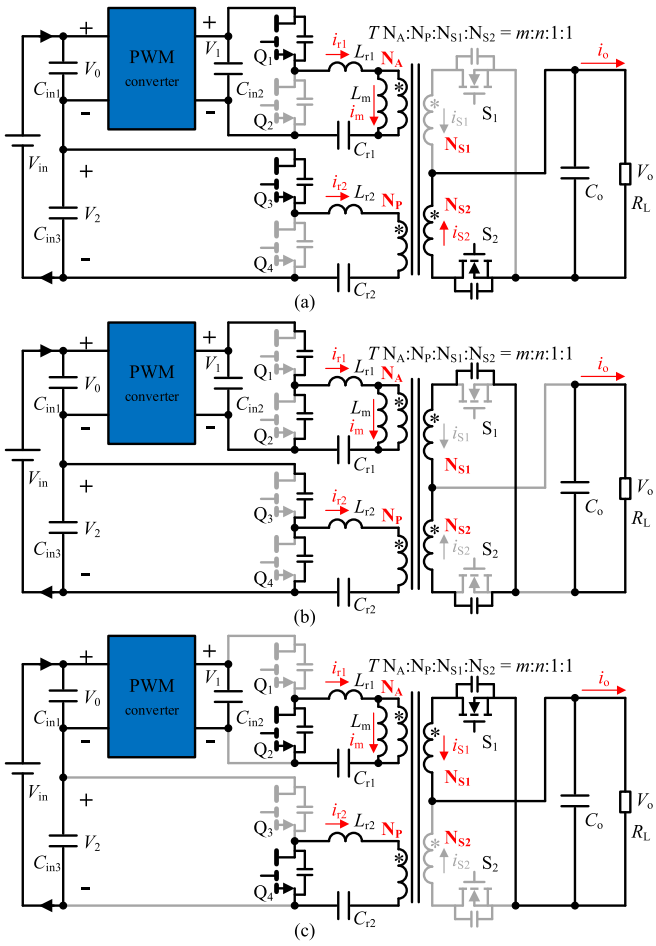

Fig. 6. Equivalent circuits of the three-ports DCX. (a) Stage I (t_0-t_1). (b) Stage II (t_1-t_2) and stage IV (t_3-t_4). (c) Stage III (t_2-t_3).

by the output capacitor during this interval. Since all the switches are turned OFF, the magnetizing inductor will not be clamped by the output voltage and then it joins the resonance. The output capacitors of Q_1, Q_3, and S_1 are charged by the magnetizing current, and the output capacitor of Q_2, Q_4, and S_2 are discharged by the magnetizing current. Until t_2 moment, the drain to source voltage of Q_2, Q_4, and S_2 are discharged to zero, Q_2, Q_4, and S_2 achieve ZVS turn ON. Then, the converter starts the next step operation.

Stage III (t_2-t_3): At t_2 moment, Q_2, Q_4, and S_2 turn ON. The bias voltage on the resonant capacitor is applied to the corresponding resonant tank. The equivalent circuit of this stage is depicted in Fig. 6(c). The magnetizing inductor is clamped by reflecting voltage to $-m \cdot V_o$ and the magnetizing current increases with a negative slope. The resonant current deviating from the magnetizing current according to a sinusoidal function and the energy is delivered to the load. Until t_3 moment, the sum of i_{r1} and $i_{r2} \cdot n/m$ meet the magnetizing current again and Q_2 and Q_4 turn OFF at the same time. Once the primary side current meets the magnetizing current, the current flows through S_2 equals zero and S_2 achieves ZCS turn OFF simultaneously.

Stage IV (t_3-t_4): After t_3 moment, all the switches are turned OFF. The equivalent circuit of this stage is similar to stage II, as shown in Fig. 6(b). Since all the switches are turned OFF, the magnetizing inductor participates in the resonance and the parasitic capacitors of Q_1, Q_3, and S_1 are discharged by the magnetizing current. Until t_4 moment, the drain to source voltage of Q_1, Q_3, and S_1 reaches zero, and then Q_1, Q_3, and S_1 obtains ZVS turn ON at the same time.

C. TCM Modulation and ZVS Operation of the PWM Converter

In the proposed converter, a PWM converter is employed for output regulation. For wide input range applications, the switching loss of the PWM converter tremendously reduces the efficiency. Generally, a complex circuit structure generates larger power loss compared to a simple circuit structure. Hence, a half-bridge buck or boost is a suitable candidate. Despite the selection of buck or boost remaining to be discussed, the operating principle of the half-bridge buck or boost is similar excluding the current flowing direction. Hence, the ZVS analysis and modulation of the TCM boost are given here.

The equivalent circuit of a half-bridge is given in Fig. 7(a). V_L is the voltage at the lower voltage port and V_H refers to the voltage at the higher voltage port. In continuous conduction mode, the upper switch can achieve natural ZVS with appropriate dead time. However, the lower switch can not achieve ZVS due to a positive inductor current. In critical conduction mode boost, the lower switch can achieve ZVS turn ON when the input voltage is less than half the output voltage. However, when the input voltage high than half the output voltage, there is no efficient energy in the inductor to discharged the node voltage to zero. To achieve ZVS turn ON, an appropriate negative current is needed. The TCM is proposed in [34] to provide enough negative current to achieve ZVS of the lower switch. The upper switch keeps turn ON at the zero crossing of the inductor current. The typical input current and switching node voltage waveforms for $V_L > V_H/2$ are shown in Fig. 7(b). A full switching period can be divided into five intervals.

Interval I (t_0-t_1): Q_L turns ON at t_0 moment and V_L is applied to the inductor, the current increases linearly. Once a given T_{on} or a given I_s is reached at t_1, Q_L turns OFF.

Interval II (t_1-t_2): As Q_H and Q_L are both in OFF-state, a resonance takes place between L and the output capacitors of the two switches. C_{oss_L} is charged by the inductor current and C_{oss_H} is discharged by the inductor current. Once the voltage across C_{oss_H} is discharged to zero at t_2, Q_H turns ON immediately and ZVS turn ON is achieved.

Interval III (t_2-t_3): Q_H turns ON at t_2 moment and the voltage difference between V_H and V_L is applied to the inductor, the inductor current decreases linearly and reaches zero at t_3. In traditional critical continuous mode, Q_H turns OFF at t_3 and then the resonance takes place. However, the voltage across C_{oss_L} can not reach zero when V_L is higher than half of V_H and the ZVS switching is lost.

Interval IV (t_3-t_4): To overcome the drawback of losing ZVS when V_L is higher than half of V_H, Q_H keeps ON-state after zero crossing of i_L. Until t_4 moment, a given reverse current or T_R is reached, Q_H turns OFF.

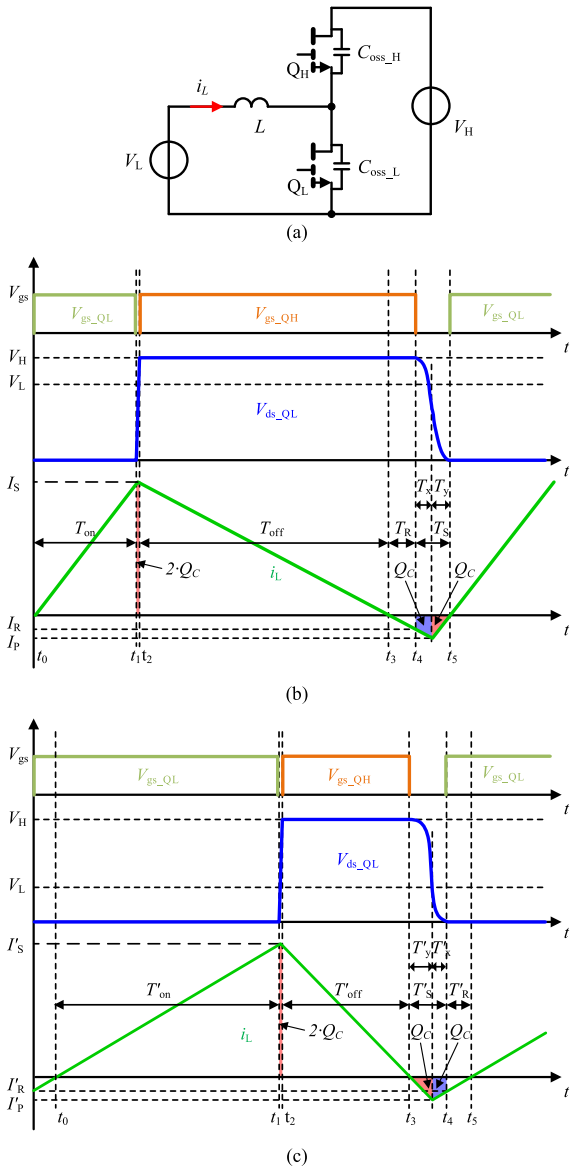

Fig. 7. (a) Equivalent circuits of boost. Key waveforms of TCM boost. (b) $V_L > V_H/2$. (c) $V_L < V_H/2$.

Interval V (t_4-t_5): Since Q_L is turned OFF at t_3, the resonance between L and C_{oss} takes place. The output capacitors are charged or discharged by the negative inductor current. Since an additional reverse current is added, the voltage across C_{oss_L} can decrease to zero at t_5. Then, Q_L turns on simultaneously, the ZVS switching of Q_L can be obtained.

During interval II and interval V, the output capacitors participate in the resonance. However, the output capacitor is nonlinear. It is hard to get an accurate current waveform for converter design. In [34], a simple and accurate model that allows for closed-form solutions of the inductor current is proposed. Considering interval II and interval V, the output capacitor of the switches is fully charged or discharged during dead time. And then, the ZVS turn ON can be obtained. The proposed model in [34] can be expressed as

$$\begin{cases} Q_C = \int_0^{V_{out}} C_{oss}(v_C)\, dv_C \\ v_C(q_C) = \begin{cases} V_H & q_C \geq Q_C \\ 0 & \text{else} \end{cases} \end{cases}. \tag{4}$$

Here, Q_C is the charge that has to be removed from one switch to achieve ZVS. Therefore, once the time integral of the current during interval II and interval V exceeds $2Q_C$ ZVS can be achieved. q_C is the charge in the capacitance $C_{oss\_H} \| C_{oss\_L}$. With this model, a triangular-shaped current and an analytical expression can be obtained [34].

Hence, the peak negative current I_P, as shown in Fig. 7(b), can be calculated with

$$\begin{cases} Q_C = -\frac{I_P T_y}{2} \\ V_L = -L\frac{I_P}{T_y}. \end{cases} \tag{5}$$

And, it can be expressed as

$$I_P = -\sqrt{\frac{2Q_C V_L}{L}}. \tag{6}$$

The required negative current I_R can also be calculated with the same method

$$I_R = -\sqrt{\frac{2Q_C(2V_L - V_H)}{L}}. \tag{7}$$

C. The average input current can be expressed as

$$I_{av} = \frac{1}{T_P}\left(\frac{I_S T_{on}}{2} + \frac{I_S T_{off}}{2} + \frac{I_R T_R}{2}\right). \tag{8}$$

Due to the large inductor current during interval II, the switching transition is very fast and interval II can be neglected. The switching period T_P can be expressed as

$$T_P = T_{on} + T_{off} + T_R + T_S. \tag{9}$$

And each interval can be calculated with

$$\begin{cases} T_{on} = \frac{I_S L}{V_L} \\ T_{off} = \frac{I_S L}{V_H - V_L} \\ T_R = -\frac{I_R L}{V_H - V_L} \\ T_S = -\frac{(I_P - I_R)L}{V_H - V_L} - \frac{I_P L}{V_L}. \end{cases} \tag{10}$$

Combining (6)–(11), the ON-time T_{ON} and period T_P can be obtained

$$\begin{cases} T_{on} = \frac{LI_{av}}{V_L} + \sqrt{\frac{L}{V_L^2}(A + B + C + D)} \\ T_P = \frac{V_H}{V_H - V_L}\left(T_{on} + \frac{B}{2V_L I_{av}}\right). \end{cases} \tag{11}$$

Here, A, B, C, and D are

$$\begin{cases} A = LI_{av}^2 \\ B = 2I_{av}\sqrt{2Q_C V_L L} \\ C = \frac{4Q_C V_L^2}{V_H} \\ D = -2Q_C V_L. \end{cases} \tag{12}$$

Once $V_{\rm L}$, $V_{\rm H}$, and $I_{\rm av}$ are confirmed, the switching period $T_{\rm P}$ and the ON-time $T_{\rm ON}$ and the needed dead time $T_{\rm s}$ for ZVS can be obtained.

When $V_{\rm L}<V_{\rm H}/2$, the ZVS turn ON of the lower switch can be obtained without any additional reverse conduction-time of the upper switch. A body diode commutation time $T_{\rm R}$ appears due to the total discharge of the capacitor of the switch node, as shown in Fig. 7(c). To reduce the conduction loss of the body diode, the lower switch can turn ON with ZVS when the node voltage reaches zero. With the previous calculation approach, each time duration for VL$>V_{\rm H}/2$ can be obtained as (14) and (15)

$$\begin{cases} I'_P = -\sqrt{\frac{2Q_C(V_H-V_L)}{L}} \\ I'_R = -\sqrt{\frac{2Q_C(2V_L-V_H)}{L}} \end{cases} \tag{13}$$

$$\begin{cases} T'_R = -\frac{I'_R L}{V_L} \\ T'_S = -\frac{(I'_P-I'_R)L}{V_L} - \frac{I'_P L}{V_H-V} \end{cases} \tag{14}$$

$$\begin{cases} T'_{\rm on} = \frac{LI_{av}}{V_L} + \sqrt{\frac{L}{V_L^2}(A'+B'+C'+D')} \\ T'_P = \frac{1}{f'_s} = \frac{V_H}{V_H-V_L}\left(T'_{\rm on} + \frac{B'}{2V_L I_{av}}\right). \end{cases} \tag{15}$$

Here, A', B', C', and D' are

$$\begin{cases} A' = LI_{av}^2 \\ B' = 2I_{av}\sqrt{2Q_C(V_H-V_L)L} \\ C' = -\frac{4Q_C V_L(V_H-V_L)}{V_H} \\ D' = 2Q_C(V_H-V_L). \end{cases} \tag{16}$$

Hereto, the boundary switching period for ZVS is obtained. Once the switching period larger than the calculated value, the ZVS can be achieved.

III. Design Considerations

A. Selection of the PWM Converter

In the proposed converter, a nonisolated PWM converter is employed for output regulation. Usually, a complex structure brings low efficiency and low power density. Hence, the buck converter and boost converter are suitable candidates. Since the characteristics of the PWM converter affect the performance of the whole converter, the selection of the PWM converter needs to be discussed. As mentioned previously, the TCM modulation strategy is adopted to achieve ZVS turn ON. And several aspects have to be taken into consideration when selecting the PWM converter.

On the one hand, the proposed converter employs different types of PWM converters, which has different port voltages and different average inductor currents under the same input and output conditions. With the TCM modulation strategy, the selection of the PWM converter will affect the switching frequency. According to the analysis in Section II, once the input voltage, output voltage, output power $Q_{\rm C}$, and inductance are given, the peak inductor current and switching frequency can be obtained. The parameters of the proposed converter with both buck and boost under the same input range and power rating are listed in Table I. To have a fair comparison, the maximum stored energy for each inductor is identical. Hence, with appropriate design, the two inductors usually have a similar volume and similar maximum flux density. Substituting the parameters given in Table I into (11) and (15), the switching frequency can be obtained. The calculated frequency versus input voltage for the proposed topology with both buck and boost are illustrated in Fig. 8(a). It can be observed from Fig. 8(a) that the switching frequency increases with the input voltage increase when employing the buck converter as the regulator and the highest frequency is reached at the maximum input voltage. What is worse is that the power delivered by the buck increases with the input voltage increases. And the peak-to-peak inductor current also increases with the input voltage increases, as depicted in Fig. 8(b). It means that a higher inductor core loss will appear at a higher input voltage. However, when a boost is employed as the regulator, the switching frequency present earlier increase and later decrease trend with the input voltage increases, and an extremely low switching frequency is obtained at the upper input limit. Furthermore, the peak-to-peak inductor current also decreases with the input voltage increase. For the whole input voltage range, the boost inductor benefit from lower switching and lower peak-to-peak current especially at the upper input limit.

TABLE I
Circuit Parameters

Parameters		With Boost	With Buck
Input Voltage/V_{in}		200–400 V	200–400 V
Output voltage/V_o		12 V	12 V
Output power/P_o		500 W	500 W
Q_C		64 nC	64 nC
Turns ratio	m	9:1	4:1
	n	8:1	4:1
V_0		8–208 V	104–304 V
V_1		216 V	96 V
V_2		192 V	96 V
Peak current/I_p		5.65 A	8.87 A
Inductance/L		62.73 uH	25.40 uH
$1/2LI_p^2$		1mJ	1 mJ

On the other hand, since the turn-ON switching loss can be eliminated by the TCM modulation strategy, only the turn-OFF switching loss and ON-state conduction loss of the PWM converter's switches need to be concerned. The root-mean-square (rms) current of the inductor that determines the ON-sate conduction loss is depicted in Fig. 8(b). It can be observed that the rms current increases with the input voltage increases in the buck inductor. Conversely, The rms current decreases with the input voltage increases in the boost inductor and it is lower than that of the buck inductor within the whole input range. It means less conduction loss will generate when employing the boost as the regulator. Since the upper switch of the boost and the lower switch of the buck turn OFF with a relatively low current, only the turn-OFF switching loss of the lower switch of the boost and the upper switch of the buck are taken into consideration. And it can be expressed as

$$P_{\rm Loss\_off} = E_{\rm off} f_s = \frac{1}{2} f_s V_{ds} I_d (t_{ru} + t_{fi}). \tag{17}$$

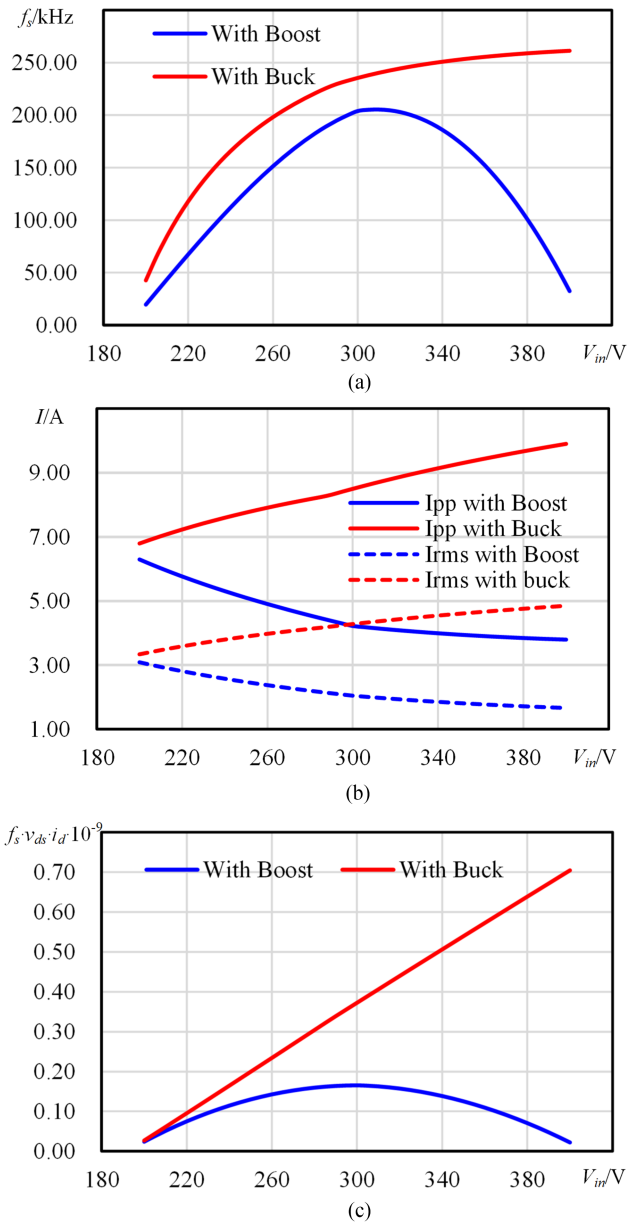

Fig. 8. (a) Switching frequency versus input voltage. (b) Peak-to-peak inductor current and rms current versus input voltage. (c) *V-I-f* product versus input voltage.

The turn-OFF switching loss is proportional to the product of $V_{\rm ds}$, $I_{\rm d}$, and $f_{\rm s}$. According to the analysis abovementioned, this parameter for both boost and buck can be calculated and the results are illustrated in Fig. 8(c). The curves indicate that less turn-OFF switching loss is generated when a boost rather than a buck is adopted as the regulator. And this advantage goes larger when the input voltage increases.

In conclusion, the proposed converter employs boost regulator benefits from lower inductor loss, device conduction loss, and turn-OFF switching loss compared to buck regulator. What is more, the boost regulator provides better performance under the upper input limit voltage. In data center power distribution systems, as illustrated in Fig. 1, the input of the isolated high step-down converter is connected to batteries with floating charge or

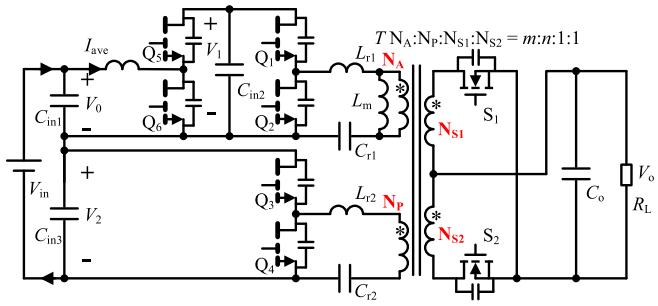

Fig. 9. Final circuit structure of the proposed converter.

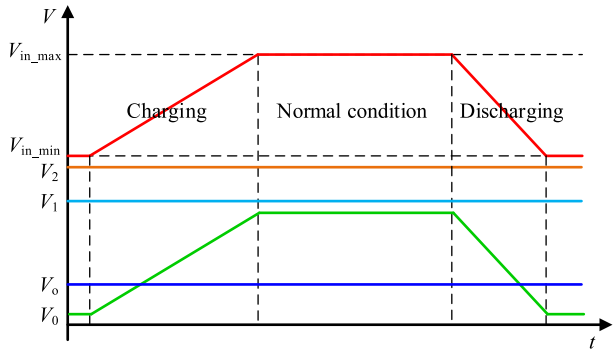

Fig. 10. Illustration of dc port voltage in proposed converter.

the output of a PFC stage. And the nominal input voltage during normal operation is usually near the upper limit of the input range. Hence, the boost regulator is selected in the proposed converter and the final circuit structure is depicted in Fig. 9.

B. Transformer Turns Ratio and Magnetizing Inductor Design

The turns ratio of the transformer affects the input voltage range as well as the efficiency and needs to be designed carefully. As mentioned in Section I, the output voltage of a power supply for the server platform is fixed. For a dc bus power distribution system, the input voltage of the isolated stage comes from the batteries. Under normal operation, the batteries are floating charged by the PFC stage and this condition usually is the highest input of the isolated converter. Once the ac input is interrupted, the system is powered by the batteries and the bus voltage dropped slowly. The input range of the isolated converter has to cover the batteries' voltage floating range. In ac bus power distribution systems, the isolated converter is powered by the PFC stage under normal operation. For the requirement of hold-up time, when the ac bus is disconnected, the isolated converter is powered by the bus capacitor, which is being discharged. The dc port voltage of the proposed converter is depicted in Fig. 10.

The voltage gain of the boost can be expressed as

$$f(d) = \frac{V_1}{V_0} = \frac{1}{1-D}. \tag{18}$$

Here, D is the duty cycle of the lower switch Q_6. Substituting (18) into (3), the total voltage gain of the proposed converter can be obtained

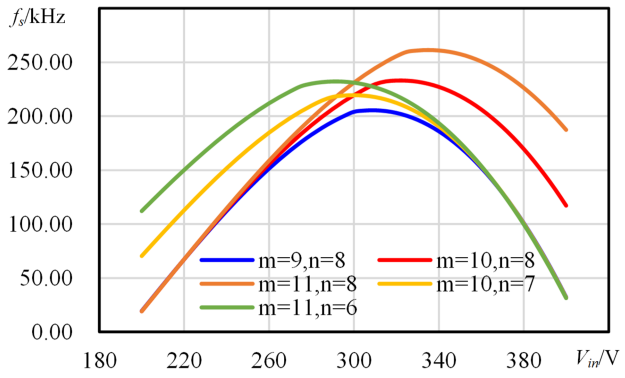

Fig. 11. Switching frequency versus input voltage with different n and m.

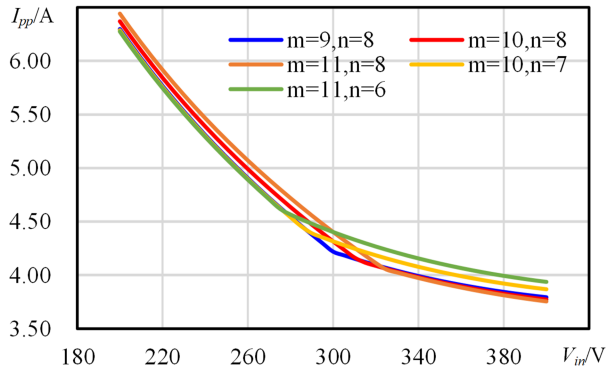

Fig. 12. Peak-to-peak inductor current versus input voltage with different n and m.

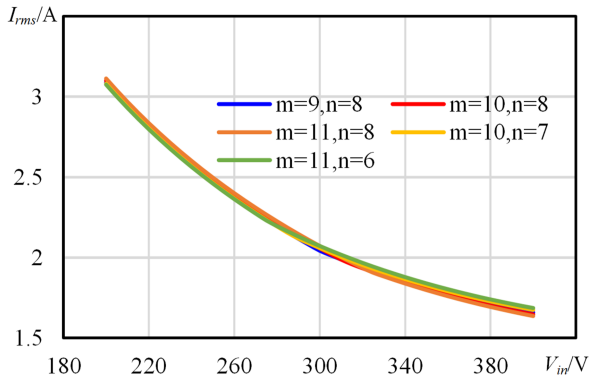

Fig. 13. Rms inductor current versus input voltage with different n and m.

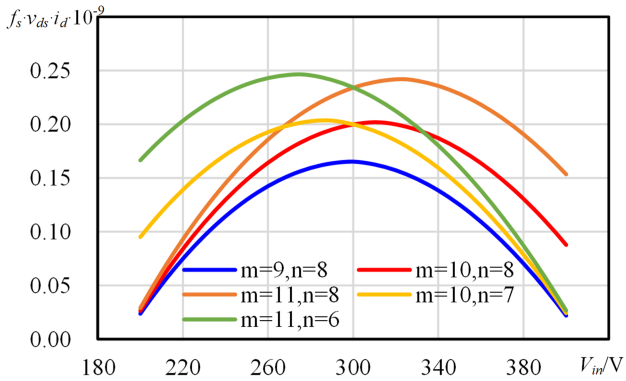

Fig. 14. *V-I-f* product versus input voltage with different n and m.

$$G(d) = \frac{1}{2n + 2m\,(1 - D)}. \tag{19}$$

With an appropriate control loop, the output voltage is tightly regulated. D can be any value between 0 to 1 depends on the needed voltage gain. To meet the maximum input and minimum input requirement, the following equation should be satisfied:

$$\begin{cases} G(d)_{\max} = \frac{1}{2n} \geq \frac{V_o}{V_{in\_\min}} \\ G(d)_{\min} = \frac{1}{2n+2m} \leq \frac{V_o}{V_{in\_\max}}. \end{cases} \tag{20}$$

With the parameters given in Table I, a series of eligible n and m can be obtained. The switching frequency, peak-to-peak inductor current, rms inductor current, and turn-OFF switching loss related factors for each set of n and m can be calculated. Fig. 11 shows the corresponding curves of switching frequency versus input voltage. It can be seen that a smaller n results in a higher switching frequency under low input voltage. And a larger m leads to a higher frequency under high input voltage. Fig. 12 shows the calculated peak-to-peak current under different n and m. It indicates that a smaller n results in a higher peak-to-peak inductor current under high input voltage, and a larger m results in a higher peak-to-peak inductor current under low input voltage. The selection of n and m has little influence on rms inductor current as well as the conduction loss of the switches, as shown in Fig. 13. The cures of turn-OFF switching related factor, the product of $f_{\rm s}$, $V_{\rm ds}$, and $I_{\rm d}$, under different n and m are depicted in Fig. 14. It is obvious that these curves have the same tendency as the switching frequency and both large m and small n result in high turn-OFF switching loss.

According to the analysis abovementioned, the n and m that satisfying (20) should be as large as possible and as small as possible, respectively, to obtain a high efficiency. Introducing the round-down function and round-up function here, the optimal turns ratio can be calculated with

$$\begin{cases} n = \left\lfloor \frac{V_{\text{in\_min}}}{2V_o} \right\rfloor \\ m = \left\lceil \frac{V_{\text{in\_max}}}{2V_o} \right\rceil - n. \end{cases} \tag{21}$$

As the output is regulated by adjusting the duty cycle and switching frequency of the boost, a special design of the resonant tank is not needed. The leakage inductor of the transformer can be utilized as the resonant inductor and no external resonant inductor is required. Therefore, the resonant capacitors are confirmed by the corresponding leakage inductance of the transformer as expressed in

$$\begin{cases} C_{r1} = \frac{1}{4\pi^2 f_r^2 L_{\text{leak1}}} \\ C_{r2} = \frac{1}{4\pi^2 f_r^2 L_{\text{leak2}}}. \end{cases} \tag{22}$$

In proposed topology, the *LLC* stage operate at the resonant frequency and act as a dc transformer. The magnetizing current is only for charging and discharging the parasitic capacitors of the power switches to realize ZVS. The resonant tank can be treated as short circuit under steady state operation. There are three windings in the transformer, the equivalent magnetizing

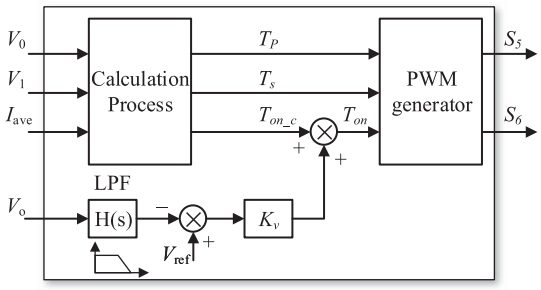

Fig. 15. Control schematic of the proposed converter.

inductor is presented at N_A port for the sake of simplicity. Within half a cycle, half the bus voltage is applied on the magnetizing inductor and result in a triangular-shaped magnetizing current. The amplitude of magnetizing current can be derived as

$$I_m = \frac{V_1}{8L_m f_s}. \tag{23}$$

During the dead time, all the parasitic capacitors are completely charged or discharged by the magnetizing current and a charge balance equation is obtained as

$$I_m t_d \geq 2C_{\text{oss\_}m}V_1 + 2\frac{n^2 C_{\text{oss\_}n}}{m^2}V_1 + 2\frac{C_{\text{oss\_}SR}}{m^2}V_1. \tag{24}$$

where t_d is the dead time, $C_{\text{oss\_m}}$ is the output capacitor of primary side devices on N_A port, $C_{\text{oss\_n}}$ is the output capacitor of primary side devices on N_P port, $C_{\text{oss\_SR}}$ is the synchronous rectifier output capacitor. Combining (23) and (24), the magnetizing inductor are finally confirmed by

$$L_m \leq \frac{t_d}{16 f_s \left(C_{\text{oss\_}m} + \frac{n^2 C_{\text{oss\_}n}}{m^2} + \frac{C_{\text{oss\_}SR}}{m^2}\right)}. \tag{25}$$

C. Control of the Proposed Converter

According to the analysis discussed in Section II, the control strategy of the proposed converter is given here. The control structure is depicted in Fig. 15. The required input variables for control are the input voltage of the boost V_0, the output voltage of the boost V_1, the average inductor current I_{ave}, and the output voltage V_o. The microcontroller unit calculates the needed switching period, ON-time, and the dead time with the input variables. The calculated period and dead time are loaded to the PWM generator directly. The output voltage is feedback to the microcontrol unit (MCU) with a low pass filter to suppress the high frequency noise. The output voltage controller is a conventionally designed PI-compensator. The output value of the controller is superposed on the calculated ON-time and is loaded to the PWM generator.

Under the circumstances of $V_0 > V_1/2$, the ON-time and the switching period are calculated with (11). The needed dead time for ZVS of the lower switch is calculated with (10). If $V_0 < V_1/2$, the ON-time and the switching period are calculated with (15). The ZVS turn ON of the lower switch can be obtained without any additional reverse conduction time and a body diode

TABLE II
CIRCUIT PARAMETERS OF THE PROTOTYPE

Parameters	Symbol	Value
Input voltage	V_{in}	190–475 V
Output voltage	V_o	12 V
Intermediate voltage	V_0	22–307 V
	V_1	312 V
	V_2	168 V
Switching frequency	f_{Boost}	22–520 kHz
	f_{DCX}	400 kHz
Boost devices	Q_5, Q_6	GS66508T
Primary devices	Q_1, Q_2	GS66508T
	Q_3, Q_4	GS66508T
Secondary devices	S_1, S_2	BSC022N04LS6*2
Transformers	T	ER32/3F36/13:7:1:1
Resonant inductors	L_{r1}	≈1.84 uH
	L_{r2}	≈1.2 uH
Resonant capacitors	C_{r1}	86 nF
	C_{r2}	132 nF
Magnetizing inductor	L_m	≈45 uH
Boost inductor	L	≈85.2 uH

commutation duration appears. To reduce the conduction loss of the body diode, the lower switch can be turned on ahead of the zero crossing of the inductor current. Hence, T'_R is counted into the ON-time

$$T_d = \begin{cases} T_s & V_0 \geq V_1/2 \\ T'_s & V_0 < V_1/2 \end{cases} \tag{26}$$

$$T_P = \begin{cases} T_P & V_0 \geq V_1/2 \\ T'_P & V_0 < V_1/2 \end{cases} \tag{27}$$

$$T_{\text{on\_}c} = \begin{cases} T_{\text{on}} & V_0 \geq V_1/2 \\ T'_{\text{on}} + T'_R & V_0 < V_1/2. \end{cases} . \tag{28}$$

Since the turn-OFF current of the lower switch is large enough, the interval II is short and a fixed dead time is loaded to the PWM generator.

IV. EXPERIMENTAL VERIFICATION

To validate the theoretical analysis abovementioned, a prototype with 190–475 V input and 12 V/500 W output is demonstrated in this section according to the design consideration given in Section III. The calculated value of *n* and *m* are 7 and 13, respectively. More detailed parameters of the prototype are listed in Table II. The photograph of the proposed prototype is depicted in Fig. 16. The dimension of the prototype is about 97.5 mm×44 mm×12.5 mm in which the bias supply and the controller system are both included.

The side view of the prototype is illustrated in Fig. 17. It can be seen that the prototype consists of five 4-layer PCB boards to form a stack structure to improve the space utilization and to keep the cost down. The boost bridge leg, the upper *LLC* bridge leg, the bias supply, one of the secondary windings, and its synchronous rectifiers are located on the top PCB board. The lower *LLC* bridge leg, the other secondary winding, and its synchronous rectifiers are located on the bottom PCB board. The microcontroller unit and other signal processing circuits are located on the signal board. The two primary winding PCB boards are sandwiched in between the top PCB board and the signal

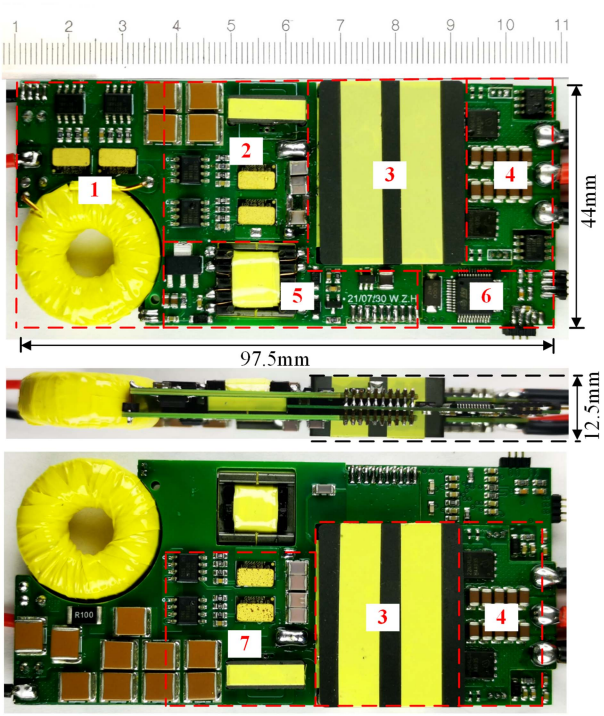

Fig. 16. Photograph of the prototype. 1) Boost stage. 2) Upper bridge leg. 3) Transformer. 4) Synchronous rectifiers. 5) Bias supply. 6) MCU. 7) Lower bridge leg.

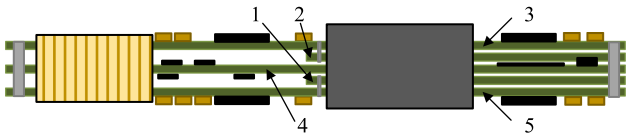

Fig. 17. Illustration of the side view of the prototype. 1) First primary winding board. 2) Second primary winding board. 3) Top board. 4) Signal board. 5) Bottom board.

board, the signal board, and the bottom PCB board, respectively. The two secondary winding are connected in parallel behind its synchronous rectifiers. To reduce the turn-OFF switching loss, the GaN devices are adopted to constitute the boost bridge leg, and the two *LLC* bridge legs. Meanwhile, Si devices are employed as synchronous rectifiers to reduce the conduction loss under high output current. A microcontroller unit from ST Microelectronics is employed to achieve digital control.

Since the switching frequency of the PWM converter increases with the load current decreases, the switching frequency boundary is set at 20% of full load in the prototype. And the switching frequency of the prototype under 20% load condition and 100% load condition within the whole input range are given in Fig. 18. As it can be seen, the prototype obtains an ultralow switching frequency at the two input limit points. The highest switching frequency measured in the prototype is about 520 kHz and it occurs at about 330 V input and 20% load current. Hence, the experimental results of the prototype under 190 V input, 330 V input, and 475 V input are given here.

Fig. 19 shows the measured waveforms of the input voltage, the output voltage, the inductor current, and the switching node

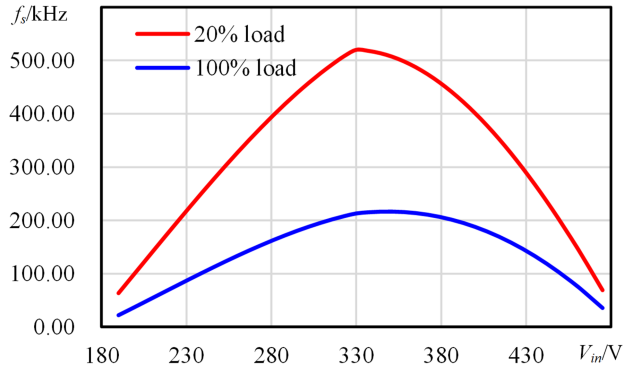

Fig. 18. Switching frequency of the prototype versus input voltage.

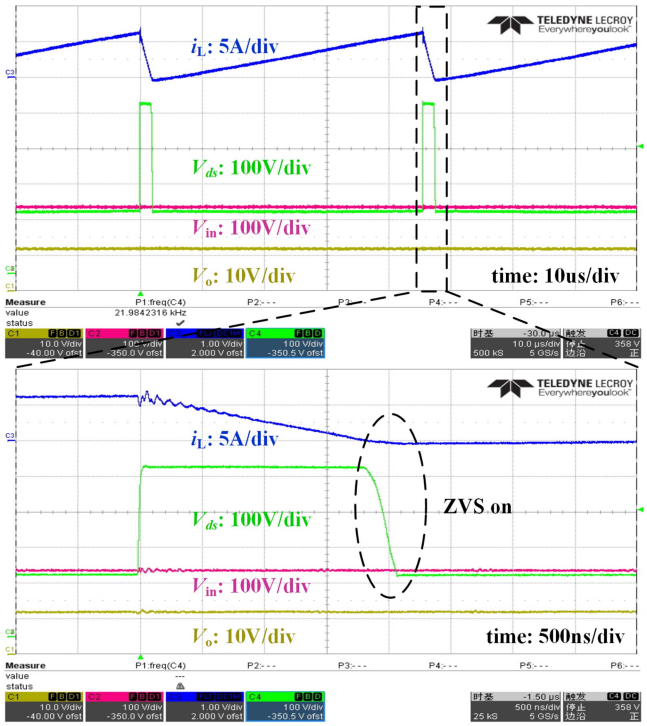

Fig. 19. Waveforms of the boost at Vin = 190 V, Po = 500 W.

of the PWM converter under 190 V input and 500 W output. The blue trace refers to the inductor current, the green trace is the voltage of the switching node, the pink trace represents the input voltage, and the yellow one is the output voltage. Under this circumstance, the input voltage of the PWM converter is lower than half of its output voltage. The ZVS turn ON of the upper switch can be easily achieved with a sufficient deadtime since the inductor current is large enough. As it can be seen, the drain to source voltage of the lower switch drops down to zero naturally when the inductor current is still in a negative direction. Hence, the ZVS turn on of the lower switch is obtained. Since the input voltage is close to the bus voltage of the lower DCX bridge leg, the switching frequency is low enough and it is about 22 kHz.

Fig. 20 shows the main waveforms of the PWM converter under 330 V input and 500 W output. Under such a circumstance,

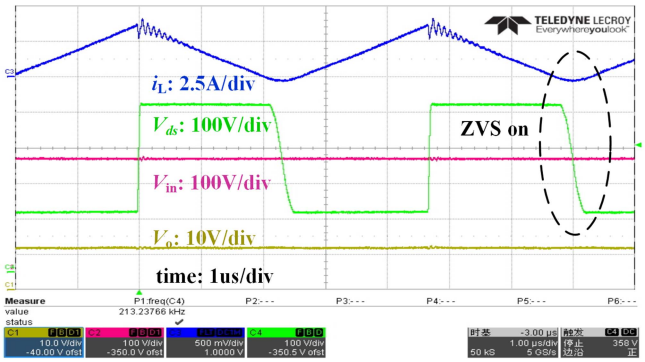

Fig. 20. Waveforms of the boost at Vin = 330 V, Po = 500 W.

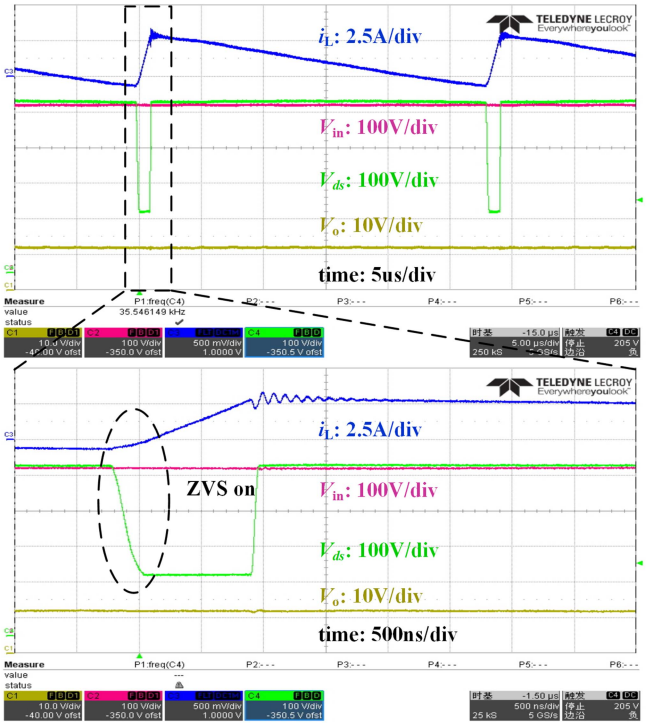

Fig. 21. Waveforms of the boost at Vin = 475 V, Po = 500 W.

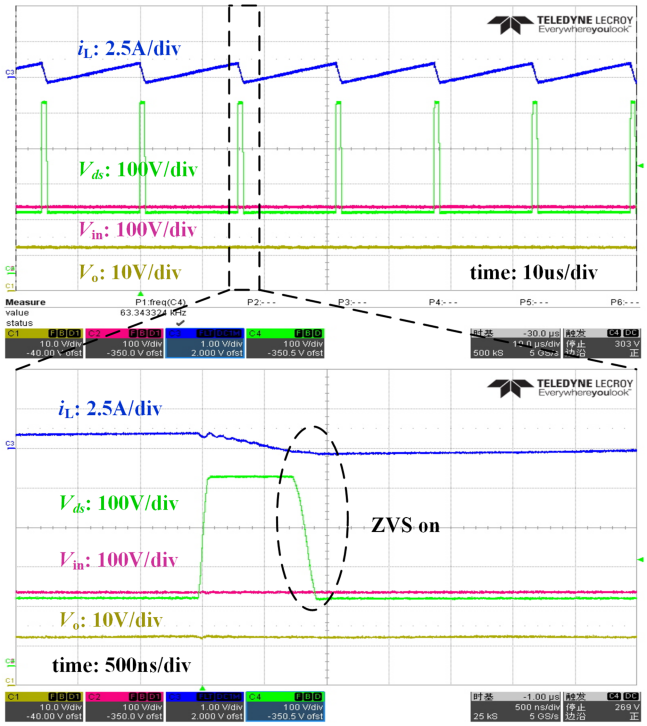

Fig. 22. Waveforms of the boost at Vin = 190 V, Po = 100 W.

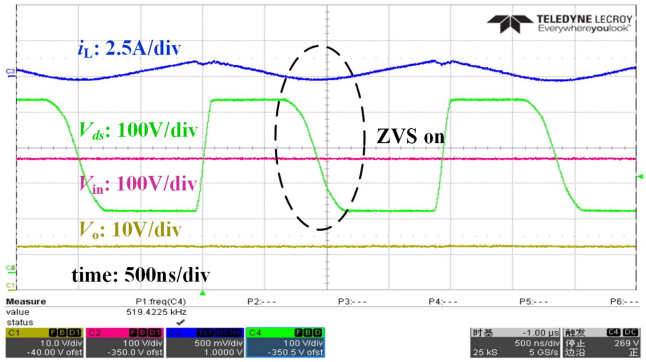

Fig. 23. Waveforms of the boost at Vin = 330 V, Po = 100 W.

the input voltage of the PWM converter is about half of its output voltage. The duty cycle of the switches is close to 0.5 and the inductor shows a high current ripple. Hence, a high switching frequency is needed to obtain an appropriate negative current and it is about 213 kHz. The ZVS turn ON for the lower switch is achieved.

The measured waveforms under 475 V input and 500 W output are shown in Fig. 21. Here, the input voltage of the PWM converter is higher than half of its output voltage. Because the input voltage is close to the bus voltage of the upper bridge leg, the switching frequency for ZVS is also low enough and it is about 36 kHz.

Figs. 22–24 depict the measured waveforms of the PWM converter under 100 W output for 190 V input, 330 V input, and 475 V input, respectively. The operating frequency is about 63 kHz, 519 kHz, and 69 kHz, respectively. It can be seen that the drain to source voltage of the lower switch reaches zero naturally before the inductor current flowing direction changes from negative to positive. It means that the ZVS turn ON can be also obtained at light load conditions. When the load current is lower than the boundary load current, the switching frequency will not increase anymore. Hence, the negative current will increase and the ZVS turn ON can be easily obtained. Furthermore, all the measured waveforms show that the output voltage of the prototype maintains at 12 V with the closed-loop control.

The measured voltage waveforms of the DCX bridge and the resonant current waveforms of the DCX under 100 W output with 190 V input, 330 V input, and 475 V input are shown in Fig. 25(a), Fig. 26(a), and Fig. 27(a), respectively. And the corresponding waveforms under 500 W output are shown in Fig. 25(b), Fig. 26(b), and Fig. 27(b), respectively. The blue trace is the resonant current waveform of the upper DCX bridge, the

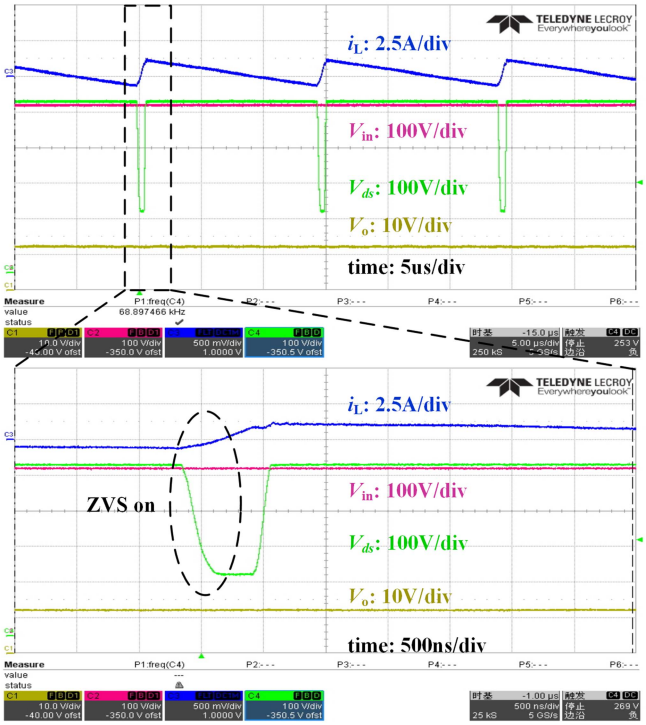

Fig. 24. Waveforms of the boost at Vin = 475 V, Po = 100 W.

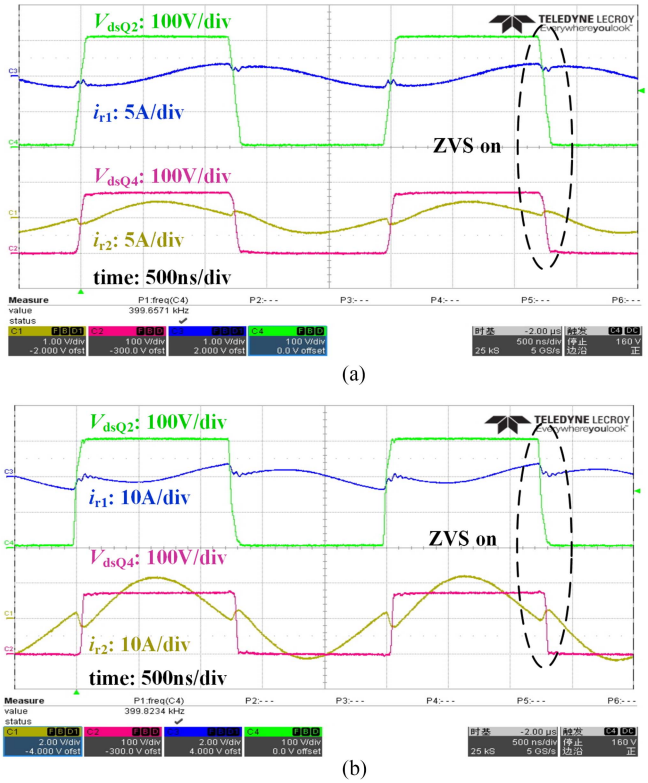

Fig. 25. Waveforms of the DCX at Vin = 190 V. (a) Po = 100 W. (a) Po = 500 W.

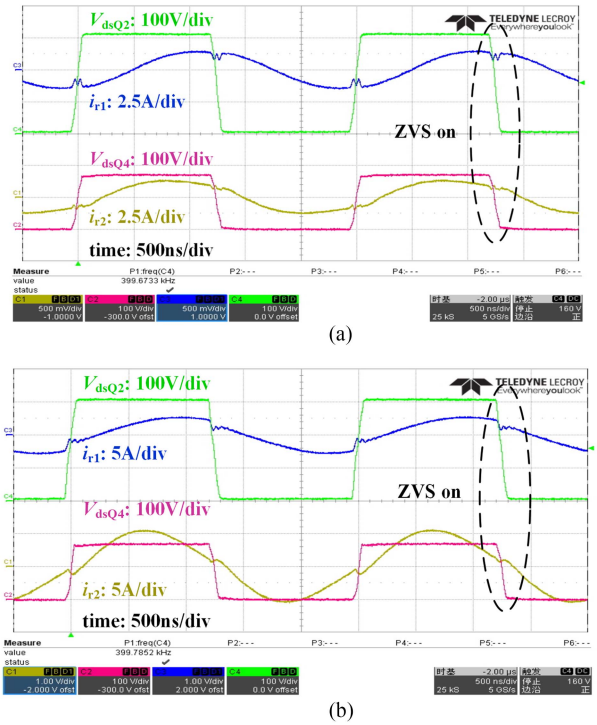

Fig. 26. Waveforms of the DCX at Vin = 330 V. (a) Po = 100 W. (a) Po = 500 W.

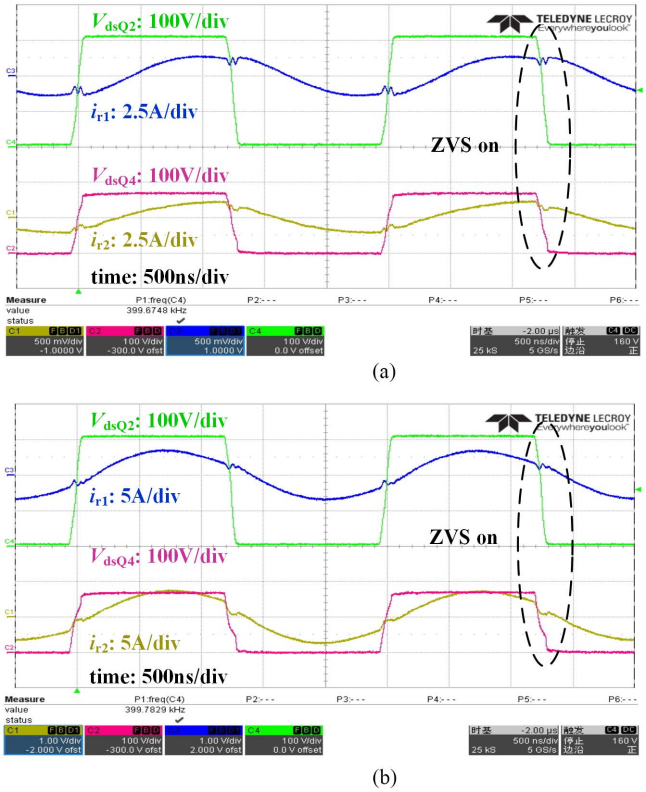

Fig. 27. Waveforms of the DCX at Vin = 475V. (a) Po = 100 W. (a) Po = 500 W.

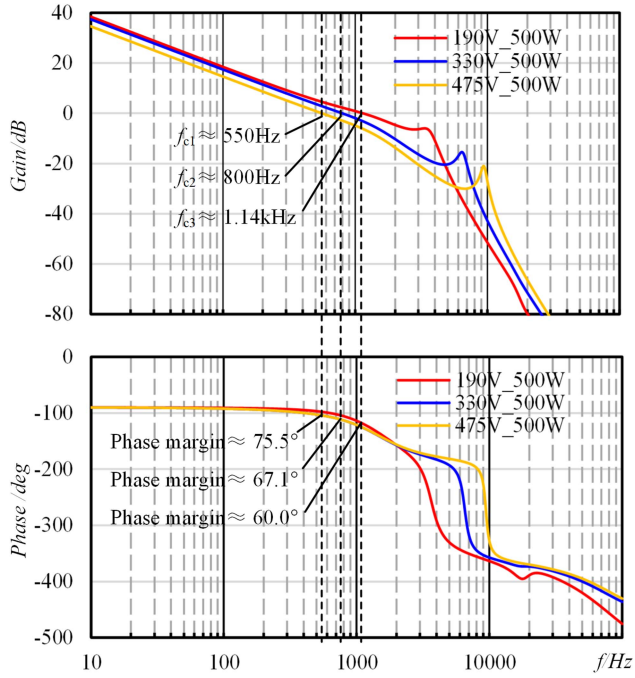

Fig. 28. Bode diagram of the compensated prototype at 500 W output power with different input voltage.

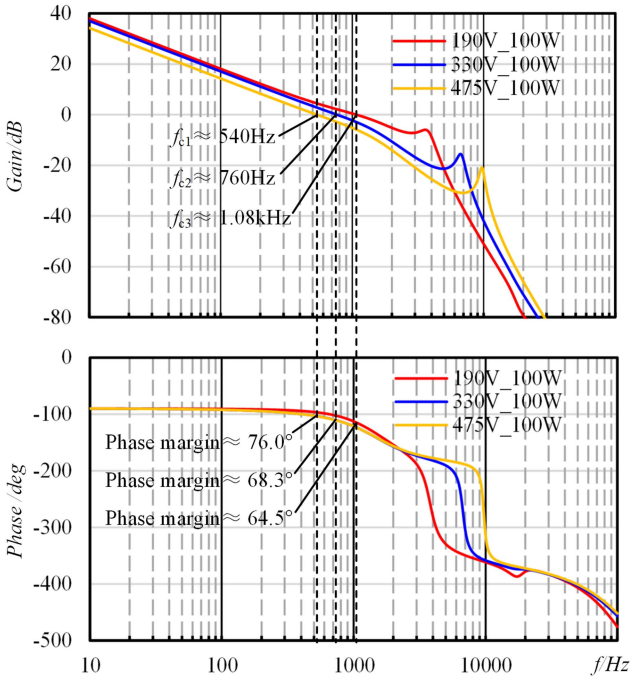

Fig. 29. Bode diagram of the compensated prototype at 100 W output power with different input voltage.

green trace is the voltage of the upper bridge leg. The yellow and the pink ones are the corresponding current waveform and the voltage waveform of the lower bridge leg. As it can be seen that the ZVS switching is achieved within the whole input range and regardless of the load condition. And with the input voltage increases the resonant current of the lower bridge leg decreases. Contrarily, the resonant current of the upper bridge leg increases with the input voltage increases. That is because the power delivered by the upper bridge increase with the input increases.

Fig. 28 shows simulated Bode diagram of compensated loop gain of the prototype at 500 W output with different input voltage. The crossover frequency of the prototype under 190 V input, 330 V input, and 475 V input are 1.14 kHz, 800 Hz, and 550 Hz, respectively. The corresponding phase margin are 60°, 67.1°, and 75.5°. It means that the system is stable enough. Fig. 29 shows the simulated bode diagram of compensated loop gain of the prototype at 100 W output with different input voltage. The crossover frequency of the prototype under 190 V input, 330 V input, and 475 V input are 1.08 kHz, 760 Hz, and 540 Hz. The corresponding phase margin are 64.5°, 68.3°, and 76.0°. The phase margin is large enough both at full load condition and at light load condition. Hence, the prototype is a stable system.

To verify the dynamic regulation capability of the proposed converter, a series of experiments are conducted. Fig. 30 shows the measured voltage and current waveforms of the prototype at load current transition at 330 V input. Fig. 30(a) shows the load current transient with the slew rate of about 2 A/us from 21–42 A. The output voltage drop is about 0.32 V and the recovery time is about 650 us. Fig. 30(b) shows the load current transient from 42–41 A. And the output voltage overshoot is about 0.34 V and the recovery time is about 710 us. Fig. 31 shows the measured transient waveforms at the input voltage transition under full load condition. The input voltage step is about 60 V and the voltage slew rate is about 30 V/ms. As it can be seen, the variation of the output voltage less than ± 0.15 V.

To show the power loss distribution of the proposed converter under different input voltage, the loss breakdown under full load with 190 V input, 330 V input, and 475 V input is analyzed, as shown in Fig. 32. It can be seen that higher loss is generated under a lower input voltage. That is because a higher current is needed under a lower input voltage for a specific output power. With the input voltage increases, the conduction loss caused by the current decreases. Moreover, the switching frequency of the PWM stage increases first and then decreases with the input voltage increases. Both low core loss on the boost inductor and low conduction loss can be obtained under 475 V input. Due to a large input current and large resonant current of the lower bridge leg, the highest power loss occurs at 190 V input and full load output. Hence, the highest temperature on the prototype also appears in this condition. The thermal performance is tested under 190 V input and 500 W output with the ambient temperature of about 20 °C and a fan with the speed of 3900 r/min and the airflow of 65 CFM. The measured highest temperature is about 80.3 °C, as shown in Fig. 33.

To have a further comparison, the main parameters of both the proposed converter and four state-of-the-art converters from literatures and industry are listed in Table III. There are four converters have a similar power rating and aim to wide input range applications. And a similar partial power regulation converter from [30] but aim to narrow input range applications. Since the input range of the converters differs from each other, their normalized gain ranges are given here. The dual-bridge *LLC* from literature [25] and the buck–boost integrated *LLC* (BB*LLC*)

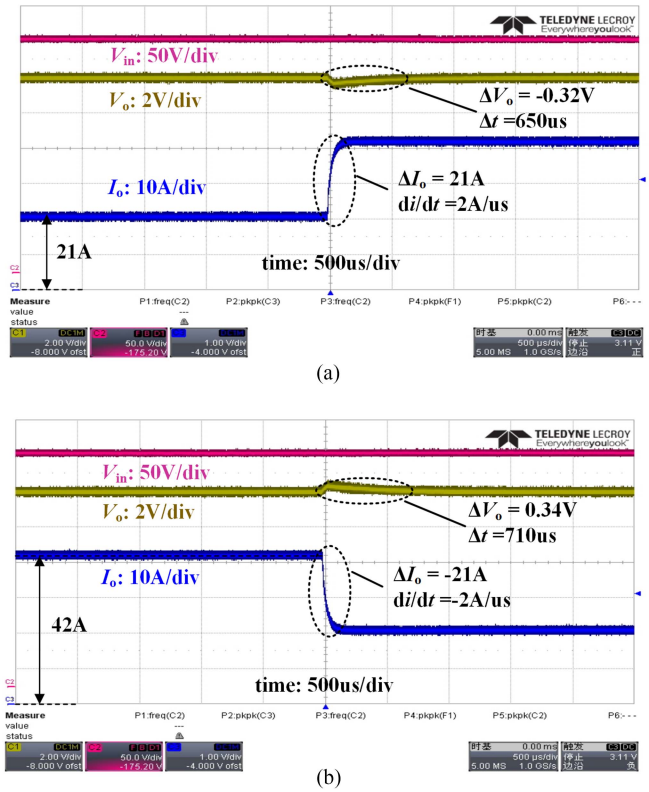

Fig. 30. Measured waveforms of the proposed converter at output current transition with a current slew rate of 2 A/us. (a) From 21 A to 42 A. (b) From 42 A to 21 A.

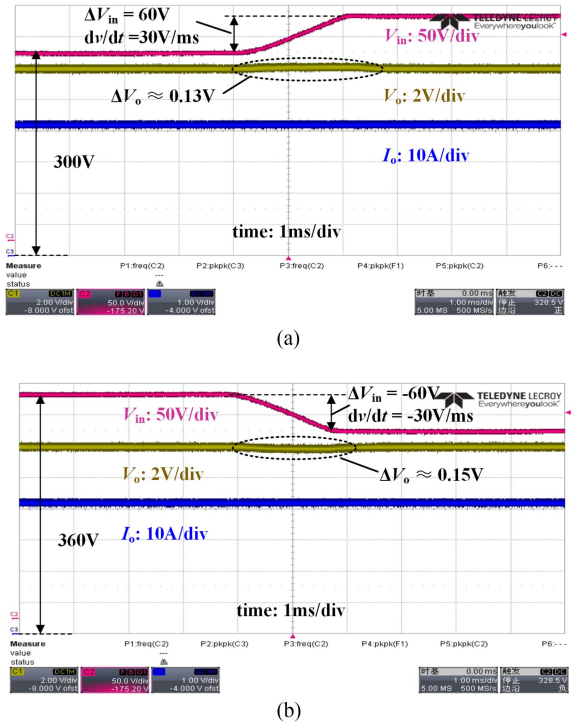

Fig. 31. Measured waveforms of the proposed converter at input voltage transition with a voltage slew rate of 30 V/ms. (a) From 300 V to 360 V. (b) From 360 V to 300 V.

converter from literature [28] are *LLC*-based converters with different gain range extension methods. The commercial product (MCOTS-C-270-12-FT) from SynQor represents the two-stage solution. As it can be seen, the proposed converter obtains similar peak full load efficiency compared to the regulated DCX (RDCX) from literature [30], but the normalized gain range of the proposed converter is far wider than that of the RDCX converter. Moreover, the normalized gain range of the proposed converter is only lightly lower than that of the commercial product but higher than both the dual-bridge *LLC* and the BB*LLC*. And within each's input range under full load conditions, the proposed converter has the highest peak efficiency compared to other counterparts. And there is about 5% improvement compared to the commercial product. Moreover, the proposed converter has the highest power density compared to these counterparts. And there is about 51% improvement compared to the commercial product.

The efficiency curves of the proposed converter under different load currents with different input voltages are also measured. In [25], the efficiency curves at 120 V input, 180 V input, and 240 V are given. In [28], the efficiency curves at 250 V input, 335 V input, and 420 V input are given. And the datasheet also gives the efficiency curves of MCOTS-C-270-12-FT with 155 V input, 270 V input, and 425 V input. Hence, the efficiency curves of the proposed converter with 190 V input, 330 V input, and 475 V input are also given here. Since not all these converter's efficiency decreases or increases monotonically with

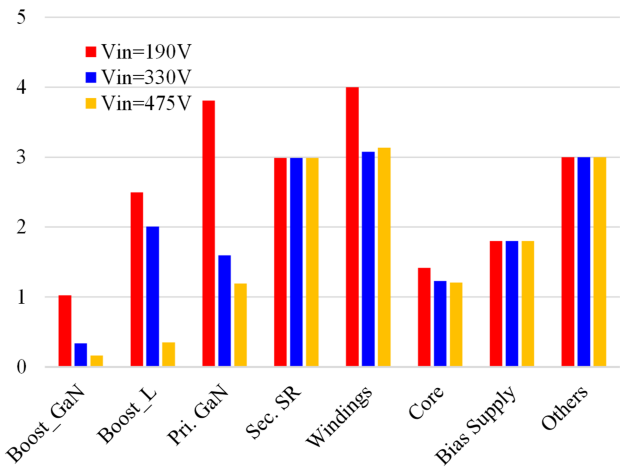

Fig. 32. Loss breakdown at different input voltage.

the input voltage, the comparison is conducted between each's optimal efficiency curve, worst efficiency curve, and the normal efficiency curve for the sake of fairness.

Fig. 34(a) shows optimal efficiency curves of four converters. The full load efficiency of the proposed converter is about 96.42% and a 5% improvement is obtained compared to the commercial product. And there are about 2.8% and 0.4% improvements, respectively, compared to the dual-bridge *LLC* and the BB*LLC*. Furthermore, the measured peak efficiency of the proposed converter is up to 97.2%, and the efficiency of the proposed converter is always higher than other counterparts within the whole load range.

TABLE III
COMPARISON OF FOUR TYPES WIDE INPUT RANGE CONVERTERS

Parameters	Proposed converter	RDCX [30]	Dual-bridge LLC [25]	BBLLC converter [28]	MCOTS-C-270-12-FT
Input range	190–475 V	342–370 V	120–240	250–420 V	155–425 V
Output voltage/ power	12 V/500 W	40 V/1000 W	24 V/480 W	24 V/720 W	12 V/600 W
Normalized gain range	1-2.5	1-1.08	1-2	1-1.68	1-2.74
Peak full load efficiency	96.42%	96.44%	92.35%	96.04%	91.41%
Power density	153W/in^3	Not Given	Not Given	149W/in^3	101W/in^3

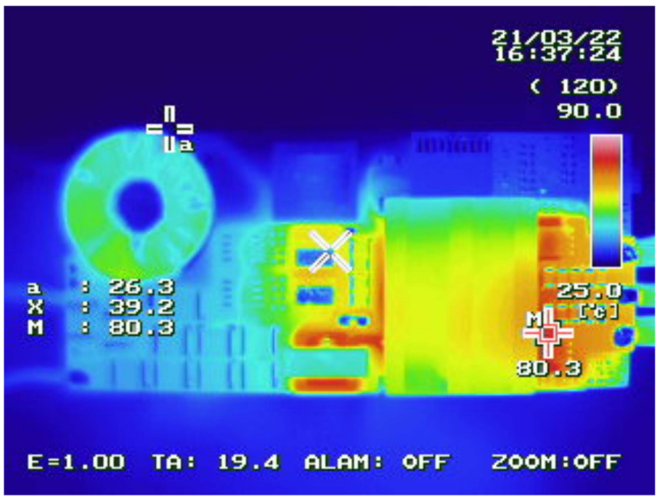

Fig. 33. Measured thermal image.

Fig. 34(b) illustrates the normal efficiency curves of the four converters. The full load efficiency of the proposed converter under this condition is about 95.91% and there are about 4.9%, 4.1%, and 0.6% improvement, respectively, compared to the commercial product, the dual-bridge *LLC*, and the BB*LLC*. The peak efficiency is about 97% and an overall high efficiency is also obtained.

Fig. 34(c) gives the worst efficiency curves of the four converters. Under this circumstance, the full load efficiency of the proposed converter is about 94.51% and there are about 4.4% and 1.7% improvements compared to the commercial product and the dual-bridge *LLC*. It is about 1% lower than the BB*LLC*. But the proposed converter has a wider input range compared to the BB*LLC*. Furthermore, when the load is lighter than 67%, the proposed converter still presents a higher efficiency than the BB*LLC*.

V. CONCLUSION

A partial power regulation topology with wide input range capability is proposed in this article and its operating principle is also analyzed. By introducing a negative inductor current, the ZVS turn ON of the PWM converter can be obtained and the modulation principle is also analyzed in detail. The circuit design consideration is also discussed for an optimal design. Finally, the theoretic analysis is verified with experiments. A 12 V/500 W prototype with a 190 V to 475 V wide input range is built according to the design consideration. Experimental result shows that the proposed converter regulates the output well within the whole input range. The measured waveforms show that the ZVS turn ON of both the PWM stage and the *LLC* bridge leg is obtained. Benefiting from that, the proposed converter obtains full load efficiency of 96.42% and a power density of 153 W/in^3. The efficiency improvement is about 5%, 2.8%, and 0.4%, respectively, compared to the commercial product, the dual-bridge *LLC*, and the BB*LLC*. The power density improvement is 51% compared to the commercial product.

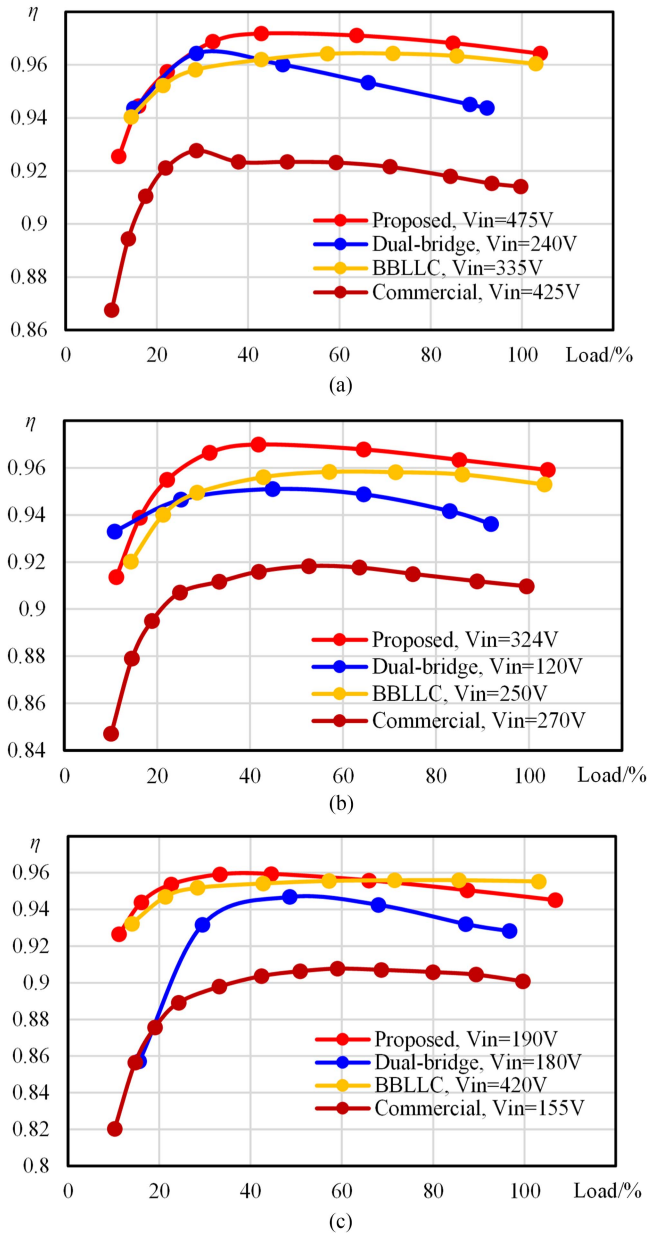

Fig. 34. Efficiency versus load condition. (a) Optimal efficiency curves. (b) Normal efficiency curves. (c) Worst efficiency curves.

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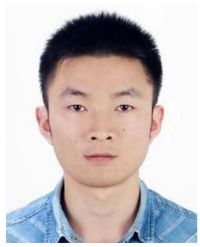

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