Letters

Fault Detection and Ride Through of CHB Converter-Based Star-Connected STATCOM Through Exploring the Inherent Information of Multiloop Controllers

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***Abstract*—A simple detection and ride-through operation approach is proposed for star-connected cascaded H-bridge (CHB) converter-based STATCOMs with a single IGBT open circuit fault. It adopts a modified current regulator with high gains at both dc and fundamental frequencies. Then, the output signals of the current regulator branches and the dc voltage balancing regulator are synthesized as an inherent indicator to quickly determine the position of the open-circuit fault IGBT. With this approach, the controller can also be considered as an inherent system state monitor, but without any additional sensors or computing burdens. Afterwards, in the ride-through operation stage, the faulty H-bridge module can switch to half-bridge operation and the corresponding dc offset voltage is compensated by the remaining healthy modules. It has been validated that the proposed approach is accurate in various conditions, including grid voltage and load disturbances.**

***Index Terms*—Cascaded h-bridge (CHB)converter, fault detection, fault ride through.**

I. Introduction

ALTHOUGH with a grid-friendly stair-case output voltage waveform and direct medium voltage integration, a cascaded H-bridge (CHB) converter based STATCOM suffers from a high possibility of power switch faults as a large number of low voltage IGBTs are used in this topology. In various types of switch fault, a single IGBT open circuit fault is the most commonly seen [1], which can happen due to bond wire breaking, missing gating signals, etc. [2]. Accordingly, in the previous research, attention has been focused on the detection of a single IGBT open circuit fault and the ride-through operation of the postfaulty system.

In general, fault detection methods can be classified into two categories. First, fault detection is realized with the help of extra sensors. For instance, when the converter output PWM voltage is measured using a high bandwidth voltage sensor [3], the faulty module can be quickly detected by comparing the expected output PWM voltage waveform with the measured one.

Fault detection can also be realized by using additional digital detectors, which are executed in parallel with the CHB closed-loop voltage and current controllers. For instance, the extended Kalman filter is used to process the transient line current and the detection is triggered by comparing the output of the Kalman filter with the preset thresholds [4]. In addition, the model predictive based identification approach [5] is proposed, where the fault type is determined according to the difference between the predicted response and the measured system response. In general, using independent detector is complicated, and the additional computational burden can be a challenge for converter digital processors.

When a fault is detected, ride-through operation approaches can be applied. For instance, the faulty module bypass and the zero sequence voltage injection can be used to maintain three-phase balanced grid current [6]. Nevertheless, a better way of addressing the faulty module is to keep the module working in a reduced power mode [7].

Alternately, a simple detection approach using existing information about the controller is proposed. It collects the output signals of the dc voltage balancing regulator, the output current harmonic branch regulator, and the output current dc component branch regulator. Then, by investigating the relationships between open-circuit faulty switch positions and the transient response of these regulators, it is found that the inherent information of multiloop regulators is sufficient to quickly determine the exact position of the open-circuit faulty IGBT. Then, the faulty module transfers to operate in a reduced modulation index manner with a dc voltage offset, and the dc voltage offset is mitigated by the other healthy modules without leaving an obvious dc current disturbance to the grid.

II. Review of Traditional Control Approach

Fig. 1 shows the diagram of a CHB converter for reactive power compensation. First, each CHB converter phase leg has three modules as a1 to a3, b1 to b3, and c1 to c3. L_s and C_f are the filter series inductance and shunt capacitance, respectively. The dc voltage of a power module is $V_{\mathrm{dc},jk}$, the CHB converter

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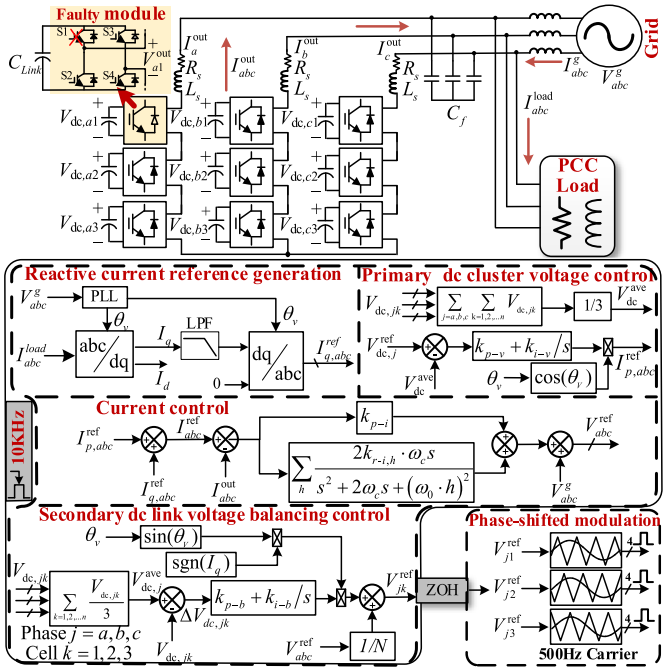
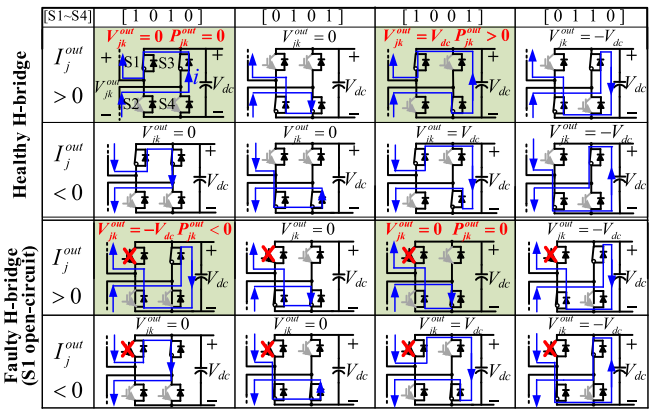


Fig. 1. Traditional control method for CHB converter based STATCOM.

TABLE I
COMPARISON OF OUTPUT VOLTAGE AND POWER BETWEEN HEALTHY AND FAULTY H-BRIDGE (S1 OPEN-CIRCUIT)



output current is I_j^{out}, the grid voltage is V_j^g, I_j^g and I_j^{load} are the grid currents and load currents respectively, where j stands for the phase leg and k is the module number. The controller of the system mainly has five parts. First, the grid phase angle is determined by a PLL as θ_v and then the output current reactive power component is obtained according to load condition as $I_{q,j}^{\text{ref}}$. Second, the averaged phase dc voltage is calculated as $V_{\text{dc},j}^{\text{ave}}$ and the real power reference output current is given by a PI regulator for V_{dc}^{ave} regulation as $I_{p,j}^{ref}$. A proportional and resonant controller with grid voltage feed-forward control is adopted for output current tracking, and the output of the current regulator is reference phase voltage V_j^{ref}. Moreover, to realize dc bus voltage balancing, each power module dc voltage is compared with the averaged module dc voltage $V_{dc,j}^{ave}$ and then a simple PI regulator produces compensation voltage amplitude, which is aligned to the corresponding phase current phasor direction for dc voltage balancing. Finally, a phase-shifted modulation is used to reduce the switching ripples in the output current.

When a single IGBT open circuit fault happens (see S1 in module a1), the transient system performance using the traditional regulator is sketched in Fig. 2. First, it can be seen that the three-phase output currents as shown in Fig. 2(a) becomes unbalanced and distorted. Furthermore, by at the current tracking error ΔI_j in Fig. 2(b) concludes that the faulty phase leg-a has a positive tracking error ΔI_a, whereas the other two phases have tracking errors with opposite polarity. The output of the dc voltage balancing regulator is shown in Fig. 2(c), where the magnitude reference $E_{S,a1}^{\text{ref}}$ of faulty module a1 falls while the magnitude references of a2 and a3 in the same phase leg increase. At the same time, the references to the other two healthy phases are roughly unaffected.

III. PROPOSED DETECTION APPROACH

A. Characteristics of the System With Different Faulty Switches

The abovementioned transient performance in Fig. 2 is mainly caused by the disturbance from the faulty module. Accordingly, it is necessary to have a detailed investigation of the faulty module output characteristic. First, the output voltage and power flow of a module under S1 fault are shown in Table I, with various types of switching states ([1,0,1,0], [0,1,0,1], [1,0,0,1], and [0,1,1,0]) and output current polarity ($I_j^{\text{out}} > 0$ and $I_j^{out} < 0$). The shaded elements mean that the power flow and the output voltage of the faulty module are not the same as the healthy module. More specifically, the faulty module always has low output power and voltage in these cases. For other elements, the faulty and healthy modules have the same output voltage and power performance.

For a high power CHB converter, the switching frequency of a power cell is typically lower than 1 kHz. In the case of a power cell IGBT open circuit fault and with 90° current phase displacement, the harmonic spectra of a power cell output voltage with 500 Hz switching frequency is shown in Fig. 3(a), where it can be seen that both the dc component and the harmonic components from the 9th to 11th harmonic orders are obvious. The characteristics of the 9th harmonic component are selected for detailed study [8].

The detailed analysis of a module with S1 to S4 open circuit is shown in Fig. 3(b). When the output voltage reference V_j^{ref} is 90° leading the output current (generating lagging reactive power), the output voltage waveform is shown in the first column. Compared to the healthy module performance at the top of the figure, the faulty module has missing voltage pulses, which are determined by the relationships of output current I_j^{out} and voltage V_j^{out} in Table I.

In addition, the output current fundamental component and 9th harmonic component are shown in the second column of the figure. As shown, for S1 fault in the antidiagonal switch pair, the 9th harmonic output current is around 90° leading of the fundamental output voltage. On the other hand, for S4 fault in the antidiagonal switch pair, the 9th harmonic output current is

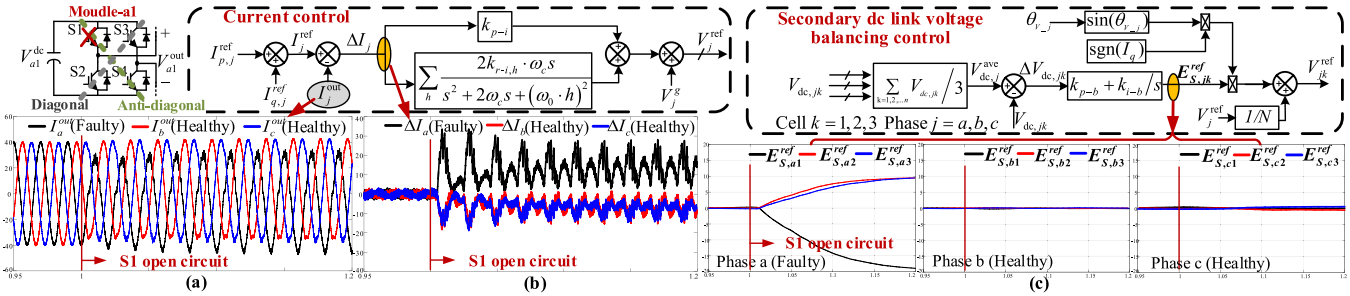


Fig. 2. Multiloop controllers intermediate node transient signals response when S1 of module-a1 open-circuited. (a) Three-phase output currents. (b) The current tracking errors. (c) The magnitude references of the dc voltage balancing regulator.

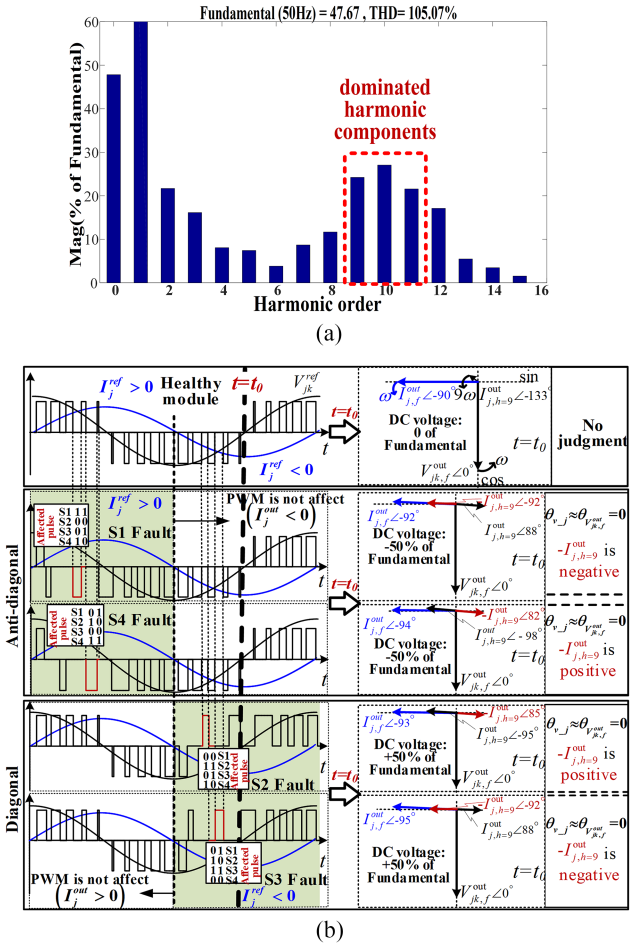


Fig. 3. (a) Harmonic spectra of a power cell with S1 open circuit (500 Hz switching frequency). (b) Diagram of the voltage and current characteristics with different switch faults.

roughly 90° lagging of output voltage. Similar conclusion can also be seen in the diagonal switch pair fault condition.

Fig. 4 has plotted the response of output current, module reference voltage, and module output voltage with both leading and lagging output current. For instance, Fig. 4(b) shows the phasor relationships in the case of lagging output current. It can be seen that $I^{out}_{j,h=9}$ roughly reaches its positive peak value when $\theta_{v\_j} = 0°$. On the other hand, $I^{out}_{j,h=9}$ roughly reaches the positive peak value when $\theta_{v\_j} = -90°$. Therefore, the detection

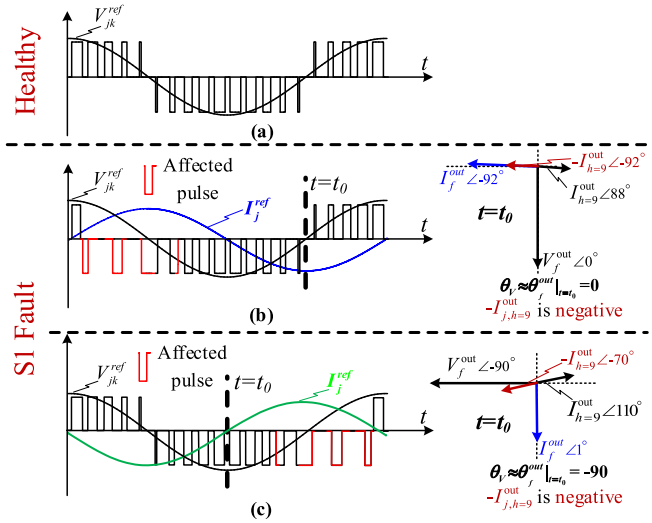


Fig. 4. Response of output voltage and output current of faulty module under leading and lagging output current. (a) The PWM pulses of output voltage. (b) The condition of lagging output current. (c) The condition of leading output current.

of faulty IGBT via 9th harmonic current response should be designed according to the angle of the grid voltage.

B. Proposed Faulty Switch Identifier

According to the discussion in the previous section and the analysis in Section II, a fault switch identifier can be developed, which fully utilizes the existing information of the modified multiloop regulator of the CHB converter.

The output current regulator and secondary voltage balancing controllers are selected and shown at the top of the Fig. 5. First, a modified current regulator with high gain at dc and harmonic frequency is given as follows:

$$V_j^{ref} = \left(\overset{\text{proportional}}{k_{p-i}} + \frac{\overset{\text{F resonant}}{k_{r-i}\cdot 2\omega_c s}}{s^2+2\omega_c s+\omega_0^2}\right)\cdot\left(I_j^{ref}-I_j^{out}\right)$$
$$\left(k_{dc}\cdot\left(\frac{\overset{\text{dc}}{\omega_{LPF}}}{s+\omega_{LPF}}\right)+\sum_{h=3\ldots9}\frac{\overset{\text{Har resonant}}{k_{r-i,h}\cdot 2\omega_c s}}{s^2+2\omega_c s+(\omega_0\cdot h)^2}\right)$$
$$\cdot\left(0-I_j^{out}\right)+\mathrm{G}_{ext}(s)\cdot V_j^{g} \quad (1)$$

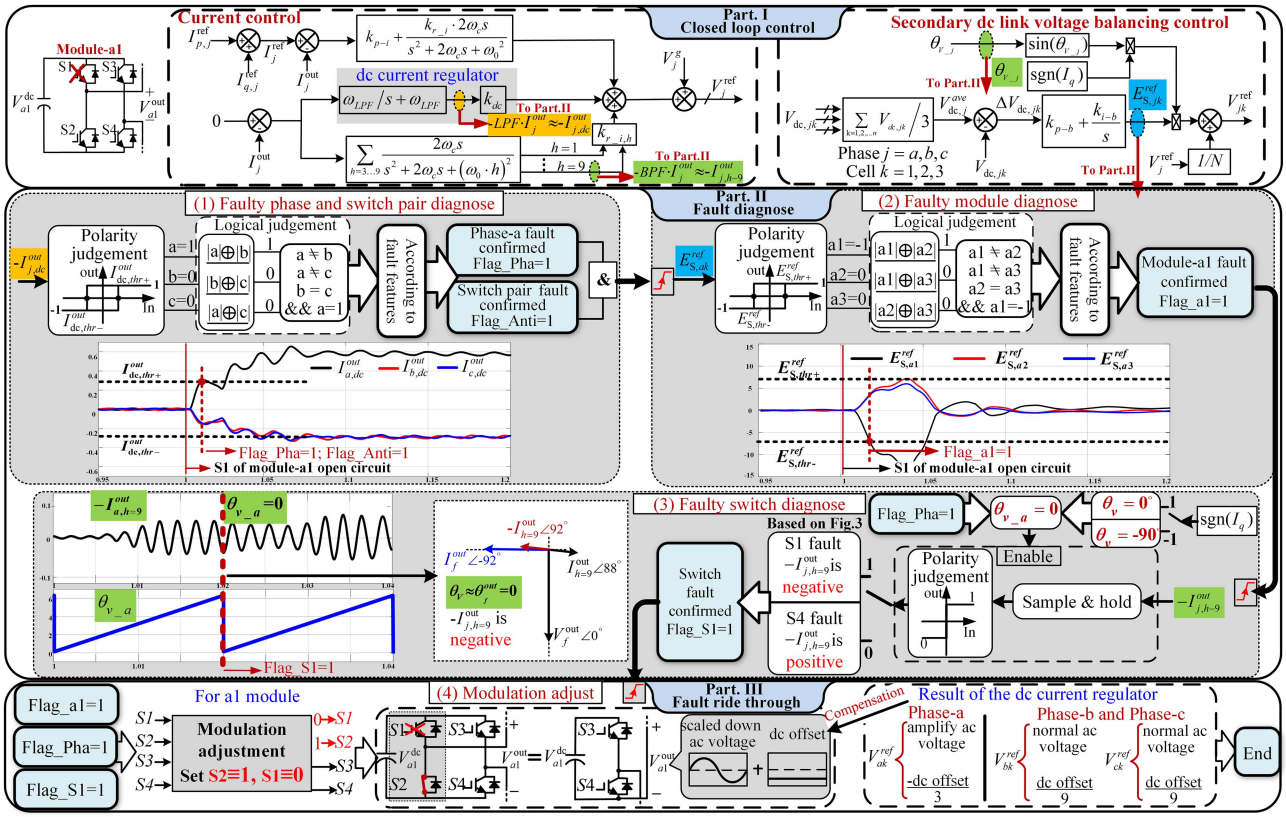


Fig. 5. Complete diagram of the proposed fault detection and fault tolerance approach. (S1 fault for case study).

where $G_{ext}(s).V_j^g$ includes the fundamental and selected low-order harmonic grid voltage as the feed-forward term, $G_{ext}(s)$ is the detector for rejecting the grid disturbance, including harmonics that may affect the accuracy of fault detection, V_j^{ref} is the reference voltage for modulation. In this case, as shown in Fig. 5. The dc component of output current $I_{j,dc}^{out}$ and the 9th harmonic component of output current $I_{j,h=9}^{out}$ are actually responses of control loop nodes. Therefore, they can also be extracted using the modified current regulator. In addition, the secondary dc voltage balancing loop is given as follows:

$$V_{jk}^{ref} = ((k_{p-b} + k_{i-b}/s) \cdot (V_{dc,j}^{ave} - V_{dc,jk})) \cdot \sin(\theta_{v\_j}) \cdot \mathrm{sgn}(I_q) + V_j^{ref} \Big/ N \tag{2}$$

$k_{p-b} + k_{i-b}/s$ is the PI regulator, θ_{v_j} is the grid voltage angle.

Similarly, θ_{v_j} and the output of the PI regulator $E_{S,jk}^{ref}$ (see the upper-right corner of Fig. 5) are captured for fault diagnosis.

When $-I_{j,dc}^{out}$, $-I_{j,h=9}^{out}$, $E_{S,jk}^{ref}$, and θ_{v_j} are obtained, they are sent to judgment blocks as shown in the Part. II(1) of the Fig. 5 for fault detection. In detail, as $-I_{a,dc}^{out}$ has an opposite polarity against that of other phases $-I_{b,dc}^{out}$ and $-I_{c,dc}^{out}$, the faulty phase can be determined (Flag_Pha = 1). Meanwhile, the faulty switch pair is determined according to the polarity of $-I_{a,dc}^{out}$ ($-I_{a,dc}^{out}<0$ for a diagonal switch pair fault and $-I_{a,dc}^{out}>0$ for an antidiagonal switch pair fault). In this study, an antidiagonal switch pair fault is determined (Flag_Anti = 1). Moreover, for a power module in the faulty phase leg has a different dc voltage variation trend ($E_{S,jk}^{ref}$) against others in the same leg, as shown in Part. II(2) of the Fig. 5, the faulty module can be determined (Flag_a1 = 1).

Finally, the detailed location of faulty IGBT is determined by checking the value information of the 9th harmonic current at the time instant t_0, where :

$$\begin{cases} \theta_{v\_j}|_{t=t_0} \approx \theta_{V_{jk,f}^{out}}|_{t=t_0} = 0^\circ & I_q > 0 \text{ Lagging power factor} \\ \theta_{v\_j}|_{t=t_0} \approx \theta_{V_{jk,f}^{out}}|_{t=t_0} = -90^\circ & I_q < 0 \text{ Leading power factor} \end{cases} \tag{3}$$

For STATCOM with lagging output current $I_q > 0$, the instantaneous value of the 9th harmonic output current $-I_{j,h=9}^{out}$ is captured when the grid voltage angle θ_{v_a} is 0°. On the other hand, $-I_{j,h=9}^{out}$ is examined when θ_{v_a} is −90°. Note that both the grid and load disturbance may cause additional 9th harmonic output current, which can affect the accuracy of the fault detection. In fact, the proposed detection approach adopts a step-by-step detection procedure as shown in Fig. 5. The final detection step using 9th harmonic current information will not be activated unless the previous two steps using dc current offset and dc rail voltage variations are completed.

When the exact fault location is known, the ride-through operation of the system can be executed. In the case of an S1 fault in module a1, the complimentary switch S2 of this module is turned ON constantly and the right half bridge with switches S3 and S4 modulates to produce a reduced ac output voltage and its associated dc output voltage is compensated by other modules. Accordingly, a part of the faulty module's a1 power rating can be used without shunting down the entire module.

TABLE II
KEY PARAMETERS OF THE EXPERIMENTAL SYSTEM

Circuit parameters		
Rated PCC voltage	V^g	110VRMS/50 Hz
module dc link voltage	V_{dc}	80 V
dc link capacitor	C_{Link}	4000 uF
Filter inductance	L_S;R_S	L_S=0.3 mH; R_S=0.01 Ω;
Power module switching frequency	f_s	500 Hz
Number of power modules in a phase	N	3
Control parameters		
Current control parameters	k_{p-i};k_{r_i} ω_{LPF}; k_{dc}	k_{p-i} = 4 A/V;k_{r-i} = 30 A/V ω_{LPF} = 0.01rad/s;k_{dc}=300A/V
Phase voltage control parameters	k_{p-v} k_{i-v}	k_{p-v}=0.2/V k_{i-v} = 0.1/(V · s)
Secondary voltage balancing control parameters	k_{p-b} k_{i-b}	k_{p-b} = 6/V k_{i-b} = 10/(V · s)
Band pass angular frequency	ω_c	ω_c =5rad/s
Fault detection parameters		
Fault tolerance threshold value	$E^{ref}_{S,thr}$ $I^{out}_{dc,thr}$	$\lvert E^{ref}_{S,thr}\rvert$ = 5V $\lvert I^{out}_{dc,thr}\rvert$=5A

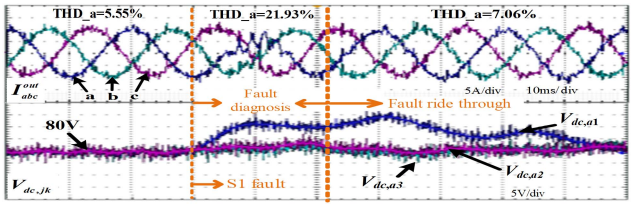


Fig. 6. Three-phase output current and the dc bus voltage of modules in phase-a.

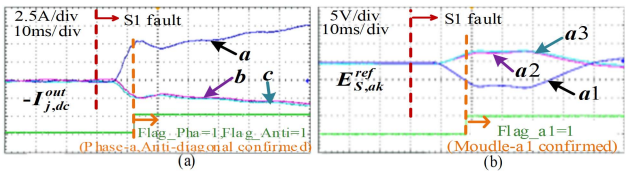


Fig. 7. Responses of the dc current regulator and dc voltage balancing controller in phase-a. (a)The response of the dc current regulator. (b)The response of the dc balance regulator.

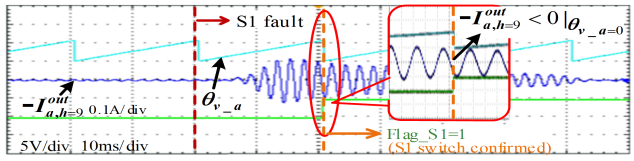


Fig. 8. Output of 9th harmonic current resonant controller and the grid voltage angle in phase-a.

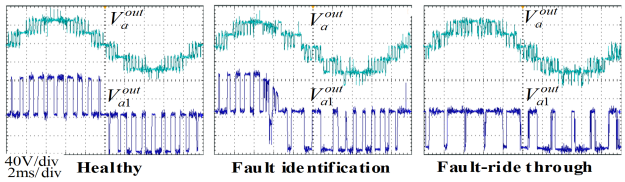


Fig. 9. Output voltage of module a1 and phase-a converter leg.

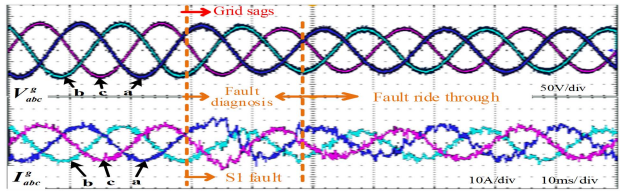


Fig. 10. Three-phase grid voltage and current under simultaneous IGBT fault and grid sags.

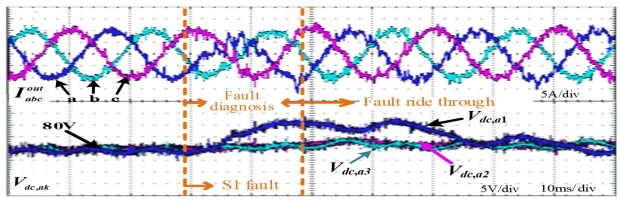


Fig. 11. Three-phase output current and the dc bus voltage of modules in phase-a under simultaneous IGBT fault and grid sags.

IV. EXPERIMENTS

Experiments have been executed on a prototype with three modules in each phase leg, with the parameters as shown in Table II.

The three-phase output current and the dc bus voltage of modules in phase-a are shown in Fig. 6, where both the output current and the dc rail voltage are well balanced before the fault. When the gating signal of S1 in module a1 is blocked to emulate a switch fault, it can be seen that the phase-a current has nontrivial distortion and the module-a1 dc voltage increases significantly. For around one cycle after the fault, the faulty location is confirmed and the ride-through control is applied. Accordingly, the output current and dc rail voltage become well balanced and sinusoidal again. However, at very low power operation, the system response time will become longer, e.g., at 0.05 pu, it will take more than six cycles to complete a fault location.

The responses of the current regulator dc branch are shown in Fig. 7(a). As seen, the $-I^{out}_{a,dc}$ is positive while $-I^{out}_{b,dc}$ and $-I^{out}_{c,dc}$ are negative. When $-I^{out}_{a,dc}$ reaches the threshold, the faulty-phase leg and the fault switch-pair are both confirmed (Flag_pha = 1, Flag_Anti = 1). The output of the dc voltage balancing controller for phase-a is given in Fig. 7(b), where the output of a1 has a negative value while the other two modules have a positive value after the fault. Accordingly, the exactly faulty module can be quickly identified (Flag_a1 = 1).

In addition, the detailed faulty switch location is identified according to the polarity of the 9th harmonic current responses $-I^{out}_{j,h=9}$ when grid voltage angle is 0 as Fig. 8, where it is easy to see that $-I^{out}_{j,h=9}$ has rough the negative peak value at this moment. Therefore, S1 fault is confirmed (Flag_S1 = 1).

Figs. 10 to 13 show the performance of the detection approach under the case of simultaneous S1 open circuit fault and three-phase grid voltage sags. It is seen that even under the case of grid disturbance, the proposed approach can obtain a rapid and accurate detection of faulty IGBT. In addition, the ride through operation approach still maintains a three-phase well balanced and harmonic mitigated output current.

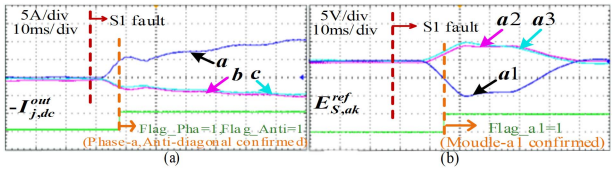


Fig. 12. Responses of the dc current regulator and dc voltage balancing controller in phase-a under simultaneous IGBT fault and grid sags. (a)The response of the dc current regulator. (b)The response of the dc balance regulator.

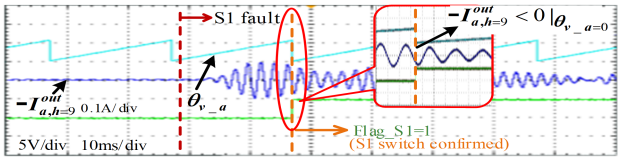


Fig. 13. Output of 9th harmonic current resonant controller and the grid voltage angle in phase-a under simultaneous IGBT fault and grid sags.

TABLE III
COMPARISON OF SWITCH FAULT DIAGNOSTIC METHODS

Functionality / Method	Fault detection	Fault ride-through	Additional sensors	Diagnosis time	Complexity	Parameter-related
Voltage and current error [9]	✓	✓	No	< 20ms	Moderate	✓
PWM voltage detection [3]	✓	✓	Yes	< 20ms	Low	×
Model Predictive Control [5]	✓	×	No	< 20ms	High	✓
PCA [10]	✓	×	Yes	At least 20ms	High	✓
Mean Voltage [11]	✓	×	No	< 20ms	High	✓
Proposed Method	✓	✓	No	About 20ms	Low	✓

When the exact faulty switch is known, the corresponding faulty module transfers to half-bridge operation and the dc output voltage is simultaneously compensated by the remaining healthy modules [7]. The detailed module a1 output voltage and the phase-a output voltage under healthy, fault diagnosis, and fault ride-through operation are shown in Fig. 9 for comparison.

V. CONCLUSION

For traditional CHB controllers, the responses of the inner control loops and branches are rarely used for system state monitoring. It has been pointed out that with direct synthesis of outputs from the inner dc output current regulator, harmonic output current regulator, and dc voltage balancing regulator, the controller of the CHB converter can be easily utilized as an inherent identifier to quickly locate the exact location of an open circuit faulty IGBT switch. Thus, there is no need to implement any independent identifiers or additional sensors. In addition, with the help of the modified controller and half-bridge modulation, the system can be seamlessly transferred to ride through operation with no disturbances to the grid.

Finally, the performance and characterstics of a few typical detection approaches are listed in Table III. As indicated, the proposed approach does not need any additional sensors and it features a relatively short detection process. However, similar to these approaches without using additional sensors, the rapidity of the proposed detection approach is affected by the control and circuitry parameters.

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