Design and Assessment of an Interoperable Wireless Power Transfer System Using an Impedance-Based Method

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***Abstract*—With the recently published standard, wireless charging systems for electric vehicles (EVs) are at the stage of preparing for mass market production. In order to have success, safe, and efficient wireless power transfer (WPT) public charging needs to be ensured and therefore interoperability is a key element in the design of such systems. In this article, a design methodology based on impedance planes is presented, which enables consideration of many interoperability aspects at an early stage in the design and has a high degree of flexibility. Four impedance interfaces are presented and operational boundaries and system requirements are added at each interface to establish capability ranges, which can be transferred to any other interface and used to define and assess the design space. Furthermore, this article shows how magnetic field leakage limitations can be considered in the design process. Experimental verification of the simulations is then undertaken and an example presented of how the primary electronics for a public charging use case scenario could be assessed or designed.**

***Index Terms*—Impedance planes, inductive charging, interoperability, SAE J2954, wireless power transfer (WPT).**

I. Introduction

THE rising demand in electric vehicles (EVs) comes with an increased research interest in charging infrastructure of EVs and the potential for delivering this using wireless charging or inductive power transfer (IPT). Due to the lack of a physical connection between the charging station (primary) and the car (secondary), IPT is known to be a convenient and safe way of charging EVs. Subsequently, this means that there is no defined interface for the energy transfer as in conductive charging systems. The power between the primary and secondary is transferred over the air by magnetic field coupling [1]. The coupling coefficient depends on the relative position and distance of the coils.

In order to establish IPT systems for the mass market or in public spaces, it has to be ensured that a charging station is compatible, or interoperable, with different secondary sides. As such, a primary has to cope with varying air-gaps, power classes, and battery voltage levels as well as positional offset (parking tolerance). This usually leads to a large range of operating points with coupling coefficients that can be either very high (small cars) or low (large cars with offset), which all have to be covered by the primary. This results in significant interdependence between the primary and secondary sides and, thus, complicates the design of interoperable wireless power transfer (WPT) systems.

The recently published standard J2954 from SAE [2] provides guidelines to enable interoperable WPT systems with an impedance-based approach, which was first introduced in [3] and expanded in [4] and [5]. To assess whether a secondary side [vehicle assembly (VA)] is interoperable with the reference primary, the impedances of all operating points of the secondary are presented to the primary side at the primary coil [ground assembly (GA)] interface. Those points form an impedance space and this space has to lie within the area which can be driven by the reference primary side electronics. This approach allows a high degree of independence when designing primary or secondary side electronics. Both sides can develop their electronics independent of each other, once the reference impedance area at the GA interface is matched, interoperability is ensured. Further recent work on this topic can be found in [6], [7], [8], [9], [10], and [11].

In [12], the authors presented a design method for interoperable WPT systems, which utilizes and extends this approach and allows constraints and limits of different components to be incorporated at each interface. Boundaries, such as the voltage ranges, current limits, and maximum phase angles, are used to derive a capability plane for a certain power level and describe it in terms of the real and imaginary parts of the resulting impedance at the interface to the next component. The goal is to enable a deeper understanding of the real capabilities and dependencies of different components and also to establish a design space for the primary or the secondary electronics. This article will expand on the previous work from [12].

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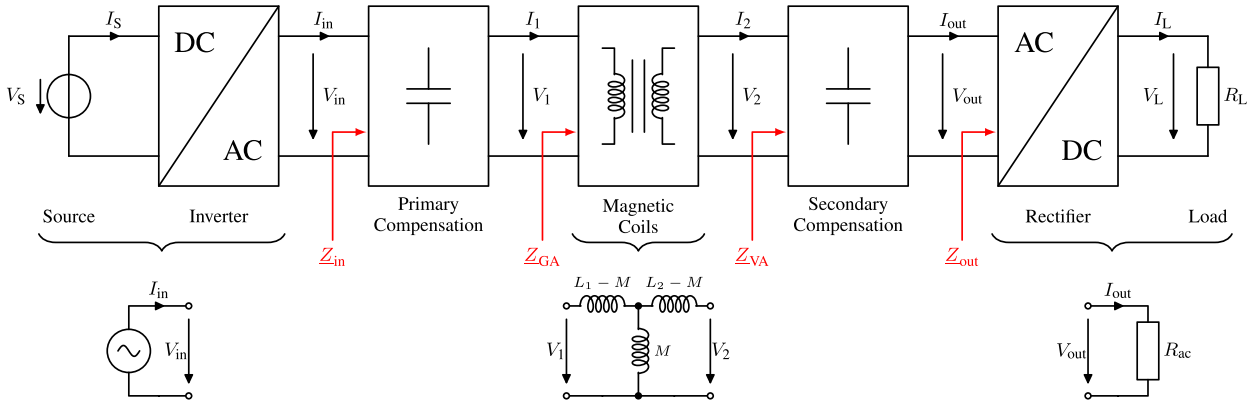


Fig. 1. Topology of a WPT system with impedance interfaces and FHA simplifications.

First, a WPT system will be described and the impedance interfaces will be defined. Second, the incorporation and transfer of various boundaries as well as power limitation aspects in the impedance planes will be presented in depth. Leakage flux limitations (e.g., by ICNIRP, see [13]) within those impedance planes will be introduced and experimental verification of the simulation models will be shown. Impedance transfer is a very powerful design tool when focusing on interoperability because of the many ways it can be used to assess the system. Subsequently, it is hard to present a general procedure or design flow. The best way to describe the design methodology is by showing applications, two of which can be found in [12] and another extensive one will be presented in Section IV, followed by a summary in Section V.

II. Fundamentals

The structure of a WPT system is shown in Fig. 1. The magnetic coils in the central block transfer power over the air-gap. Due to the application related high air-gap, WPT (or in this case IPT) systems for EV charging have low couplings which is why reactive power compensation at each coil is necessary along with operation, at or near resonance.

The topology of each block can vary, which makes a universal system level design complex. The compensation networks, for example, could consist of simple passive series compensation or a more complex *LCC* compensation on both sides (see Section IV).

The four interfaces between the inverter and rectifier, highlighted in Fig. 1, represent the impedance interfaces which are used for this design method. Common limitations in such systems are the maximum or minimum currents which can be driven by the inverter and coils, the voltage range and phase angles, which can be provided by the inverter as well as maximum coil terminal voltages. The goal of an IPT system for EV charging is to transfer a certain (active) power to the battery which further imposes requirements on the load and transferred power at each interface with the additional limitation that the grid (or PFC) only provides limited (apparent) power as well.

Based on the limitations at an interface, an area which can be driven or accessed by any component, a so called capability plane, can be derived. With circuit analysis those capability planes can be transferred to any other interface, which was first presented in [12]. The relationship between voltage and current vectors for the ports on each side can be described as

$$\begin{bmatrix} \underline{v}_1 \\ \underline{i}_1 \end{bmatrix} = \underset{\sim}{A} \cdot \begin{bmatrix} \underline{v}_2 \\ -\underline{i}_2 \end{bmatrix} \tag{1}$$

with $\underline{v} = V \cdot e^{j\varphi_v}$, $\underline{i} = I \cdot e^{j\varphi_i}$ in steady state (see [12]) whereas φ_v and φ_i define the phase angle of the impedance with $\varphi_z = \varphi_v - \varphi_i$.

Thus, with (1), any impedance $\underline{Z}_1$ defined by $\underline{v}_1$ and $\underline{i}_1$ can be expressed in terms of $\underline{v}_2$ and $\underline{i}_2$ and vice versa. The transfer matrix $\underset{\sim}{A}$ can be derived for any compensation topologies of interest as well as for the transformer representing the coils. The results for most common topologies are shown in Table I with the impedances being $\underline{Z}_{Ls1} = j\omega L_{s1}$, $\underline{Z}_{Cs1} = \frac{1}{j\omega C_{s1}}$, $\underline{Z}_{Cp1} = \frac{1}{j\omega C_{p1}}$, $\underline{Z}_{L1} = j\omega L_1$, $\underline{Z}_{L2} = j\omega L_2$, $\underline{Z}_M = j\omega M$ and $\underline{Z}_{LCC} = \underline{Z}_{Ls1} + \underline{Z}_{Cs1} + \frac{\underline{Z}_{Ls1}\underline{Z}_{Cs1}}{\underline{Z}_{Cp1}}$.

As this design method aims for insights at an early stage, the harmonics or losses of the inverter and rectifier are neglected, so the circuit can be further simplified, as shown in Fig. 1. For fundamental analysis (first harmonic approach, FHA), the inverter is replaced by a voltage source and according to [14], load and rectifier can be expressed by its ac equivalent resistance R_{ac}.

A. Inverter Capability Plane (ICP)

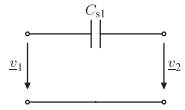
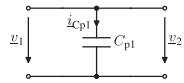
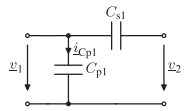
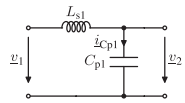
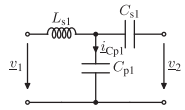
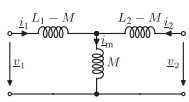
The impedance at the inverter interface[1] in Fig. 1 can be described by

$$\underline{Z}_{in} = \frac{\underline{v}_{in}}{\underline{i}_{in}} = \frac{V_{in} \cdot e^{j\varphi_v}}{I_{in} \cdot e^{j\varphi_i}} = \frac{V_{in}}{I_{in}} \cdot e^{j\varphi_z} = R_{in} + jX_{in}. \tag{2}$$

It can be highlighted that the impedance only depends on the rms values of the inverter voltage, current, and their phase angle. This leads to an area which can be addressed by the inverter and is defined by various combinations of $\underline{v}_{in}$ and $\underline{i}_{in}$ and

[1]The indices "in," "1," "2," and "out" will be used to describe the inverter, primary coil, secondary coil, and rectifier interface, respectively.

TABLE I
OVERVIEW OF TRANSFER MATRICES

Circuit topology	Two-port network matrix	Circuit topology	Two-port network matrix
	Series tuning $\underset{\sim}{A}_{\mathrm{S}} = \begin{bmatrix} 1 & \underline{Z}_{\mathrm{Cs1}} \\ 0 & 1 \end{bmatrix}$		Parallel tuning $\underset{\sim}{A}_{\mathrm{P}} = \begin{bmatrix} 1 & 0 \\ \frac{1}{\underline{Z}_{\mathrm{Cp1}}} & 1 \end{bmatrix}$
	Partial-series tuning $\underset{\sim}{A}_{\mathrm{PS}} = \begin{bmatrix} 1 & \underline{Z}_{\mathrm{Cs1}} \\ \frac{1}{\underline{Z}_{\mathrm{Cp1}}} & \frac{\underline{Z}_{\mathrm{Cs1}}}{\underline{Z}_{\mathrm{Cp1}}} + 1 \end{bmatrix}$		*LCL* tuning $\underset{\sim}{A}_{\mathrm{LCL}} = \begin{bmatrix} \frac{\underline{Z}_{\mathrm{Ls1}}}{\underline{Z}_{\mathrm{Cp1}}} + 1 & \underline{Z}_{\mathrm{Ls1}} \\ \frac{1}{\underline{Z}_{\mathrm{Cp1}}} & 1 \end{bmatrix}$
	*LCC* tuning $\underset{\sim}{A}_{\mathrm{LCC}} = \begin{bmatrix} \frac{\underline{Z}_{\mathrm{Ls1}}}{\underline{Z}_{\mathrm{Cp1}}} + 1 & \underline{Z}_{\mathrm{LCC}} \\ \frac{1}{\underline{Z}_{\mathrm{Cp1}}} & \frac{\underline{Z}_{\mathrm{Cs1}}}{\underline{Z}_{\mathrm{Cp1}}} + 1 \end{bmatrix}$		Coil-transformer $\underset{\sim}{A}_{\mathrm{L}} = \underset{\sim}{A}_{\mathrm{L1}} \cdot \underset{\sim}{A}_{\mathrm{M}} \cdot \underset{\sim}{A}_{\mathrm{L2}} = \begin{bmatrix} 1 & \underline{Z}_{\mathrm{L1}} \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} 0 & -\underline{Z}_{\mathrm{M}} \\ \frac{1}{\underline{Z}_{\mathrm{M}}} & 0 \end{bmatrix} \cdot \begin{bmatrix} 1 & \underline{Z}_{\mathrm{L2}} \\ 0 & 1 \end{bmatrix}$

subsequently by many different impedances $\underline{Z}_{\mathrm{in}}$. These values can then be transferred to the GA interface by inverting the following equation:

$$\begin{bmatrix} \underline{v}_{\mathrm{in}} \\ \underline{i}_{\mathrm{in}} \end{bmatrix} = \underset{\sim}{A} \cdot \begin{bmatrix} \underline{v}_1 \\ \underline{i}_1 \end{bmatrix}$$

where $\underset{\sim}{A}$ is chosen from Table I, depending on the compensation topology.

Equation (2) shows that this results in a maximum and minimum magnitude of the impedance where

$$Z_{\mathrm{min}} = \frac{V_{\mathrm{min}}}{I_{\mathrm{max}}}, \quad \text{and} \quad Z_{\mathrm{max}} = \frac{V_{\mathrm{max}}}{I_{\mathrm{min}}}. \tag{3}$$

In general, (2) can be rearranged and expressed in terms of real and imaginary part as

$$R^2 + X^2 = \left(\frac{V}{I}\right)^2 \tag{4}$$

which describes a circle in the complex plane with the magnitude of the impedance as radius. Consequently, the inverter limitations result in an inner and outer circle as boundaries, where only the area in between does not exceeded the limits given by the component. An example is visualized in Fig. 2 where the black shaded area lies outside of the inverter capability, restricted by its voltage and current limits from (2). Further restrictions are given by phase angle limitations, shown in red, which narrow the resulting area down to a fraction of the remaining "donut." All inverter limitations together leave the so-called ICP as a useable impedance area, which is highlighted in green.

If V_{min} or I_{min} are zero, then the inner or outer boundary disappears, because $Z_{\mathrm{min}} = 0$ or $Z_{\mathrm{max}} \to \infty$, respectively.

B. Integration of System Boundaries Into Impedance Planes

To improve the significance of the ICP, this section describes how common boundaries can be incorporated into these impedance planes in general.

1) Maximum Power: Power classes in [2] are defined by the maximum available apparent power (e.g., WPT3 = 11.1 kVA)

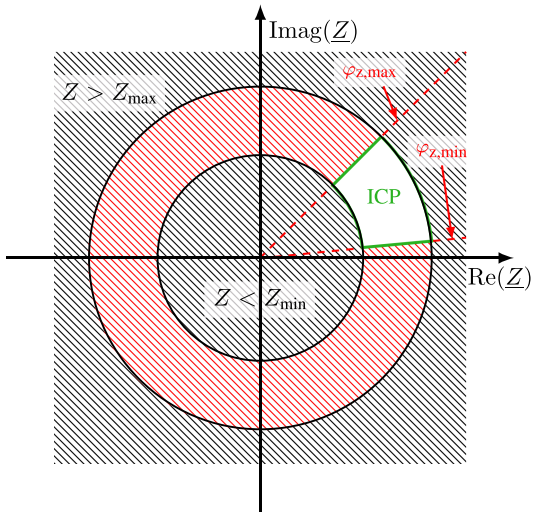


Fig. 2. ICP (green) restricted by voltage and current boundaries (black and shaded black) as well as phase angle limitations (red and shaded red).

and this is often also the limit which can be provided by the grid. The equations for the apparent power

$$\underline{S} = \underline{v} \cdot \underline{i}^* = \frac{\underline{v}^2}{\underline{Z}} = \underline{Z} \cdot \underline{i}^2 \tag{5}$$

$$S = |\underline{S}| = I^2 \cdot |\underline{Z}| = \frac{U^2}{|\underline{Z}|} \tag{6}$$

can also be expressed in circle equation form in the complex impedance plane where (6) leads to

$$R^2 + X^2 = \left(\frac{V^2}{S}\right)^2 \tag{7}$$

and

$$R^2 + X^2 = \left(\frac{S}{I^2}\right)^2. \tag{8}$$

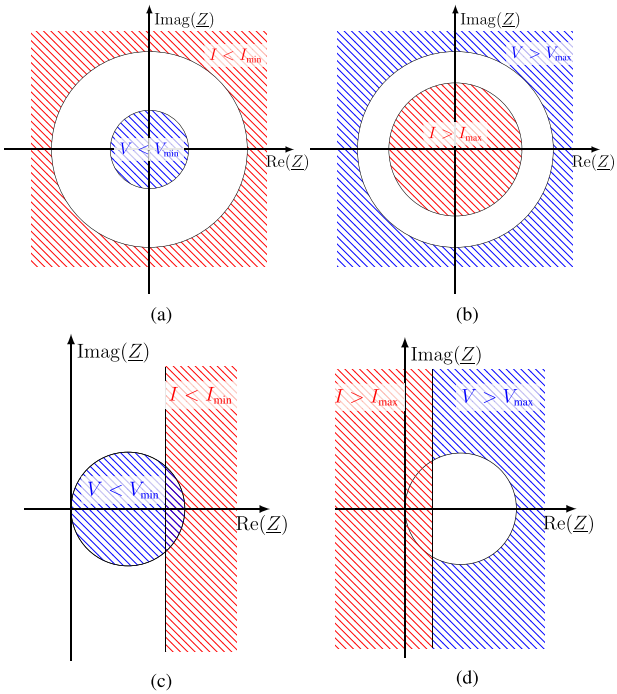


Fig. 3. Impedance planes (white) for different apparent and active power restrictions caused by component voltage (blue) and current (red) limitations, (a) $S \leq S_{\max}$, (b) $S \geq S_{\min}$, (c) $P \leq P_{\max}$, and (d) $P \geq P_{\min}$.

Similar to the previous section, this results in two circles with the inner limitation set by $Z_{\min} = V_{\min}^2/S_{\max}$ and the outer limitation by $Z_{\max} = S_{\max}/I_{\min}^2$. This is visualized in Fig. 3(a), where the red shaded area represents the restrictions by the current and the blue area is the one restraint by the voltage. It has to be emphasized that those values may differ from the boundaries provided by the inverter interface.

If apparent power is limited to a maximum rated value, active and reactive power are also limited to the same value. To study the effects of a given $P_{\max}$ and $Q_{\max}$, (5) can be split into real and imaginary part

$$\underline{S} = R \cdot \underline{i}^2 + j \cdot X\underline{i}^2 = P + jQ \tag{9}$$

$$\underline{S} = \frac{\underline{v}^2 \cdot R}{R^2 + X^2} + j \cdot \frac{\underline{v}^2 \cdot X}{R^2 + X^2} = P + jQ. \tag{10}$$

When looking at maximum active power[2] $P_{\max}$, (9) yields

$$R = \frac{P}{I^2} \tag{11}$$

and this is maximized for $P_{\max}/I_{\min}^2$. This is the maximum real part of the impedance which cannot be exceeded and is shown as the red area in Fig. 3(c).

In terms of maximum active power and voltage limitations, (10) results in

$$\left(R - \frac{1}{2}\frac{V^2}{P}\right)^2 + X^2 = \left(\frac{1}{2}\frac{V^2}{P}\right)^2 \tag{12}$$

[2]Following analysis focuses on active power because reactive power is usually not directly restricted or may be less important in real operation. Nevertheless, similar conclusions can be derived for reactive power limitations.

which results in a circle with the smallest radius $0.5V_{\min}^2/P_{\max}$ and a real part offset with the same value. This is marked as the blue area in Fig. 3(c). Again, these boundaries diminish if one of both $V_{\min}$ or $I_{\min}$ is zero.

If $S_{\max} = P_{\max}$, then the restrictions from (9) and (10) are already included in (7) and (8) or Fig. 3(a), respectively. Nevertheless, the approach of this work is to provide the possibility of imposing the boundaries as general as possible since requirements may differ for each application.

2) Minimum Power: Usually, the purpose of a charging station is to transfer a certain amount of active power, which leads to another boundary for the impedance planes. The same equations as in the previous section can be applied, with the results for the apparent power shown in Fig. 3(b) and for the active power in Fig. 3(d).

In this case, the maximum values of the component voltage and current limitations define the boundaries and the relations are reversed. $I_{\max}$ now provides the inner circle [see Fig. 3(b)] or left side boundary [see Fig. 3(d)] and now the outside of the $V_{\max}$ circle is the restricted area (blue), which represents a severe restriction especially for the $P \geq P_{\min}$ case.

3) Voltage, Current, and Phase Angle Limitations: When the impedance planes are directly related to a certain power level such as $P = P_{\text{out}}$ further boundaries may emerge from the voltage and current. With $P = V \cdot I$ the left and right boundaries for the real part of the impedance plane can be calculated as

$$R_{\min,I} = \frac{P_{\text{out}}}{I_{\max}^2}, \quad R_{\max,I} = \frac{P_{\text{out}}}{I_{\min}^2} \tag{13}$$

$$R_{\min,V} = \frac{V_{\min}^2}{P_{\text{out}}}, \quad R_{\max,V} = \frac{V_{\max}^2}{P_{\text{out}}} \tag{14}$$

where the larger of both lower limits and the smaller of both upper limits represent the impedance plane boundaries.

Phase angle limitations are not directly affecting the transfer of active power, but they affect the required apparent power with $S = P\cos(\varphi)$ and the impedance with $\underline{Z} = Z \cdot e^{j\varphi}$ and have to be considered if there are respective limitations. Their effects were discussed in both previous sections and in Section II-A.

All discussed limitations together result in an ICP, showed in green in Fig. 4. In this impedance, area a minimum active power transfer of $P_{\text{out,min}}$ is now ensured whilst never exceeding voltage, current and phase angle limitations from the inverter and never requiring more apparent (grid) power than $S_{\text{in,max}}$.

C. Coil Capability Plane (CCP)—Consideration of Magnetics

The magnetic coils used for WPT are usually only limited in maximum voltage and current. Since there are no lower limitations for voltage and current, a minimum active power $P \geq P_{\min}$ is required to create a (meaningful) CCP. It can be created similar to the ICP with the methods from the previous section and will have a shape like the one in Fig. 3(d). The CCP is very large since the volt-amperes from the magnetic coils are typically high. An example for a primary coil on the GA interface for $P_{\text{out}} = 10$ kW is shown in Fig. 5(a) in blue.

To evaluate the magnetic coupling between two coils, the VA CCP on the GA interface or vice versa is of interest, since this

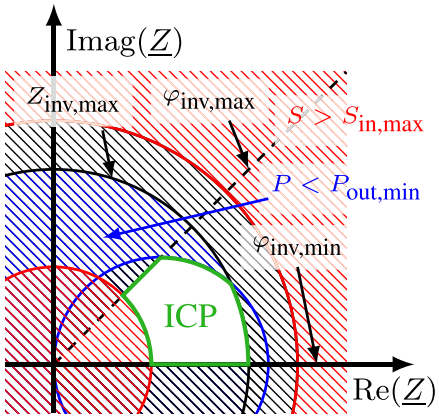


Fig. 4. ICP (green) for delivering $P \geq P_{\text{out,min}}$ with a maximum apparent power limitation (red) and inverter boundaries (black).

presents the coil capability at the other side of the air-gap. Due to the low coupling in WPT systems (because of high ground clearance) the large CCP from the VA coil transferred onto the GA interface becomes very small, which can be seen in Fig. 5(a). In Fig. 5(b), a closer look of the black square from Fig. 5(a) is provided. The same VA CCP is transferred to the GA interface (by use of (1) and $\underset{\sim}{A}_L$ from Table I, see [12]) for different couplings and it can be seen that the coupling factor k directly relates to the size of the VA CCP, which shrinks drastically with lower coupling[3].

A closer look at the matrix $\underset{\sim}{A}_L$ from Table I shows it can be split into three parts, each one only affected by L_1, L_2, or M, respectively. The matrices $\underset{\sim}{A}_{L1}$ and $\underset{\sim}{A}_{L2}$ are upper triangle matrices and represent (like series tuning) a simple upwards or downwards shift of the impedance plane in the complex plane, depending on the sign of the impedance (capacitive or inductive). As such, the shrinking effect mostly relates to the mutual inductance M and since the variations in L_1 and L_2 are usually low (especially at high air-gaps), it is mainly due to the coupling factor k.

If this transfer of VA CCPs to the GA interface (or vice versa) is repeated for many secondaries or for one secondary at many different positions and air-gaps, an interoperability zone can be derived in which safe operation at all positions or all coil combinations (within the coil boundaries) can be ensured. As another result of this process, a minimum coupling factor k_{min} for the coils (or coil sets) in order to be interoperable can be derived. The interoperability zone for Fig. 5(b) is shown in Fig. 5(c). It can be seen in Fig. 5(b) that the case of $k = 0.08$ does not overlap with the GA CCP and hence this VA coil cannot operate with the GA coil under this condition or coupling. For this example it was determined that the lowest allowed coupling factor in order to overlap with the GA CCP has to be $k_{\text{min}} = 0.085$.

This approach allows an evaluation of different magnetic coils and their coupling by comparing the resulting impedance planes, without the need to consider electronics. An example of this application was first presented in [12].

D. Integration of Leakage Flux Limitations Into Impedance Planes

Due to EMF exposure and safety reasons another requirement demanded of IPT systems for EV charging is for the magnetic leakage flux density to stay below the reference value $B_{\text{max}} = 15\ \mu\text{T}$ around the vehicle [2], [13]. In order to comply with this, measurements and simulations of the maximum magnetic flux density are conducted in XZ or YZ planes at an 800 mm distance (in x- or y-direction) from the secondary coil center which is where the vehicle body supposedly ends, and hence, this is the area of interest for safety [15], [16], [17], [18].

Typically, this is accomplished with an additional finite-element-method (FEM) simulation step by using the determined coil currents from the designed operating point to validate that the system stays below the guidelines [19], [20], [21], [22], [23], [24], [25]. In this section, an approach is presented with which leakage flux information of the coils can be considered in the impedance planes without requiring an additional FEM simulation.

The flux density depends on the coil currents I_1 and I_2 but for systems with small secondaries, the primary is the main contributor of leakage flux [16], [26]. This can be confirmed with Fig. 6(a) where the magnetic leakage flux of the system from the following section for different coil currents is shown.

If ferrite saturation effects are neglected, which is a feasible assumption for the currents at the power classes $P \leq 10\,\text{kW}$,[4] the leakage flux B_{max} is linearly proportional to I_1. The graph from Fig. 6(a) can now be used to determine the maximum allowed coil current $I_{B\text{max}}$ for a certain B_{max} limitation which produces a new coil current limit for the impedance plane at the GA interface and hence a new $R_{\text{min},I}$, see (13).

This was done for $B_{\text{max}} = 15\ \mu\text{T}$ for the system from Fig. 6(a). The resulting $I_{B\text{max}}$ for different air-gaps is shown in Fig. 6(b) for nominal (solid red) and offset (dashed red) positions. Fig. 6(b) also shows the required primary current in order to transfer $P_{\text{out}} = 10$ kW for different air-gaps (series–series tuned). It can be seen that the allowed primary current is very high at low air-gaps but drastically reduces with offset as well as with increasing air-gap. In some cases the required primary current cannot comply with the EMF exposure limitations.[5]

For the CCP, this now means that the minimum allowed real part is dependent on coil positioning and thus the coupling factor k. Subsequently, this may change the k_{min} from Section II-C as shown in Fig. 6(c). The new interoperability zone now also ensures that the desired leakage limitations are satisfied. In order to achieve this, only the relations of $B_{\text{max}} = f(I_1)$ and $B_{\text{max}} = f(I_2)$ are required. Those can be obtained in an additional post

[3]The coil boundaries were set to $V_{1,\text{max}} = V_{2,\text{max}} = 2.5$ kV and $I_{1,\text{max}} = I_{2,\text{max}} = 75$ A for all cases.

[4]The smallest nonbrital ferrite sizes are normally big enough at this power level.

[5]Usually there is another limitation for the coil currents, caused by the litz-wire capabilities which depend on the material as well as winding turns and should be considered as well.

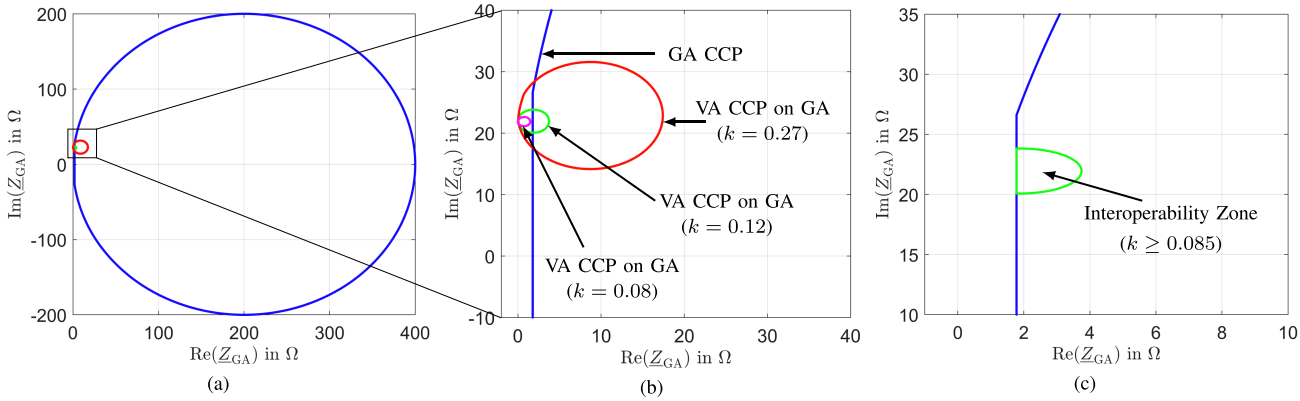


Fig. 5. GA CCP (blue) for $P_{\text{out}} = 10$ kW with VA CCPs (red, green, and magenta) transferred to the GA interface under different conditions. (a) Total view, (b) detailed view of the VA CCPs for different couplings, and (c) resulting interoperability zone for k_{min}.

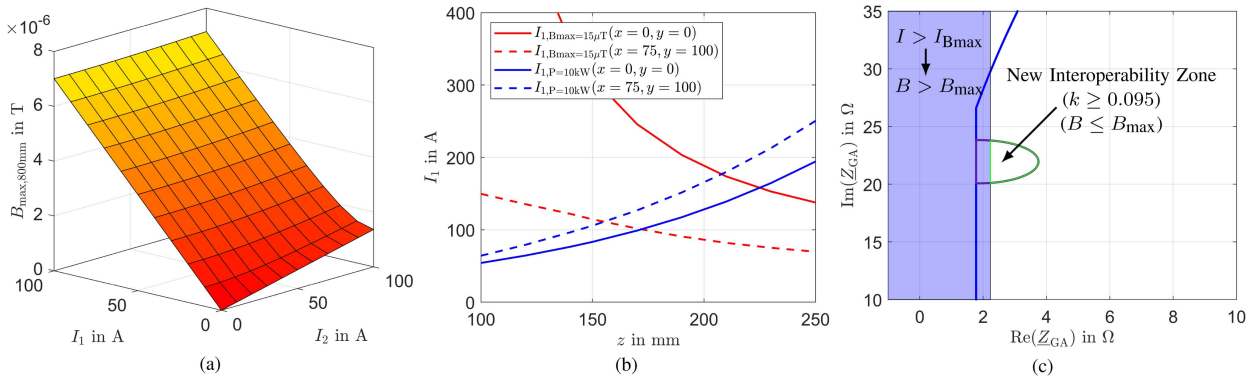


Fig. 6. Integration of leakage flux effects into the CCP. (a) B_{max} as a function of I_1 and I_2, (b) maximum allowed primary coil current for $B < 15$ μT (red) and required I_1 for $P_{\text{out}} = 10$ kW (blue), and (c) effects of leakage consideration on the CCP with a new interoperability zone and k_{min}.

processing step during the initial FEM simulations which are necessary for obtaining the inductances of the coils.

It has to be emphasized that the proposed method also works for systems with larger secondaries, when the leakage contribution of I_2 is not negligible. The same procedure can be applied with the difference that $I_{B\text{max}}$ at the GA interface is also a function of I_2. Fig. 7(a) shows the leakage flux density similar to Fig. 6(a) but with identical coils on the primary and secondary.[6] It can be seen that the influence of I_2 is increased. As a consequence, the maximum allowed primary current cannot be described by one curve as was done in Fig. 6(b). It now changes with different I_2 values as shown in Fig. 7(b). Since I_2 is usually known in a fully determined circuit, this does not pose a problem. Otherwise a worst case assumption for I_2 can be conducted as well. Further information can be found in [27] where the method was applied to a 50 kW matched system.

III. Experimental Verification

It is not feasible to set up experiments for all operating points from an impedance plane. Therefore, measurements were conducted for one known system in order to validate the simulations in general, so that they can be used to apply the presented method in the following section.

A. System and Measurements

The system which was used for the experimental verification, consists of two circular coils similar to the WPT3 Z2 system from [2]. The circuit of the measurement setup is depicted in Fig. 8. The switching frequency was set to $f_s = 85$ kHz and the input and output voltages were fixed to $V_{\text{in}} = 450$ V and $V_{\text{bat}} = 420$ V, respectively. The compensation networks consist of an *LCC*-topology on the primary and a partial–series compensation on the secondary. A boost converter was used on the secondary in order to regulate the output voltage. All measurements were conducted with a car mimic plate (aluminum shield, (800×800×1) mm) on top of the secondary and a picture of the measurement setup in the lab is shown in Fig. 9.

Two operating points were set up and the inductances, leakage values and input and output voltages and currents were measured with the results shown in Table II. The difference between both operating points was the coil position, which first was set up to nominal position, $(x, y, z) = (0, 0, 210)$ mm and in the second operating point at offset position which is $(x, y, z) = (75, 100, 210)$ mm. In order to keep the output voltage constant the duty cycle of the boost converter was set to $D = 0.23$ at nominal and $D = 0$ in offset position. Fig. 10(a) shows the

[6]The primary coil from the following section was used with the same air-gap as in Fig. 6(a).

TABLE II
COMPARISON BETWEEN MEASUREMENTS AND SIMULATIONS

	L_1 [µH]	L_2 [µH]	k	$B_{\text{max,800mm}}$ [µH]	$B_{\text{max,1000mm}}$ [µH]	I_1 [A]	I_2 [A]	I_{in} [A]	I_{out} [A]	P_{in} [kW]	P_{out} [kW]	P_{loss} [kW]	$\eta_{\text{dc-dc}}$ [%]
Nominal Position $\rightarrow (x, y, z) = (0, 0, 210)$ mm, $V_{\text{in}} = 450$ V, $V_{\text{bat}} = 420$ V, $D = 0.23$													
Measurement	38.16	43.41	0.116	5.9	2.5	75.5	59.2	25.0	24.6	11.3	10.4	0.9	92.0
Simulation	38.03	41.03	0.122	6.7 (6.68)	2.6 (2.63)	71.8	66.9	25.7	26.3	11.6	11.1	0.5	95.7
Offset Position $\rightarrow (x, y, z) = (75, 100, 210)$ mm, $V_{\text{in}} = 450$ V, $V_{\text{bat}} = 420$ V, $D = 0$													
Measurement	38.78	43.44	0.088	13.6	5.2	77.5	68.3	25.0	24.5	11.3	10.4	0.9	92.0
Simulation	38.56	40.99	0.089	14.3 (14.17)	5.1 (5.04)	75.6	76.8	25.1	25.5	11.2	10.7	0.5	95.6

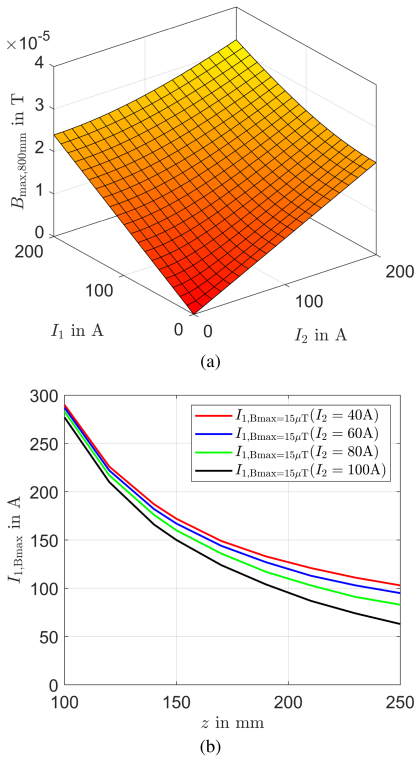


Fig. 7. Leakage flux effects for a matched coil system. (a) B_{max} as a function of I_1 and I_2 and (b) maximum allowed primary coil current for $B < 15$ μT for different values of I_2.

captured waveforms of the coil currents and inverter bridge and Fig. 10(b) shows a screenshot of the measured output values, both for the nominal operating point.

The probes for the leakage measurement were placed at the same position where $B = B_{\text{max}}$ occurred in the FEM simulation, as shown in Fig. 11.

B. Simulation and Verification

For comparison, the same system and similar operating points were set up in the simulations and the results are also shown in Table II. Ansys Electromagnetics was used for the FEM simulations and the coil models are shown in Fig. 12. For the circuit simulations PLECS was used.

To obtain the maximum leakage values with their exact position (which was necessary for the measurements), the measured currents of both operating points were set in another FEM simulation as shown in Fig. 11 and the results are first listed in Table II. The second value shown in brackets was derived by using the simplified scaling method described in Section II-D. The values are almost identical, which confirms that the simplified approach can be used in this case.

The boost converter can either be modeled (in circuit simulations) or included into the R_{ac} load (first harmonic approach as shown in Fig. 1). The formula is given in [28]

$$R_{\text{ac}} = \frac{\pi^2}{8}(1 - D)^2 R_L. \tag{15}$$

The comparison between measured and simulated values shows very good agreement with the simulations and with the measurements in general.

There are slight deviations in the secondary currents, which are caused by the rectifier. The thermal and ohmic losses of the diodes were not modeled and they account for around 3.5% of the efficiency and also explain the slightly higher current in the simulations.

Furthermore, the simulated leakage values at 800 mm distance are slightly higher than the measured ones. This can be explained by the fact that it is very hard to put the probe in the exact same point as in the simulation as well as set up the coils into the exact same position, which also explains the slight offset in L_2. Especially at low leakage, capturing the correct leakage flux is difficult given that a manufacturing margin is present as well.

IV. APPLICATION OF THE IMPEDANCE PLANE METHOD

To demonstrate how the described method from Section II can be used, this sections applies the method to a use-case where the interoperability of the primary coil from the previous section is investigated for use in public charging spaces.

A. Use-Case Scenario and System Boundaries

To assess whether a primary side can be used for public charging, the interoperability of this primary should be investigated. To demonstrate how this can be accomplished with the use of impedance planes, a scenario was created where the primary side has to operate with four different secondaries, which each differ either in their respective air-gap or tuning topology (cases 1–4). This yields four coil combinations with different couplings[7] and

[7]The secondary coil for cases 1 and 2 is similar to the one from Section III whereas cases 3 and 4 use the WPT3 Z3 system from [2] with the respective

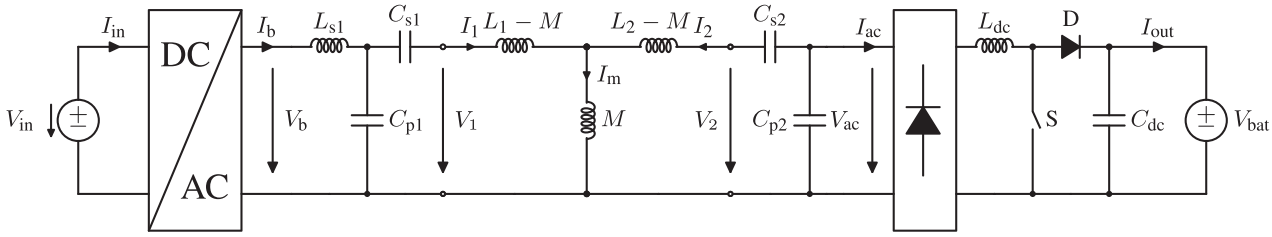


Fig. 8. Circuit topology of the measured system.

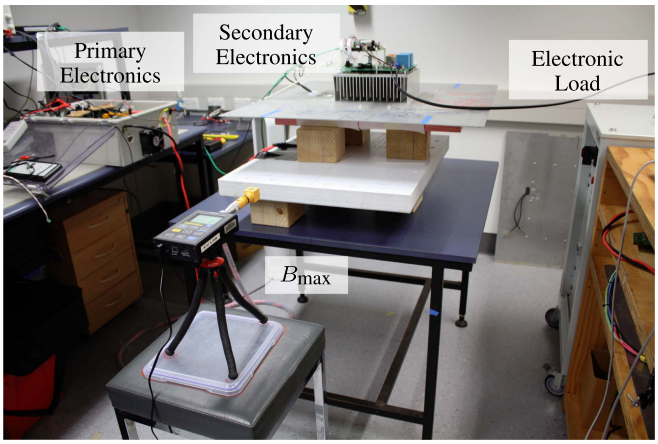
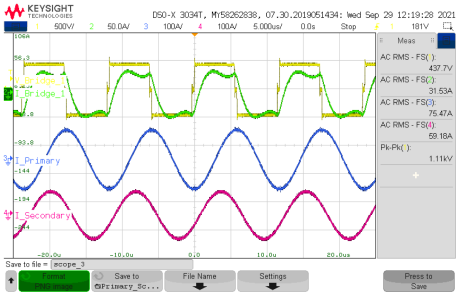
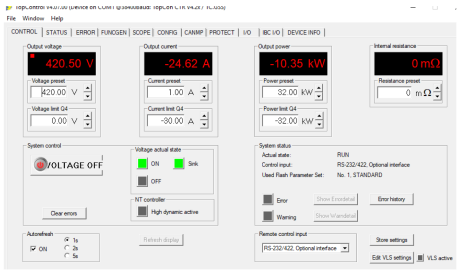


Fig. 9. Lab leakage measurement setup.



(a)



(b)

Fig. 10. Scopes of the circuit measurements for the nominal position, (a) waveforms of coil currents and inverter bridge and (b) captured output values.

the schematics of the described use-case is presented in Fig. 13.

rectifier. The rectifier can be simplified and included into an equivalent load as shown in [5].

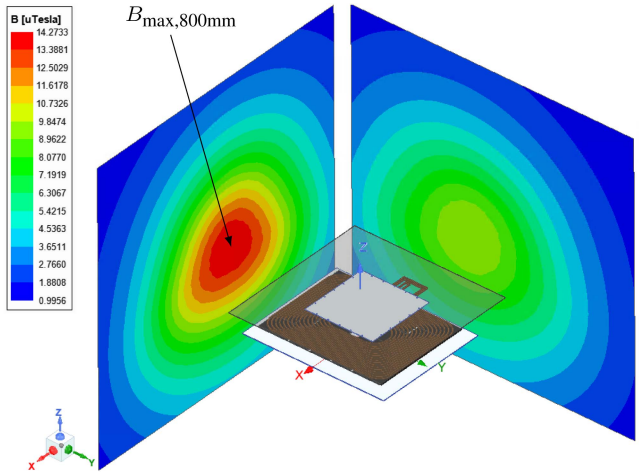


Fig. 11. FEM simulation for obtaining the leakage flux values.

Case 2 resembles the experimentally validated system from the previous Section III.

Each case is considered at its air-gap (z height) and its nominal as well as offset ($x = 75$ mm and $y = 100$ mm) position, which ultimately results in eight different CCPs presented at the GA interface (by impedance transfer as shown in Section II-C).

Battery voltage variations are also considered which result in different loads and, thus, different operating points presented to the GA.

The goal of the use-case scenario is now to compare two different sets of primary electronics consisting of the same inverter with different tuning, case A and case B in Fig. 13, and to assess which one is better suited for working with the primary coil as a public charging station under those requirements.

The system boundaries which were set for this example are summarized in Table III.[8]

Information on the tuning values as well as the equations on how the values were calculated can be found in the appendix. Perfect tuning is not the scope of this use-case and thus is not discussed in depth. The approach of this use-case is to present four secondaries to the primary and analyze the primary capabilities even if the secondaries are detuned with which a public charging station may need to cope nonetheless.

[8]The boundaries were estimated since the use-case was created for this example.

TABLE III
SYSTEM BOUNDARIES FOR THE USE-CASE SCENARIO

Grid/inverter	Coils	Rectifier/load
$S_{\text{in,max}} = 11.1$ kVA	$V_{1,\text{max}} = V_{2,\text{max}} = 2.5$ kV	$V_{\text{bat}} = (280 - 420)$ V
$V_{\text{in}} = (50 - 500)$ V	$(I_{1,\text{max}}, I_{2,\text{max}}) = (100, 100)$ A	$P_{\text{out}} = 10$ kW
$I_{\text{in}} = (5 - 60)$ A	$(x, y, z)_{\text{min}} = (0, 0, 140)$ mm	$R_{\text{ac}} = 8/\pi^2 \cdot V_{\text{bat}}^2/P_{\text{out}}$
$\varphi_{\text{in}} = (0 - 45)$ deg	$(x, y, z)_{\text{max}} = (75, 100, 250)$ mm	$R_{\text{ac2}} = \pi^2/8 \cdot V_{\text{bat}}^2/P_{\text{out}}$
	$B_{\text{max}} = 15$ µT	$R_{\text{ac3}} = (X_{\text{rect}}^2 + R_{\text{ac}}^2)/R_{\text{ac}}$

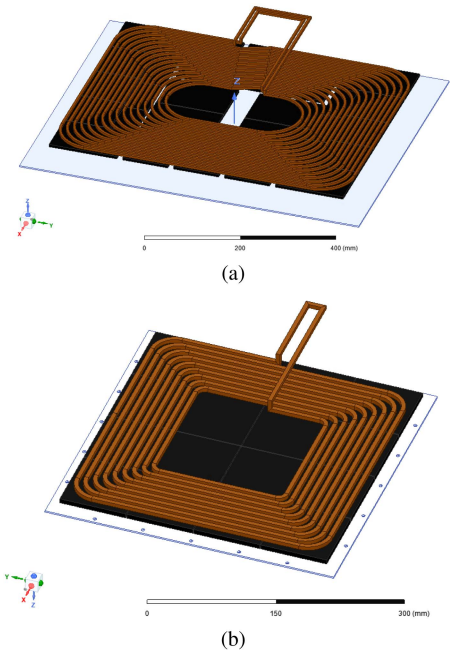


Fig. 12. FEM simulation models of the coils, (a) primary coil and (b) secondary coil. The car mimic aluminum shield is not shown.

With the circuits fully parameterized, the impedance planes and operating points for all cases can be derived.

B. Process Flowchart of the Use-Case

In Fig. 14, the flowchart of the use-case goal is shown. The blue colored steps describe the electronic side of the process in order to derive the ICP, whereas the green steps describe the procedure related to the magnetics in order to get the CCPs. The inverter boundaries and power limitations can be implemented with the procedures described in Section II to derive the ICP and has to be repeated for each inverter under investigation, in this case two times for case A and case B. With the primary tuning topology, the transfer matrices $\underset{\sim}{A}_S$ and $\underset{\sim}{A}_{LCC}$ can be determined and each ICP can be transferred to the GA interface.

With the inductances as an input, each VA CCP can be derived for the given power level as shown in Section II-C. After imposing the boundaries on the CCP, the impedance plane can be transferred to the GA interface by using the corresponding $\underset{\sim}{A}_L$ where the primary side as well as the leakage boundaries have to be imposed as described in Section II-D. This has to be repeated for each offset position and each secondary coil in consideration.

As a third process, the operating points which are dependent of the power level, battery voltage, and frequency have to be calculated and transferred back to the GA interface by using the transfer matrices defined by each secondary tuning topology and the coil transfer matrices of each coil position and secondary coil.

The ICPs under investigation, the considered CCPs and their respective operating points from the use-case conditions can now be combined at the GA interface and directly compared or assessed. Steps 1–7 were done for each secondary coil separately and the results are shown in Fig. 15(a)–(d) whereas all results together are visualized in Fig. 15(e) (step 8).

As shown in Fig. 14, these results can now be used to assess the ICPs, and hence, the inverters with their tuning topologies or the resulting combination of ICPs and CCPs (if existing) can be used as a design space for a new set of primary electronics.

C. Results and Discussion

The results of the described process for each coil are shown in Fig. 15. In each figure, the red and green planes represent the CCP at nominal and offset position, respectively. The operating points are also shown for the nominal (black) and offset (magenta) position. The ICP of case B, the series tuned ICP$_S$ is shown in purple and the ICP$_{LCC}$ of case A in blue.

It can be seen that although providing a much larger ICP, less operating points can be driven with case B compared to case A. Here the operating points for the offset positions lie mostly outside of the ICP$_S$. The reason for this can be found in the current limitation from the inverter. The current which passes through the inverter is similar to the coil current when series tuning is used and the required primary coil currents are too high for case B. If the inverter coil limitation is increased, the left side boundary of the ICP$_S$ moves to the left.

Furthermore, it can be seen that the coupling quality is sufficient for all cases since all nominal (black) operating points lie within their correspondent CCP (red) which also applies for the offset cases (magenta operating points in green CCP) even though cases 2 and 3 provide very small CCPs.

Another observation is that the operating points of the secondary *LCC* tuning (cases 3 and 4) are grouped very closely together at the GA interface. This simplifies the design of the primary side electronics since less area has to be covered. Additionally, closely grouped operating points pose less stress

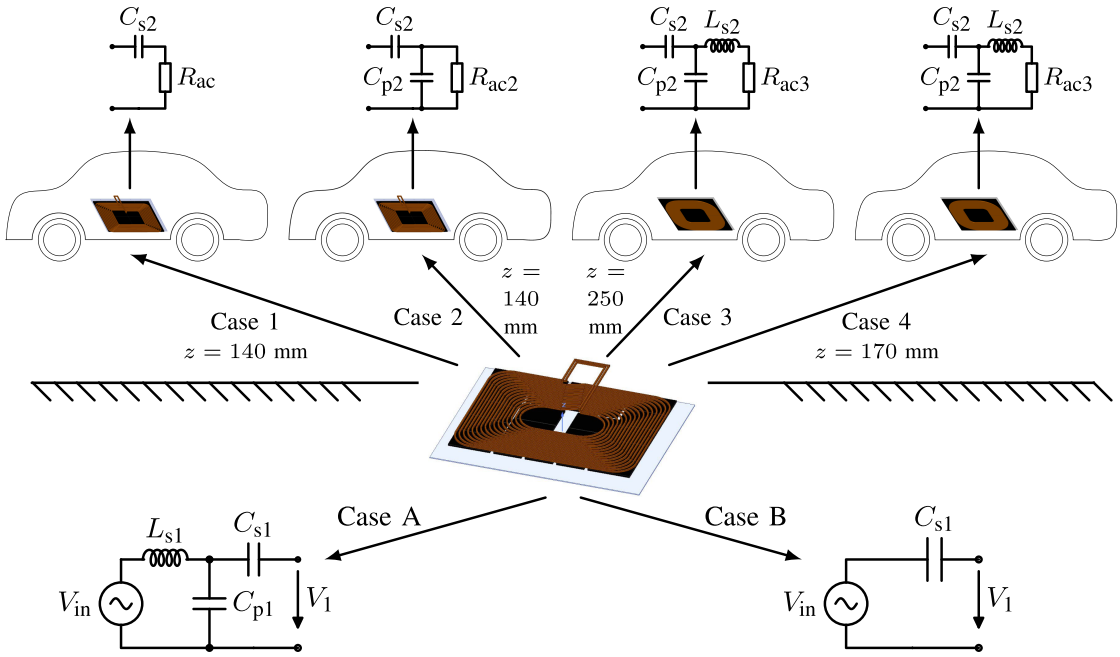


Fig. 13. Overview of the use-case scenario. The electronics of case A or case B are connected to the primary coil and four different cars are parking over this charging station and should be charged under different parking and battery voltage conditions with $P_{out} = 10$ kW.

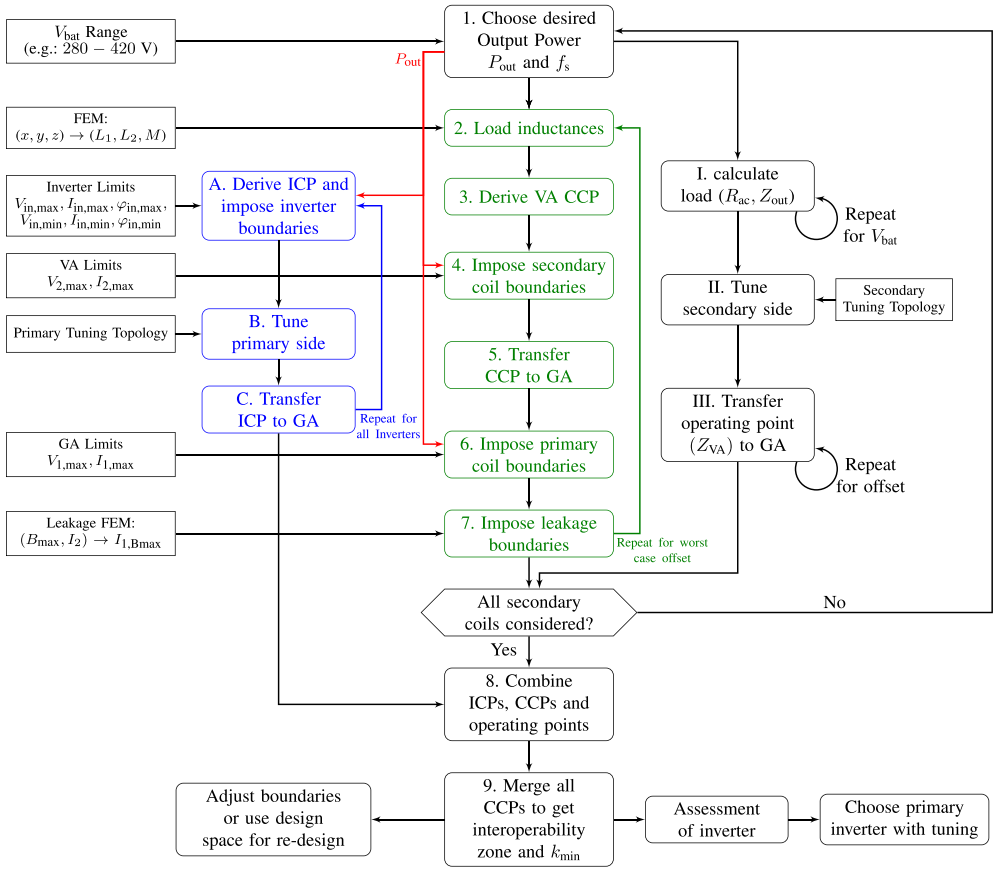


Fig. 14. Flowcharts of the public charging use-case.

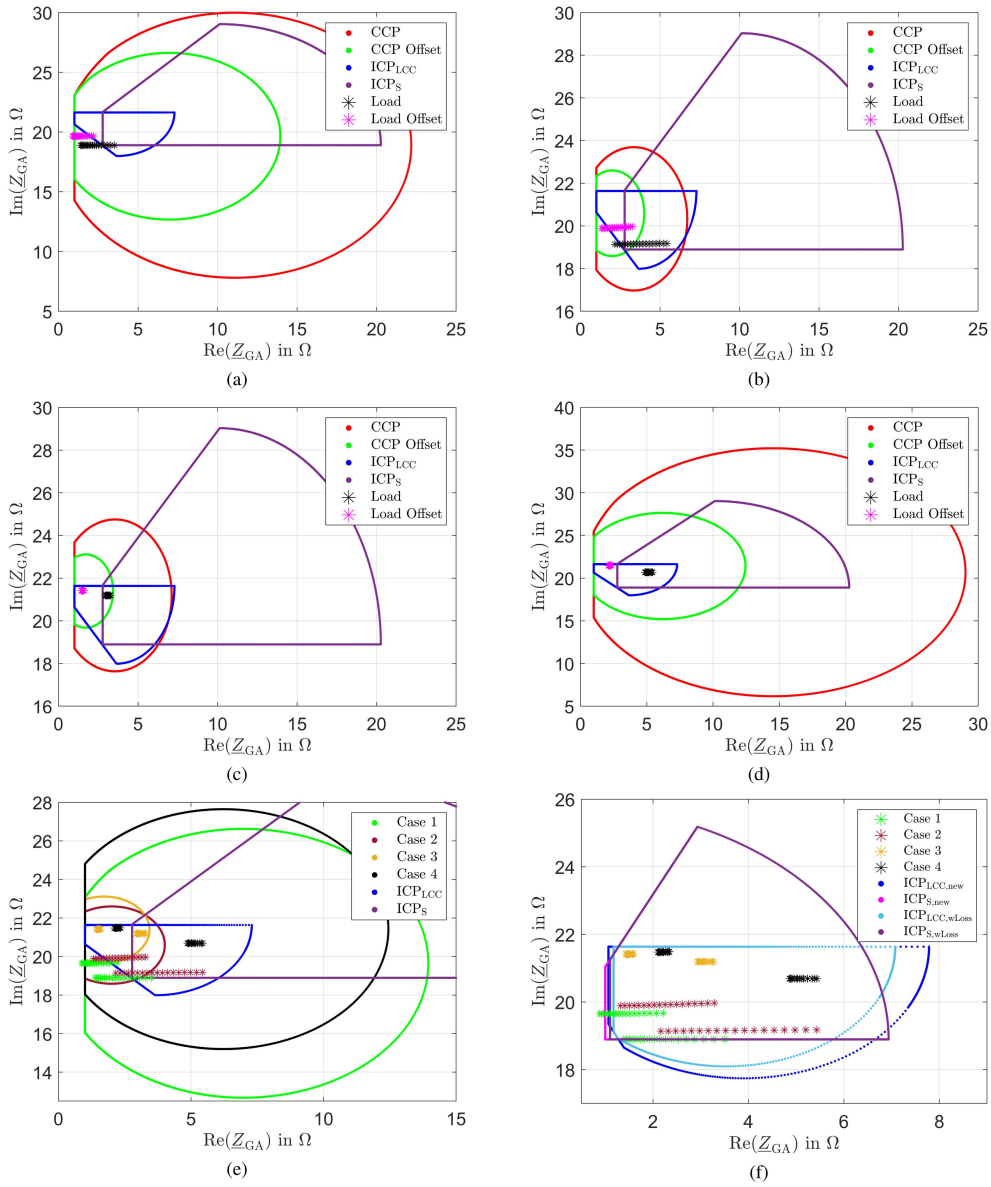


Fig. 15. Results of the process flowchart from Fig. 14 for (a)–(d) each secondary case (case 1–4), (e) all cases and (f) new ICPs.

on the electronics, lead to a more tolerant system and hence are preferable. Another design goal should be to create CCPs, which have a small buffer to the operating points or vice versa. If most operating points are close to the left side CCP boundary, as it is in case 1–3, the system always operates near the coil current limitation. This means that the real system may exceed the leakage limitation given the assumptions made for this use-case (FHA) and the comparison of measurement and results from Section III, which show slightly higher primary currents in the measurements.

Since the magnetics do not pose much of a problem, interoperability in this case can be ensured for both cases A and B if all operating points lie within their ICPs. In order to achieve this, the tunings and boundaries of both cases were adjusted and the redesigned ICP$_S$ and ICP$_{LCC}$ are shown in Fig. 15(f) and their boundaries are shown in the appendix. By increasing the allowed current and the phase angle, the ICP$_S$ now reaches almost all operating points. It is not required for a charging station to deliver rated power at the rectifier interface in all cases [2], thus the operating points from case 1 which are still outside the ICP can be reached if the required output power is reduced slightly. The initial ICP$_{LCC}$ already covered almost all operating points, so in this case only the allowed phase angle and the tuning had to be adjusted slightly to ensure interoperability.

There are many other possibilities to approach this use-case in order to improve a case or achieve interoperability. The interoperability zone of all coil combinations could be used as a ultimate design space since it is guaranteed to stay within the magnetic and leakage limits. If both primary and secondary side electronics are designed to match the CCP, interoperability is

ensured. The same applies for active tuning designs which could be designed to move all operating points (secondary tuning) or the ICP (primary tuning) into the CCP.

Another approach could be to assess the system and derive limitations for its interoperability. For instance, the consequences of the assessment could be to only allow coils with a coupling factor higher than a certain k_{min}, only allow lower air-gaps classes (e.g., only Z1 can be driven) or reduce the transferred power (e.g., the system is only capable to provide WPT1-2). Some of those constraints lead to the conclusion that the system may not be suited for public charging but could be reasonably good for cheaper or fleet based systems.

With slight changes in the flowchart from Fig. 14, the proposed method can also be used to assess coupler geometries for given electronics. An evaluation can be conducted by comparing the resulting CCP sizes, interoperability zones and $I_{B\text{max}}$-curves of all combined couplers.

It has to be emphasized that these results were obtained without the consideration of inverter (switching) losses and rectifier losses as well as harmonics. Those losses heavily depend on the actual circuit and the operating point itself. Hence, it is quite difficult to derive exact losses for a variety of operating points. A conservative loss estimation of $P_{\text{loss}} = 10\% \cdot P_{\text{out}}$ was done and applied to the redesigned ICPs from Fig. 15(f). The new ICPs are shown in light blue and violet. It can be seen that the ICPs decrease since the inverter has to cover the losses and that this only affects a few operating points from case 1 which cannot be driven by the ICP$_{S,w\text{Loss}}$ anymore. A thorough study of losses, harmonics, and their impact on ICPs and CCPs is important for good quality results and part of our future work.

TABLE IV
OVERVIEW OF TUNING EQUATIONS FOR SECTION IV

Topology	$C_{\text{s1,s2}}$	$C_{\text{p1,p2}}$	$L_{\text{s1,s2}}$	$X_{1,2}$
Series	$\frac{1}{\omega^2 L_{1,2}}$	–	–	$\omega L_{1,2}$
Partial-series	$\frac{1}{\omega^2 L_{1,2} - \omega X_{1,2}}$	$\frac{1}{\omega X_{1,2}}$	–	$\omega L_{1,2} - \frac{1}{\omega C_{\text{s1,s2}}}$
LCC	$\frac{1}{\omega^2 L_{1,2} - \omega X_{1,2}}$	$\frac{1}{\omega X_{1,2}}$	$\frac{X_{1,2}}{\omega}$	$\omega L_{1,2} - \frac{1}{\omega C_{\text{s1,s2}}}$

TABLE V
OVERVIEW OF TUNING VALUES FOR SECTION IV

Case	X_1	X_2
S–S	ωL_1	ωL_2
S–PS	ωL_1	5.5
S–*LCC*1	ωL_1	7
S–*LCC*2	ωL_1	11
LCC–S	4.5	ωL_2
LCC–PS	4.5	5.5
LCC–*LCC*1	4.5	7
LCC–*LCC*2	4.5	11

TABLE VI
NEW INVERTER BOUNDARIES

Inverter	
Case A	Case B
$V_{\text{in}} = (50 - 500)$ V $I_{\text{in}} = (5 - 60)$ A $\varphi_{\text{in}} = (0 - 65)$ deg $X_{1,\text{new}} = 4.65$	$V_{\text{in}} = (50 - 500)$ V $I_{\text{in}} = (40 - 100)$ A $\varphi_{\text{in}} = (0 - 65)$ deg $X_{1,\text{new}} = \omega L_1$

V. SUMMARY

A design method for WPT systems using impedance planes was presented. This method enables diverse interoperability considerations at different IPT design stages due its general approach. Operational system boundaries from power electronics and magnetics are used to derive capability planes that can be shifted to any interface by impedance transfer and thus used for designing or assessing a system component. Furthermore, it was shown how different operational boundaries for EV charging such as the transfer of a minimum active power, maximum leakage flux density, or maximum available apparent power can be implemented into these impedance planes.

The method was applied to a use-case in order to demonstrate its suitability for evaluating interoperability of public charging stations and to compare different primary side electronics.

Some further applications of the proposed method include the ability to:

1) assess compensation topologies by exchanging the matrix $\underset{\sim}{A}$ to compare the resulting impedance planes;
2) derive capability planes for the inverter or the magnetic coils and visualize them;
3) present the many operating points associated to the different secondary positions as seen by the primary electronics and derive a suitable design space for the electronics;
4) visualize and include actual operational boundaries of any selected component in the design by including boundaries of other components;
5) assess coil setups by deriving a required minimal coupling for interoperability;
6) derive a design space for secondary coils by calculating an interoperability zone of the primary;
7) study the effects of various limitations;
8) analyze in depth the effects of any chosen impedance matching network.

For recent activities in WPT research, such as fast charging (high power transfer) and heavy duty charging, this method can usefully provide insight on interoperability issues at an early design stage. Particularly as higher variance in air-gaps, leakage limitations with increasing current and interoperability across power classes become more relevant.

APPENDIX

The compensation topologies in Section IV-A were designed with the purpose of covering most of the associated ICPs and in some cases a tradeoff between covering the CCP or the ICP had to be done. Perfect or active tuning is not the scope of this work and plenty of information on this can be found in the literature [29], [30], [31], [32], [33].

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