Comprehensive Analysis and Evaluation of DC-Link Voltage and Current Ripples in Symmetric and Asymmetric Two-Level Six-Phase Voltage Source Inverters

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***Abstract*—Multiphase drives (MPD) in general and six-phase in particular have been gaining popularity in many industries, which calls for a proper multiphase inverter (MPI) design. For voltage source inverter (VSI)-fed drives, the knowledge of voltage and current stresses on the dc-link are imperative for input capacitor sizing. To this end, the voltage and current stresses on the dc-link capacitor in two-level six-phase VSIs are examined thoroughly in this article for two configurations of load/winding spatial distribution: symmetric and asymmetric. First, the harmonic spectrum of the input dc current of each inverter is analyzed in detail by benchmarking them against the conventional three-phase VSI, to precisely establish the dc-capacitor requirement reduction in six-phase counterparts. Second, analytical formulae for the dc-link capacitor voltage ripples are derived for both configurations. Third, simple formulae for dc-capacitor sizing for six-phase VSIs with different load configurations are provided. The accuracy of the derived formulae is verified by simulation and experimental testing at various power factors and modulation depth. It is found that six-phase VSI supplying symmetric and asymmetric loads reaps 10% and 7% lower dc-link current ripples, respectively. Hence, six-phase symmetric loads yield the smallest capacitor size.**

***Index Terms*—Capacitors, dc–ac converters, inverters, multiphase drives (MPD), pulsewidth modulation.**

I. Introduction

MULTIPHASE drives (MPDs) offer numerous advantages over conventional three-phase counterparts, namely, reduced per-phase current handling, improved fault tolerance capability, lower torque pulsations, better noise characteristics, and modularity [1], [2], [3], [4]. Currently, many industries are opting for MPDs over three-phase drives. For example, Dana TM4 offers 265 kW six-phase motor/inverter systems designed for light- to medium-duty electrified trucks [5].

Six-phase drives are among the most popular MPDs as they offer the best tradeoff between reduced (halved) per-phase power requirement and modularity on one hand, and complexity and cost premium on the other [1]. They have been profusely studied from various perspectives including modeling [6], machine design [7], control [8], and fault-tolerance [9]. A relatively overlooked aspect of MPDs, though, is the multiphase inverter (MPI) design. Particularly, the design requirements for the dc-bus capacitor. This primarily stems from the fact that three-phase inverters can be extended to MPIs by simply adding additional switching legs [10]. Another reason is the modularity of six-phase machines with two isolated neutrals, which can be treated as two three-phase sets, commonly referred to as dual three-phase machines [11]. In essence, n-phase machine with n multiples of three can be decomposed into $n/3$ three-phase systems [12]. Therefore, as far as hardware implementation is concerned, these machines can be driven by multiple three-phase voltage source inverters (VSIs). However, the resulting MPI system is usually oversized with switches rated at twice the rated current and two dc-bus capacitors, in the case of six-phase systems.

The dc-bus capacitor is indispensable component of VSI and accounts for one to two thirds the volume of the inverter [13]. Hence, optimizing its size is imperative to improving the power density of the inverter. Capacitor sizing is mainly dictated by two metrics [14]: rms current ripple and allowable dc-voltage ripple. The current rating of the capacitor must withstand the inverter input current ripple, and its capacitance must be high enough to allow only a small voltage ripple, typically 5%. Engineers and researchers alike depend on mathematical formulae to evaluate those two metrics for a given inverter rating in order to design the capacitor [15]. However, such formulae have not been established for six-phase inverters.

Input voltage and current ripples for three-phase VSIs have been investigated in [15], [16], [17], [18], [19], [20], [21], [22], and [23]. The fundamentals of dc ripples analysis was outlined in [16] and [17] for various modulation schemes, including

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sinusoidal PWM (SPWM), space vector modulation (SVM), and third harmonic injection (THI). It was found that SVM leads to reduced dc voltage ripples when compared to SPWM for three-phase VSIs. However, the dc current ripple was found to be almost the same [19]. Evaluation of the dc current ripple for switched reluctance motor (SRM) drives was explored in [23]. Spectral analysis of the dc current ripples using double Fourier series was investigated in [18] and [20] for continuous and discontinuous modulation schemes in two-level and multilevel three-phase VSIs. Discontinuous PWM (DPWM) was observed to result in a higher dc current stress [21]. Multicarrier DPWM was recently suggested in [24] to reduce the dc current ripple, at the expense of increased output current THD. The dc ripples analysis in [16] was extended to unbalanced loads in [22]. Segmentation of three-phase motor windings to from two three-phase drives connected in parallel demonstrated a significant dc ripple current reduction by about 50% [25]. An adaptive minimization modulation technique was proposed in [26] to reduce the dc ripple current further in the segmented motor drive. Lastly, the effect of the reverse recovery of the antiparallel diodes on the dc voltage and current stresses was studied in [15] and found to be negligible.

Evaluation of input voltage and current ripples for MPIs have been investigated in literature for n odd number of phases. In this case, the spatial distribution of phases is always symmetric with $2\pi/n$ radians between subsequent phases. In [27], the input current ripple and voltage ripple analytical expressions for five-phase VSI were derived and verified experimentally. Additionally, the authors found that sinusoidal PWM (SPWM) yields the minimum input voltage ripple. In [28], [29], and [30], the peak-to-peak voltage ripple amplitude was analytically derived for five- and seven-phase VSIs. The derived peak-to-peak voltage ripple expressions enable visualizing the instantaneous ripple envelope experienced by the dc-link capacitor. The authors considered two modulation schemes: SPWM and SVM, and their impact on voltage ripple was examined. In contrast to conventional three-phase VSI [16], the reported results showed no tangible attenuation in voltage ripples when using SVM over SPWM. On the contrary, at high modulation index, SPWM led to reduced voltage ripples in [28] in seven-phase VSI when compared to SVM, which is in line with the findings in [27] for five-phase VSIs. Numerical analysis of input and output current ripples of nine-phase VSI was attempted in [31] using conventional SPWM and dual-carrier PWM. The authors claimed a reduced input and output current ripple for asymmetric loads with dual-carrier PWM.

For $n = 6$, fewer studies were reported. In [32], input current ripple for six-phase VSI with arbitrary spatial displacement angle, δ between the two three-phase sets was examined. It was found that the input current ripple is minimal when the load is symmetric (i.e., $\delta = \pi/3$). Therefore, unlike n-phase inverters with odd number of phases, input current stress is a function of δ for six-phase VSI. Analytical expression of the input current ripple for six-phase VSI with symmetric load was derived in [32]. In [33], the input current ripple analytical expressions were given for six-phase VSI supplying split ($\delta = 0$), asymmetric ($\delta = \pi/6$), and open-end winding machines with a single power source. However, mathematical derivations were not outlined for all cases.

A generalized model for the dc-link capacitor in MPIs with $n > 3$ phases was reported in [34]. The modeling assumed symmetric and balanced loads operating in the linear modulation region. Accordingly, a comparative analysis for the dc-capacitor, in terms of input voltage and current ripples, was presented. Also, the effects of modulation scheme (SPWM versus SVM), carrier waveform (triangular versus sawtooth) and interleaving techniques on voltage ripples were examined for nine-phase VSI. The authors reported a potential for dc-link capacitor size reduction in nine-phase VSI of up to two-thirds when using SVM with three interleaving triangular carriers. In interleaved multi-carrier PWM, the n phases are divided into p groups of three-phases. A multiple of p carriers, shifted by δ degrees, can be used to modulate three signals to generate the gate pulses for n switches. The same strategy was implemented and reported in [35] for $n = 15$. However, the same did not apply to six-phase VSIs; no improvement was observed with two interleaving triangular carriers [34].

To this end, there exists a gap in knowledge for input current and voltage ripples in six-phase VSIs with different load configurations (i.e., different δ). More specifically, input current ripple analysis was partially covered in [32] and [33] for symmetric and asymmetric loads, respectively. Furthermore, to the best of the authors' knowledge, input voltage ripple for six-phase VSI was not examined for any load configuration, and therefore, their analytical formulae have not been established yet. Subsequently, this study fills in this gap by delivering the following.

1) A thorough analysis of input current ripple analysis for symmetric and asymmetric six-phase loads, along with analytical formulae.
2) Mathematical formulae derivation of input voltage ripple for symmetric and asymmetric six-phase VSIs.
3) Experimental validation of derived formulae at various power factors (PFs) and modulation indices.
4) Capacitor design rules for six-phase VSIs based on maximum dc voltage and dc current stresses.

The foregoing contributions enables the designer to properly size the dc-bus capacitor in six-phase VSIs in order to achieve the best power density. The rest of the article is organized as follows. Six-phase VSI modeling with symmetric and asymmetric loads is reviewed in Section II. Derivations of dc-capacitor current and voltage ripples are investigated in Sections III and IV, respectively. Simulation and experimental validations of derived analytical formulae and benchmarking against conventional three-phase VSI are presented in Section VI. Finally, Section VII concludes this article.

II. Six-Phase VSI Modeling

The schematic of the six-phase VSI is depicted in Fig. 1. The dc supply is assumed constant and is connected through a line impedance, $Z_{dc} = R_{dc} + j\omega_s L_{dc}$, where ω_s is the switching angular frequency. The six-phase load/motor windings, ABC_1 and ABC_2, can be configured as split ($\delta = 0$), symmetric ($\delta = \pi/3$), or asymmetric ($\delta = \pi/6$) manner. Asymmetric six-phase

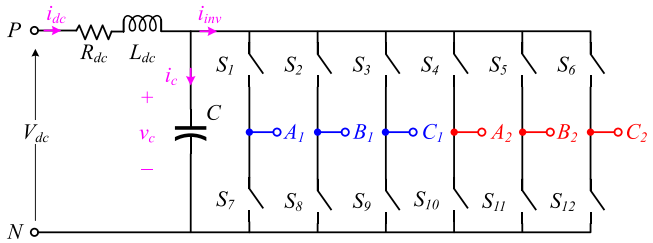


Fig. 1. Schematic diagram of a six-phase voltage source inverter (VSI).

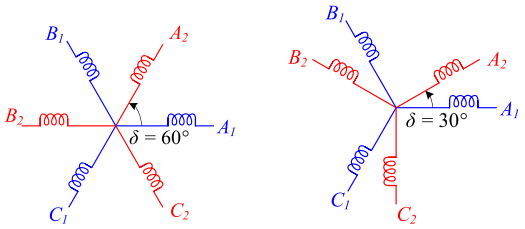


Fig. 2. Six-phase winding configurations. (a) Symmetric. (b) Asymmetric.

machines are the most popular among the three configurations owing to reduced torque pulsation [36]. On the other hand, symmetric six-phase machines have been finding application in EVs for their superior fault-tolerance capability [37], [38], [39]. Split configuration is the least popular as it exhibits the worst fault-tolerance capability. Moreover, no dc ripples reduction over three-phase system is obtained using split configuration [32], and therefore, was not considered in this article. Fig. 2 shows the symmetric and asymmetric six-phase configurations. The modulating voltage signals and fundamental phase currents of the six-phase inverter are given in (1) and (2), respectively

$$\begin{aligned}
v_{A1} &= M\sin\theta + v_0 \\
v_{B1} &= M\sin\left(\theta - \frac{2}{3}\pi\right) + v_0 \\
v_{C1} &= M\sin\left(\theta + \frac{2}{3}\pi\right) + v_0 \\
v_{A2} &= M\sin\left(\theta - \delta\right) + v_0 \\
v_{B2} &= M\sin\left(\theta - \frac{2}{3}\pi - \delta\right) + v_0 \\
v_{C2} &= M\sin\left(\theta + \frac{2}{3}\pi - \delta\right) + v_0
\end{aligned} \tag{1}$$

$$\begin{aligned}
i_{A1} &= \sqrt{2}I_L\sin\left(\theta - \phi\right) \\
i_{B1} &= \sqrt{2}I_L\sin\left(\theta - \frac{2}{3}\pi - \phi\right) \\
i_{C1} &= \sqrt{2}I_L\sin\left(\theta + \frac{2}{3}\pi - \phi\right) \\
i_{A2} &= \sqrt{2}I_L\sin\left(\theta - \phi - \delta\right) \\
i_{B2} &= \sqrt{2}I_L\sin\left(\theta - \frac{2}{3}\pi - \phi - \delta\right) \\
i_{C2} &= \sqrt{2}I_L\sin\left(\theta + \frac{2}{3}\pi - \phi - \delta\right)
\end{aligned} \tag{2}$$

where $\theta = 2\pi f_1 t$ and f_1 is the fundamental frequency, ϕ is the angle between the phase voltage and phase current (i.e., PF angle), δ is the phase displacement angle between the two three-phase sets ($\delta = \pi/3$ and $\pi/6$ for symmetric and asymmetric spatial displacements, respectively), I_L is the RMS load current, M is the modulation index, and v_0 is an arbitrary zero-sequence voltage.

The dc capacitor current, i_c is obtained from Fig. 1 and given in (3). The currents in (3) are decomposed into average current components, represented by capital letter and a $\bar{}$ accent, and ripple components, represented by a $\tilde{}$ accent

$$\left(\bar{I}_c + \tilde{i}_c\right) = \left(\bar{I}_{dc} + \tilde{i}_{dc}\right) - \left(\bar{I}_{inv} + \tilde{i}_{inv}\right). \tag{3}$$

In steady-state, the average capacitor current is zero (i.e., $\bar{I}_c = 0$). It follows that $\bar{I}_{dc} = \bar{I}_{inv}$. Additionally, if the capacitance of the dc-bus capacitor, C is large enough to filter most of the ripple of the dc input current, then $\tilde{i}_{dc} \simeq 0$. It follows that $\tilde{i}_c \simeq -\tilde{i}_{inv}$. Therefore, the dc-bus current ripple can be analyzed by analyzing i_{inv}. The i_{inv} can be defined in terms of the output phase currents and the switching states of the inverter legs as [34]

$$i_{inv} = \sum_x i_x \times S_x \tag{4}$$

where $x \in \{A1, B1, C1, A2, B2, C2\}$, i_x is the inverter output currents, and S_x is a Boolean switching function that models the ON/OFF state of the switch, and can be expressed as

$$S_x = \begin{cases} 1, & \textit{top switch is} \text{ ON} \\ 0, & \textit{bottom switch is} \text{ ON}. \end{cases} \tag{5}$$

Next, we develop the numerical expressions of i_{inv} and its average and ripple components for the symmetric and asymmetric spatial displacements in six-phase VSI.

III. DC-Bus Current Ripples

The derivations of the dc-bus current ripples herein assumes sinusoidal output current, which is a valid assumption when the switching frequency, f_s is very high. This is typically the case in low to medium voltage applications. The current ripple analysis in this section considers symmetric and asymmetric loads. Fig. 3 shows the output sinusoidal current waveforms for symmetric and asymmetric six-phase configurations. Additionally, when the modulation frequency $m_f = f_s/f_1$ is very high, the reference voltages can be treated as constants within one switching period, T_s [16]. Owing to its simplicity and wide application, the modulation technique considered in the derivation is SPWM with a triangular carrier, $v_{cr} \in [-1, 1]$.

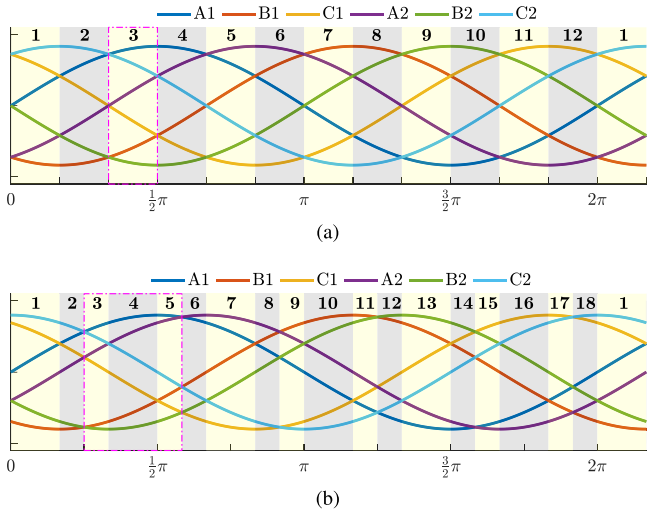


Fig. 3. Six-phase waveforms with corresponding modes of operation within one fundamental period. (a) Symmetric load. (b) Asymmetric load.

A. Symmetric Configuration

When the six-phase VSI is connected to a load (machine) with symmetric spatial displacement (windings), i_{inv} has 12 unique modes of operation in one fundamental cycle, as shown in Fig. 3(a). Those modes are evenly distributed with $\pi/6$ intervals. Fig. 4 shows the detailed PWM and switching states of the upper switches, along with i_{inv} and v_c when the inverter is in Mode 3 ($\pi/3$ to $\pi/2$). From (4) and Fig. 4, i_{inv} can be expressed as given in (6). Also, from Fig. 4, the relationship between the dwell times, T_0 to T_6 and T_s can be defined as given in (7) [16]

$$i_{inv} = \begin{cases} 0, & \text{for } t_0 \le t < t_1 \\ i_{A1}, & \text{for } t_1 \le t < t_2 \\ i_{A1} + i_{C2}, & \text{for } t_2 \le t < t_3 \\ i_{A1} - i_{B2}, & \text{for } t_3 \le t < t_4 \\ -(i_{B1} + i_{B2}), & \text{for } t_4 \le t < t_5 \\ -i_{B2}, & \text{for } t_5 \le t < t_6 \\ 0, & \text{for } t_6 \le t < t_8 \\ -i_{B2}, & \text{for } t_8 \le t < t_9 \\ -(i_{B1} + i_{B2}), & \text{for } t_9 \le t < t_{10} \\ i_{A1} - i_{B2}, & \text{for } t_{10} \le t < t_{11} \\ i_{A1} + i_{C2}, & \text{for } t_{11} \le t < t_{12} \\ i_{A1}, & \text{for } t_{12} \le t < t_{13} \\ 0, & \text{for } t_{13} \le t < t_{14} \end{cases} \tag{6}$$

$$\begin{aligned} T_0 &= \frac{T_s}{4}(1 - v_{A1}) & T_4 &= \frac{T_s}{4}(v_{C1} - v_{B1}) \\ T_1 &= \frac{T_s}{4}(v_{A1} - v_{C2}) & T_5 &= \frac{T_s}{4}(v_{B1} - v_{B2}) \\ T_2 &= \frac{T_s}{4}(v_{C2} - v_{A2}) & T_6 &= \frac{T_s}{4}(1 + v_{B2}) \\ T_3 &= \frac{T_s}{4}(v_{A2} - v_{C1}). \end{aligned} \tag{7}$$

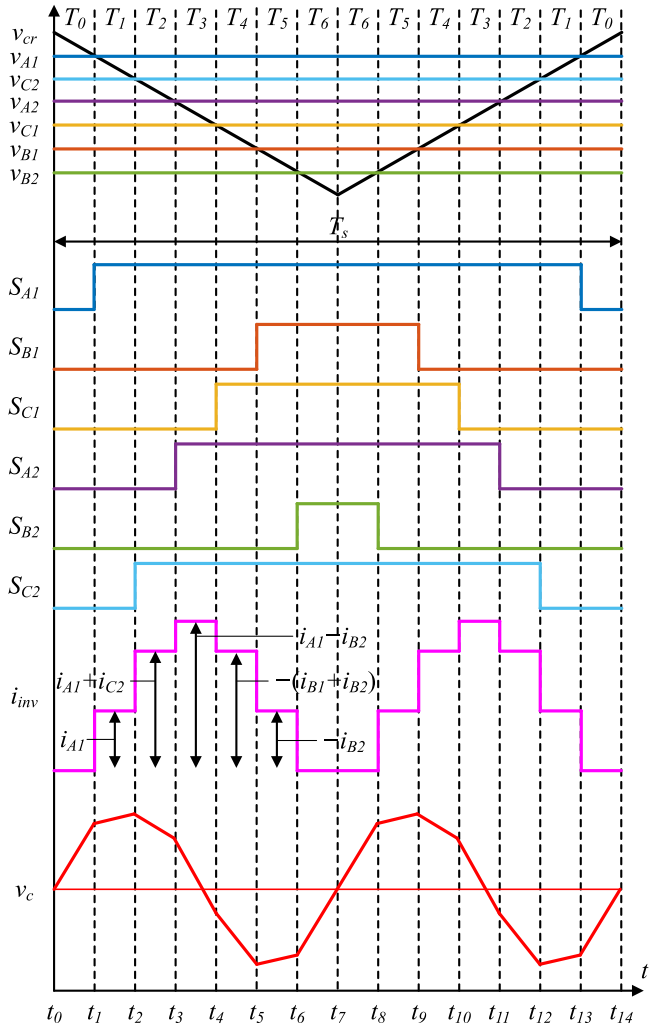


Fig. 4. Symmetric six-phase VSI: Switching pulses of upper switches, $S_{ABC1,ABC2}$, inverter input current, i_{inv}, and capacitor voltage, v_c during one switching period in Mode 3.

The mean square value of i_{inv} is defined as [16]

$$\begin{aligned} I_{inv}^2 &= \frac{1}{T_s}\int_{t_0}^{t_0+T_s} i_{inv}^2\, dt \\ &= \frac{2T_1}{T_s} i_{A1}^2 + \frac{2T_2}{T_s}(i_{A1} + i_{C2})^2 + \frac{2T_3}{T_s}(i_{A2} - i_{B2})^2 \\ &\quad + \frac{2T_4}{T_s}(i_{B1} + i_{B2})^2 + \frac{2T_5}{T_s} i_{B2}^2. \end{aligned} \tag{8}$$

Substituting (1)–(2) and (6)–(7) in (8), the average square value of (8) can be computed as

$$I_{inv,avg}^2 = \frac{6}{\pi}\int_{\pi/3}^{\pi/2} I_{inv}^2\, d\theta. \tag{9}$$

Since the inverter is connected to a symmetric load, the average value over the other eleven 60° intervals [see Fig. 3(a)] is the same. The average inverter input current, $\bar{I}_{inv}$ can be derived from the power balance between the ac and dc sides

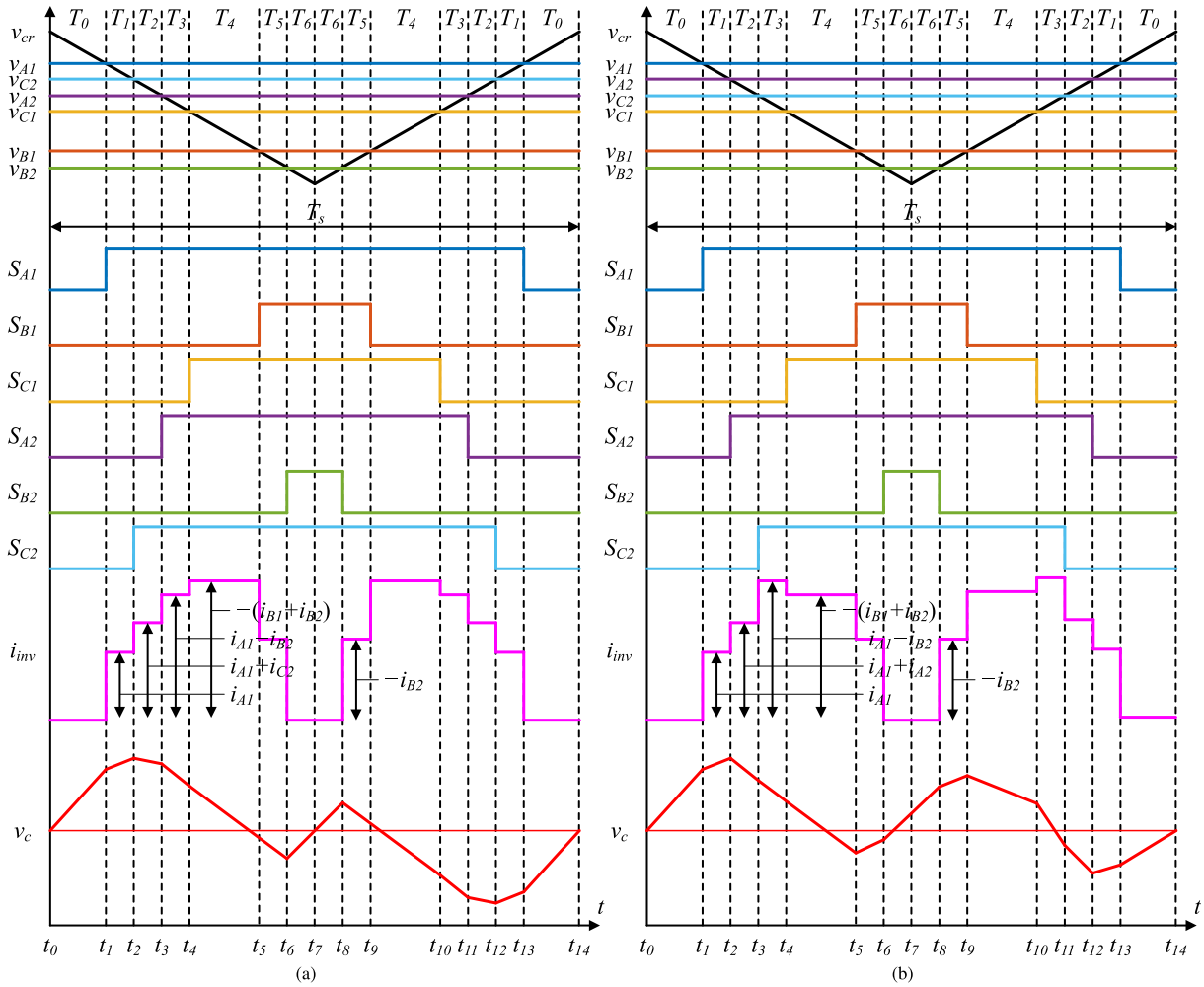


Fig. 5. Asymmetric six-phase VSI: Switching pulses of upper switches, $S_{ABC1,ABC2}$, inverter input current, i_{inv}, and capacitor voltage, v_c during one switching period in (a) Mode 3 and (b) Mode 4.

of the inverter, neglecting power loss. Therefore

$$\bar{I}_{inv} = \frac{3}{\sqrt{2}} M I_L \cos\phi. \tag{10}$$

At last, the rms value of the inverter input current ripple, $\tilde{I}_{inv}$ is computed as

$$\begin{aligned}\tilde{I}_{inv} &= \sqrt{I^2_{inv,avg} - \bar{I}^2_{inv}} \\ &= I_L \left\{ \frac{M}{\pi} \left(3 + 3\sqrt{3} - \frac{9\pi}{4} M + \right. \right. \\ &\quad \left. \left. \left(4 + 2\sqrt{3} - \frac{9\pi}{4} M \right) \cos 2\phi \right) \right\}^{1/2}. \end{aligned} \tag{11}$$

B. Asymmetric Configuration

When the six-phase VSI is connected to a load (machine) with asymmetric spatial displacement (windings), i_{inv} has 18 unique modes of operation in one fundamental cycle, as shown in Fig. 3(b). That is *six* additional modes when compared to the symmetric case. Unlike symmetric loads, the modes are not evenly distributed. Six out of the 18 modes span an interval of $\pi/6$ [Modes 1, 4, 7, 10, 13, and 16 in Fig. 3(b)], whereas the other intervals span an interval of $\pi/12$. The former and later modes are henceforth called *large modes* and *small modes*, respectively. In between two consecutive large modes, there are two small modes. If *large* and *small* modes were to be represented by "1" and "0," then the sequence of modes for asymmetric currents would be "100100..." In light of this breakdown of modes of operation, three intervals are required to derive the dc-current ripple. In this article, Modes 3–5 are considered, as shown in Fig. 3(b). Fig. 5 shows the detailed PWM and switching states of the upper switches, along with i_{inv} and v_c when the inverter is in Mode 3 ($\pi/4$ to $\pi/3$) and Mode 4 ($\pi/3$ to $\pi/2$) for asymmetric spatial displacement. Note that the vertical spacing between phase voltages in Fig. 5 is due to asymmetry.

The i_{inv} and dwell times for Modes 3 and 4, can be deduced from Fig. 5 in the same manner discussed in the previous subsection. Then, the intermediate steps involving mean square value of i_{inv} derivations are similar to those in (8), and hence are not repeated for brevity. The same applies for Mode 5, which is not shown in Fig. 5 due to space limitation. The average square value of the inverter input current over one T_s is computed using

the weighted average of Modes 3–5 as

$$I^2_{inv,avg} = \frac{1}{4}\left(I^2_{inv3,avg} + 2I^2_{inv4,avg} + I^2_{inv5,avg}\right) \quad (12)$$

where the 3, 4, and 5 subscripts in i_{inv} denote Modes 3, 4, and 5, respectively. The rms value of the inverter input current ripple for the asymmetric six-phase inverter is

$$\tilde{I}_{inv} = I_L\left\{\frac{M}{2\pi}\left[2\left(\sqrt{3}-\sqrt{2}\right)+\sqrt{6}+\left(4\sqrt{2}+8\sqrt{3}+4\sqrt{6}-9\pi M\right)\cos^2\phi\right]\right\}^{1/2}. \quad (13)$$

Note that v_0 cancels out in $\tilde{I}_{inv}$ in (11) and (13). Therefore, $\tilde{I}_{inv}$ cannot be made smaller using SVM, or any other zero-sequence injection technique. Also, $\tilde{I}_{inv}$ is independent of C and f_{sw}, but rather a function of I_L, M, and PF only. Put otherwise, $\tilde{I}_{inv}$ cannot be reduced by increasing the switching frequency or enlarging the dc-link capacitor. This is not the case for voltage ripples, as will be shown next.

C. Harmonic Spectrum Comparison

Comparing the analytical expressions in (11) and (13), the behavior of $\tilde{I}_{inv}$ is obviously different for the symmetric and asymmetric six-phase loads. Further analysis, in terms of harmonic spectrum, is sought to identify the underlying reasons for this difference. The analysis is conducted with respect to the conventional three-phase VSI to provide a benchmark measure for the six-phase counterpart. Furthermore, the following analysis can be generalized to any $3k$-phase systems ($k \in [1, 2, \dots]$).

Six-phase systems can be treated as dual three-phase systems with a phase displacement δ between the two sets of three-phases. As such, (4) can be rewritten as

$$\begin{aligned} i_{inv} &= \sum_{x1} i_{x1} \times S_{x1} + \sum_{x2} i_{x2} \times S_{x2} \\ &= i_{inv_1} + i_{inv_2} = i_{inv}\angle 0 + i_{inv}\angle\delta \end{aligned} \quad (14)$$

where $x1 \in \{A1, B1, C1\}$, $x2 \in \{A2, B2, C2\}$, and $i_{inv_{1,2}}$ is the inverter input current for each of the three-phase sets. Since the input dc current is the superposition summation of all phase-leg currents, the fundamental, the second harmonic, and all triplen carrier-sidebands get canceled for balanced three-phase loads [20]. Hence, $\tilde{i}_{inv_1}$ only includes switching carrier harmonics and nontriplen sidebands. The presence of i_{inv_2} in six-phase systems affect the remaining harmonics. The harmonic content of the input dc-current ripple in three-phase VSI (i.e., i_{inv_1}), shown in Fig. 6(a), can be categorized into three groups.

1) Group 1: carrier harmonics, mf_s with even m.
2) Group 2: sideband harmonics, $mf_s \pm nf_1$ with odd m and triplen n.
3) Group 3: sideband harmonics, $mf_s \pm nf_1$ with even m and $n = 6k$, $k \in \mathbb{N}$.

For six-phase VSI, Group 1 harmonics are equal to those in the three-phase VSI, irrespective of load configuration. This is because each three-phase set (i.e., ABC_1 and ABC_2) produces

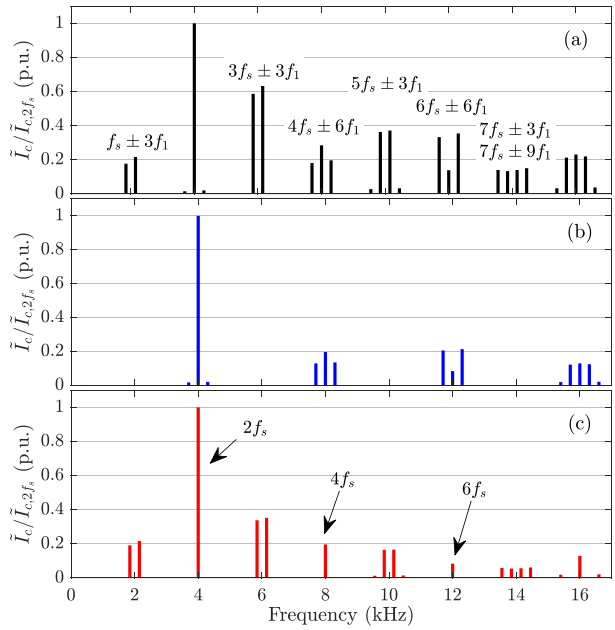


Fig. 6. Simulated harmonic spectra of input current ripple, $\tilde{I}_{inv}$ for three- and six-phase VSIs of the same VA rating ($f_1 = 50$ Hz, $f_s = 2$ kHz, $PF = 0.6$, $M = 0.7$). (a) Three-phase VSI. Six-phase VSI with (b) symmetric load and (c) asymmetric load.

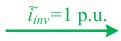
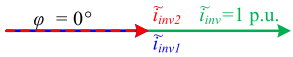
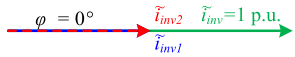
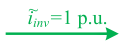
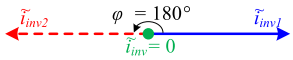
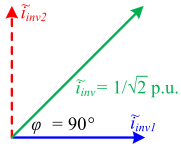
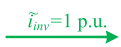
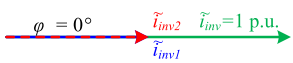
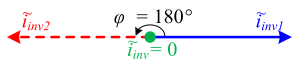
harmonics of equal magnitude and zero phase shift (i.e., $\tilde{i}_{inv1} = \tilde{i}_{inv2}$), thus they sum up. Yet, the magnitude of each of them is half of that of the three-phase VSI for the same VA rating.

For six-phase VSI with symmetric loads [see Fig. 6(b)], Group 2 harmonics get eliminated. The magnitude of such harmonics from each three-phase set (i.e., ABC_1 and ABC_2) is equal but 180° out of phase (i.e., $\tilde{i}_{inv1} = -\tilde{i}_{inv2}$). Hence, they cancel out due to symmetry. This originates from $\delta = \pi/3$ for symmetric six-phase loads. So, Group 2 harmonics of the second three-phase set (i.e., ABC_2) are phase shifted by $\varphi = n\delta = n\pi$, for triplen n. On the other hand, Group 2 harmonics are 90° out of phase for six-phase VSI with asymmetric loads. In this case, $\delta = \pi/6$ and $\varphi = n\delta = n(\pi/2)$, for triplen n. Thus, their per-unit magnitude sum is $\sqrt{2}$. But since the phase current in six-phase systems is half of that of three-phase ones, the resulting magnitude of such harmonics are reduced by a factor of $1/\sqrt{2}$ [see Fig. 6(c)].

Group 3 harmonics in each of the three-phase sets of the six-phase VSI with symmetric loads are in-phase (i.e., $\varphi = n\delta = n2\pi$ for $\delta = \pi/3$ and $n = 6k$), and thus, remain the same, for the same reason as Group 1 (i.e., the halves add up). However, such harmonics are 180° out of phase for six-phase VSI with asymmetric loads, hence they cancel out (i.e., $\varphi = n\delta = n\pi$ for $\delta = \pi/6$ and $n = 6k$).

In summary, each of the different six-phase configurations contain only two out of the three harmonic groups in three-phase VSI, with even multiples of carrier harmonics being mutual in both six-phase loads. Yet the harmonics eliminated in the six-phase symmetric load (i.e., Group 2) are more dominant than those eliminated in the asymmetric load (i.e., Group 3).

TABLE I
HARMONIC SPECTRUM COMPARISON BETWEEN SYMMETRIC AND ASYMMETRIC SIX-PHASE VSI BY HARMONIC GROUPS

Harmonic Group*	Three-Phase System	Six-Phase Load/Winding Configuration	
		Symmetric	Asymmetric
Group 1 mf_s, even m			
Group 2 $mf_s \pm nf_1$, odd m, triplen n			
Group 3 $mf_s \pm nf_1$, even m, $n = 6k$, $k \in \mathbb{N}$			

*Normalized $\tilde{i}_{inv}$ per harmonic group to their three-phase equivalent.

Therefore, six-phase VSI with symmetric loads yields the lowest dc-capacitor RMS current.

Table I summarizes the vector diagrams of the different harmonic groups of the input dc current ripple in the symmetric and asymmetric six-phase VSI.

IV. DC-BUS VOLTAGE RIPPLES

After deriving numerical expressions for the dc capacitor rms current ripple in the previous section (recall $\tilde{i}_c \simeq -\tilde{i}_{inv}$), numerical expressions for the dc capacitor voltage ripple, $\tilde{v}_c$ are now sought for symmetric and asymmetric six-phase configurations. The $\tilde{v}_c$ can be defined as [16]

$$\tilde{v}_c = \frac{1}{C}\int \tilde{i}_c\, dt = \frac{1}{C}\int \left(\bar{I}_{inv} - i_{inv}\right)\, dt \qquad (15)$$

A. Symmetric Configuration

The $\tilde{v}_c$ can be obtained by substituting (6) in (15). This yields $\tilde{v}_c$ in (16) shown at the bottom of this page, with $C_i = v_i(t_i), \quad i \in \{1, 2, \ldots, 5\}$. The C_i in (16) shown at the bottom of this page, are the constants resulting from the integration operation in (15). C_i is obtained by evaluating $v_{(i-1)}$ at $T_{(i-1)}$. This yields

$$C_1 = T_0$$

$$C_2 = C_1 + \left(1 - \frac{i_{A1}}{\bar{I}_{inv}}\right) T_1$$

$$C_3 = C_2 + \left(1 - \frac{i_{A1} - i_{C2}}{\bar{I}_{inv}}\right) T_2$$

$$\tilde{v}_c = \frac{\bar{I}_{inv}}{C} \begin{cases} v_0 = t - t_0, & \text{for } t_0 \le t < t_1 \\ v_1 = \left(1 - \frac{i_{A1}}{\bar{I}_{inv}}\right)(t - t_1) + C_1, & \text{for } t_1 \le t < t_2 \\ v_2 = \left(1 - \frac{i_{A1}+i_{C2}}{\bar{I}_{inv}}\right)(t - t_2) + C_2, & \text{for } t_2 \le t < t_3 \\ v_3 = \left(1 - \frac{i_{A1}-i_{B2}}{\bar{I}_{inv}}\right)(t - t_3) + C_3, & \text{for } t_3 \le t < t_4 \\ v_4 = \left(1 + \frac{i_{B1}+i_{B2}}{\bar{I}_{inv}}\right)(t - t_4) + C_4, & \text{for } t_4 \le t < t_5 \\ v_5 = \left(1 + \frac{i_{B2}}{\bar{I}_{inv}}\right)(t - t_5) + C_5, & \text{for } t_5 \le t < t_6 \\ v_6 = t - t_7, & \text{for } t_6 \le t < t_8 \\ \left(1 + \frac{i_{B2}}{\bar{I}_{inv}}\right)(t - t_5) - C_5, & \text{for } t_8 \le t < t_9 \\ \left(1 + \frac{i_{B1}+i_{B2}}{\bar{I}_{inv}}\right)(t - t_4) - C_4, & \text{for } t_9 \le t < t_{10} \\ \left(1 - \frac{i_{A1}-i_{B2}}{\bar{I}_{inv}}\right)(t - t_3) - C_3, & \text{for } t_{10} \le t < t_{11} \\ \left(1 - \frac{i_{A1}+i_{C2}}{\bar{I}_{inv}}\right)(t - t_2) - C_2, & \text{for } t_{11} \le t < t_{12} \\ \left(1 - \frac{i_{A1}}{\bar{I}_{inv}}\right)(t - t_1) - C_1, & \text{for } t_{12} \le t < t_{13} \\ t - t_{14}, & \text{for } t_{13} \le t < t_{14}. \end{cases} \qquad (16)$$

$$C_4 = C_3 + \left(1 - \frac{i_{A1} - i_{B2}}{\bar{I}_{inv}}\right) T_3$$
$$C_5 = C_4 + \left(1 + \frac{i_{B1} - i_{B2}}{\bar{I}_{inv}}\right) T_4. \tag{17}$$

The $\tilde{v}_c$ for symmetric six-phase VSI in Mode 3 is depicted in Fig. 4. One can note that $\tilde{v}_c$ is symmetric around t_7. Hence, the mean square value of $\tilde{v}_c$ can be calculated as

$$\tilde{V}_c^2 = \frac{1}{T_s}\int_{t_0}^{t_0+T_s} \tilde{v}_c^2 \, dt = \frac{2\bar{I}_{inv}^2}{C^2 T_s}\left[\sum_{i=0}^{6}\int_0^{T_i} v_i^2 \, dt\right]. \tag{18}$$

The rms inverter dc-link voltage ripple, $\tilde{V}_c$ over Mode 3 is computed as

$$\tilde{V}_c = \sqrt{\frac{6}{\pi}\int_{\pi/3}^{\pi/2} \tilde{V}_c^2 \, d\theta}. \tag{19}$$

Substituting (2) and (7) in (18) and performing the integration in (18), results in

$$\tilde{V}_c = K_v M \sqrt{\frac{1}{60}M + \left(6 - \frac{65}{2\pi}M + \frac{9}{2}M^2 + 18v_0^2\right)\cos^2\phi} \tag{20}$$

where $K_v = I_L/8Cf_s$. For symmetric balanced loads, the average value over the other eleven 60° intervals [see Fig. 3(a)] is the same.

B. Asymmetric Configuration

Similar to the methodology undertaken in Section III-B, Modes 3–5 are analyzed to derive $\tilde{V}_c$ for six-phase VSI with asymmetric loads. Again, derivations for $\tilde{V}_c$ in Mode 3 are similar to those carried out in the previous subsection and hence are not repeated. For Modes 4 and 5, $\tilde{v}_c$ is similar to that of Mode 3 defined in (15), but using i_{inv4} and i_{inv5} instead of i_{inv3} in (6), respectively. Therefore, intermediate steps pertaining to $\tilde{v}_c$ and $\tilde{V}_c^2$ are not shown for brevity. The rms inverter dc-link voltage ripple over one fundamental cycle is the weighted sum of $\tilde{V}_c^2$ in Modes 3–5, given as

$$[b]\tilde{V}_c = \left\{\frac{3}{\pi}\int_{\pi/4}^{\pi/3} \tilde{V}_{c3}^2 \, d\theta + \frac{3}{\pi}\int_{\pi/3}^{\pi/2} \tilde{V}_{c4}^2 \, d\theta + \frac{3}{\pi}\int_{\pi/2}^{7\pi/12} \tilde{V}_{c5}^2 \, d\theta\right\}^{1/2}. \tag{21}$$

Performing the integration in (21) yields

$$[b]\tilde{V}_c = K_v M\left\{3 - \frac{24}{5}M + \frac{9}{4}M^2 + 9v_0^2 - \frac{16}{5\pi}Mv_0\sin 2\phi + \left(3 - \frac{21}{4}M + \frac{9}{4}M^2\right)\cos 2\phi\right\}^{1/2}. \tag{22}$$

Note that some numerical approximations were conducted in (20) and (22) in order to yield simple and closed-form formula. While this study is limited to SPWM (i.e., $v_0 = 0$), previous studies [27], [28], [29], [30] suggested no improvement in input voltage ripples for MPIs when using SVM. Nonetheless, the expressions are given in terms of v_0 for future work.

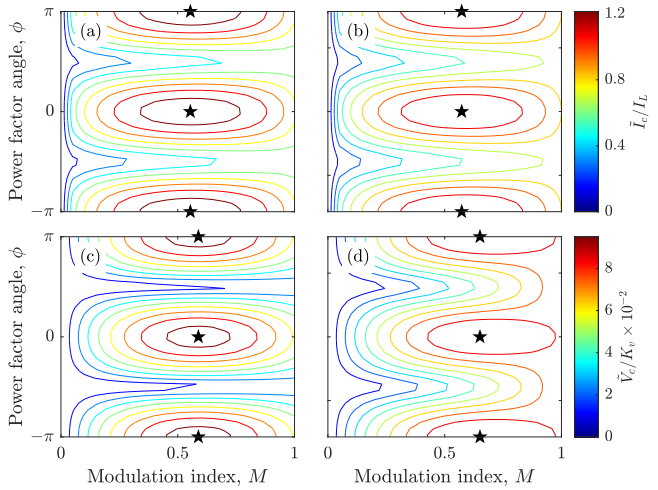


Fig. 7. Contour map of $f(\mathbf{x})$ showing $\mathbf{x}^*$. Normalized current ripple, $\hat{I}_c = \tilde{I}_c/I_L$ for (a) symmetric and (b) asymmetric loads, and normalized voltage ripple, $\hat{V}_c = \tilde{V}_c/K_v$ for (c) symmetric and (d) asymmetric six-phase loads.

V. DC Capacitor Design

The dc-link capacitor is designed to meet the requirements of the inverter system. Among them, it must satisfy two criteria related to dc stresses: 1) a continuous current rating higher than the maximum $\tilde{I}_c$; and 2) withstand an allowable voltage ripple, typically below 10%. As such, the points at which the current and voltage ripples are at their maximum must be defined. Using the derived expressions for $\tilde{I}_c$ and $\tilde{V}_c$ in Sections III and IV, the maximum dc stress points in six-phase VSI are found in this section. Then, simple formulae for capacitor selection is provided, considering symmetric and asymmetric loads.

Consider the variables affecting the current and voltage ripples in (11), (13), (20), and (22). They can be classified as design-specific and operation-specific variables. The former variables are I_L, C, and f_s, whereas the latter variables are M and ϕ. The design-specific variables are irrelevant when determining the points of maximum stress and rather act as scaling factors. Thus, they can be normalized when solving for the maximum points. It follows that the normalized capacitor current and voltage ripples are $\hat{I}_c = \tilde{I}_{inv}/I_L$ and $\hat{V}_c = \tilde{V}_c/K_v$, respectively. The maximum stress points can then be treated as an optimization problem defined as

$$\mathbf{x}^* = \arg\max_{\mathbf{x}} f(\mathbf{x}) \tag{23}$$

subject to

$$\begin{aligned} 0 \le \mathrm{x}_1 \le 1 \\ 0 \le \mathrm{x}_2 \le 2\pi \end{aligned} \tag{24}$$

where $f(\mathbf{x})$ is $\hat{I}_c$ and $\hat{V}_c$, and $\mathbf{x} = [\mathrm{x}_1 \quad \mathrm{x}_2]^T = [M \quad \phi]^T$. The 2-D nonlinear $f(\mathbf{x})$ can be solved using any of the classical optimization methods [40]. Fig. 7 depicts the maximum stress points, $\mathbf{x}^*$ in the $f(\mathbf{x})$ space. In terms of ϕ, the maximum

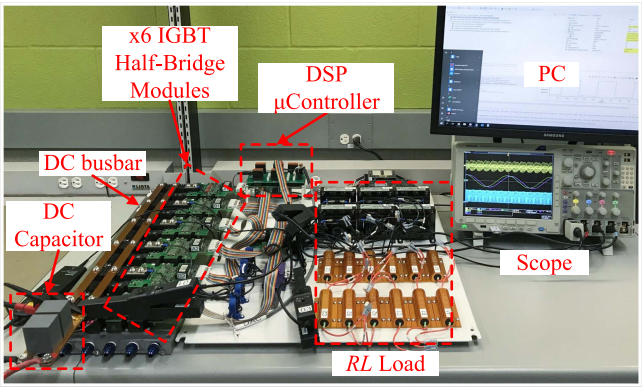


Fig. 8. Experimental setup of a six-phase VSI with RL load.

current and voltage stress occurs at the same point: $\phi^* = k\pi, k \in \{0, 1, 2\ldots\}$ (i.e., unity PF), irrespective of load configuration. On the other hand, the maximum stress points occur at different M: the maximum current stress occurs at $M^* = 0.55$ and 0.57 and the maximum voltage stress occurs at $M^* = 0.59$ and 0.65 for symmetric and asymmetric loads, respectively.

Evaluating $\tilde{I}_{inv}$ in (11) and (13) at $\mathbf{x}^*$ yields

$$I_{CAP} \geq \begin{cases} 6/5 \cdot I_L, & \text{for symmetric loads} \\ 5/4 \cdot I_L, & \text{for asymmetric loads} \end{cases} \tag{25}$$

where I_{CAP} is the rated continuous current of the dc capacitor. Similarly, the required capacitance, C to guarantee an acceptable dc voltage ripple can be found by evaluating $\tilde{V}_c$ in (20) and (22) at $\mathbf{x}^*$. This yields

$$C \geq \begin{cases} \dfrac{3\sqrt{3}I_L}{16 f_s \Delta V_{pp}}, & \text{for symmetric loads} \\ \dfrac{4\sqrt{3}I_L}{21 f_s \Delta V_{pp}}, & \text{for asymmetric loads} \end{cases} \tag{26}$$

where ΔV_{pp} is the allowable peak-to-peak voltage ripple. Note that I_{CAP} and C for asymmetric six-phase loads is higher than its symmetric counterpart by approximately 5%. Hence, if the six-phase inverter is designed to be suitable for both load configurations, the formulae for asymmetric loads should be employed for the dc capacitor sizing.

The accuracy of the derived formulae for the dc-capacitor current and voltage stresses is examined next.

VI. Results and Discussions

The developed analytical formulae for the dc-bus capacitor rms voltage and current ripples are verified by numerical simulations and experimental testing. Fig. 8 depicts the experimental setup a six-phase VSI connected to a passive RL load. The passive load is chosen for its flexibility to be configured as symmetric and asymmetric load by simply adjusting the angle δ of the virtual reference voltage in the controller. Nevertheless, the following experimentation and analysis are equally applicable to motor loads, if the load currents are balanced and almost sinusoidal. Table II lists the experimental setup parameters.

TABLE II
Experimental Setup and Simulation Parameters

Parameter	Symbol	Value	Unit
dc-link voltage	V_{dc}	100	V
dc-link capacitor	C	80	μF
dc-line resistance	R_{dc}	30	mΩ
dc-line inductance	L_{dc}	10	μH
Fundamental frequency	f_1	50	Hz
Switching frequency	f_s	10	kHz
Switching dead time	t_d	2	μs

TABLE III
Per-Phase RL Load Parameters

PF ($f_1 = 50$ Hz)	**0.6**	**0.8**	**0.9**
R (Ω)	1.1	2.2	4.4
L (mH)	5.0	5.0	5.0

The VSI is made up of six Infineon half-bridge 1200 V/600 A IGBT FF600R12IE4 modules connected via dc busbars made of copper to reduce the stray inductance. The inverter is controlled via a 32-b, dual-core, floating-point TI TMS320F28377D DSP. The employed dc-link capacitor bank is two-paralleled 40 μF film capacitors. Note that the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL) of the film capacitors on the voltage ripple estimation is negligible [30]. The dc voltage is supplied from a Keysight N8932 A dc source. The employed RL load is made adjustable to facilitate testing at different PF points where industrial drives are typically operated (0.6–0.9), as tabulated in Table III. The dc-line impedance, Z_{dc} is the impedance of the dc cable between the power source and the inverter, whose resistance is $R_{dc} = 30\ m\Omega$ and its inductance is estimated based on the cable's length and diameter to be $L_{dc} = 10\ \mu$H.

Experimental measurements are acquired using MDO4024 C Tektronix oscilloscope with THDP0200 differential voltage probe and SL261 current probes. The remainder of the section discusses the experiments and simulations by: 1) comparing symmetric to asymmetric six-phase VSI, in terms of voltage and current stress on the dc-capacitor; 2) validating the accuracy of the derived formulae; 3) comparing six-phase VSI to conventional three-phase counterpart; 4) practical considerations on the employment of the derived formulae.

A. Symmetric Versus Asymmetric Six-Phase VSI

Fig. 9 depicts the experimental measurements of the dc-capacitor voltage and current stresses at $PF = 0.6$ for symmetric and asymmetric loads for $M = 0.4$, 0.7, and 0.9. It can be observed that the dc-capacitor experiences a higher voltage and current stresses when the load is asymmetric, especially at low PFs. Therefore, the symmetric distribution leads to reduced voltage and current stress on the dc-capacitor.

To further analyze the voltage and current stresses on the dc-capacitor for the different load configurations, the experimentally obtained harmonic spectra of $\tilde{i}_{inv}$ and $\tilde{v}_c$ in Fig. 9(b) are shown in Fig. 10. The dominant harmonic of $\tilde{i}_{inv}$ and $\tilde{v}_c$ is at $2f_s$. This dominant harmonic is of the same magnitude for both load

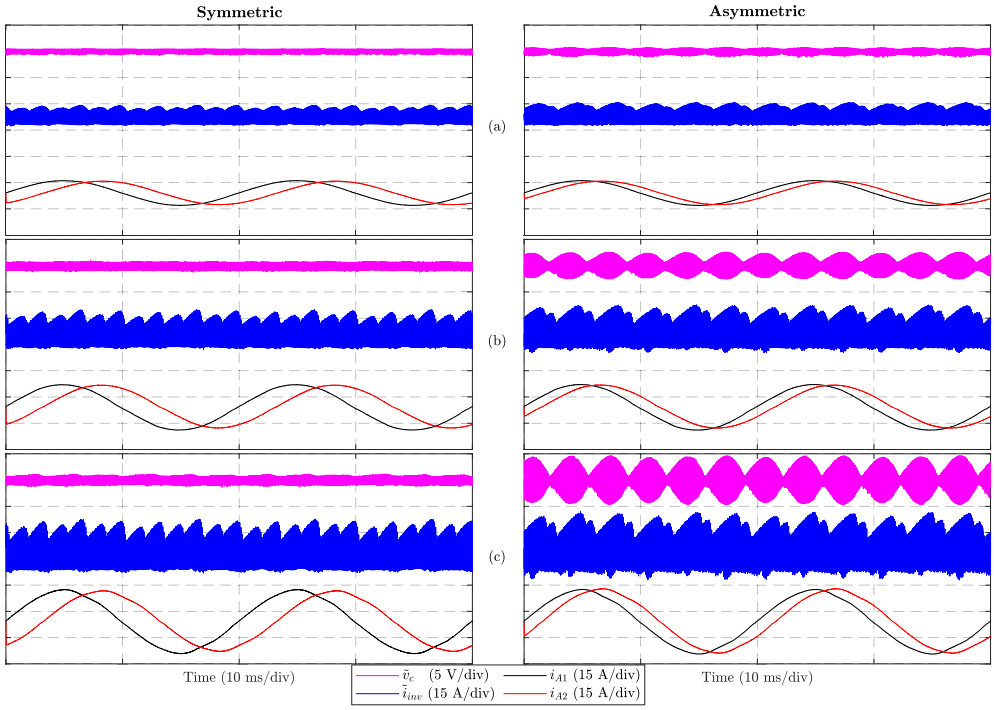


Fig. 9. Experimental results for DC-bus capacitor voltage and current ripples in six-phase VSI for symmetric (left column) and asymmetric (right column) loads ($f_1 = 50$ Hz, $f_s = 10$ kHz, $V_{dc} = 100$ V, $PF = 0.6$). (a) $M = 0.4$. (b) $M = 0.7$. (c) $M = 0.9$.

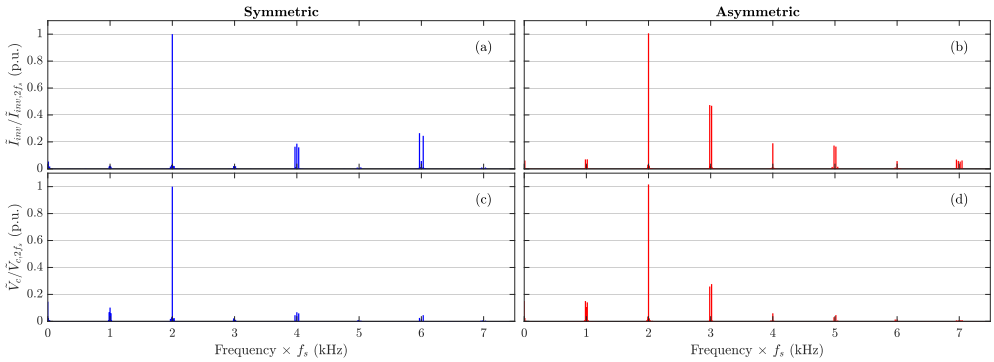


Fig. 10. Experimental harmonic spectra of DC-capacitor voltage and current ripples in six-phase VSI with symmetric (left column) and asymmetric (right column) loads ($f_1 = 50$ Hz, $f_s = 10$ kHz, $V_{dc} = 100$ V, $PF = 0.6$, $M = 0.7$). (a)–(b) $\tilde{I}_{inv,n}$. (c)–(d) $\tilde{V}_{c,n}$.

configurations, symmetric and asymmetric, when the operating conditions are similar. However, the harmonic distribution is different, which is why $\tilde{I}_{inv}$ and $\tilde{V}_c$ differ from one load configuration to the other. Sideband harmonics, $mf_s \pm nf_1$ around mf_s where m is an even multiple exist only in the asymmetric load for $\tilde{I}_{inv}$ and $\tilde{V}_c$ [see Fig. 10(b) and 10(d)]. Put otherwise, even sideband harmonics are cancelled when supplying a symmetric six-phase load. This confirms the harmonic analysis of the dc current ripple discussed in Section III-C. Furthermore, the harmonic spectra in Fig. 6(b) and 6(c) match the experimentally measured spectra in Figs. 10(a) and 10(b), respectively.

B. *Validity of the Derived Formulae*

For accuracy verification of the derived formulae of $\tilde{i}_{inv}$ and $\tilde{v}_c$ for symmetric and asymmetric six-phase VSI, a modulation index sweep is conducted at PF =0.6, 0.8, and 0.9. The measured RMS values of $\tilde{I}_{inv}$ and $\tilde{V}_c$, both experimentally and in simulation, are benchmarked against the computed values using the derived formulae. The simulations are conducted in MATLAB/Simulink using the same parameters in Table II, along with the IGBT module characteristics and dc-capacitor parasitics (series-connected RLC model) found in the datasheets. Fig. 11 show the measured and computed values of $\tilde{I}_{inv}$ and $\tilde{V}_c$ at the different PF points. A very good agreement between the measured, simulated, and computed $\tilde{I}_{inv}$ and $\tilde{V}_c$ is evident in Fig. 11, for both load configurations. Additionally, Fig. 11 reiterate the findings in Figs. 9 and 10 that the dc-capacitor experiences a higher voltage and current stress when supplying an asymmetric load. The root-mean-square error (rmse) between the calculated $\tilde{I}_{inv}$ and $\tilde{V}_c$ using the derived formulae and the experimentally measured counterparts over the range of

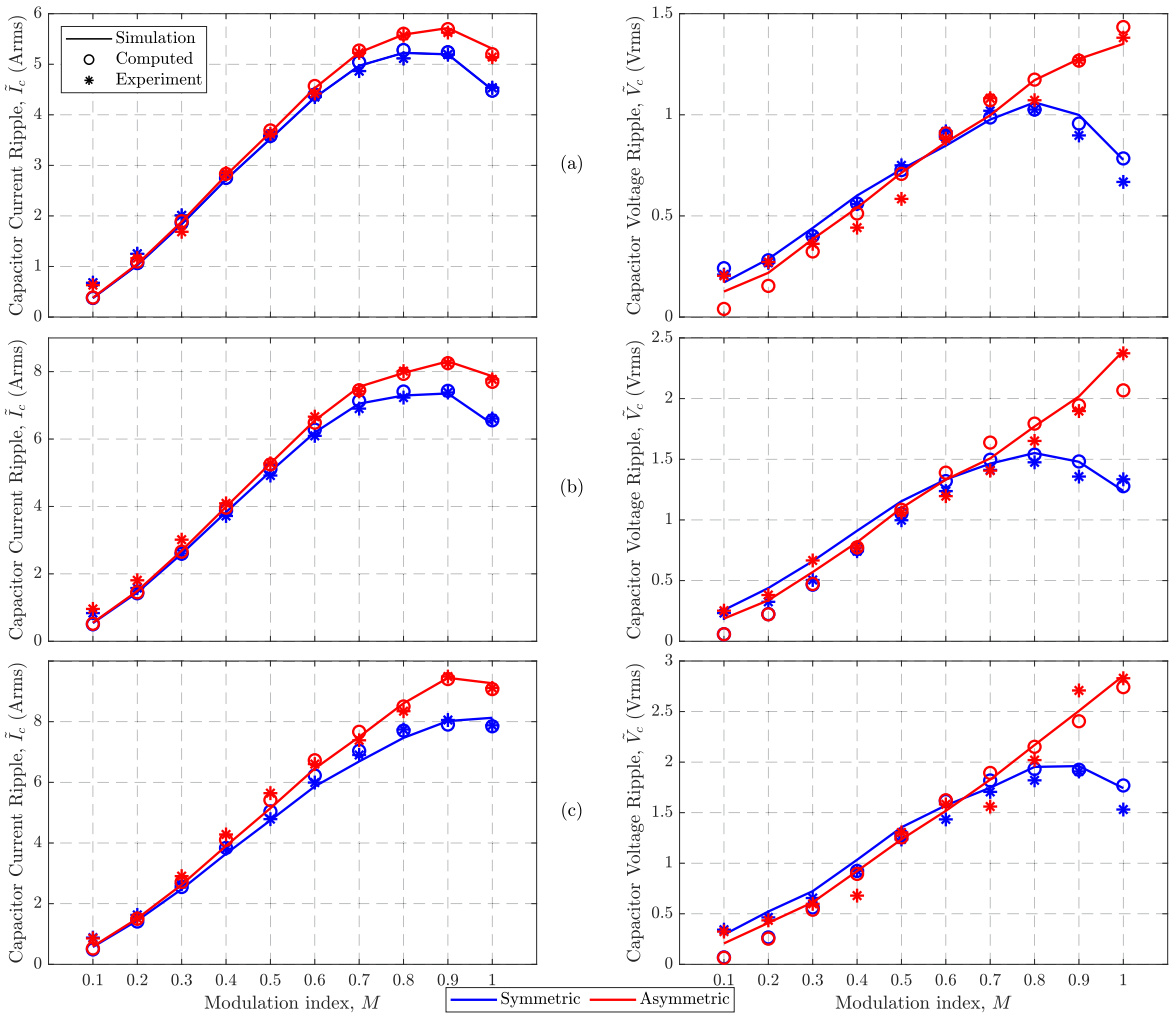


Fig. 11. Experimental verification of $\tilde{I}_{inv}$ formulae in (11) and (13) (left column) and $\tilde{V}_c$ formulae in (20) and (22) (right column) for symmetric and asymmetric six-phase loads, respectively. (a) $PF = 0.9$. (b) $PF = 0.8$. (c) $PF = 0.6$.

TABLE IV
ROOT-MEAN-SQUARE ERROR (RMSE) BETWEEN CALCULATED AND EXPERIMENTALLY MEASURED DC-CAPACITOR RMS VOLTAGE AND CURRENT RIPPLES

Configuration	Symbol	Eq.	PF	RMSE	Unit
Symmetric	$\tilde{I}_{inv}$	(11)	0.9	0.15	A
			0.8	0.18	
			0.6	0.29	
	$\tilde{v}_c$	(20)	0.9	0.05	V
			0.8	0.09	
			0.6	0.15	
Asymmetric	$\tilde{I}_{inv}$	(13)	0.9	0.12	A
			0.8	0.23	
			0.6	0.19	
	$\tilde{v}_c$	(22)	0.9	0.09	V
			0.8	0.18	
			0.6	0.20	

$M \in [0.1, 1]$ of Fig. 11 is given in Table IV. A very high accuracy of the derived formulae for $\tilde{I}_{inv}$ and $\tilde{V}_c$ is demonstrated with an rmse below using the derived formulae (11) and (13), for symmetric and asymmetric loads, respectively, with an rmse below 0.25 A and 0.20 V, respectively.

C. Six-Phase Versus Three-Phase VSI

To summarize the harmonic content of I_c for the three inverters, the content factor (CF) is computed for each harmonic group. The CF in this article is defined as the ratio of the rms square of the harmonics in a given group to the rms square of I_c, as

$$\text{CF} = \frac{\sum_{m,n} I^2_{c,mf_s \pm nf_1}}{I_c^2} \tag{27}$$

where the selection of m and n in the numerator is based on the aforementioned harmonic group definition. Table V summarizes the CF of each harmonic group for the three inverters, computed to the 600th harmonic. Table V confirms the fact that Group 2 harmonics are more dominant than Group 3 in three-phase VSI,

TABLE V
CONTENT FACTOR (CF) OF DC-CAPACITOR CURRENT HARMONIC GROUPS IN THREE- AND SIX-PHASE VSIS

Harmonic Group	3-phase	6-phase	
		Symm.	Asymm.
Group 1	36%	82%	70%
Group 2	46%	0%	29%
Group 3	18%	16%	0%

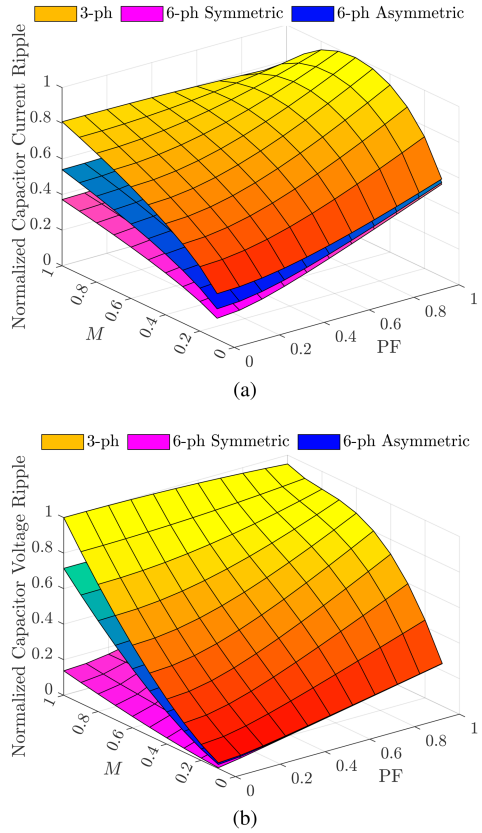


Fig. 12. Normalized voltage and current stresses on the DC-bus capacitor in three-phase and six-phase VSIs. (a) Current stress. (b) Voltage stress.

with a ratio of five to two. Thus, the elimination of Group 2 in the symmetric six-phase VSI yields the smallest I_c.

The same harmonic content analysis applies to the dc-capacitor voltage ripple, as demonstrated in Fig. 10(c) and 10(d), since $\tilde{V}_{c,n} = \tilde{I}_{c,n}/Z_{c,n}$, where Z_c is the impedance of the capacitor and the n subscript denotes frequency order. However, the ratio of voltage harmonic to current harmonic ($V_{c,n}/I_{c,n}$) is not the same for all nth harmonic in Fig. 10(c) and 10(d) as the reactance of the capacitor, $X_{c,n} = 1/(\omega_n C)$ decreases for higher frequencies.

To quantify the dc-capacitor requirement reduction in six-phase VSI, when compared to its three-phase counterpart, the dc-capacitor voltage and current ripples are evaluated over the entire operation envelop. Fig. 12 depicts the normalized $\tilde{I}_c$ (i.e., $\hat{I}_c = \tilde{I}_c/I_L$) and $\tilde{V}_c$ (i.e., $\hat{V}_c = \tilde{V}_c/K_v$) for three- and six-phase VSIs over M and $PF \in [0, 1]$. The normalized $\tilde{I}_c$ and $\tilde{V}_c$ maps are in line with the previous findings: six-phase VSI achieves lower

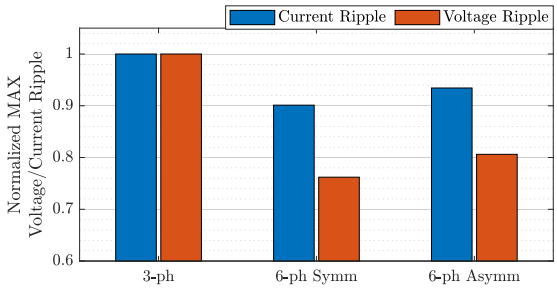


Fig. 13. Normalized maximum DC-capacitor voltage and current stress in three-phase and six-phase VSIs with symmetric and asymmetric loads.

dc-capacitor voltage and current ripples, and they are the lowest in the case of symmetric loads/machines. Since the dc-capacitor is always designed to handle the maximum voltage and current stresses, the normalized maximum voltage and current stresses in Fig. 12 are shown in Fig. 13. Six-phase VSI with symmetric loads/machines yields dc-capacitor voltage and current ripple reduction by 24% and 10%, respectively, compared to 20% and 7% for the asymmetric case, respectively, when benchmarked against the three-phase VSI. It is to be highlighted that current ripple handling by the dc-capacitor are usually the bottleneck in capacitor design for inverters operating beyond 10 kHz, and hence dominate the selection criteria.

D. Practical Considerations

The derived formulae for current and voltage ripples for the six-phase VSI were obtained under two main assumptions: very high capacitance of the dc-bus capacitor and very high switching frequency. The validity of such assumptions are assessed in this section.

1) Input Filter: Ideally, where the dc-side impedance is zero, the current ripple is supplied entirely by the source, and the capacitor voltage ripple is zero. However, some ripple exists in i_{dc} due to the stray inductance of the cables and the dc source. This can also occur when C is not large enough to sink all the ripples, as assumed earlier. In this case, the effect of L_{dc} becomes significant and must be evaluated. Fig. 14(a) depicts the equivalent dc circuit of the inverter.

Assuming a symmetrical pulsating i_{inv} with 50% duty cycle, as shown in Fig. 14(b), i_{inv} can be written as a summation of the dc (average) component and the high-frequency components as

$$i_{inv} = i_0 - \frac{4}{\pi} I_p \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \sin(2n\omega_s t) \tag{28}$$

where $i_0 = I_p/2$ is the average component passing through L_{dc}. By superposition and after phasor calculations, i_{dc} can be expressed as

$$i_{dc} = \frac{I_p}{2} - \frac{4}{\pi} I_p \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \sin(2n\omega_s t) \cdot \left| \frac{1/\omega_s C}{\omega_s L_{dc} - 1/\omega_s C} \right|. \tag{29}$$

Using (29), an inductance sweep code is run in MATLAB to investigate the change in the current ripple with different L_{dc}

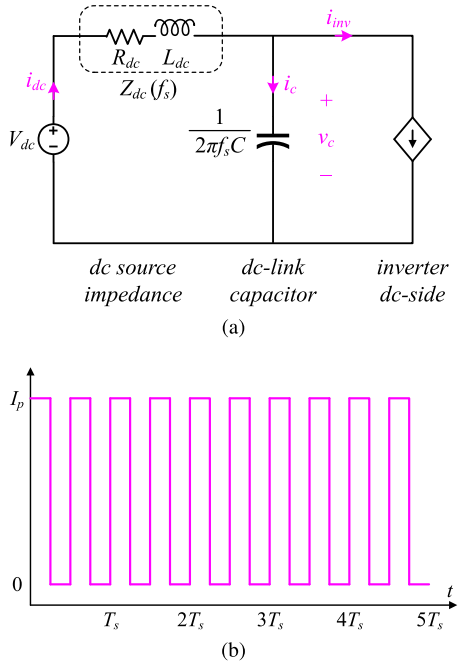


Fig. 14. Equivalent circuit of the DC-side of the inverter at the switching frequency, f_s. (a) Circuit diagram. (b) i_{inv} waveform.

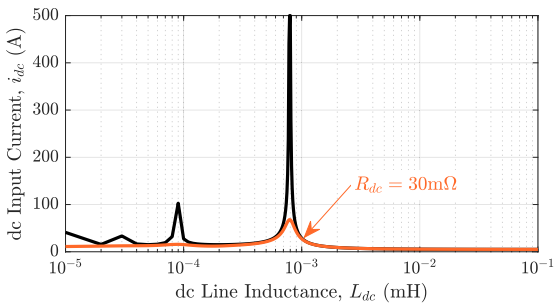


Fig. 15. DC input current i_{dc} versus DC line inductance L_{dc}.

values. The resulting i_{dc} waveform at $f_s = 10$ kHz with $I_p = 10$ A and $C = 80$ μF is shown in Fig. 15. The values of L_{dc} at which i_{dc} spikes are the values where L_{dc} and C resonate with the switching frequency and its odd multiples. However, practically, the series resistances of the dc cables and the ESR of the dc capacitor limit the spike value at the resonant frequency, as demonstrated by the orange trace in Fig. 15 when considering $R_{dc} = 30$ mΩ. The maximum current ripple is suppressed at all operating conditions, especially at resonant points. In this article, L_{dc} is assumed to be $\geq 2/(\omega_s^2 C)$. In this region, the dc-side current only supplies the dc current and almost all current ripple passes through the capacitor, i.e., $\tilde{i}_{dc} = 0$.

2) Modulation Frequency: The derived formulae for the dc current and voltage ripples assume mostly sinusoidal output currents. However, this assumption is only valid under certain circumstances for m_f. In order to determine the validity of the analysis under different values of m_f and M, extensive simulations were performed over a range of values for the two foregoing variables. The range for M is 0.1–0.9 with steps of 0.1.

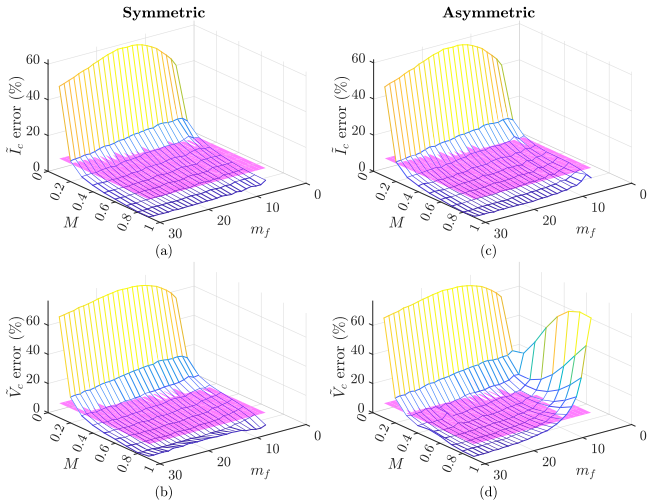


Fig. 16. Calculation error of derived formulae for current ripple, $\tilde{I}_c$ and voltage ripples, $\tilde{V}_c$ in six-phase symmetric (left column) and asymmetric (right column) load configuration as a function of modulation frequency, m_f and modulation index, M.

The range for m_f is 6–30, with steps of 1. The error in the values of calculated and measured current and voltage are depicted in the Fig. 16 for both symmetrical and asymmetrical loads. The pink plane is the threshold for a 10% calculation error. The error decreases with the increase in the values of m_f and M.

In summary, the following conditions must be met for $\leq$10% calculation error using the derived formulae dc current and voltage ripple estimation in six-phase inverters.

1) The switching frequency is higher than or equal to ten times the output fundamental frequency, i.e., $f_s \geq 12 f_1$ or $m_f \geq 12$.
2) The switching frequency is higher than or equal to the $\sqrt{2}$ of the resonant frequency of the dc-side filter, $f_r = 1/(2\pi\sqrt{L_{dc}C})$, i.e., $f_s \geq \sqrt{2} f_r$. This can alternatively be expressed as $L_{dc} \geq 2/(\omega_s^2 C)$.
3) The output ac currents are balanced, and their total harmonic distortion (THD) is $\leq$15%.
4) The modulation index, M is ≥ 0.3.

The foregoing conditions are normally fulfilled in motor drive applications employing high frequency switching devices, and therefore, the derived formulae are applicable over a wide range of operating conditions.

VII. Conclusion

Detailed analyses of dc-bus voltage and current ripples in six-phase symmetric and asymmetric VSIs were presented in this article. The analyses rendered, for the first time, analytical formulae to evaluate the voltage and current stresses on the dc-capacitor in six-phase VSI supplying symmetric and asymmetric loads. The accuracy of the derived formulae was verified by simulation and experimental testing. The derived formulae can evaluate the dc-capacitor voltage and current ripple over a wide range of operating conditions. Subsequently, simple capacitor sizing rules for symmetric and asymmetric six-phase VSIs were

proposed for SPWM. Furthermore, the harmonic spectra of the dc-capacitor current in six-phase VSI was analyzed and benchmarked against its conventional three-phase counterpart. The spatial distribution of the additional three-phases in six-phase VSI leads to cancelation of some dominant carrier-sideband harmonics that renders reduced current stress on the dc-capacitor. This in turn yields a reduced capacitor size in six-phase VSI when compared to its three-phase counterpart, for the same VA rating. The current stress is minimized when the supplied load/machine is of symmetric spatial distribution with 10% reduction when compared to three-phase VSI, or 3% lower than six-phase asymmetric loads.

The derived formulae are beneficial for dc-capacitor selection in six-phase VSIs based on voltage and current ripples ratings, and can be used for capacitor derating and lifetime prediction.

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