Bidirectional Buck–Boost Converter With Reduced Power Loss and No Right-Half-Plane Zero

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***Abstract*—This article presents a novel hybrid bidirectional buck–boost converter (HBBC) for lithium-ion battery management. Unlike the conventional four-switch buck–boost converter (FBBC), whose power efficiency is greatly limited at heavy loads mainly due to high conduction loss from a high dc resistance (DCR) inductor, the proposed HBBC adopts assisted capacitive paths to reduce the current stress on the main inductive path. Thus, the conductive loss of inductor's DCR is greatly reduced in both the buck and boost modes. To verify the effectiveness of the proposed structure, detailed analyses on both the loop performance and conduction loss are provided. Compared with FBBC, the conversion efficiency of the proposed HBBC is increased by 23.3% in the boost mode, and the peak efficiency is up to 97.8% with an adopted inductor with a DCR of 270 mΩ.**

***Index Terms*—Battery management, bidirectional dc–dc converter, buck–boost converter, high-DCR inductor.**

I. Introduction

FOR mobile electronic devices, a 5-V universal serial bus (USB) receptacle is commonly used to power electronic devices or/and refresh rechargeable batteries, as shown in Fig. 1(a). The load module, which consists of a processor, sensors, etc., is connected to both the USB charger and the regulated output of the proposed bidirectional dc–dc converter with input from a battery. When plugged in, the excess energy from the USB charger, which is beyond the load requirement in idle or working mode, will be fed into the battery. Meanwhile, the battery serves as an energy buffer, supplying load peaks that may momentarily exceed the input current limit. When unplugged, the battery supplies the stored energy to the loads by discharging itself. Typically, the battery's charging and discharging functions are controlled by two separated power modules. A bidirectional dc/dc converter, which combines the two power modules together, achieves a compact design and reduces system cost [1], [2].

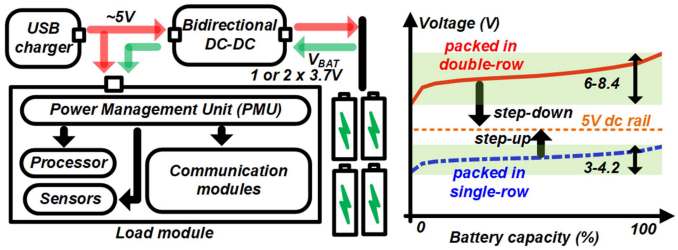

Fig. 1. Block diagrams of the battery-powered devices. (b) Li-ion battery voltage curves related to their energy capacity.

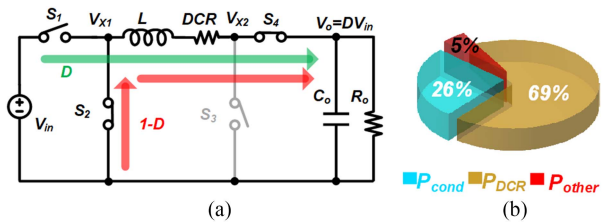

Fig. 2. (a) Power stage of the conventional FBBC and its operation in the buck mode. (b) Power loss distribution of FBBC at $V_{\rm in} = 7.4$ V, $V_o = 5$ V, DCR = 270 mΩ, and $I_o = 1$ A.

Lithium-ion (Li-ion) batteries have been widely utilized in electronic devices, given their longer runtime, portability, and convenient charging [3]. The nominal voltage of Li-ion batteries is 3.7 V per cell, and a battery pack can connect the cells in parallel to increase the capacity and/or in series to increase the voltage level, as illustrated in Fig. 1(a). The previously mentioned bidirectional converter acts as an interlink between the 5-V dc rail and the Li-ion battery packs. When a single-row Li-ion battery (i.e., 3.7 V) is adopted, the bidirectional dc/dc converter charges the battery in the step-down mode (buck) whereas discharges it in the step-up mode (boost), as shown in Fig. 1(b). However, when the Li-ion battery is stacked in two rows (i.e., 7.4 V), the charging process turns into the boost mode, whereas the discharging process operates in the buck mode instead. Thus, the conventional four-switch buck–boost converter (FBBC) with bidirectional power-flow and step-up/down features, as shown

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in Fig. 2(a) [4], is often used in the battery management system (BMS).

Low-profile and long-runtime portable electronic devices are always preferable in the market. These impose strict constraints on the efficiency and profile of the BMS. The size specifications of BMS, especially the height, are generally limited by the adopted power inductors used in the embedded dc/dc converters. Unfortunately, shrinking the inductor's size inevitably increases its dc resistance (DCR). For example, when the profile of a 4.7-μH inductor from TDK is reduced from $13 \times 12.5 \times 6.4$ mm^3 [5] to $3.2 \times 3 \times 1.2$ mm^3 [6], its DCR is increased dramatically from 7.1 to 270 mΩ. Thus, it is difficult to achieve high efficiency at heavy loads with a low-profile inductor. Fig. 2(b) shows the comparison of the power loss components when the converter works in the buck mode at a 1-A load, where the power loss by the DCR (P_{DCR}) takes up 69% of the overall power loss and is more than a double of the conduction loss by switches (P_{cond}) [7].

Multiphase buck converter was reported to reduce P_{DCR}. The large load current is averaged among different switching phases [8], [9], [10], [11], [12]. Yet, the multiphase converter increases production cost and design complexity. In [13], [14], and [15], a dual-path scheme with one inductive power path and another capacitive power path was introduced to alleviate the current stress on the inductor. However, only either buck or boost mode is achieved. Although the buck–boost operation is implemented in [4], [16], [17], and [18], the properties of unidirectional power flow and restricted inductive current reduction still limit its application for BMS. Moreover, the conventional boost converter suffers from the right-half-plane (RHP) zero in its transfer function, which worsens the circuit performance and complicates the compensation design. In [14], although the conversion efficiency is improved via the dual-path power delivery scheme in its boost operation, the RHP zero is not eliminated but pushed farther into the RHP, thus weakening its effect on the system response. In [19], a tristate boost converter is presented to eliminate the RHP zero with the cost of reduced efficiency, and the efficiency drop is even worse with a high-DCR inductor being utilized. Generally, there is no RHP zero issue in the buck converter. However, when it comes to the dual-path hybrid buck converters presented in [12], [13], and [15], the efficiency is improved with the penalty of degraded system performance by introducing an RHP zero. Thus, it is desirable to develop a buck–boost converter that has both the RHP-zero-free and high-conversion-efficiency features.

In this article, a bidirectional hybrid buck–boost converter (HBBC) for high-efficiency Li-ion battery management is proposed using a low-profile inductor (i.e., no low-DCR inductor needed). The high-efficiency feature is achieved by reducing the average inductor current magnitude in both the buck and boost modes, with the help of assistive capacitive power paths. Moreover, the symmetrical circuit structure of the proposed HBBC enables bidirectional power flow. Additionally, the RHP zero is removed in both the buck and boost operations of the proposed converter.

The rest of this article is organized as follows. In Section II, the working mechanisms of the proposed HBBC will be explained in detail. A comprehensive analysis on the proposed converter's loop performances and conduction loss will be given in Section III. Measurement results and performance comparison will be provided in Section IV. Finally, Section V concludes this article.

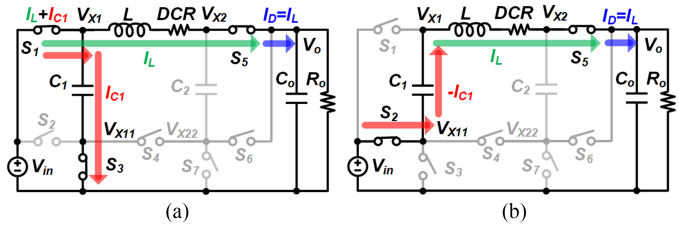

Fig. 3. Operation of the proposed HBBC in the boost mode and its switching states and current flows in (a) phase 1 and (b) phase 2.

II. Proposed Bidirectional Buck–Boost Converter

A. Boost Mode

The HBBC consists of one inductor (L), an output capacitor (C_o), two flying capacitors (C_1 and C_2), and seven switches (S_1–S_7), as shown in Fig. 3. When the input voltage (V_{in}) is lower than the desired output voltage (V_o), the converter operates in the boost mode. In this mode, S_1, S_3, and S_2 are switched in a complementary way, whereas S_5 is always ON, and S_4, S_6, and S_7 are always OFF. The two-phase operation of the proposed HBBC is shown in Fig. 3. In phase 1, S_1 and S_3 are turned ON to charge the flying capacitor C_1 to V_{in}. Simultaneously, the energy is transferred to the output (i.e., V_o) via the inductive path (denoted in green). In phase 2, S_2 is turned ON, whereas S_1 and S_3 are OFF. During this phase, C_1 acts as a voltage source, and the inductor current (I_L) ramps up as the voltage drop across L ($= 2\,V_{\mathrm{in}} - V_o$) is positive. By periodically repeating phases 1 and 2, the output delivery current (I_D) of the proposed HBBC is transferred to V_o continuously. The conversion ratio M ($= V_o/V_{\mathrm{in}}$) can be derived from the inductor's voltage-second balance as follows:

$$D\,(V_{\mathrm{in}} - V_o) + (1 - D)\;(2V_{\mathrm{in}} - V_o) = 0 \tag{1}$$

$$M = V_o/V_{\mathrm{in}} = \;2 - D,\;(0 < D < 1) \tag{2}$$

where D is the duty cycle of phase 1. Similarly, the capacitor current (I_{C1}) during phase 1 ($\Phi 1$) and I_L can be obtained by the capacitors' charge balance as follows:

$$I_{C1,\,\Phi 1} = I_L\,(1 - D)\,/D \tag{3}$$

$$I_L = I_O \tag{4}$$

whereI_O is the output current

In (2), since D varies from 0 to 1, M changes from 2 to 1. When considering the discharging process of the single-row Li-ion battery, V_{in} changes from 3 to 4.2 V, depending on the battery's energy capacity, as shown in Fig. 1(b). Thus, to generate the desired output of 5 V, the required step-up conversion ratio is from 1.2 to 1.7, which can be satisfied by the proposed HBBC in the boost mode.

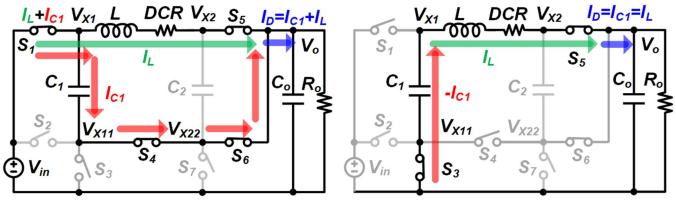

Fig. 4. Operation of "partial-dual-path" buck-mode HBBC and its switching states and current flows in (a) phase 1 and (b) phase 2.

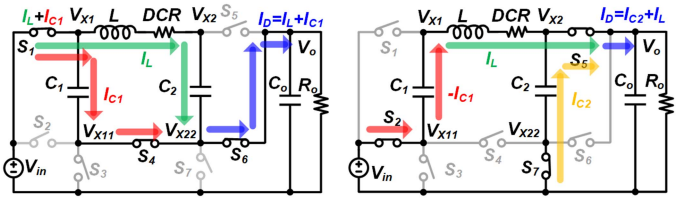

Fig. 5. Operation of the proposed "always-dual-path" HBBC in the buck mode and its switching states and current flows in (a) phase 1 and (b) phase 2.

B. "Partial-Dual-Path" Buck Mode

When V_{in} is higher than V_o , the converter operates in the buck mode. In this mode, only switches S_1, S_3, and S_4 take the switching actions. Meanwhile, S_5 and S_6 are always ON, and S_2 and S_7 are always OFF. The two-phase operation for this step-down converter is shown in Fig. 4. In phase 1, S_1 is turned ON to build up I_L, as shown in Fig. 4(a). Simultaneously, S_4 is ON, and C_1 is connected in series with V_o to form a capacitive power path (denoted in red). Then, I_D is the sum of I_L and I_{C1}. In phase 2, S_3 is turned ON, whereas S_1 and S_4 are OFF. Accordingly, L and C_1 are connected in series. As the inductor keeps its I_L status as a current source, I_{C1} is set to I_L flowing to V_o through L. Based on the above-mentioned descriptions, it can be found that I_D is divided into dual paths only in phase 1, and thus this kind of circuit is named as "partial-dual-path" buck-mode HBBC. M is calculated as follows:

$$D\left(V_{\text{in}}-V_o\right)+(1-D)\ \left(V_{\text{in}}-2V_o\right)=\ 0 \tag{5}$$

$$M=V_o/V_{\text{in}}=1/\left(2-D\right),(0<D<1). \tag{6}$$

From the charge balance of C_1 and C_{o}, the following relationships can be derived:

$$I_{C,\,\Phi 1}=I_L\ \left(1-D\right)/D \tag{7}$$

$$I_L=I_O\ /\left(2-D\right). \tag{8}$$

In (6), as D varies from 0 to 1, M ranges from 0.5 to 1. When it comes to the discharging process of the double-row Li-ion battery, V_{in} changes from 6 to 8.4 V depending on the energy capacity of the battery pack. Thus, to produce the desired output of 5 V, the required step-up conversion ratio is from 0.6 to 0.83, which can be satisfied by this "partial-dual-path" buck-mode HBBC.

C. "Always-Dual-Path" Buck Mode

In the above-mentioned "partial-dual-path" buck mode, only one flying capacitor (C_1) is utilized, whereas C_2 is simply shorted. Thus, the "always-dual-path" scheme is ultimately designed to utilize both C_1 and C_2, where the dual-path power delivery is achieved in both phase 1 and phase 2. The two-phase operation for the "always-dual-path" buck-mode HBBC is shown in Fig. 5. It can be found that no extra switches or passive components are required. In this mode, switches S_1, S_2, S_4, S_5, S_6, and S_7 take the switching actions, whereas S_3 is always OFF.

During phase 1, S_1, S_4 and S_6 are turned ON, whereas S_2, S_5 and S_7 are OFF, as shown in Fig. 5(a). Thus, L and C_2 are connected in series to build an inductive power path (denoted in green), and C_1 is connected to V_o to form a capacitive power path (denoted in red). Then, I_D is the sum of I_L and I_{C1}.

During phase 2, S_2, S_5, and S_7 are switched ON, whereas S_1, S_4, and S_6 are OFF. At this time, the inductive path is composed of L and C_1, and the capacitive path is built by C_2. Thus, I_D is the sum of I_L and I_{C2} in phase 2.

Therefore, I_D is always divided into dual paths in both phases, and the "always-dual-path" property is achieved. Based on the above-mentioned descriptions, M in the "always-dual-path" buck-mode HBBC is calculated as follows:

$$D\left(V_{\text{in}}-2V_o\right)+(1-D)\ \left(2V_{\text{in}}-2V_o\right)=\ 0 \tag{9}$$

$$M\ =V_o/V_{\text{in}}\ =\left(2-D\right)/2\ ,\ (0<D<1). \tag{10}$$

From the charge balance of C_1, C_2, and C_o, the following relationships can be derived:

$$DI_{C1,\,\Phi 1}-(1-D)\ I_L=\ 0 \tag{11}$$

$$(1-D)\,I_{C2,\,\Phi 2}-D\,I_L=\ 0 \tag{12}$$

$$(I_L+I_{C1,\,\Phi 1})D+(I_L+I_{C2,\,\Phi 2})\ (1-D)-I_O=\ 0. \tag{13}$$

Equations (11)–(13) can be simplified as follows:

$$I_{C1,\,\Phi 1}=I_L\ \left(1-D\right)/D \tag{14}$$

$$I_{C2,\,\Phi 2}=I_L\ D/\left(1-D\right) \tag{15}$$

$$I_L=I_O\ /2. \tag{16}$$

In (10), as D varies from 0 to 1, M of the "always-dual-path" buck mode ranges from 1 to 0.5, which is the same as that of the "partial-dual-path" buck mode. In (16), I_L is unrelated to D and always equals half of I_O, which is the theoretically lowest I_L achieved by (8). The reduced I_L further decreases P_{DCR} when compared with the "partial-dual-path" scheme, and thus the "always-dual-path" method is finally selected for the step-down conversion of the proposed HBBC.

D. Bidirectional Operation of HBBC

When the power provided by the USB receptacle is more than that consumed by the device's normal operation, the battery pack changes its role from "discharging" to "charging." Taking the double-row battery as an example, the reverse boost operation of

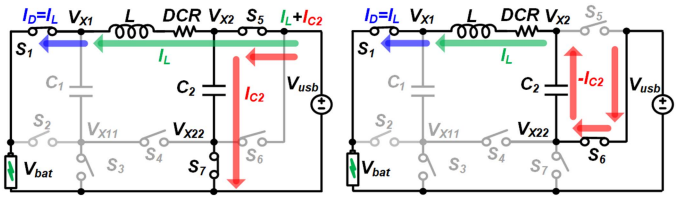

Fig. 6. Operation of the proposed HBBC in the reverse boost mode and its switching states and current flows in (a) phase 1 and (b) phase 2.

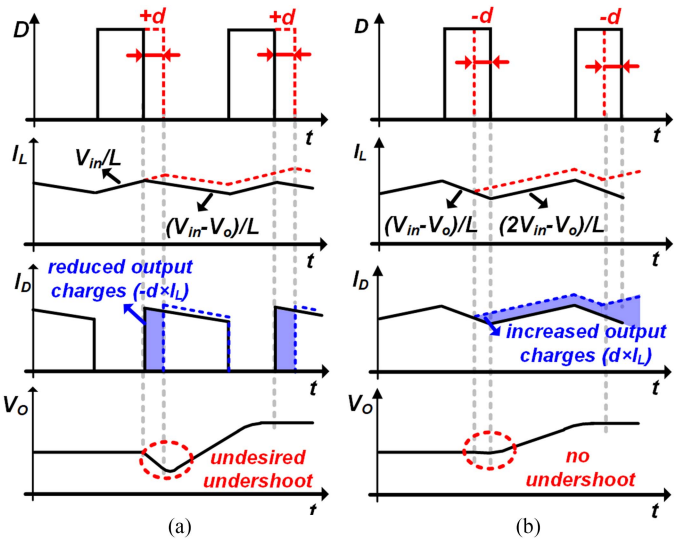

Fig. 7. Current and voltage waveforms when D brutally changes for (a) boost-mode FBBC and (b) proposed boost-mode HBBC.

HBBC is illustrated in Fig. 6, where V_{usb} is the 5-V USB voltage and the required V_{bat} is around 7.4 V. Similar to the previous forward boost operation presented in Section II-A, only S_5, S_6, and S_7 take the switching actions, whereas S_1 is always ON, and S_2, S_3, and S_4 are always OFF. In phase 1, S_5 and S_7 are turned ON, and S_6 is OFF. Thus, the flying capacitor C_2 is charged to V_{usb}. In phase 2, S_6 is switched ON, whereas S_5 and S_7 are OFF. In this case, the switching node (i.e., V_{X2}) rises to 2 V_{usb} , and I_L ramps up. The required M from V_{usb} of 5 V to V_o of 7.4 V is 1.48, which can be satisfied according to (2). Similar analysis can be extended to the reverse buck operation.

III. Operation and Power Loss Analysis

A. Analysis on RHP Zero in the Boost Mode

In the conventional boost-mode FBBC, V_o ($= V_{\text{in}}/(1-D)$) becomes higher with a larger D. However, when there is a brutal increase in D, the output current of the boost-mode FBBC, which is given by $I_L(1-D)$, is reduced, which temporarily causes a voltage drop at V_o, as demonstrated in Fig. 7(a). This contradictory phenomenon is due to the RHP zero in the boost-mode FBBC, which limits the bandwidth and worsens the transient response [20]. The RHP zero of the boost-mode FBBC is written

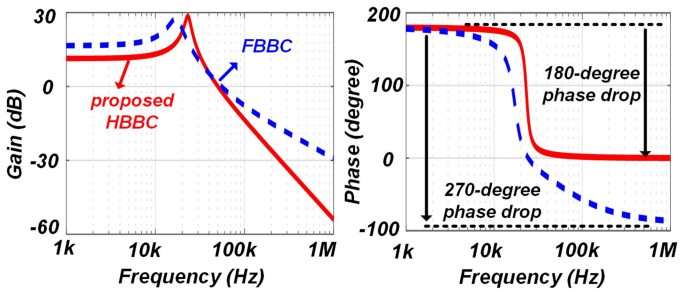

Fig. 8. Loop performance comparison between the boost-mode FBBC and the proposed boost-mode HBBC.

as follows [21]:

$$\omega_z = (1-D)^2 R_o/L. \tag{17}$$

From (17), this RHP zero is located at a lower frequency under a heavier load with larger inductance and higher duty cycle. Although operating the dc–dc converter at a higher frequency can move the RHP zero to a higher frequency due to the availability to use a smaller inductance, power efficiency is degraded seriously due to higher switching loss. Fortunately, the proposed HBBC can solve this RHP-zero problem without increasing switching frequency (f_{sw}). Since V_o ($= V_{\text{in}}(2-D)$) of the proposed HBBC in the boost mode increases with a reduced D, D is shrunk by $-d$ for comparison fairness, as shown in Fig. 7(b). Compared with the boost-mode FBBC, I_L of the proposed HBBC is continuously transferred to the output in both phase 1 and phase 2. Therefore, the output charges increase with a narrower D, and no undershoot will be observed. Thus, the RHP zero is removed from the boost mode of the proposed HBBC.

To mathematically verify its effectiveness, the transfer function of the boost-mode HBBC, $G_{vd,\text{bo}}(s)$, is written as below. It is noted that the detailed calculation to achieve (18) has been included in Appendix I. In (18), there exist two poles only but no RHP zero. In Fig. 8, the bode plots of the transfer functions for the boost-mode FBBC and

$$G_{vd,\text{bo}}\ (s) = \frac{V_O}{2-D} \cdot \frac{1}{LC_o s^2 + \frac{L}{R_o} s + 1} \tag{18}$$

the proposed boost-mode HBBC are drawn. Due to the existence of an RHP zero and two poles in the boost-mode FBBC's transfer function, the total phase drop is 270°. Yet, the total phase drop for the boost-mode HBBC is only 180° after the removal of RHP zero.

B. Analysis on RHP Zero in the Buck Mode

Although the "partial-dual-path" buck-mode HBBC has the same conversion range (i.e., 0.5–1) and similar switching scheme with its "always-dual-path" counterpart, their ac performances are much different.

Following the RHP-zero analysis shown in Fig. 7, a brutal duty increase (i.e., $+d$) is applied to the "partial-dual-path" buck-mode HBBC, as shown in Fig. 9(a). Note that only the negative

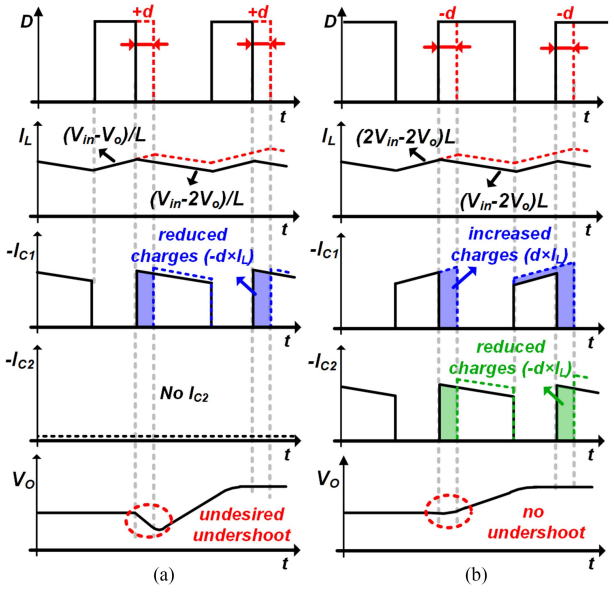

Fig. 9. Current and voltage waveforms when D brutally changes for (a) "partial-dual-path" buck-mode HBBC and (b) "always-dual-path" buck-mode HBBC.

part of I_{C1} is plotted, whereas the positive part of I_{C1} can be simply derived based on the capacitor's charge balance [14]. From (6), V_o ($= V_{\text{in}}/(2-D)$) is expected to be higher with a larger D. However, compared with the slowly rising I_L, the capacitive charge provided by C_1 ($= I_L(1-D)$) is decreased instantly by the amount of $-d\times I_L$, which causes an undershoot at V_o. Similar to the previous analysis for the boost-mode FBBC, this phenomenon is due to the RHP zero in the "partial-dual-path" buck-mode HBBC.

Fortunately, this RHP zero is removed in the proposed "always-dual-path" buck-mode HBBC. Since M ($=(2-D)/2$) increases with a smaller D in this mode, a brutal decrease "$-d$" is applied to D, as shown in Fig. 9(b). Similarly, only the negative parts of I_{C1} and I_{C2} are plotted for simplicity. From (11) and (12), when D becomes smaller, the output charge by C_2 ($=DI_L$) is reduced by $-d\times I_L$, whereas the one by C_1 ($=(1-D)I_L$) is increased by $d\times I_L$. In this case, the output charge decreases in C_2 (i.e., $-d\times I_L$) is counteracted by the output charge increases in C_1 (i.e., $d\times I_L$). Furthermore, it is important that their sum (I_L) is increased with a smaller D, and thus the RHP zero is removed.

To verify the effectiveness, the corresponding transfer functions of the "partial-dual-path" and "always-dual-path" buck modes (i.e., $G_{vd,\text{bu\_partial}}(s)$ and $G_{vd,\text{bu\_always}}(s)$) are also derived. Again, the detailed calculation steps have been included in Appendix I. It is noted that an RHP zero ($\omega_z = R_o(2-D)^2/L$) is introduced in (19), whereas no RHP zero exists in (20)

$$G_{vd,\text{bu\_partial}}(s)=\frac{\hat{v}_o}{\hat{d}}=\frac{V_O}{2-D}\cdot\frac{1-\frac{L}{R_o(2-D)^2}s}{\frac{L(C_O+C_1)}{(2-D)^2}s^2+\frac{L}{R_o(2-D)^2}s+1} \tag{19}$$

$$G_{vd,\text{bu\_always}}(s)=\frac{\hat{v}_o}{\hat{d}}=\frac{V_O}{2-D}\cdot\frac{1}{\frac{L(C_O+C_1+C_2)}{4}s^2+\frac{L}{4R_o}s+1}. \tag{20}$$

C. Operation Analysis on Flying Capacitors

In the proposed "partial-dual-path" and "always-dual-path" buck modes, the voltages across C_1 and C_2 (i.e., V_1 and V_2) are easily fixed to constant values (i.e., $(V_{\text{in}}-V_o)$ for V_1 and V_o for V_2) without any particular schemes, unlike that of the flying capacitor in the three-level buck converter [22].

In (7), (11), and (12), the descriptions are based on the steady states, where the capacitors' voltage variations (i.e., ΔV_1 and ΔV_2) are considered as zero. To make the analysis more complete, the operations of C_1 and C_2 during load transients are discussed in the following, where ΔV_1 and ΔV_2 are no longer zero.

In the "partial-dual-path" buck mode, the equation based on charge balance of C_1 is written as follows:

$$DT_sI_{C1,\Phi1}-(1-D)T_s\,I_L=C_1\Delta V_1=C_1\Delta(V_{\text{in}}-V_o) \tag{21}$$

where T_s is the switching period. Assuming that V_{in} is constant (i.e., $\Delta V_{\text{in}}=0$), $I_{C1,\Phi1}$ is rederived as follows:

$$I_{C1,\Phi1}=(1-D)I_L/D-C_1\Delta V_o/DT_s. \tag{22}$$

Compared with (7), the effect of ΔV_o is introduced to $I_{C1,\Phi1}$. As illustrated in Fig. 9(a), when D increases suddenly, an undesired undershoot will be observed at V_o (i.e., $\Delta V_o<0$) due to the reduced $I_{C1,\Phi1}$. Yet, the drop in $I_{C1,\Phi1}$ is counteracted by this negative ΔV_o, and thus the undershoot at V_o is alleviated when compared with the conventional FBBC without capacitive power path(s). In this way, it explains why the position of the RHP zero (i.e., $\omega_z = R_o(2-D)^2/L$) in the "partial-dual-path" buck-mode HBBC is higher than that (i.e., $\omega_z = R_o(1-D)^2/L$) in the boost-mode FBBC.

When it comes to the "always-dual-path" buck mode, (11) and (12) are rewritten as follows:

$$DT_sI_{C1,\Phi1}-(1-D)T_s\,I_L=C_1\Delta(V_{\text{in}}-V_o) \tag{23}$$

$$(1-D)T_sI_{C2,\Phi2}-DT_s\,I_L=-C_2\Delta V_{22}=-C_2\Delta V_o. \tag{24}$$

Assuming that 1) C_1 and C_2 are equal and 2) V_{in} is constant (i.e., $\Delta V_{\text{in}}=0$), the summed capacitive current $I_{C,\text{sum}}$ is derived as follows:

$$I_{C,\text{sum}}=DI_{C1,\Phi1}+(1-D)\,I_{C2,\Phi2}=I_L-2C_1\Delta V_o/T_s. \tag{25}$$

From (25), $I_{C,\text{sum}}$ is not exactly the same as I_L when ΔV_o is not zero. To illustrate the effect of ΔV_o on $I_{C,\text{sum}}$, the voltage and current waveforms during the load transients between 1 and 2 A loading currents are plotted in Fig. 10. It is noted that $I_{C1,\Phi1}$, $I_{C2,\Phi2}$, $I_{C,\text{sum}}$, and I_L are averaged over one switching period for easier observation. Take the step-up load transient for example, the averaged capacitive currents (i.e., $I_{C1,\Phi1}$, $I_{C2,\Phi2}$, and $I_{C,\text{sum}}$) are increased instantly with the undershoot at V_o (i.e., $\Delta V_o<0$), as shown in Fig. 10(a). Yet, the rising edge of

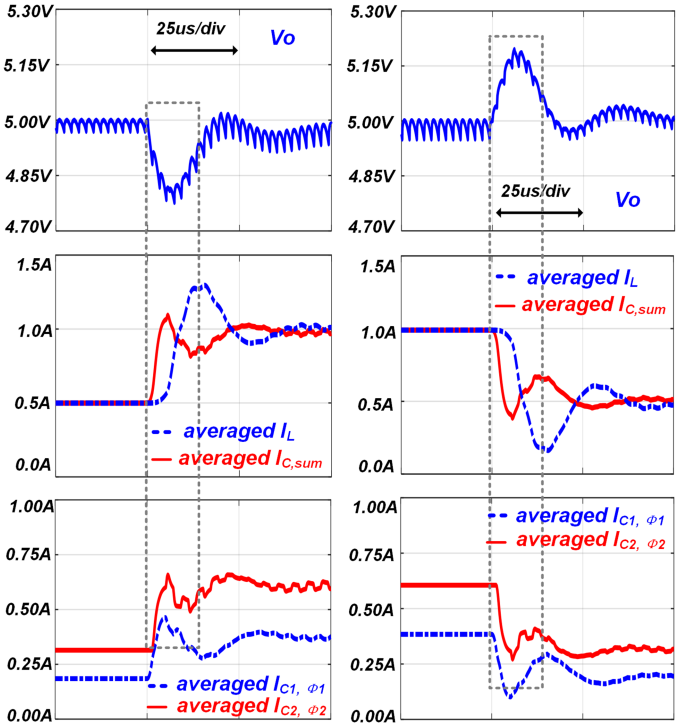

Fig. 10. Simulated waveforms of V_o and averaged I_L, $I_{C,\mathrm{sum}}$, $I_{C1,\Phi1}$, and $I_{C2,\Phi2}$ in the "always-dual-path" buck mode. (a) Step-up load transient from 1 to 2 A. (b) Step-down load transient from 2 to 1 A.

I_L lags behind that of $I_{C,\mathrm{sum}}$. Similarly, the averaged $I_{C,\mathrm{sum}}$ also leads before I_L during the step-down load transient, as shown in Fig. 10(b). Compared with the single capacitive power path in "partial-dual-path" buck-mode HBBC, the instant response of dual capacitive power paths in its "always-dual-path" counterpart further reduces the undershoot and overshoot during the load transients. Meanwhile, it can be observed that the averaged $I_{C,\mathrm{sum}}$ is equal to the averaged I_L after the converter is settled down (i.e., $\Delta V_o = 0$).

D. Power Loss Analysis

To simplify the analysis, the current ripple is ignored for the heavy load application [8], and the ON-resistance of all switches is assumed to be the same and denoted as R_{on}. Given that the capacitor's equivalent series resistance (ESR) is generally much lower than the inductor's DCR and switches' ON-resistance, it is neglected in the conduction loss in this calculation [13].

First, the conduction loss ($P_{\mathrm{FBB,\ cond|boost}}$) of FBBC in the boost mode, which is the sum of S_1, S_3, S_4, and DCR in Fig. 2(a), is given as follows:

$$P_{\mathrm{FBB,\ cond|boost}} = (2R_{\mathrm{on}} + DCR)\ I_o^2 M^2. \tag{26}$$

Then, the conduction loss ($P_{\mathrm{HBB,\ cond|boost}}$) of HBBC in the boost mode is given as follows:

$$P_{\mathrm{HBB,\ cond|boost}} = (1-D)\ (2R_{\mathrm{on}} + DCR)\, I_L^2 + DR_{\mathrm{on}}(I_L + I_{C1})^2 + DR_{\mathrm{on}} I_{C1}^2 + D\,(DCR + R_{\mathrm{on}})\, I_L^2$$

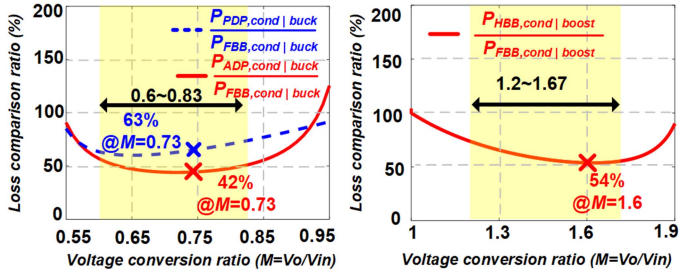

Fig. 11. Conduction loss comparison between the conventional FBBC and the proposed HBBC (a) in the buck mode and (b) in the boost mode.

$$= (M \times DCR - 2R_{\mathrm{on}} - 2DCR)\, I_o^2/(M-2). \tag{27}$$

Similarly, the equation of $P_{\mathrm{FBB,\ cond|buck}}$ of FBBC in the buck mode, which is the sum of S_1, S_2, and S_4, and DCR in Fig. 2(a), is given as follows:

$$P_{\mathrm{FBB,\ cond|buck}} = (2R_{\mathrm{on}} + \mathrm{DCR})\ I_o^2. \tag{28}$$

Finally, the conduction loss ($P_{\mathrm{ADP,\ cond|buck}}$) of HBBC in the "always-dual-path" buck mode is given as follows:

$$P_{\mathrm{ADP,\ cond|buck}} = D\left[2R_{\mathrm{on}}(I_L + I_{C1})^2 + DCR \times I_L^2 + R_{\mathrm{on}} I_{C1}^2\right] + (1-D)\left[(R_{\mathrm{on}} + DCR) \times I_L^2 + R_{\mathrm{on}} I_{C2}^2 + R_{\mathrm{on}}(I_L + I_{C2})^2\right] = \frac{\left[\mathrm{DCR}\left(4M^2 - 6M + 2\right) + R_{\mathrm{on}}\left(8M^3 - 28M^2 + 26M - 9\right)\right] I_o^2}{16M^2 - 24M + 8}. \tag{29}$$

For comparison, the conduction loss ($P_{\mathrm{PDP,\ cond|buck}}$) of HBBC in the "partial-dual-path" buck mode is also given as follows:

$$P_{\mathrm{PDP,\ cond|buck}} = (1-D)\,(2R_{\mathrm{on}} + \mathrm{DCR})\, I_L^2 + DR_{\mathrm{on}}(I_o + I_{C1})^2 + 2DR_{\mathrm{on}} I_{C1}^2 + D\,(\mathrm{DCR} + R_{\mathrm{on}})\, I_L^2 = \frac{\left[\mathrm{DCR}\left(2M^3 - M^2\right) + R_{\mathrm{on}}\left(3M^3 - 2M^2 + M\right)\right] I_o^2}{2M - 1}. \tag{30}$$

Based on (26)–(30), the conduction losses of HBBC are compared with those of FBBC, and the loss comparison ratios in the buck and boost modes are plotted in Fig. 11, where DCR is set as five times of R_{on}. Given the bidirectional power flow and flexibility of single-row and double-row battery packs, M for the design is 1) 0.6–0.83 in the buck mode and 2) 1.2–1.67 in the boost mode. It can be observed that the conduction loss of HBBC is greatly reduced in the utilized conversion regions, denoted in the light-yellow areas in Fig. 11. With the help of two flying capacitors in the proposed "always-dual-path" buck-mode HBBC, the conduction loss is reduced by up to 58% at the conversion ratio of 0.73, whereas the loss is reduced by only 37% at the same ratio for the "partial-dual-path" buck-mode HBBC, where only one flying capacitor is used. When it comes to the boost-mode HBBC, the conduction loss is reduced by 46% at $M = 1.6$, as shown in Fig. 11(b).

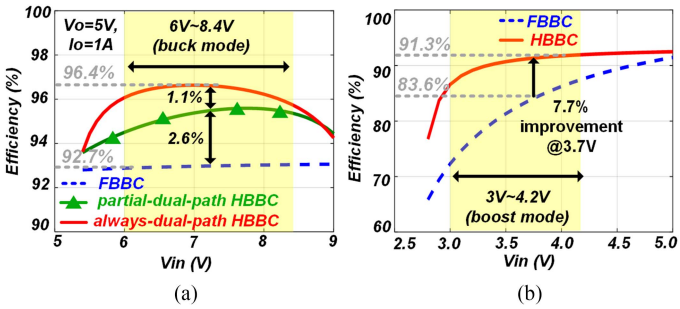

Fig. 12. Simulated conversion efficiency comparison between the proposed HBBC and the conventional FBBC (a) in the buck mode and (b) in the boost mode.

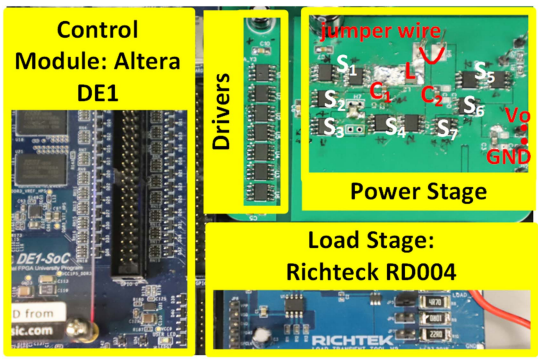

Fig. 13. Measurement setup of the proposed HBBC.

In Fig. 12, the simulated conversion efficiency comparison between the proposed HBBC and conventional FBBC is demonstrated, where different input voltages are applied while the output voltage and current are fixed to 5 V and 1 A, respectively, for fair comparison (i.e., same output power level for all cases). The DCR is 270 mΩ for all cases that will be mentioned below. Moreover, dynamic losses and control power are also taken into consideration, though they are much smaller than the above-discussed conduction losses and have minor effects on efficiency. Compared with the buck-mode FBBC, the "partial-dual-path" buck-mode HBBC improves the conversion efficiency from 92.7% to 95.3%, whereas the proposed "always-dual-path" buck-mode HBBC further improves it by 1.1% at $V_{\text{in}} = 7.4$ V. Although the total efficiency increment is only 3.7% in the buck mode, it is still meaningful and important because even a few percentage points of efficiency decrement at heavy load can cause severe heating problem in portable devices. When the conventional FBBC enters into the boost mode, the average I_L is M times of I_o, and thus the conduction loss in the boost mode is much higher than that in the buck mode for the same I_o. In Fig. 12(b), the conversion efficiency is increased from 83.6% to 91.3% with V_{in} of 3.7 V.

IV. Experimental Results

The measurement setup is shown in Fig. 13, and the utilized components are listed in Table I. The control algorithm is implemented on the field-programmable gate array (FPGA) platform, *Altera DE1*, and the load stage is *Richtek RD004*. Since the maximum voltage of this work occurs at the switching node V_{X1} of the "always-dual-path" buck-mode HBBC, which is $2V_{\text{in}}$ (< 16.8 V) during the start-up process, a power P-MOSFET, which has a breakdown voltage of 20 V, is used. Also, the utilized power P-MOSFETs and N-MOSFETs are specially chosen to have similar switching characteristics, and thus the deadtime length can be reduced to improve the conversion efficiency and system stability. The jumper wire is used for I_L measurement. It should be mentioned that printed circuit boards (PCBs) for the conventional FBBC and two existing HBBCs in [14] and [15] are also built and measured for comparison. In the measurement of the forward power delivery mode, the input sources are battery packs providing 3.7 V or 7.4 V, and the desired output voltage is V_{usb} of 5 V. When it comes to the measurement of the reverse power delivery mode, the previous V_{usb} of 5 V changes its role from output to input, and the desired output voltages are 3.7 V in the buck mode and 7.4 V in the boost mode.

In [14], a hybrid boost converter is developed and analyzed in detail. Although a dual-path power delivery scheme is achieved in this design, an RHP zero still exists in its transfer function. For comparison, three types of boost converters, which are the boost-mode FBBC, the hybrid boost converter presented in [14], and the proposed boost-mode HBBC, are built with the same power switches, drivers, controllers, etc. The measured load step responses of these three boost converters are shown in Fig. 14, where V_{in} and V_o are 3.7 and 5 V, respectively. It is noted that the load current slope is larger than 10 A/μs. It shows that the I_L variation (i.e., ΔI_L) of the proposed boost-mode HBBC is the same as the load variation as 1 A, whereas ΔI_L of the boost-mode FBBC is up to 1.35 A. Thus, the current stress on the high-DCR inductor of the boost-mode HBBC is much relieved (i.e., reduced by 35%). Although the hybrid boost converter presented in [14] has the lowest ΔI_L ($= 0.85$ A), its settling time and voltage ripple are more than 90 μs and up to 0.8 V, respectively. Comparatively, the proposed boost-mode HBBC has shorter settling time (< 60 μs) and smaller voltage ripple ($<$ 0.7 V) due to the removal of RHP zero.

TABLE I
Circuit Components

Components	Parameters
Inductor (L)	4.7 μH, DCR = 270 mΩ [6]
Power P-Channel Metal-Oxide Semiconductor (S_1, S_2, S_4, S_5 and S_6)	*Si9933CDY-T1-GE*, R_{on} = 58 mΩ, C_g = 1.7 nF, Q_{rr} = 17 nC, C_{oss} = 140 pF, V_{body_diode} = 0.77 V, t_r = *15 ns*, t_f = *9 ns* [23]
Power N-Channel Metal-Oxide Semiconductor (S_3 and S_7)	*STS10DN3LH5*, R_{on} = 28 mΩ, C_g = 920 pC, Q_{rr} = 7.8 nC, C_{oss} = 97 pF, V_{body_diode} = 1.1 V, t_r = *22 ns*, t_f = *2.8 ns* [24]
Drivers	*UCC27424* [25]
Output Capacitor (C_o)	10 μF, *ESR* = 10 mΩ
Flying Capacitors (C_1 and C_2)	5 μF, *ESR* = 10mΩ

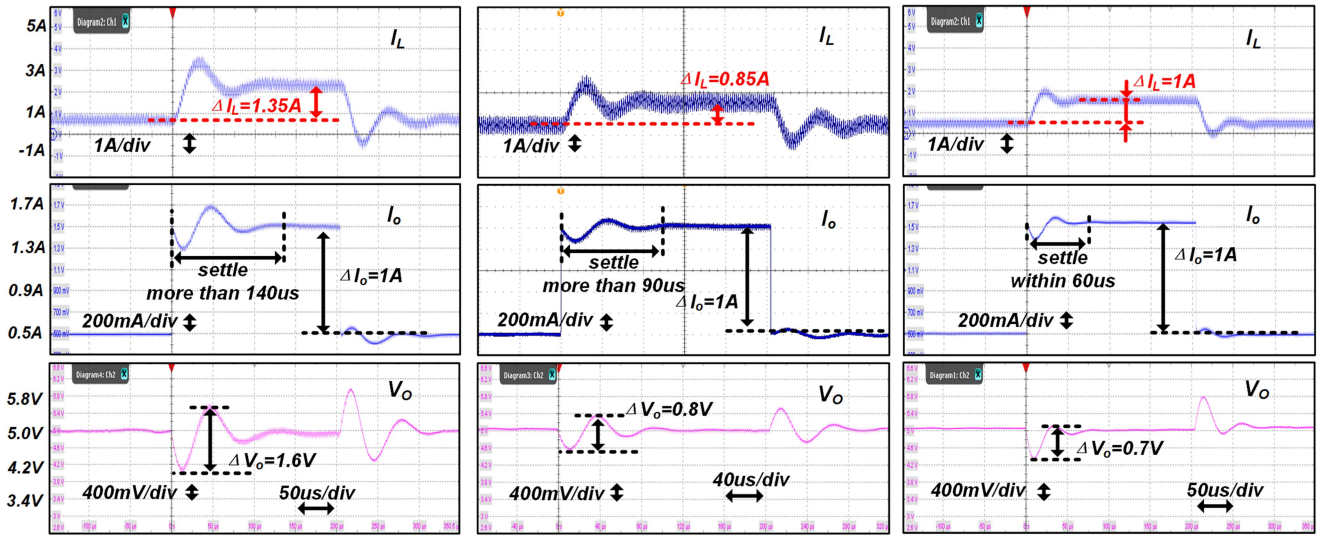

Fig. 14. Measured inductor current, output current, and voltage waveforms of (a) boost-mode FBBC, (b) hybrid boost converter presented in [14], and (c) boost-mode HBBC when the load current changes between 0.5 and 1.5 A.

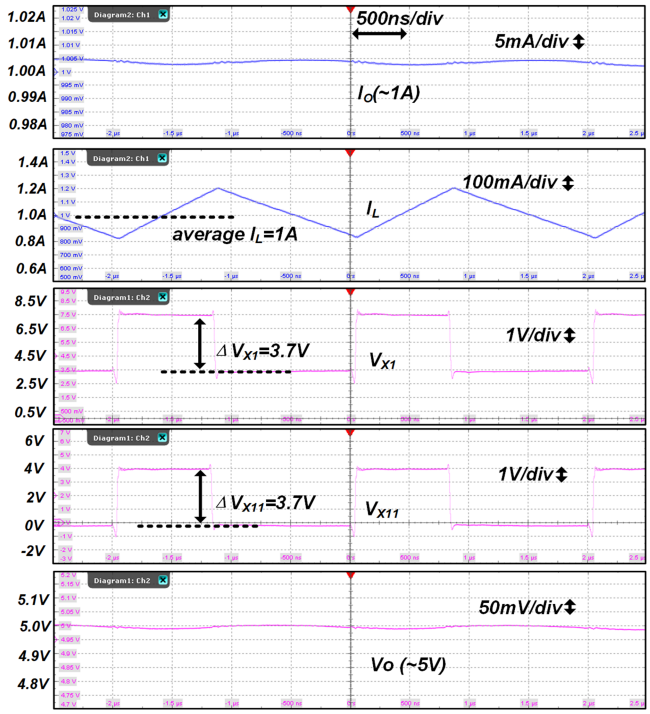

Fig. 15. Measured waveforms of the proposed HBBC in the boost mode when the load current stays at 1 A.

The steady-state operation for the boost-mode HBBC at 1-A load is shown in Fig. 15. It is shown that V_{x1} changes between V_{in} (i.e., 3.7 V) and $2V_{\text{in}}$ (i.e., 7.4 V), whereas V_{x11} changes between ground (i.e., 0 V) and V_{in} (i.e., 3.7 V) in the two phases. Moreover, the ripple of V_o is only 10 mV owing to the advantage of continuous I_D.

In [15], a hybrid buck converter is presented without the analysis of its loop performance. Yet, it can be easily verified that an RHP zero exists in its transfer function. For comparison, four types of buck converters, which are the buck-mode FBBC, the hybrid buck converter presented in [15], and the proposed "partial-dual-path" and "always-dual-path" HBBCs, are built with the same circuit components, and the measured load transient responses of these four buck converters are shown in Fig. 16, where V_{in} and V_o are 7.4 and 5 V, respectively. In the buck-mode FBBC, the average I_L follows I_o, and thus ΔI_L of 1 A is observed for the load step from 1 to 2 A, as shown in Fig. 16(a). Since a dual-path power delivery scheme is applied in [15], ΔI_L is reduced to 0.67 A for the same ΔI_o of 1 A. Yet, the settling time is more than 120 μs because of the annoying RHP zero. Similarly, although ΔI_L of the "partial-dual-path" buck-mode HBBC is decreased to 700 mA, the long settling time of 170 μs is caused by the existence of RHP zero. When it comes to the "always-dual-path" buck converter, ΔI_L is 500 mA only, which is merely half of ΔI_o. Meanwhile, the settling time is reduced below 50 μs due to the removal of RHP zero. The RHP-zero-free feature of the proposed "always-dual-path" buck-mode HBBC reduces the complexity of compensation, and thus it also eases the design of analog or digital controllers. Moreover, due to the instant response of the capacitive power path, the undershoot of the "partial-dual-path" buck-mode HBBC is reduced from 0.8 to 0.6 V when compared with the conventional buck-mode FBBC. Furthermore, the undershoot is reduced to 0.4 V in the "always-dual-path" buck-mode HBBC with the help of dual capacitive paths.

The steady-state operations of the "partial-dual-path" and "always-dual-path" buck-mode HBBCs are demonstrated in Figs. 17 and 18, respectively, where the load current is kept at 1 A for both cases. In Fig. 17, the average I_L of the "partial-dual-path" buck-mode HBBC is around 690 mA with the help of the single assisted capacitive power path. Comparatively, the average I_L of the "always-dual-path" buck converter is further reduced to 500 mA due to the dual assistive capacitive paths.

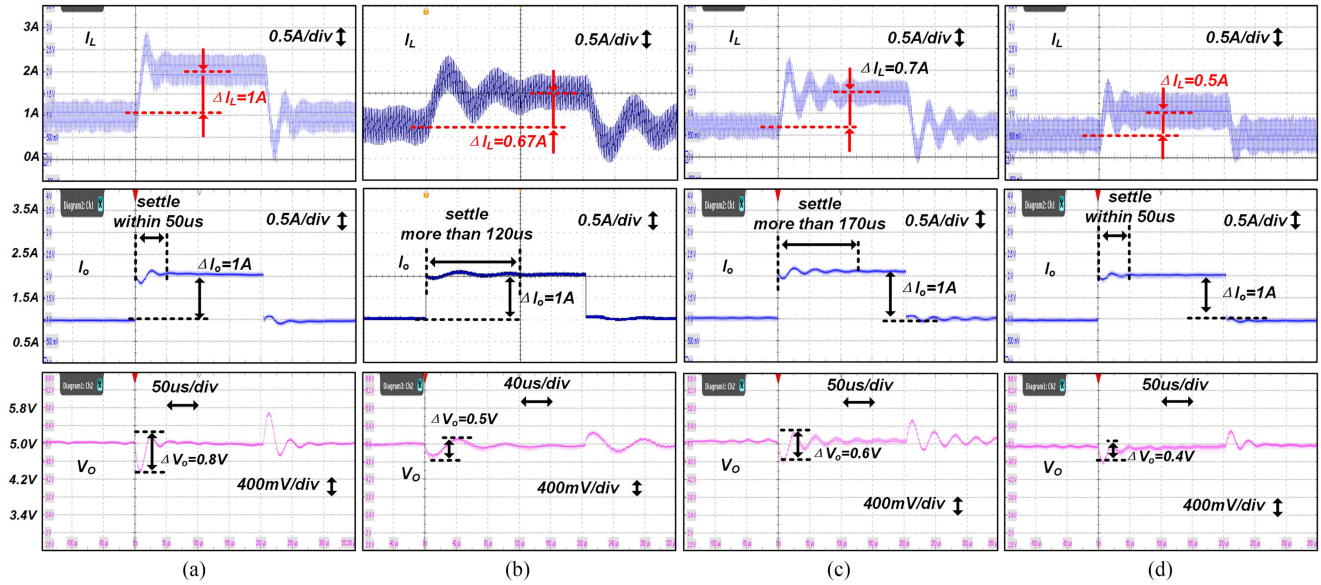

Fig. 16. Measured inductor current, output current, and voltage waveforms of (a) buck-mode FBBC, (b) hybrid buck converter presented in [15], (c) "partial-dual-path" buck-mode HBBC, and (d) "always-dual-path" buck-mode HBBC when the load current changes between 1 and 2 A.

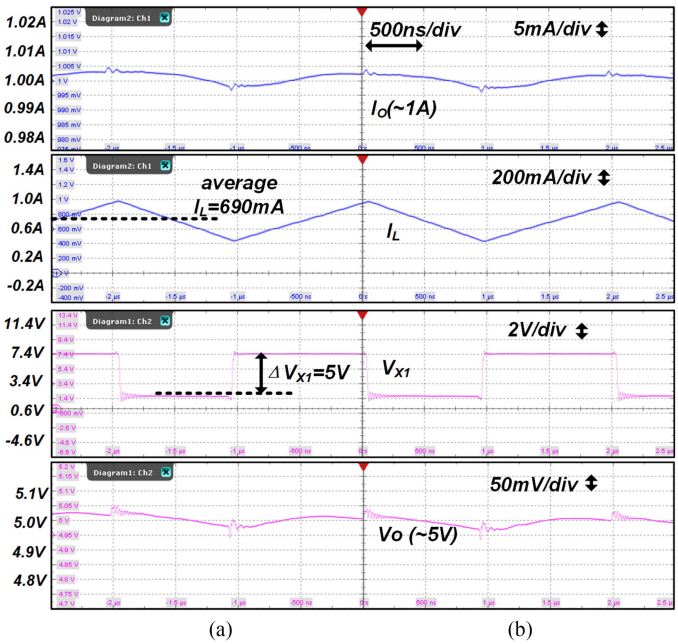

Fig. 17. Measured waveforms of the "partial-dual-path" buck-mode HBBC when the load current stays at 1 A.

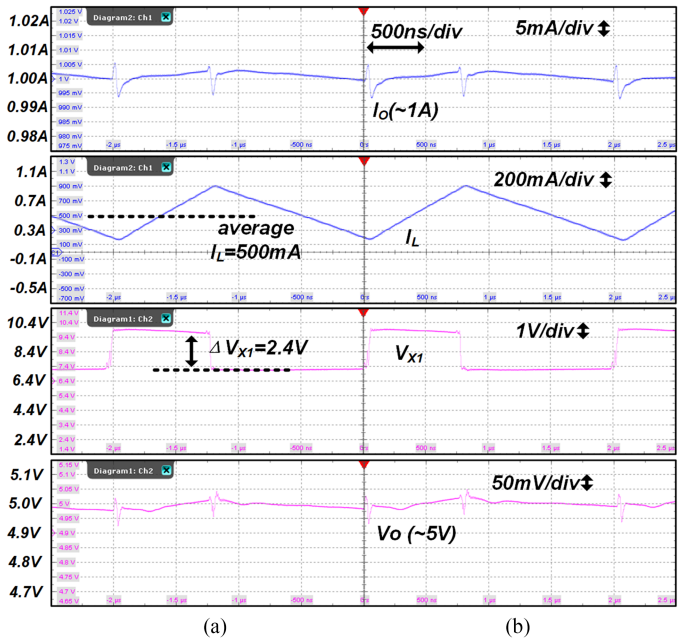

Fig. 18. Measured waveforms of the "always-dual-path" buck-mode HBBC when the load current stays at 1 A.

In the previous measurements, only the forward power delivery of the proposed converter is demonstrated. In Figs. 19 and 20, the reverse power delivery mode of the proposed HBBC is shown, where $V_{\rm usb}$ of 5 V is used as supply.

In the reverse boost mode, the desired V_o is 7.4 V. In Fig. 19, the load transient waveforms of the boost-mode FBBC and the proposed boost-mode HBBC are shown. Similar to the forward power delivery mode, ΔI_L (= 1 A) of the proposed boost-mode HBBC is lower than that of the boost-mode FBBC, which is 1.7 A. Thus, the DCR loss of the proposed boost-mode HBBC is also relieved in reverse power delivery. Meanwhile, the settling time and ΔV_o of the proposed boost-mode HBBC are much reduced to 40 μs and 1 V, respectively.

In the reverse buck mode, the desired V_o is 3.7 V. The load-transient waveforms of "partial-dual-path" and "always-dual-path" buck-mode HBBCs are shown in Fig. 20. With the help of two assisted capacitive power paths, ΔI_L and ΔV_o of the "always-dual-path" buck-mode HBBC are only 0.5 A and 0.4

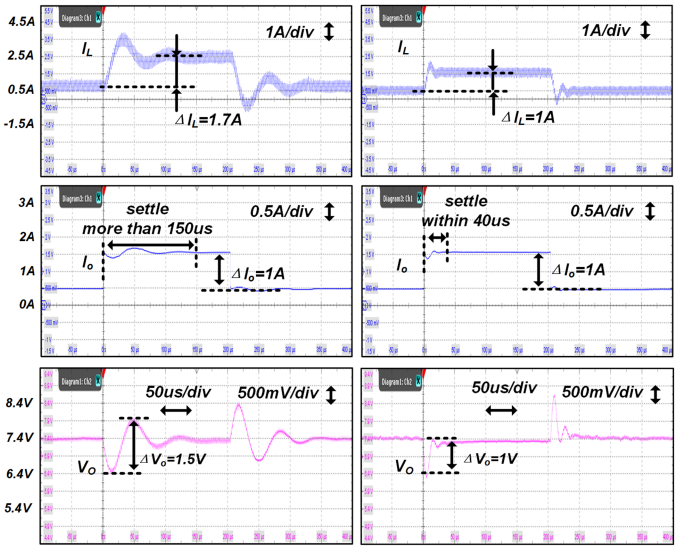

Fig. 19. Measured inductor current, output current, and voltage waveforms of (a) boost-mode FBBC and (b) proposed boost-mode HBBC when the load current changes between 0.5 and 1.5 A in reverse mode.

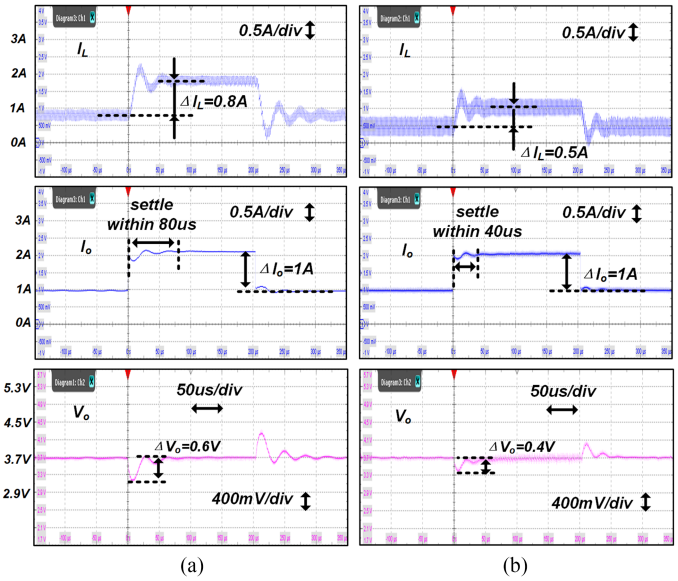

Fig. 20. Measured inductor current, output current and voltage waveforms of (a) "partial-dual-path" buck-mode HBBC, and (b) "always-dual-path" buck-mode HBBC when the load current changes between 1 A and 2 A in reverse mode.

V, whereas those of the "partial-dual-path" buck-mode HBBC are 0.8 A and 0.6 V, respectively.

The measured efficiency curves for the proposed HBBC and conventional FBBC are plotted in Fig. 21, where the power consumed by the controller and drivers is not considered. Specifically, when compared with the conventional FBBC with the same DCR of 270 mΩ, the efficiency achieved by the proposed HBBC at a load of 2 A is increased by 4.1% in the buck mode and 23.3% in the boost mode. When compared with the simulated

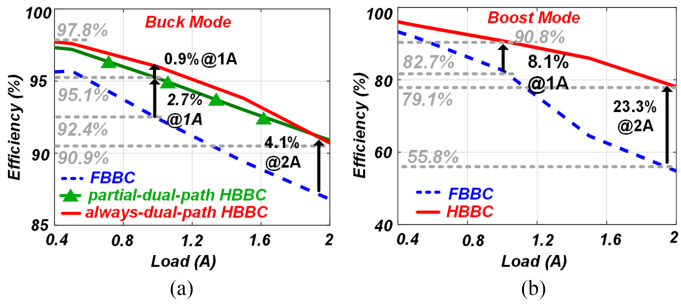

Fig. 21. Measured conversion efficiencies of HBBC and conventional FBBC. (a) $V_o/V_{\rm in}$ = 5 V/7.4 V. (b) $V_o/V_{\rm in}$ = 5 V/3.7 V.

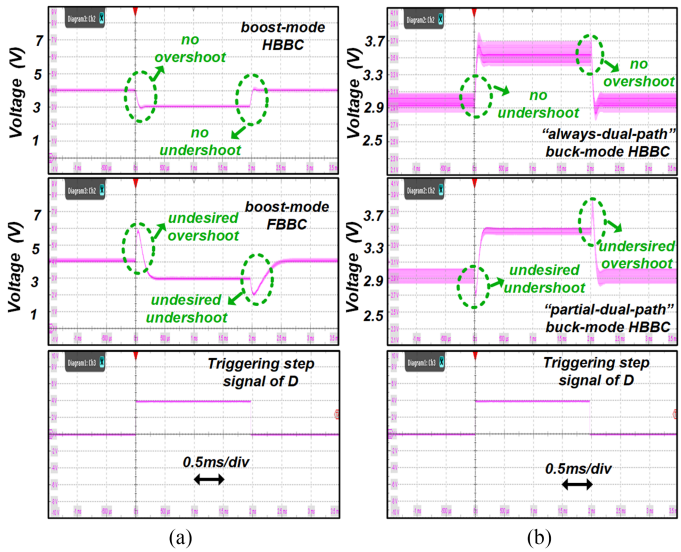

Fig. 22. Measured waveforms of V_o for (a) boost-mode HBBC and FBBC and (b) "always-dual-path" and "partial-dual-path" buck-mode HBBCs when a step of D is applied.

efficiencies of the case with a 1-A load in Fig. 12, the overall efficiencies are dropped by less than 0.5% in both the buck and boost modes.

Table II shows the comparison of the proposed HBBC with other recently reported hybrid dc/dc converters. Compared with others, the proposed design achieves bidirectional buck–boost operation, but others cannot. Moreover, the dc value of I_L (i.e., $I_{L,\,\rm DC}$) is reduced in both the buck and boost modes. Specifically, $I_{L,\,\rm DC}$ of the proposed "always-dual-path" buck-mode HBBC is reduced by 1/2, whereas $I_{L,\,\rm DC}$ of other buck converters is decreased by less than one-third. Although $I_{L,\,\rm DC}$ reduction in [14] is up to 37%, this design works in the boost mode only and cannot solve the RHP zero problem. In the proposed design, a high conversion efficiency of up to 97.8% can be achieved even though the DCR of the inductor is 270 mΩ. As a remark, $f_{\rm sw}$ = 500 kHz is used in the proposed dc/dc converter since the maximum sampling frequency of the FPGA built-in analog-to-digital converter (*LTC2308*) is 500 kHz.

Finally, a step of D is applied to different buck and boost converters, and the measured waveforms of V_o are shown in Fig. 22. Different from the previous measurements where L =

TABLE II
COMPARISON WITH STATE-OF-THE-ART HYBRID DC–DC CONVERTERS

	[4]	[13]	[14]	[15]	[16]	This work
Control method	Digital	Analog	Analog	N.A.	Analog	Digital
Conversion type	Buck and Boost	Buck only	Boost only	Buck only	Buck and Boost	Buck and Boost
Bidirectional operation	No	No	No	No	No	Yes
RHP-Zero Free	Yes	No	No	No	Yes	Yes
$I_{L,DC}$ reduction in buck mode[a] (reduced ratio, %)	No (0)	Yes (32)	N.A.	Yes (32)	No (0)	Yes (50)
$I_{L,DC}$ reduction in boost mode[b] (reduced ratio, %)	Yes (26)	N.A.	Yes (37)	N.A.	Yes (26)	Yes (26)
f_{sw} (MHz)	1.45	1	1	0.1	1	0.5
V_{in} (V)	2.9–6.3	4.5	2–4.2	24	2.7–4.2	6–8.4 and 3–4.2
V_o (V)	4.6	0.8–4	3–5	13	3.4	5
I_o (A)	0.05–0.6	0.2–1.6	0.01–0.8	<15	0.03–1	0.4–2
No. of passive components	1L 2C (4.7μH, 10μF, 470nF[c])	1L 2C (4.7μH, 10μF, 10μF[c])	1L 2C (4.7μH, 10μF, 10μF[c])	1L 3C (10μH, 264μF, 2×264μF[c])	1L 3C (2.2μH, 10μF, 2×10μF[c])	1L 3C (4.7μH, 10μF, 2×5μF[c])
Peak efficiency (DCR of L, mΩ)	97.5% (N.A.)	96.2% (250)	95.2% (200)	97.4%[d] (6.8)	97% (N.A.)	97.8%[d] (270)

[a]Compared with I_L of the buck-mode FBBC for the conversion from 7.4-V V_{in} to 5-V V_o.
[b]Compared with I_L of the boost-mode FBBC for the conversion from 3.7-V V_{in} to 5-V V_o.
[c]Flying capacitor.
[d]The power losses by the controller and drivers are not included.

4.7 μH and $R_o > 2.5\ \Omega$, the large L of 100 μH and small R_o of 1 Ω are utilized in this measurement with the aim to move ω_z to a lower frequency region. As a result, the effect of ω_z can be easily observed. When D suddenly changes at the rising edge of the triggering step signal of D in the boost-mode FBBC, an overshoot of V_o is first observed, and then V_o gradually drops to 3 V from 4 V, as shown in Fig. 22(a). When it comes to the proposed boost-mode HBBC, neither overshoot nor undershoot of V_o is observed during the transient step of D. Because the RHP zero is removed in the "always-dual-path" buck-mode HBBC, V_o rises from 3 and 3.5 V directly, as shown in Fig. 22(b). Instead, V_o of the "partial-dual-path" buck-mode HBBC dips before climbing to the final value of 3.5 V.

V. CONCLUSION

In this article, a novel bidirectional buck–boost converter for Li-ion battery management is presented. The average inductor current is reduced in both the buck and boost modes as the capacitive power paths share the current with the load. Thus, the current stress on the high-DCR inductor is much reduced, which leads to lower DCR's conduction loss and higher conversion efficiency in both the buck and boost modes. Measured results verify that the proposed HBBC works efficiently over a wide range of input voltage, and a 97.8% peak efficiency is achieved with an inductor with a DCR of 270 mΩ.

APPENDIX I

The purpose of Appendix I is to provide the derivation of the transfer functions of the proposed HBBC used in Section III-A and -B.

A. Derivation of Transfer Function in the Boost Mode

The state-space averaging method is utilized to obtain the steady-state and the small-signal models of the boost-mode HBBC. Based on the two-operation shown in Fig. 3, three equations are obtained based on the current and voltage relationships of the energy storing elements, i.e., C_1, C_o, and L. In phase 1, the following three equations are obtained:

$$C_O \frac{dv_O(t)}{dt} = i_L - v_O/R_o \tag{A1}$$

$$C_1 \frac{dv_1(t)}{dt} = (v_{\text{in}} - v_1)/R_1 \tag{A2}$$

$$L \frac{di_L(t)}{dt} = v_{\text{in}} - v_O - i_L \text{DCR} \tag{A3}$$

TABLE III
MATRICES FOR STATE-SPACE EQUATIONS IN THE BOOST MODE

Matrices for state-space equation	$A_1=\begin{bmatrix}-1/R_OC_O & 0 & 1/C_O\\ 0 & -1/R_1C_1 & 0\\ -1/L & 0 & -DCR/L\end{bmatrix}, B_1=\begin{bmatrix}0\\ 1/R_1C_1\\ 1/L\end{bmatrix}, A_2=\begin{bmatrix}-1/R_OC_O & 0 & 1/C_O\\ 0 & 0 & -1/C_1\\ -1/L & 1/L & -DCR/L\end{bmatrix}, B_2=\begin{bmatrix}0\\ 0\\ 1/L\end{bmatrix}$
Average matrices	$A=DA_1+(1-D)A_2=\begin{bmatrix}-1/R_OC_O & 0 & 1/C_O\\ 0 & -D/R_1C_1 & (D-1)/C_1\\ -1/L & (1-D)/L & -DCR/L\end{bmatrix}, B=B_1D+B_2(1-D)=\begin{bmatrix}0\\ D/R_1C_1\\ 1/L\end{bmatrix}$
Steady-state values	$X=-A^{-1}BU=\begin{bmatrix}\frac{V_{in}(2R_OD-R_OD^2)}{R_1+DCR\cdot D-2DR_1+D^2R_1+DR_o}\\ \frac{V_{in}(DCR\cdot D-R_1-2DR_1+DR_1+DR_o)}{R_1+DCR\cdot D-2DR_1+D^2R_1+DR_o}\\ \frac{V_{in}(-D^2+2D)}{R_1+DCR\cdot D-2DR_1+D^2R_1+DR_o}\end{bmatrix}$ $\overset{R_1=0}{\Longrightarrow}\begin{bmatrix}V_{in}(2R_OD-R_OD^2)/(DCR\cdot D+DR_o)\\ V_{in}\\ V_{in}(2-D)/(R_o+DCR)\end{bmatrix}\overset{DCR=0}{\Longrightarrow}\begin{bmatrix}V_{in}(2-D)\\ V_{in}\\ V_{in}(2-D)/R_o\end{bmatrix}$

where v_1 and R_1 are the voltage drop across C_1 and the parasitic resistance of the capacitive path by C_1, including both C_1's ESR and $R_{\rm on}$ of the power switches, respectively. Based on the perturbation analysis presented in [21], the state signal x ($=[\ v_O(t)\quad v_1(t)\quad i_L(t)\ ]'$) is equal to their corresponding steady values X ($=[\ V_O\quad V_1\quad I_L\ ]'$) plus the small ac variation $\hat{x}$ ($=[\ \hat{v}_{\rm O}\quad \hat{v}_1\quad \hat{i}_L\ ]'$). The same applies to the input signal u ($=[v_{in}(t)]$). The equations are as follows:

$$x = X+\hat{x}=\begin{bmatrix}V_O\\ V_1\\ I_{\rm L}\end{bmatrix}+\begin{bmatrix}\hat{v}_{\rm O}\\ \hat{\rm v}_1\\ \hat{i}_{\rm L}\end{bmatrix} \tag{A4}$$

$$u = U+\hat{u}=[V_{\rm in}]+[\hat{v}_{\rm in}]. \tag{A5}$$

Thus, (A1)–(A3) can be represented in matrix format as follows:

$$\begin{aligned}\dot{x} &= A_1x+B_1u\\ &=\begin{bmatrix}-\frac{1}{R_oC_o} & 0 & \frac{1}{C_o}\\ 0 & -\frac{1}{R_1C_1} & 0\\ -\frac{1}{L} & 0 & -{\rm DCR}/L\end{bmatrix}\begin{bmatrix}v_O(t)\\ v_1(t)\\ i_L(t)\end{bmatrix}\\ &\quad+\begin{bmatrix}0\\ 1/R_1C_1\\ 1/L\end{bmatrix}[v_{\rm in}(t)]\end{aligned} \tag{A6}$$

where $\dot{x}$ is the derivative matrix of x. According to the above-mentioned method, the state equation in phase 2 can also be derived as follows (all the matrices including both A_2 and B_2 are listed in Table III):

$$\dot{x} = A_2\,x+B_2u. \tag{A7}$$

Therefore, the steady-state and the state equations of the small ac model can be solved as follows:

$$X = -A^{-1}BU \tag{A8}$$

$$\dot{\hat{x}} = A\hat{x}+B\hat{u}+E\hat{d} \tag{A9}$$

where $\hat{d}$ is the perturbed quantity of the duty D and the matrix E is $(A_1-A_2)X+(B_1-B_2)U$. To simplify the derivation process, R_1 is assumed to be negligible. The transfer function $G_{vd,\ {\rm bo}}(s)$ is given as follows:

$$\begin{aligned}G_{vd,{\rm bo}}\ (s) &= \frac{V_{\rm in}R_o}{LC_OR_os^2+(L+C_OR_o\cdot{\rm DCR})\,s+({\rm DCR}+R_o)}\\ &\xrightarrow{\rm DCR\,=\,0} V_{\rm in}\cdot\frac{1}{LC_Os^2+\frac{L}{R_o}s+1}.\end{aligned} \tag{A10}$$

B. Derivation of Transfer Function in the "Partial-Dual-Path" Buck Mode

In the "partial-dual-path" buck mode, the small-signal model is different from the boost mode. Based on the two-phase operation shown in Fig. 4, the following three equations are obtained in phase 1

$$C_O\,\frac{dv_O\,(t)}{dt} = I_L\ +\frac{v_{\rm in}-v_o-v_1}{R_1}-\frac{v_o}{R_O} \tag{A11}$$

$$C_1\,\frac{dV_1\,(t)}{dt} = \frac{v_{\rm in}-v_o-v_1}{R_1} \tag{A12}$$

$$L\,\frac{dI_L\,(t)}{dt} = V_{\rm in}\ -V_o-i_L{\rm DCR}. \tag{A13}$$

Similarly, it can be represented in the matrix format (all the matrices for the "partial-dual-path" buck-mode HBBC are listed in Table IV). Following the same steps in the boost part, the transfer function $G_{vd,{\rm bu\_partial}}(s)$ is given as follows:

$$\begin{aligned}&G_{vd,{\rm bu\_partial}}\ (s)=\tfrac{\hat{v}_o}{\hat{d}}\\ &=\tfrac{1}{(D-2)^2R_o-{\rm DCR}}\\ &\times\tfrac{-R_oLV_{\rm in}s+R_oV_{\rm in}\left((D-2)^2R_o-{\rm DCR}\right)}{LR_o(C_f+C_o)s^2+(L+{\rm DCR}\cdot R_o(C_f+C_o))s+(D-2)^2R_o+{\rm DCR}}\\ &\xrightarrow{\rm DCR\,=\,0}\tfrac{V_o}{2-D}\cdot\tfrac{1-\frac{L}{R_o(2-D)^2}s}{\frac{L(C_o+C_1)}{(2-D)^2}s^2+\frac{L}{R_o(2-D)^2}s+1}.\end{aligned} \tag{A14}$$

TABLE IV
MATRICES FOR STATE-SPACE EQUATIONS IN THE PARTIAL-DUAL-PATH BUCK MODE

Matrices for state-space equation	$A_1=\begin{bmatrix}-1/R_1C_o-1/R_oC_o & -1/R_1C_o & 1/C_o\\ -1/R_1C_1 & -1/R_1C_1 & 0\\ -1/L & 0 & -DCR/L\end{bmatrix}, B_1=\begin{bmatrix}1/R_1C_o\\ 1/R_1C_1\\ 1/L\end{bmatrix}, A_2=\begin{bmatrix}-1/R_oC_o & 0 & 1/C_o\\ 0 & 0 & -1/C_1\\ -1/L & 1/L & -DCR/L\end{bmatrix}, B_2=\begin{bmatrix}0\\0\\0\end{bmatrix}$
Average matrices	$A=DA_1+(1-D)A_2=\begin{bmatrix}-D/R_1C_o-1/R_oC_o & -D/R_1C_o & 1/C_o\\ -D/R_1C_1 & -D/R_1C_1 & (D-1)/C_1\\ -1/L & (1-D)/L & -DCR/L\end{bmatrix}$ $\mathrm{B}=B_1D+B_2(1-D)=\begin{bmatrix}D/R_1C_o\\ D/R_1C_1\\ D/L\end{bmatrix}$
Steady-state values	$X=-A^{-1}BU=\begin{bmatrix}\frac{V_{in}(2R_oD-R_oD^2)}{R_1+DCR\cdot D-2DR_1-4R_oD^2+R_oD^3+R_1D^2+4R_oD}\\ \frac{V_{in}(DCR\cdot D-R_1D-3R_oD^2+R_oD^3+R_1D^2+4R_oD)}{R_1+DCR\cdot D-2DR_1-4R_oD^2+R_oD^3+R_1D^2+4R_oD}\\ \frac{DV_{in}}{R_1+DCR\cdot D-2DR_1-4R_oD^2+R_oD^3+R_1D^2+4R_oD}\end{bmatrix}$ $\overset{R_1=0}{\Longrightarrow}\begin{bmatrix}V_{in}R_o(2-D)/(DCR+R_o(D-2)^2)\\ V_{in}(DCR+R_o(D-2)(D-1))/(DCR+R_o(D-2)^2)\\ V_{in}/((2-D)^2R_o+DCR)\end{bmatrix}\overset{DCR=0}{\Longrightarrow}\begin{bmatrix}V_{in}/(2-D)\\ V_{in}(D-1)/(D-2)\\ V_{in}/(2-D)^2R_o\end{bmatrix}$

C. Derivation of Transfer Function in the "Always-Dual-Path" Buck Mode

Based on the two-phase operation shown in Fig. 5, the following four equations are obtained in phase 1. It should be noted that the parasitic resistance of C_1 and C_2 are both set as R_f for simplicity

$$C_O\frac{dv_O(t)}{dt}=I_L+\frac{v_{\text{in}}-v_o-v_1}{R_f}-\frac{v_o}{R_o} \tag{A15}$$

$$C_1\frac{dV_1(t)}{dt}=\frac{v_{\text{in}}-v_o-v_1}{R_f} \tag{A16}$$

$$C_2\frac{dV_2(t)}{dt}=I_L \tag{A17}$$

$$L\frac{dI_L(t)}{dt}=V_{\text{in}}-V_{C2}-V_o-I_L\text{DCR}. \tag{A18}$$

Since two flying capacitors (i.e., C_1 and C_2) are utilized, the state signal x is redefined as follows:

$$x=X+\hat{x}=\begin{bmatrix}V_o\\ V_1\\ V_2\\ I_{\text{L}}\end{bmatrix}+\begin{bmatrix}\hat{v}_{\text{o}}\\ \hat{\text{v}}_1\\ \hat{\text{v}}_2\\ \hat{i}_{\text{L}}\end{bmatrix} \tag{A19}$$

where the voltage of C_2 (i.e., v_2) is added. Likewise, (A15)–(A19) are rewritten in the matrix format, as shown in Table V. Following the same steps in the previous parts, the transfer function $G_{vd,\text{bu\_always}}(s)$ is given as follows:

$$\begin{aligned}G_{vd,\text{bu\_always}}(s)&=\frac{\hat{v}_o}{\hat{d}}\\ &=\frac{2V_{\text{in}}}{L(C_o+C_1+C_2)s^2+\left[\frac{L}{R_o}+\text{DCR}(C_o+C_1+C_2)\right]s+\left(4+\frac{\text{DCR}}{R_o}\right)}\\ &\overset{\text{DCR}=0}{\Longrightarrow}\frac{V_o}{2-D}\cdot\frac{1}{\frac{L(C_o+C_1+C_2)}{4}s^2+\frac{L}{4R_o}s+1}.\end{aligned} \tag{A20}$$

For comparison, the transfer function of the conventional buck converter (i.e., $G_{vd,\text{cbu}}(s)$) is given as follows [21]:

$$G_{vd,\text{cbu}}(s)=\frac{V_o}{D}\cdot\frac{1}{LC_os^2+\frac{L}{R_o}s+1}. \tag{A21}$$

The important parameters of $G_{vd,\text{cbu}}(s)$ and $G_{vd,\text{bu\_always}}(s)$, such as the low frequency gains (i.e., $G_{d0,\text{cbu}}$ and $G_{d0,\text{always}}$), double pole frequencies (i.e., $\omega_{0,\text{cbu}}$ and $\omega_{0,\text{always}}$), and quality factors (i.e., Q_{cbu} and Q_{always}), are obtained as follows:

$$G_{d0,\text{cbu}}=V_o/D=V_{\text{in}} \tag{A22}$$

$$G_{d0,\text{always}}=V_o/(2-D)=V_{\text{in}}/2 \tag{A23}$$

$$\omega_{0,\text{cbu}}=1/\sqrt{LC_o} \tag{A24}$$

$$\omega_{0,\text{always}}=2/\sqrt{L(C_o+C_1+C_1)} \tag{A25}$$

$$Q_{\text{cbu}}=R_o\cdot\sqrt{\frac{C_o}{L}} \tag{A26}$$

$$Q_{\text{always}}=2R_o\cdot\sqrt{\frac{C_o+C_1+C_1}{L}}. \tag{A27}$$

TABLE V
MATRICES FOR STATE-SPACE EQUATIONS IN THE ALWAYS-DUAL-PATH BUCK MODE

Matrices for state-space equation	$A_1=\begin{bmatrix} -1/R_oC_o-1/R_fC_o & -1/R_fC_o & 0 & 1/C_o \\ -1/R_fC_1 & -1/R_fC_1 & 0 & 0 \\ 0 & 0 & 0 & 1/C_2 \\ -1/L & 0 & -1/L & -DCR/L \end{bmatrix}, B_1=\begin{bmatrix} 1/R_fC_o \\ 1/R_fC_1 \\ 0 \\ 1/L \end{bmatrix}$ $A_2=\begin{bmatrix} -1/R_oC_o-1/R_fC_o & 0 & 1/R_fC_o & 1/C_o \\ 0 & 0 & 0 & -1/C_1 \\ 1/R_fC_2 & 0 & -1/R_fC_2 & 0 \\ -1/L & 1/L & 0 & -DCR/L \end{bmatrix}, B_2=\begin{bmatrix} 0 \\ 0 \\ 0 \\ 1/L \end{bmatrix}$
Average matrices	$A=DA_1+(1-D)A_2=\begin{bmatrix} -1/R_fC_o-1/R_oC_o & -D/R_fC_o & (1-\mathrm{D})/R_fC_o & 1/C_o \\ -D/R_fC_1 & -D/R_fC_1 & 0 & (D-2)/C_1 \\ (1-D)/R_fC_2 & 0 & (D-1)/R_fC_2 & D/C_2 \\ -1/L & (1-D)/L & -D/L & -R_f/L \end{bmatrix}$ $\mathrm{B}=B_1D+B_2(1-D)=\begin{bmatrix} D/R_fC_o \\ D/R_fC_1 \\ 0 \\ 1/L \end{bmatrix}$
Steady-state values	$X=-A^{-1}BU=\begin{bmatrix} \frac{2V_{in}R_o(D^3-3D^2+2D)}{R_f+DCR\cdot D-3DR_f-4R_oD^2-DCR\cdot D^2+3R_fD^2+4R_oD} \\ \frac{-V_{in}(R_f-DCR\cdot D-2R_fD-2R_oD^2+2D^3R_o+DCR\cdot D^2+R_fD^2-R_fD^3)}{R_f+DCR\cdot D-3DR_f-4R_oD^2-DCR\cdot D^2+3R_fD^2+4R_oD} \\ \frac{V_{in}(2R_oD^3-6R_oD^2+2R_fD^2-R_fD^3+4DR_o)}{R_f+DCR\cdot D-3DR_f-4R_oD^2-DCR\cdot D^2+3R_fD^2+4R_oD} \\ \frac{V_{in}(D^3-3D^2+2D)}{R_f+DCR\cdot D-3DR_f-4R_oD^2-DCR\cdot D^2+3R_fD^3+4R_oD} \end{bmatrix}$ $\xrightarrow{R_f=0}\begin{bmatrix} \frac{2V_{in}R_o(D^2-3D+2)}{DCR-DCR\cdot D+4R_o-4R_oD} \\ \frac{V_{in}(DCR-DCR\cdot D+2R_oD-2R_oD^2)}{DCR-DCR\cdot D+4R_o-4R_oD} \\ \frac{V_{in}(2R_oD^2-6R_oD+4R_o)}{DCR-DCR\cdot D+4R_o-4R_oD} \\ \frac{V_{in}(D^2-3D+2)}{DCR-DCR\cdot D+4R_o-4R_oD} \end{bmatrix}\xrightarrow{DCR=0}\begin{bmatrix} V_{in}(2-D)/2 \\ DV_{in}/2 \\ V_{in}(2-D)/2 \\ V_{in}(2-D)/4R_o \end{bmatrix}$

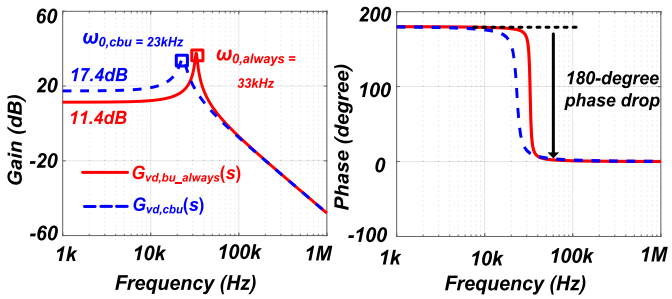

Fig. 23. Loop performance comparison between the conventional buck converter and the proposed "always-dual-path" buck-mode HBBC.

In Fig. 23, the loop performances of these two types of buck converter are plotted, where $V_{\rm in}=7.4$ V, $R_o=5\ \Omega$, $L=4.7$ μH, $C_o=10$ μF, and $C_1=C_2=5$ μF. From (A22) and (A23), $G_{d0,\rm always}$ is half of $G_{d0,\rm cbu}$, which corresponds to the gain difference of 6 dB in Fig. 23. Yet, this reduced dc gain can be easily compensated for, and thus it is not a problem. Given that $\omega_{0,\rm always}$ is higher than $\omega_{0,\rm cbu}$, the Q peak of the "always-dual-path" buck-mode HBBC is pushed to a higher frequency (i.e., from 23 to 33 kHz), which improves the stability.

APPENDIX II

The purpose of Appendix II is to provide the switching loss analysis of the proposed converter. Since an increase in the number of power switches increases switching losses, a brief analysis is conducted to confirm this tendency. Note that all switching losses are calculated as hard switching, and the deadtime is not considered for simplicity.

In the boost-mode HBBC, only three power switches take the switching actions, which are S_1, S_2, and S_3 in Fig. 3. First, the sustained voltages of these three switches during their "OFF" state are listed for the proposed boost-mode HBBC

$$V_{S1}=V_{S2}=V_{S3}=V_{\rm in}. \tag{A28}$$

Then, the currents of S_1, S_2 and S_3 during their "ON" state are also provided

$$\begin{aligned} I_{S1}&=I_L+I_{C1,\phi1},\\ I_{S2}&=I_L,\\ I_{S3}&=I_{C1,\phi1}. \end{aligned} \tag{A29}$$

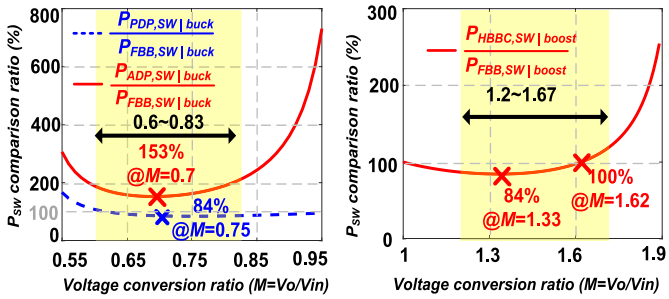

Fig. 24. Switching loss comparison between the conventional FBBC and the proposed HBBC in (a) buck mode and (b) boost mode.

Finally, the total switching loss in the proposed boost-mode HBBC ($P_{\mathrm{HBB,\ SW|boost}}$) can be derived as follows:

$$P_{\mathrm{HBB,SW|boost}} = \frac{f_{\mathrm{sw}} V_{S1} I_{S1} (t_r + t_f)}{2} + \frac{f_{\mathrm{sw}} V_{S2} I_{S2} (t_r + t_f)}{2} + \frac{f_{\mathrm{sw}} V_{S3} I_{S3} (t_r + t_f)}{2} = I_o V_{\mathrm{in}} (t_r + t_f) / (2 - M) \quad \text{(A30)}$$

where t_r and t_f are the rising and falling times of the utilized power MOSFETs, respectively. Following the same steps, the total switching loss in the conventional boost-mode FBBC ($P_{\mathrm{FBB,SW|boost}}$) is also given

$$V_{S3} = V_{S4} = V_o \quad \text{(A31)}$$

$$I_{S3} = I_{S4} = I_L \quad \text{(A32)}$$

$$P_{\mathrm{FBB,SW|boost}} = \frac{f_{\mathrm{sw}} V_{S3} I_{S3} (t_r + t_f)}{2} + \frac{f_{\mathrm{sw}} V_{S4} I_{S4} (t_r + t_f)}{2} = I_o V_{\mathrm{in}} (t_r + t_f) M^2. \quad \text{(A33)}$$

When it comes to the buck-mode operation, the switching losses of the "always-dual-path" and "partial-dual-path" buck-mode HBBCs (i.e., $P_{\mathrm{ADP,SW|buck}}$ and $P_{\mathrm{PDP,SW|buck}}$) are given as follows:

$$P_{\mathrm{ADP,\ SW|buck}} = \frac{\left(-8M^3 + 12M^2 - 8M + 1\right)(t_r + t_f) I_o V_{\mathrm{in}}}{16M^2 - 24M + 8} \quad \text{(A34)}$$

$$P_{\mathrm{PDP,\ SW|buck}} = \frac{M^3 (t_r + t_f) I_o V_{\mathrm{in}}}{2M - 1}. \quad \text{(A35)}$$

For comparison, the switching loss of the buck-mode FBBC (i.e., $P_{\mathrm{FBB,SW|buck}}$) is written as follows:

$$P_{\mathrm{FBB,\ SW|buck}} = (t_r + t_f)\ I_o V_{\mathrm{in}}. \quad \text{(A36)}$$

Based on the above-mentioned analyses, the switching loss comparison ratios in the buck and boost modes are plotted in Fig. 24. The switch voltage stress in the proposed boost-mode HBBC is V_{in}, whereas it is V_o ($> \mathrm{V_{in}}$) in the conventional boost-mode FBBC. Accordingly, although the proposed boost-mode HBBC has three power switches to take the switching actions, its switching loss is lower than that of the boost-mode FBBC when $1 < M < 1.62$, as shown in Fig. 24(b). In Fig. 24(a), similar switching loss improvement can be observed for the "partial-dual-path" buck-mode HBBC, where the switch voltage stress is V_o and smaller than V_{in} in the buck-mode FBBC. $P_{\mathrm{ADP,SW|buck}}$ is higher than $P_{\mathrm{FBB,SW|buck}}$ because six power switches take the switching actions in the "always-dual-path" buck-mode HBBC. Yet, since the "always-dual-path" buck-mode HBBC reduces I_L by half, which decreases the DCR loss of the inductor (P_{DCR}) by 75%, the increased switching loss is counteracted by the dramatically reduced P_{DCR}. This advantage becomes more significant when a high-DCR inductor is utilized.

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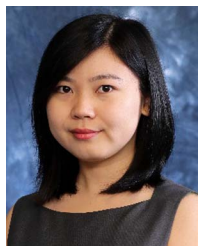

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