Analysis of Dead-Time Energy Loss in GaN-Based TCM Converters With an Improved GaN HEMT Model

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***Abstract*—For gallium nitride (GaN) based triangular current mode (TCM) applications, the dead-time has a significant effect on the switching loss. However, previous GaN high electron mobility transistor (HEMT) models focus on the turn-ON/OFF process without fully considering the effect of the dead-time. Hence, this article analyzes the switching transients under the superfluous and insufficient dead-time and evaluates the dead-time loss with an improved GaN HEMT model. The proposed model improves an existing GaN HEMT model by adding the voltage rising/falling time of the gate driver, the dynamic threshold voltage of Schottky-type GaN HEMTs, and an equivalent gate-drain capacitance obtained from the datasheet. Verified by a GaN-based double-pulse test, the proposed model can more accurately calculate the gate-source voltage and the self-commutated reverse conduction voltage. Verified by a GaN-based TCM Buck converter, the proposed model can predict the dead-time loss well and has higher simulation accuracy for the turn-ON process induced by the inappropriate dead-time.**

***Index Terms*—Dead-time, device model, gallium nitride high electron mobility transistor (GaN HEMT), triangular current mode (TCM).**

I. Introduction

GALLIUM nitride (GaN) high electron mobility transistors (HEMTs) are favored for converters with high switching frequency due to the characteristics of low junction capacitance, small gate charge, and improved reverse recovery [1]. Besides, GaN HEMTs show the advantage of ultralow turn-OFF loss [2], which is preferred for zero-voltage-switching (ZVS) applications. In recent years, a novel ZVS switching technology, triangular current mode (TCM) modulation method, has been developed [3] and [4]. By using GaN devices, high-frequency TCM converters can achieve high power density with high efficiency [5], [6], [7]. Liu et al. [5] proposed a 1.2 kW MHz dual-phase interleaved totem-pole PFC with 99% efficiency and 220 W/in^3 power density. A 1 kW MHz interleaved single-phase inverter is verified to achieve a peak efficiency of 98% and 135 W/in^3 power density in literature [6].

For TCM converters, the energy stored in the output junction capacitor (E_{oss}) during the turn-OFF transition will be dumped before the turn-ON process, so the energy dissipation of the turn-OFF transition is ultralow. Compared with the turn-OFF loss, the loss induced by dead-time may be more dominant in the switching loss. When the dead-time is insufficient, ZVS is not achievable, resulting in an extra turn-ON loss. When the dead-time is superfluous, the freewheeling transistor will conduct reversely under the off gate driving voltage (Although e-mode GaN HEMT does not have a body-diode, it demonstrates a self-commutated reverse conduction (SCRC) mechanism, which provides diode-like behavior [1].), which will lead to an extra reverse conduction loss. Compared with the voltage drop on a MOSFET body diode, the SCRC voltage drop is usually quite higher, so GaN-based converters will suffer a huger reverse conduction loss during the redundant dead-time [8].

Since the turn-OFF time of a GaN device is influenced by operating parameters, such as turn-OFF current (I_{OFF}), input voltage, and output voltage, the optimal dead-time, which corresponds to the minimum switching loss will vary with operating conditions. As described in [9], when I_{OFF} is reduced from the rated to 1 A, the turn-OFF time will increase by around 20 times. Therefore, if a relatively short dead-time is used to restrain the reverse conduction loss for heavy loads, huge extra turn-ON losses may arise when the load gets light. Although some dynamic dead-time adjustment methods have been proposed to restrain the dead-time loss [10], [11], [12], [13], [14], [15], they require extra high-speed detection circuits [10], [11], [12] or precalculated look-up tables for the dead-time [13], [14], [15], which increases the system complexity. Therefore, fixed dead-time is still widely used in TCM applications [4] and [5], where the effect of dead-time needs to be assessed during the design process for efficiency evaluation, maximum junction temperature prediction, and thermal design.

Extra losses under different dead-time were experimentally investigated in [16], [17], and [18]. Although the experimental method is accurate, it is specific to a particular converter and requires a lot of experiments for converters with a wide

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operating range. In literature [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], device models are established to evaluate the switching process of transistors. Based on the specific implementation method, these device models can be divided into the physics-based model [19] and [20], the behavioral model [21], [22], [23], and the analytical model [8], [13], [14], [15], [24], [25], [26], [27], [28], [29], [30], and [31]. Physics-based models are established based on the physical structure of semiconductors [19] and [20]. They can simulate experimental results very well, but are usually time-consuming and rely on the physical model from the device manufacturer. Behavior models are widely used in simulation software (e.g., PSpice) because they are faster than physics-based models and can provide relatively accurate results [21], [22], [23]. However, behavior models are not suitable for processing massive data [15] and [31]. Therefore, analytical models are proposed for faster calculation speed and the convenience to achieve batch processing for massive data.

Analytical models are based on circuit equations, where the challenge is how to improve the accuracy. In literature [8], [24], [25], and [26], the switching process is divided into several switching modes, and corresponding equations are established to describe these modes. Based on these equations, the analytical expressions of state variables (e.g., the drain-source voltage) or switching losses are solved to evaluate the switching performance. In literature [27], [28], and [29], the nonlinear parameters of devices such as the junction capacitance are expressed by the fitting functions of state variables. Based on circuit equations with fitting functions, analytical expressions of the transient waveforms are solved, which can reflect the nonlinear characteristics of devices. Literatures [13], [14], [15], [30], and [31] calculate the numerical solution of the switching transient waveforms instead of the analytical expressions. In these models, the nonlinear characteristics are extracted from the datasheet and updated in the solution flow. To distinguish from the models with analytical expressions [8], [24], [25], [26], [27], [28], and [29], the models proposed by [13], [14], [15], [30], and [31] are called transient models in this article. Compared with the model with analytical expressions, the transient model is more complicated but more accurate because it can reflect the nonlinear characteristics of devices, including the parasitic inductance and the coupling of the gate loop and power loop. Compared with the physics-based model and behavior model, the transient model is simpler and can help to make a better understanding of the switching transient process at the circuit level [15] and [31]. Moreover, the transient model is easy to implement in MATLAB with the advantages of good batch processing capacity. Therefore, this article uses the transient model to evaluate the switching process.

For transient models in literature [13], [14], [15], [30], and [31], the gate driver voltage ($V_{\rm g}$) is approximated as an ideal step voltage source. This approximation, however, will cause a considerable error in the calculation of the gate delay period because of the ultralow gate charge ($Q_{\rm g}$) of GaN devices. Besides, these models have not considered the dynamic threshold voltage ($V_{\rm th}$) of Schottky-type GaN HEMTs, which affects the turn-ON process under insufficient dead-time and the SCRC voltage [23]. Moreover, according to the datasheet, the total $Q_{\rm g}$ during the turn-ON process is higher than the sum of the gate-source charge and gate-drain charge obtained from the "Typical $C_{\rm iss}$, $C_{\rm rss}$, and $C_{\rm oss}$ versus $v_{\rm ds}$" curve. Therefore, if the gate-drain capacitance ($C_{\rm gd}$) is only obtained from the "$C_{\rm rss}$ versus $v_{\rm ds}$" curve, the calculated turn-ON transition is significantly faster than the practical.

This article aims to evaluate the dead-time loss in GaN-based TCM converters with an improved GaN HEMT model, which can help designers better grasp the effect of the dead-time. Since predicting the turn-OFF time of the device is the basis for evaluating the dead-time loss, first, this article proposed an improved transient model to simulate the turn-OFF process of GaN HEMT more accurately. In the proposed model, the step $V_{\rm g}$ is replaced by a ramp $V_{\rm g}$ to calculate the gate delay time more accurately, and the dynamic $V_{\rm th}$ of Schottky-type GaN HEMTs is considered. To calculate the dynamic $V_{\rm th}$, a simplified method based on a double-pulse test (DPT) is used to extract the capacitance between the floating *p*-GaN layer and gate ($C_{\rm sh}$) [23]. Then, the effect of dead-time on TCM converters is analyzed. Although the method to calculate the dead-time for realizing ZVS in TCM converters has been given in the previous literature [3], [4], [5], [6], [7], huge reverse conduction loss will arise at heavy load if the dead-time is selected according to the lightest $I_{\rm OFF}$, especially for ac applications. To obtain the lowest comprehensive loss, the selection of dead-time should be the tradeoff between the reverse conduction loss and the extra turn-ON loss (caused by insufficient dead-time) rather than simply eliminating one or the other. Therefore, the turn-ON process under insufficient dead-time is considered. Besides, in traditional designs, a long dead-time is often proposed to ensure ZVS at small $I_{\rm OFF}$. However, due to the low filter inductance of TCM, a superfluous dead-time could induce the extra turn-ON loss too, which is also analyzed in this article. Based on the analysis, the proposed model is used to theoretically evaluate the dead-time-related loss. To improve the simulation accuracy for the turn-ON process, according to $Q_{\rm g}$ provided by the datasheet, the proposed model adds an equivalent capacitance to the $C_{\rm gd}$ obtained from the "$C_{\rm rss}$ versus $v_{\rm ds}$" curve.

The rest of this article is organized as follows. In Section II, the switching process under TCM modulation is introduced. In Section III, the improved GaN HEMT model is established and verified by a DPT. In Section IV, the effect of dead-time on TCM converter is analyzed, and the proposed model is used to evaluate the dead-time loss. In Section V, a GaN-based TCM Buck converter is established to verify the dead-time loss calculation of the proposed model. Finally, Section VI concludes this article.

II. Brief Introduction of TCM

To realize high power density with high efficiency, Marxgut et al. [3] proposed a soft-switching modulation method called TCM modulation due to its triangular-shaped inductor currents. In TCM, before the transistor is turned on, an extra reverse current (from the source to the drain) is introduced to discharge the drain-source capacitance ($C_{\rm ds}$) of the device to the SCRC

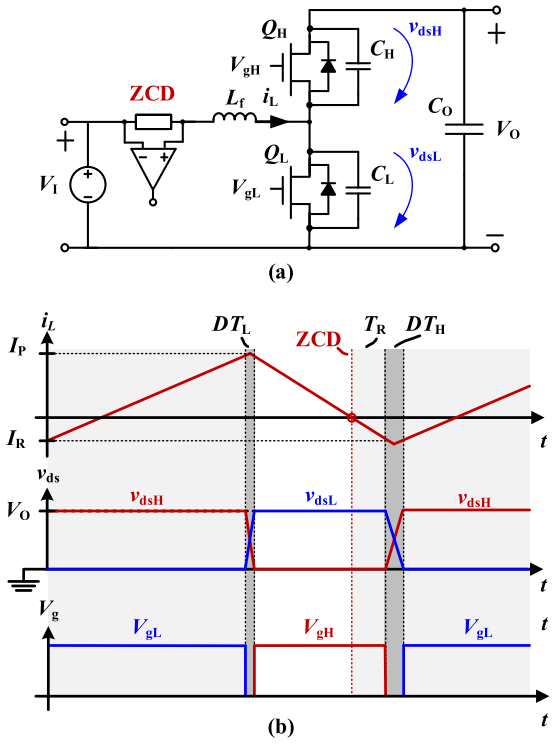

Fig. 1. (a) Equivalent circuit of the boost circuit. (b) Typical TCM operation waveforms.

voltage. Take the boost circuit as an example, the equivalent circuit and typical TCM operation waveforms are shown in Fig. 1(a) and (b) [4], where Q_H and Q_L are the high-side and low-side transistors, and C_H and C_L are their output junction capacitors. When Q_L is ON, V_I is applied on the filter inductance (L_f), and the inductor current (i_L) rises linearly. After i_L reaches the desired peak value (I_P), Q_L is turned OFF. When the dead-time DT_L is enough, i_L will discharge v_{dsH} to the SCRC voltage, and then Q_H can be turned ON at zero voltage. After Q_H conducts reversely, i_L falls linearly. In TCM control, based on the zero-current detection of i_L, a reverse inductor current (I_R) is introduced by a programmed delay (T_R). After T_R, Q_H is turned OFF, and C_L is discharged by I_R. When the dead-time DT_H is enough, i_L will discharge v_{dsL} to the SCRC voltage, and then Q_L can be turned ON at zero voltage.

Based on the abovementioned analysis, the difference between TCM and traditional continuous conduction mode (CCM) converter can be concluded as follows.

1) When the dead-time is enough, both Q_H and Q_L are turned ON at zero voltage, so the turn-ON loss is ignorable. Besides, since E_{oss} is dumped during the dead-time, it should be subtracted from the traditional loss calculation (1).
2) To realize the triangular-shaped inductor current with a high switching frequency, the filter inductance used in the TCM converter is usually much smaller.
3) Both Q_L and Q_H are turned OFF at positive I_{OFF} (from drain to source), so communication between the high-side and low-side transistors happens as soon as the transistor is

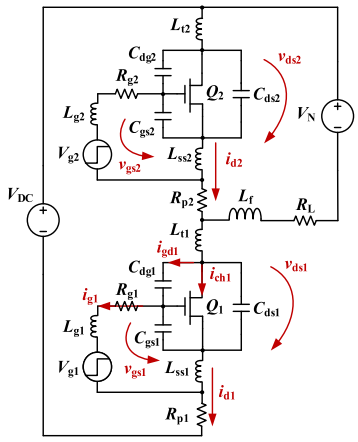

Fig. 2. Equivalent circuit for GaN HEMTs.

turned OFF

$$E_{off} = \int i_d \cdot v_{ds} dt. \tag{1}$$

III. Improved GaN HEMT Model

A. Equivalent Circuits of the Proposed Model

To evaluate the turn-OFF loss and calculate the turn-OFF time for dead-time loss evaluation, this article improves the previous transient models [13], [14], [15], [30], and [31] for GaN HEMT. Fig. 2 shows the equivalent circuit used to analyze the switching process of GaN HEMTs. Since both the upper and lower switches of TCM converters are turned OFF at positive I_{OFF}, their turn-OFF process can be analyzed, as Q_1 in Fig. 2, which is turned OFF at I_P and $-I_R$, respectively. Around the ideal HEMTs Q_1 and Q_2, there are the junction capacitance (C_{gs} for the gate-source capacitance, C_{gd} for the gate-drain capacitance, and C_{ds} for the drain-source capacitance), the stray resistance (R_{p2} for the upper leg, R_{p1} for the lower leg, and R_L for the filter inductor), and the parasitic inductance (L_g for the gate stray inductance, L_t for the power loop stray inductance, and L_{ss} for the common-source inductance). V_{dc} is the turn-OFF dc voltage, which is V_O for boost circuits. V_N is an equivalent output voltage that is determined by the connection mode of the output filter capacitor. Take the boost circuit in Fig. 1 as an example, V_N is V_I for the upper switch Q_H, while V_N is "$V_O - V_I$" for the lower switch Q_L.

As proposed in the literature [31], the transistor has two different turn-OFF processes, as shown in Fig. 3(a) and (b). In the beginning, the gate-source voltage v_{gs1} is the on gate voltage (V_{gON}), and Q_1 is ON. At t_1, the output voltage of the gate driver (V_{g1}) goes to the OFF gate voltage (V_{gOFF}), and v_{gs1} starts to decrease. Accordingly, the inductor current i_L at t_1 is I_{OFF}. Before v_{gs1} falls below the Miller voltage V_{mil} ($V_{mil} = V_{th} + i_L / g_m$: g_m for the trans-conductance, and V_{th} for the threshold voltage), Q_1 remains ON. At t_2, v_{gs1} falls to V_{mil}. Controlled by v_{gs1}, the channel current of Q_1 (i_{ch1}) starts to decrease, and the current flows into C_{ds1} and C_{ds2} to force v_{ds1} to rise (v_{ds2} to fall). Since the charging current of C_{dg1} (i_{gd1}) induced by dv_{ds1}/dt occupies

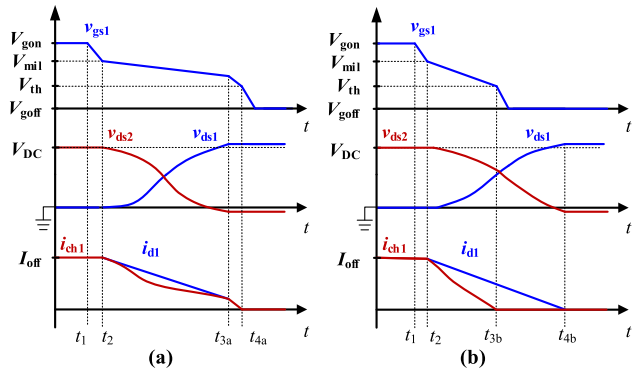

Fig. 3. Equivalent turn-OFF waveforms. (a) Process 1. (b) Process 2.

the gate current (i_{g1}), v_{gs1} will enter a platform region known as the Miller platform.

Process 1 [see Fig. 3(a)]: When Q_1 is turned OFF at high I_{OFF}, higher i_L can provide a larger current to charge C_{ds}, which leads to higher i_{gd1}. When i_{g1} is fully occupied by i_{gd1}, v_{gs1} cannot further decrease during the v_{ds1} rising process "$t_2 - t_{3a}$". This v_{gs} platform will not disappear until v_{ds2} decreases to the SCRC voltage (V_{RC}), which can be calculated as "$-V_{th} + V_{gOFF} + R_{ON} * i_{d2}$" for GaN HEMTs. At t_{3a}, v_{ds2} decreases to V_{RC}, Q_2 conducts reversely, so v_{ds1} is clamped to $V_{dc} - V_{RC}$. Since dv_{ds1} / dt gets 0, i_{gd1} disappears and v_{gs1} begins to decrease further. Then, when v_{gs1} falls below V_{th} at t_{4a}, i_{ch1} falls to 0 A, and Process 1 ends. Similarly, besides large I_{OFF}, a slow gate driver (e.g., huge R_{g1}), which cannot provide enough i_{g1}, will also lead to Process 1.

Process 2 [see Fig. 3(b)]: When Q_1 is turned OFF at a small I_{OFF} or with a fast gate driver (e.g., small R_{g1}, or negative V_{gOFF}), i_{gd1} cannot cover i_{g1}, so v_{gs1} keeps falling. Therefore, v_{gs1} falls below V_{th} earlier than v_{ds2} falls below V_{RC}. After t_{3b}, v_{gs1} falls below V_{th} and the channel of Q_1 is OFF, so all of i_L flows into the junction capacitors to discharge v_{ds2} (charge v_{ds1}). When v_{ds2} is discharged to V_{RC} at t_{4b}, Q_2 conducts reversely, and Process 2 ends.

After Process 1/ Process 2, Q_1 has been fully turned OFF. Then, the parasitic inductance will resonate with the junction capacitance, which generates a voltage overshoot at v_{ds1}. According to the equivalent turn-OFF waveforms, the turn-OFF process can be divided into five switching periods: the gate delay period ($t_1 - t_2$), the voltage rising period ($t_2 - t_{3a}$ or t_{3b}), the current falling period ($t_{3a} - t_{4a}$), the C_{oss} charging period ($t_{3b} - t_{4b}$), and the parasitic resonance period (after t_{4a} and t_{4b}). The equivalent circuits of these switching periods are shown in Fig. 4(a)–(e). Since Q_2 is OFF during these periods, v_{ds2} is represented by the output capacitor voltage (v_{co2}). Based on the equivalent circuits, (8)–(15) is derived to describe the turn-OFF transition. Based on (2)–(13), the state (T1) are derived to calculate the gate delay period with the initial conditions: $v_{gs1} = V_{gON}$, $i_{g1} = 0$, $v_{ds1} = R_{ON} * I_{OFF}$, $i_{d1} = I_{OFF}$, $v_{ds2} = V_{dc} - R_{ON} * I_{OFF}$, $i_L = I_{OFF.}$, which is shown in the appendix. Based on (8), (9), and (11)–(14), the state (T2) are derived to calculate the voltage rising period. Based on (8), (9), (11), (14), and (15), the state (T3) are derived to calculate the current falling period. Since the only difference between the C_{oss} charging interval and the voltage rising interval is that the channel of Q_1 is OFF, the C_{oss} charging interval can be calculated by T2 with $g_m = 0$. Similarly, the parasitic resonance period can be calculated by T3 with $g_m = 0$.

To reflect the nonlinear parameters such as the junction capacitance, the state (T1)–(T3) are solved by the iteration calculation method [13], [14], [15], [30], and [31]. The proposed model can be implemented in MATLAB to calculate the transient waveforms numerically.

B. Improvement of the Proposed Model

In the previous works [13], [14], [15], [30], and [31], V_g is regarded as an idea step voltage. However, shown as the yellow curve in Fig. 5, the practical unloaded V_g has a falling time of around 14 ns. Because Q_g of GaN devices is ultrasmall, using the step V_g, the v_{gs1} falling speed obtained by simulation will be considerably faster than the practical. To increase the simulation accuracy, the proposed model uses a ramp V_g, as the blue curve in Fig. 5, which can be obtained from the datasheet of the gate drive IC without experiment.

In the previous works [13], [14], [15], [30], and [31], V_{th} is constant. However, according to literature [23], the Schottky-type GaN HEMTs show the dynamic threshold voltage related to v_{ds} and V_{dc}, which is caused by the charge stored in the floating *p*-GaN layer. As proposed by literature [23], the relationship between the increment of threshold voltage (ΔV_{th}), v_{ds}, and V_{dc} can be expressed by (2), where C_{sh} is the capacitance between the floating *p*-GaN layer and the gate. For Q_2, the SCRC voltage is "V_{gOFF} - $V_{th} + R_{ON} * i_d$", which is affected by the dynamic threshold voltage. To accurately calculate the conduction loss during the redundant dead-time, this article adds ΔV_{th} to the transient model. In literature [23], to extract C_{sh}, dynamic V_{th} is experimentally obtained by measuring the "i_d versus v_{gs}" characteristics after voltage transition (The GaN HEMT is first stressed at a high V_{dc} and then switched to lower voltage $v_{ds.}$), which needs complex measuring equipment. Since the expression of ΔV_{th} has been confirmed, C_{sh} can be extracted more simply based on DPT, which will be analyzed following:

$$\Delta V_{th} = \left(\int_{0V}^{V_{dc}} C_{gd} dv_{ds} - \int_{0V}^{v_{ds}} C_{gd} dv_{ds} \right) / C_{sh}. \quad (2)$$

C. Experimental Verification

A GaN-based DPT circuit shown in Fig. 6 is established to verify the improvement of the proposed model in the turn-OFF waveforms simulation. The used device is GS66516T from GaNSystems, which is driven by Si8271-GB. The waveforms are recorded by a LeCroy oscilloscope. The drain current of the device is tested by the shunt SSDN-10 from T and M research products. To ensure that the measurements of v_{gs1}, v_{ds1}, and i_{d1} have a common ground, the shunt is reversely connected, as depicted in Fig. 6(a), so the tested i_{d1} is inverted. The electric parameters used in the DPT circuit are listed in Table I. The parasitic parameters are extracted by Q3D simulation. The used L_f is 52 uH.

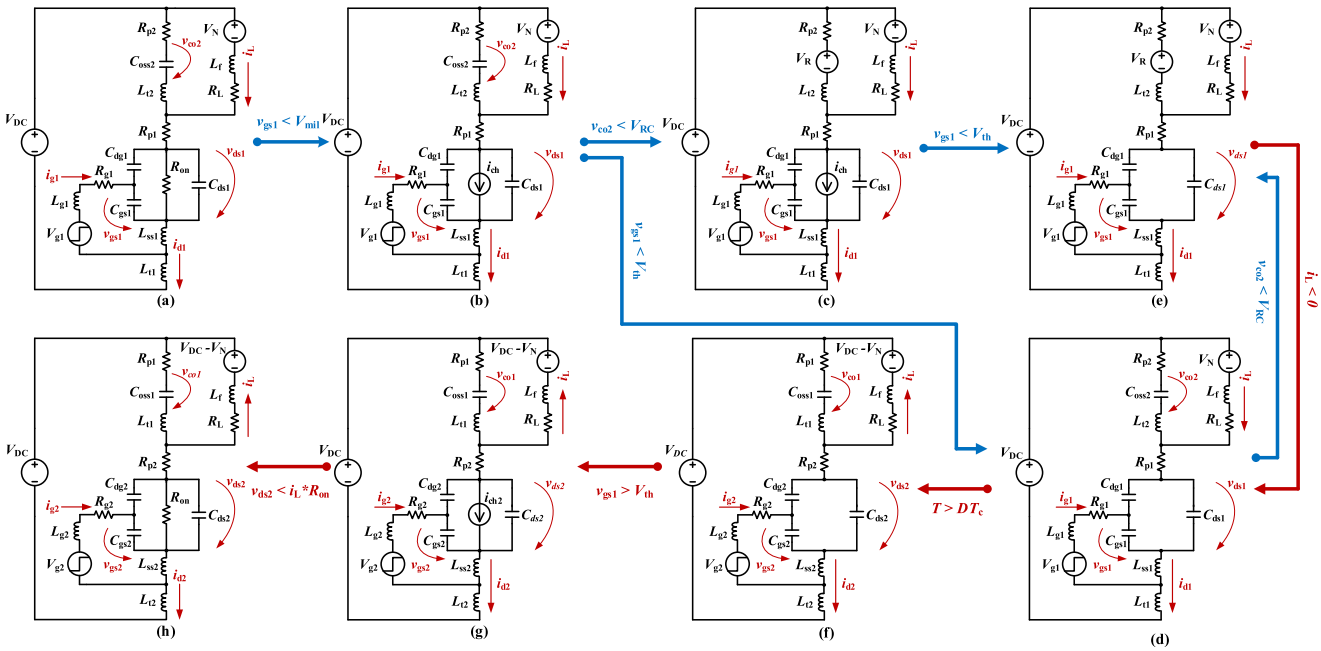

Fig. 4. Turn-OFF periods of GaN HEMTs. (a) Gate delay period ($t_1 - t_2$). (b) Voltage rising period ($t_2 - t_{3a}$ or t_{3b}). (c) Current falling period ($t_{3a} - t_{4a}$). (d) C_{oss} charging period ($t_{3b} - t_{4b}$). (e) Parasitic resonance period (after t_{4a} and t_{4b}). (f) Turn-ON delay period [$t_5 - t_6$ in Fig. 10(c)]. (g) Voltage falling period [$t_6 - t_7$ in Fig. 10(c)]. (h) Conduction period [after t_7 in Fig. 3(a) and (b)].

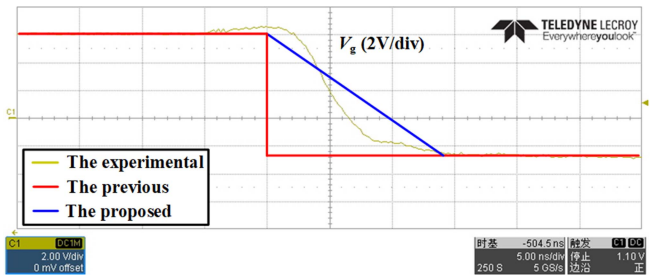

Fig. 5. Waveforms of the gate driver voltage V_g.

TABLE I
PARASITIC PARAMENTS OF DPT CIRCUIT

Part.	Value	Part.	Value
V_{dc}	400 V	V_{gon}	6 V
V_{goff}	-3 V	$R_{p1/p2}$	34.4/4.6 mΩ
R_g	5.74 Ω	R_L	0.17 Ω
L_g	6.3 nH	L_{p1}	11.92 nH
L_{p2}	1.62 nH	L_{ss}	0.18 nH

First, to acquire C_{sh}, V_{RC}, which can be calculated by "V_{gOFF} - V_{th} + R_{ON} * i_d", is measured. By connecting points O and -dc in Fig. 6(a), Q_2 acts as an active transistor, and Q_1 acts as a freewheeling transistor, so V_{RC} can be directly measured by a passive probe. Fig. 7 shows V_{RC} at different V_{dc}. It is obvious that ignoring the dynamic V_{th} will result in a less SCRC loss compared with the practical, especially in applications with high V_{dc}. Based on the tested V_{RC}, C_{sh} can be calculated by (3). Then, V_{RC} under different V_{dc} can be obtained according to (2)

$$C_{sh} = \left(\int_{0V}^{V_{dc1}} C_{gd} dv_{ds} - \int_{0V}^{V_{dc2}} C_{gd} dv_{ds} \right) / (V_{RC@V_{dc2}} - V_{RC@V_{dc1}}). \quad (3)$$

By connecting point O and +dc in Fig. 6(a), Q_1 acts as an active transistor, and Q_2 acts as a freewheeling transistor, so the turn-OFF transient waveforms can be directly measured by passive probes. The experimental waveforms are compared with the simulated results in Fig. 8. For comparison, the results simulated by the previous transient model are also shown in Fig. 8. According to literature [31], C_{ds} has an internal resistance, which scarcely affects the switching transient, but has considerable influence on the damping time of the C_{oss}-L_p resonance in the parasitic resonance period. Therefore, an equivalent resistance is calculated by the damping time of the measured switching waveforms [32] and added into R_{p1} in the parasitic resonance period. Fig. 8(a) shows the turn-OFF waveforms at 1 A I_{OFF}. At small I_{OFF}, the C_{oss} charging period dominates the turn-OFF time "t_1 - t_{4b}". Therefore, the difference between the proposed and the previous transient models is inconspicuous, and both of them can fit the experiment well. However, as shown in Fig. 8(b), as I_{OFF} increases to 22 A, the voltage rising period and C_{oss} charging period decreases greatly. By contrast, the gate delay time takes up a more significant part of the turn-OFF time. For the previous model, although it can simulate v_{ds} and i_d well, the simulated gate delay period is much shorter than the experiment because V_g is approximated as an ideal step voltage source. Using the ramp V_g, the proposed model can better fit the output of the gate driver, so the simulated v_{gs} is more accurate.

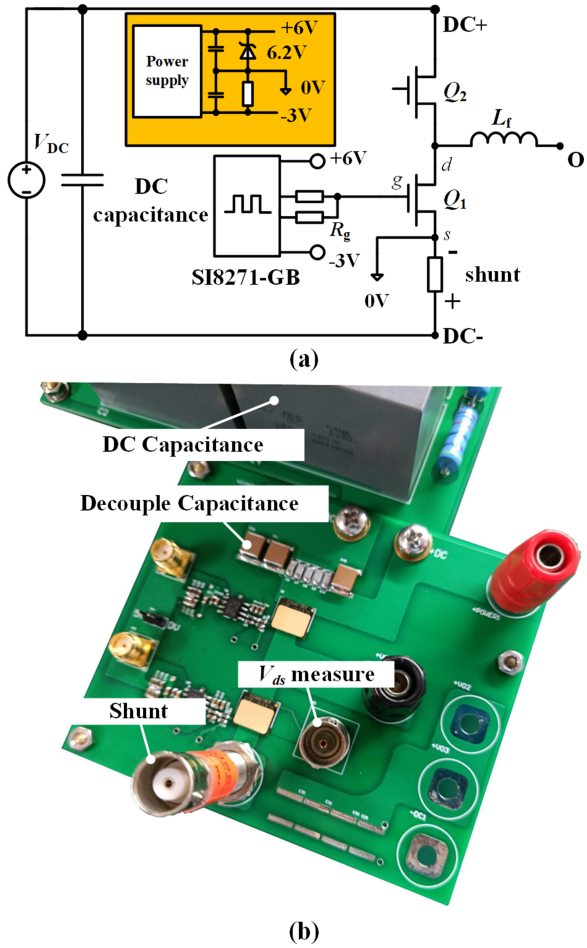

Fig. 6. (a) Schematic of the DPT circuit. (b) Prototype of DPT circuit.

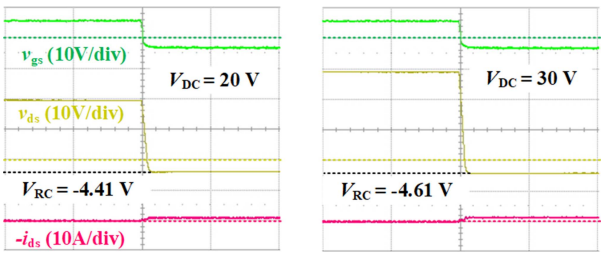

Fig. 7. V_{RC} at 20 / 30 V V_{dc}.

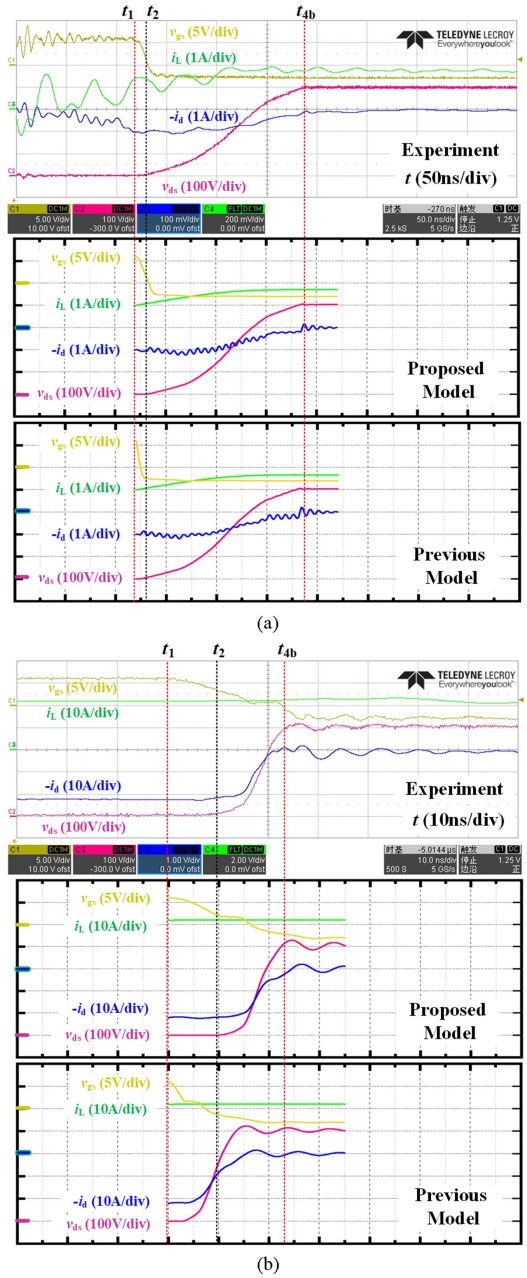

Fig. 8. Waveforms acquired by the experiment, the proposed model, and the previous model. (a) At 1 A I_{OFF}. (b) At 22 A I_{OFF}.

IV. Model-Based Evaluation of the Dead-Time Loss in GaN-Based TCM Converters

After Q_1 is fully turned OFF, the zero-voltage turn ON of Q_2 can be realized. To minimize the switching loss, the channel of Q_2 should be turned ON at t_{4a} or t_{4b}, which means v_{gs2} rises to V_{th} at t_{4a} or t_{4b}. However, because the turn-OFF time "t_1 - t_{4a}/t_{4b}" are affected by operating parameters such as I_{OFF} and V_{dc}, a fixed dead-time can not fit all the working conditions. As proposed in literature [8], losses caused by inappropriate dead-time could dominate the switching loss. Therefore, in this section, the dead-time transients are analyzed, and the proposed model is used to evaluate the dead-time loss.

A. Analysis of Dead-Time Effect

Fig. 9(a) and (b) shows the operation waveforms under superfluous dead-time (for simplicity, the transfer delay of the gate signal is ignored, which will be discussed following). After Q_1 is fully turned OFF at t_{4a}/t_{4b}, the extra reverse conduction loss arises in "t_{4a}/t_{4b} to t_6" because of the relatively high SCRC voltage. At t_5, the turn-ON gate drive signal comes, and then v_{gs2} rises to V_{th} at t_6. The extra energy dissipation caused by the redundant dead-time (E_{RC}) can be calculated by

$$E_{RC} = \int_{t_{4a}/t_{4b}}^{t_6} i_{d2}(V_{goff} - V_{th})dt \tag{4}$$

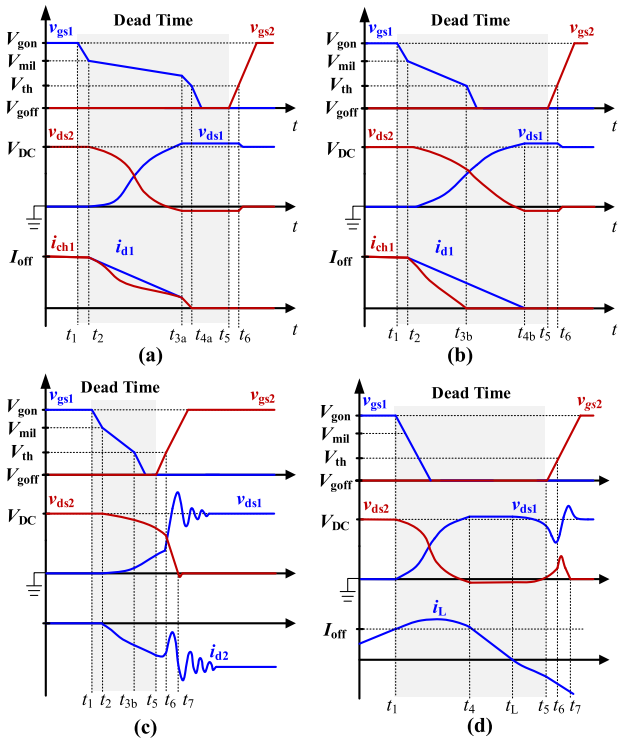

Fig. 9. Equivalent waveforms at different dead-time. (a) Process 1 under superfluous dead-time. (b) Process 2 under superfluous dead-time. (c) Turn-ON process under insufficient dead-time. (d) Turn-ON process under superfulous dead-time.

When the dead-time is insufficient, its effect depends on $v_{\rm gs1}$. If the channel of Q_2 is turned ON when $v_{\rm gs1}$ is above $V_{\rm th}$ ($t_1 - t_{4a}$, or $t_1 - t_{3b}$), the short-circuit through the channel of Q_1 and Q_2 happens. Since the huge short-circuit current will damage the devices, this situation must be avoided.

When Q_2 is turned ON between t_{3b} and t_{4b}, the short-circuit will not happen because $v_{\rm gs1}$ has fallen below $V_{\rm th}$. However, since $v_{\rm ds2}$ has not fallen below $V_{\rm RC}$, Q_2 is turned ON at a voltage below $V_{\rm dc}$, which will cause extra turn-ON loss compared with the zero-voltage turn ON. As shown in Fig. 9(c), $v_{\rm gs2}$ rises to $V_{\rm th}$ at t_6 before $v_{\rm ds2}$ falls to 0 V. Since the channel of Q_1 is OFF, $V_{\rm dc}$ charges $C_{\rm ds1}$ through the channel of Q_2 ($C_{\rm ds2}$ discharges at the same time). These processes will make $i_{\rm d1}$ and $i_{\rm d2}$ increase sharply and increase the $v_{\rm ds1}$ rising speed ($v_{\rm ds2}$ falling speed). When $v_{\rm ds2}$ falls to $R_{\rm ON} * i_{\rm d2}$ at t_7, the turn-ON process of Q_2 ends. Since the high current and voltage are applied on the channel of Q_2 during "$t_6 - t_7$", the extra turn-ON energy ($E_{\rm TO}$) is dissipated, which can be calculated by (5) [Due to the increase of $i_{\rm d1}$ and $i_{\rm d2}$, extra energy is dissipated in the loop resistance, which is also added in (5)]

$$E_{\rm TO} = \int_{t_6}^{t_7} (v_{\rm ds2} i_{\rm ch2} + i_{\rm d2}^2 R_{\rm p2} + i_{\rm d1}^2 R_{\rm p1}) dt. \qquad (5)$$

Since $E_{\rm RC}$ is relatively light at small $i_{\rm d2}$, a long dead-time is often recommended for small $I_{\rm OFF}$ in traditional CCM converters. However, using a superfluous dead-time could cause an extra turn-ON loss in TCM converters. After Q_1 is fully turned OFF at t_4, the negative voltage is applied on $L_{\rm f}$, which forces $i_{\rm L}$ to decrease. In TCM converters, $L_{\rm f}$ is usually much smaller than in traditional CCM converters, so $i_{\rm L}$ decreases more rapidly. In addition, $i_{\rm L}$ is easier to fall to 0 A at smaller $I_{\rm off}$ (eg., -$I_{\rm R}$). Fig. 9(d) depicts the equivalent waveforms of the turn-ON process under superfluous dead-time. At $t_{\rm L}$, $i_{\rm L}$ falls below 0 A, and Q_2 stops reversely conducting. Because Q_2 has not been turned ON, $C_{\rm oss}$ will resonate with $L_{\rm f}$, which makes $v_{\rm ds2}$ rise again. At t_6, the channel of Q_2 is turned on at a voltage below $V_{\rm dc}$, and the subsequent process is the same as depicted in Fig. 9(c) previously.

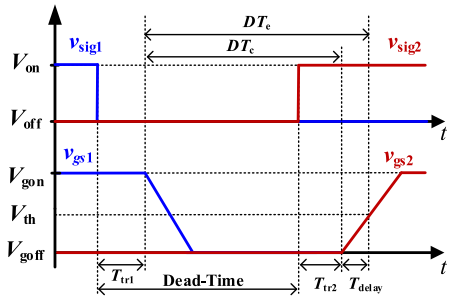

Fig. 10. Relationship between $DT_{\rm c}$, $DT_{\rm e}$ and the dead-time.

B. Equivalent Circuits of the Dead-Time Transients

In general, the dead-time refers to the interval between the ON-signal of the upper and bottom transistor sent by the controller. In the proposed model, $DT_{\rm c}$ and $DT_{\rm e}$ are used, which are depicted in Fig. 10. After the control signal ($v_{\rm sig1}$ and $v_{\rm sig2}$) goes ON or OFF, it takes the transfer time ($T_{\rm tr1}$ and $T_{\rm tr2}$) to act on the gate of devices. The transfer time is affected by several factors, such as the gate driver and layout, and is almost unchanged with the operation condition. For converters with the symmetrical signal layout, $T_{\rm tr1}$ and $T_{\rm tr2}$ are mainly dominated by the propagation delay of the gate drive isolator, which can be obtained from the datasheet. After the turn-ON signal of Q_2 is given, the gate delay time $T_{\rm delay}$ can be calculated by T3 with the initial condition: $v_{\rm gs1} = V_{\rm gOFF}$, and terminal conditions: $v_{\rm gs1} = V_{\rm th}$. Accordingly, $DT_{\rm c}$ can be calculated by "dead-time – $T_{\rm tr1}$ + $T_{\rm tr2}$," and $DT_{\rm e}$ can be calculated by "$DT_{\rm c} + T_{\rm delay}$."

As analyzed previously, when $DT_{\rm e}$ ends in the gate delay period, the voltage rising period, and the current falling period ($v_{\rm gs1} > V_{\rm th}$), short-circuit happens because $v_{\rm gs1}$ is above $V_{\rm th}$, which must be avoided. When $DT_{\rm e}$ ends in the $C_{\rm oss}$ charging period ($v_{\rm gs1} < V_{\rm th}$), the device is turned ON at the voltage below $V_{\rm dc}$, as depicted in Fig. 9(c). According to the equivalent waveforms, the turn-ON process can be divided into three switching periods: the turn-ON delay period, the voltage falling period, and the conduction period.

Turn-ON delay period [see $t_5 - t_6$ in Fig. 9(c)]: Fig. 4(f) shows the equivalent circuits. When the simulation time $T = DT_{\rm c}$, the final value of $v_{\rm ds1}$, $v_{\rm co2}$, $i_{\rm d1}$, and $i_{\rm L}$ is saved as the initial conditions of the turn-ON process. For Q_2, $i_{\rm L}$ is reversed, and the output voltage is $V_{\rm dc} - V_{\rm N}$. Because the turn-ON delay period is symmetrical to the $C_{\rm oss}$ charging period, it can be calculated by

T2 ($g_m = 0$) by changing the state variables of Q_1 to Q_2. When v_{gs2} rises to V_{th}, this period ends.

Voltage falling period [$t_6 - t_7$ in Fig. 9(c)]: Fig. 4(g) shows the equivalent circuits. Since the channel of Q_2 is controlled by v_{gs2}, it is represented by a controlled current source. Because the voltage falling period is symmetric with the voltage rising period, it can be calculated by T2 by changing the state variables of Q_1 to Q_2. When v_{ds2} falls below $-i_L * R_{ON}$, Q_2 is fully turned ON and this period ends.

Conduction period [after t_7 in Fig. 9(c)]: Fig. 4(h) shows the equivalent circuits. Since Q_2 has been fully turned ON, it is regarded as the ON-resistance R_{ON}. the conduction period is symmetric with the gate delay period, so it can be calculated by (T1) by changing the state variables of Q_1 to Q_2.

When DT_e ends after t_{4a}/t_{4b}, the effect is dependent on i_L. If DT_e ends before i_L falls below 0, there is only E_{RC} generated in the parasitic resonance period. After i_L falls to 0 A, Q_2 stops conducting reversely, and the process returns to the C_{oss} charging period again. If DT_e ends in this situation, the following process is the same as that analyzed in the turn-ON delay period, the voltage falling period, and the conduction period.

As mentioned in Section III, the state equations are solved based on the iteration calculation method. For Schottky-type GaN HEMTs, according to (2), V_{th} will increase as v_{ds} falls [23] during the turn-ON process. Ignoring the dynamic V_{th}, the simulated turn-ON process will be faster than the practical. Therefore, during the solution process, V_{th} is also updated by (2), where C_{sh} is obtained by DPT.

As shown in the datasheet provided by GaNSystems [32], the total gate charge Q_g of the turn-ON process is higher than "$Q_{gd} + Q_{gs}$" obtained by the "Typical C_{iss}, C_{rss}, and C_{oss} versus v_{ds}" curve. Since the required Q_g is higher, if the used C_{gd} is only read from the "C_{rss} versus v_{ds}" curve, the simulated turn-ON speed will be faster than the practical. To compensate for the difference between Q_g and "$Q_{gd} + Q_{gs}$," an equivalent gate-drain capacitance (C_{agd}) is added to the C_{gd} read from the "C_{rss} versus v_{ds}" curve in the turn-ON process. C_{agd} is calculated by (6), where Q_g is obtained from the "Typical v_{gs} versus Q_g" curve

$$C_{agd} = \left(Q_g - \int_{0V}^{V_{gon}} C_{gs} dv_{gs} - \int_{0V}^{V_{dc}} C_{gd} dv_{ds} \right) / V_{dc}. \quad (6)$$

According to the abovementioned analysis, the superfluous and insufficient dead-time will induce extra energy loss. The proposed model can be used to solve the dead-time transients, and E_{RC} and E_{TO} can be, respectively, calculated by (4) and (5) based on the transient waveforms.

V. Experimental Results

To verify the proposed model, a TCM Buck converter is established based on the DPT circuit shown in Fig. 11. Two heat sinks are mounted on the top-cooling pads of the devices for heat dissipation. The load is the dc electronic load KEITHLEY 2380-500-30. The used filter inductance is 45 uH. According to literature [4], the theoretically required I_R can be calculated by (7), where Q_{oss} is the charge of C_{oss}. Considering the loop

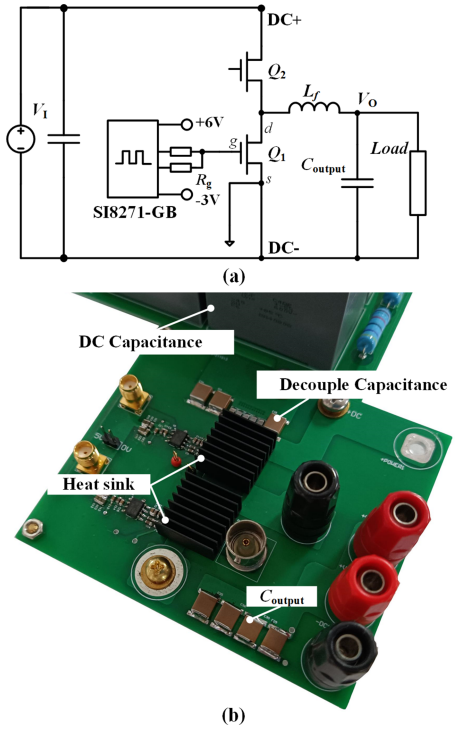

Fig. 11. (a) Schematic of the buck circuit. (b) Prototype of buck circuit.

resistance, in this article, a -0.5 A margin is added into I_R when the turn-ON signal of Q_1 is calculated

$$I_R = \begin{cases} -\sqrt{\frac{2Q_{oss}}{L}(V_I - 2V_O)}, & \text{if } V_I > 2V_O \\ 0, & \text{else.} \end{cases} \quad (7)$$

First, the proposed model is used to calculate a reference dead-time ($DT_{ref} = t_{4a}/t_{4b} - t_1 + t_6 - t_5 + T_{tr2} - T_{tr1}$). Fig. 12 shows the operation waveforms at 400 V V_I / 200 V V_O / 500 W load when DT_{ref} is used. As seen from Fig. 12(b) and (c), the zero-voltage turn ON can be realized without obvious redundant dead-time at both I_P and I_R, which verifies that DT_{ref} is very close to the optimal dead-time. Thanks to the full zero-voltage turn ON, the system efficiency under DT_{ref} is 98.5% where the switching frequency (f_{sw}) is 305 kHz.

Taking DT_{ref} as a reference, the dead-time losses tested by the experiment and calculated by the proposed model under different dead-time are listed in Fig. 13. The experimental results are shown as the red curve (P_{EX}). As the dead-time increases, P_{EX} decreases first and then increases. As the experiment results show, the extra loss caused by the unoptimized dead-time could account for 44.5% of the total loss, which is considerable in loss evaluations and thermal designs.

The extra turn-ON loss (caused by insufficient or superfluous dead-time) and the extra reverse conduction loss (caused by redundant dead-time) calculated by the proposed model are shown as P_{TO} and P_{RC} in Fig. 13. Under 150 ns, the dead-time is insufficient when Q_1 is turned OFF at I_R, so Q_2 cannot be turned ON at zero voltage, which causes P_{TO}. For Q_2, which is turned OFF at I_P, 150 ns dead-time is superfluous, so there is

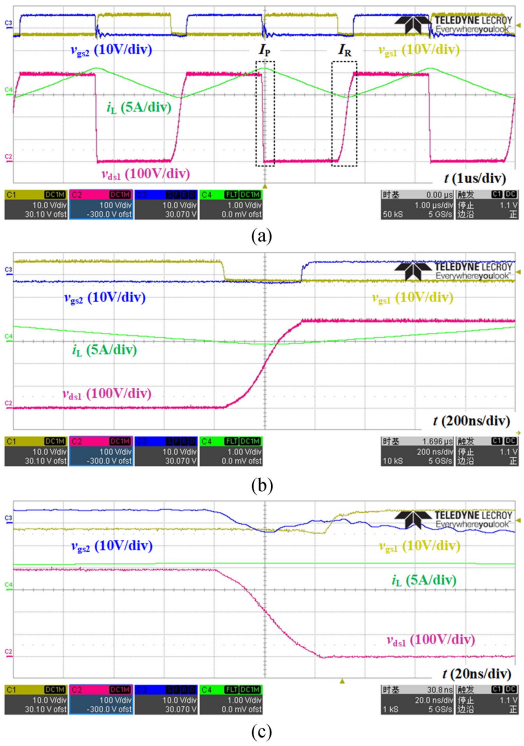

Fig. 12. Operation waveforms at 400 V V_I / 200 V V_O / 500 W load under DT_{ref}: (a) Whole. (b) At I_R. (c) At I_P.

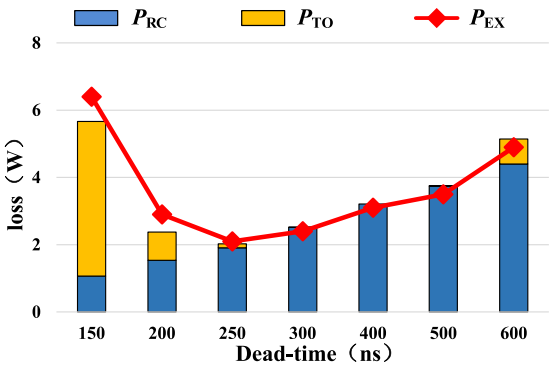

Fig. 13. Extra loss induced by the dead-time at 400 V V_I / 200 V V_O / 500 W load under the different dead-time.

still P_{RC}. As the dead-time increases, P_{RC} increases because the redundant dead-time at I_P increases. However, the total loss decreases because the longer dead-time can reduce P_{TO} significantly by decreasing the turn-ON voltage of Q_2. After the dead-time increases above 300 ns, P_{TO} disappears completely, which means the dead-time is enough for I_R. When the dead time is between 150 ns and 300 ns, as the dead-time increases, P_{TO} decreases, while P_{RC} increases. Hence, a dead-time that corresponds to the minimum total loss (DT_O) can be found in this area. As the dead-time increases further, P_{TO} arises again under 600 ns dead-time because i_L rises above 0 A during the dead-time at I_R. Further increasing the dead-time will increase

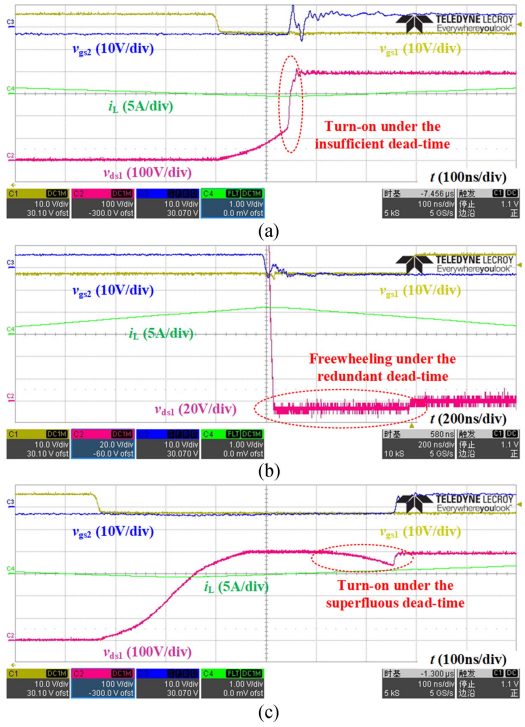

Fig. 14. Operation waveforms at 400 V V_I / 200 V V_O / 500 W load. (a) At I_R under 150 ns. (b) At I_P under 600 ns. (c) At I_R under 600 ns.

the turn-ON voltage of Q_2 as well as the redundant dead-time at I_P, so both P_{TO} and P_{RC} increase further.

As verified by the experiment, the proposed model can predict the dead-time loss well. Using the proposed model, P_{TO} and P_{RC} can be calculated, respectively, which can guide designers to select the dead-time (Take an example: If the proportion of P_{TO} is high while P_{RC} is low, the designer can increase the dead-time to obtain a lower comprehensive loss.). Moreover, using the proposed model, DT_O can be found. As analyzed previously, the selection of DT_O is the tradeoff between P_{TO} and P_{RC} rather than simply eliminating one or the other. Although the contribution of DT_O is limited for a Buck circuit, it is significant for ac applications such as an inverter where I_{OFF} and V_O vary periodically.

Fig. 14 shows the switching waveforms under 150 ns and 600 ns dead-time. Fig. 14(a) shows the waveforms at I_R under 150 ns dead-time. Before v_{ds1} increases to V_{dc}, Q_2 has been turned ON, which has accelerated the rising of v_{ds1} and generated considerable P_{TO}. Fig. 14(b) shows the waveforms at I_P under 600 ns dead-time, because of the high SCRC voltage of Q_2, v_{ds1} is obviously lower than 0 V during the redundant dead-time. Fig. 14(c) shows the waveforms at I_R under 600 ns dead-time. After i_L rises above 0 A, v_{ds1} falls again. When Q_2 is turned ON, v_{ds1} rises to V_{dc} again.

To verify the proposed model further, Fig. 15 compares the experimented and simulated waveforms of v_{ds1} at I_R under 150 ns and 600 ns dead-time. As a comparison, the waveform simulated by a contrast model, which includes the ramp V_g but does not include dynamic V_{th} and C_{agd} is also shown in Fig. 15.

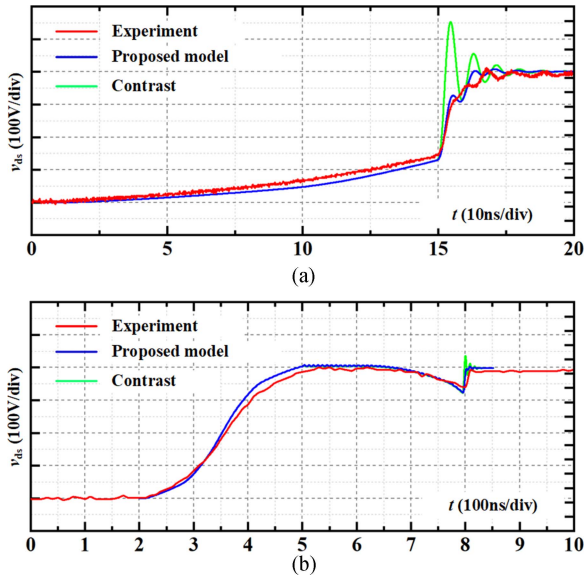

Fig. 15. Waveforms of vds1 at IR. (a) Under 150 ns dead-time. (b) Under 600 ns dead-time.

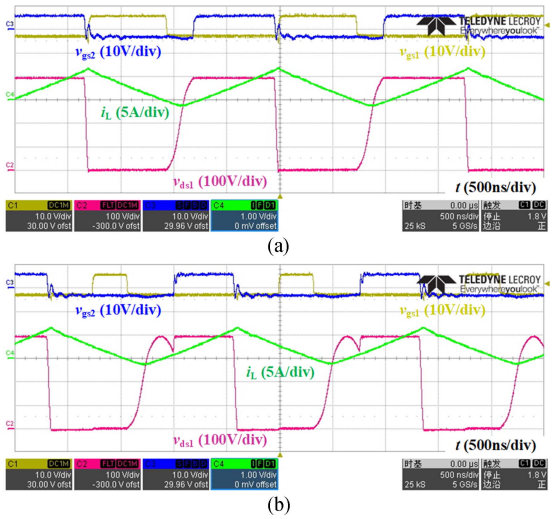

Fig. 16. Operation waveforms at 400 V VI / 200 V VO / 500 W under 21.5 uH Lf. (a) Under DTref. (b) Under 450 ns.

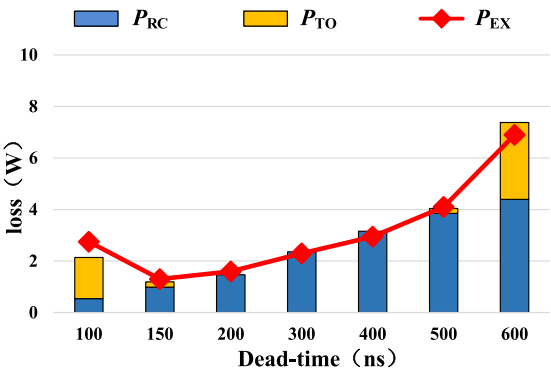

Fig. 17. Extra loss induced by the dead-time at 400 V V_I / 150 V V_O / 500 W load under the different dead-time.

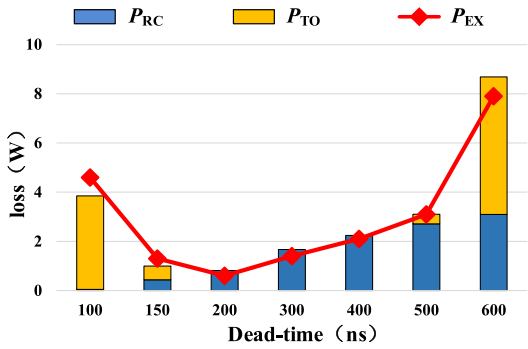

Fig. 18. Extra loss induced by the dead-time at 400 V VI / 150 V VO / 100 W load under the different dead-time.

Compared with the experiment, the turn-ON process obtained by the contrast model is obviously faster with a higher overshoot on v_{ds1}, which is consistent with the previous analyses. By contrast, the proposed model can fit the experiment better.

P_{TO} caused by the superfluous dead-time gets more serious as L_f decreases. Fig. 16 shows the waveforms under 21.5 uH L_f. Since i_L rises more rapidly after Q_1 is turned OFF at I_R, the turn-ON voltage under 450 ns dead-time is higher than 600 ns under 45 uH L_f. Therefore, using long dead-time for small I_{OFF} without optimization is not suitable for applications with small filter inductance.

Fig. 17 shows the extra losses at 400 V V_I / 150 V V_O / 500 W load. According to (7), a huger reverse current is needed as V_O decreases to 150 V. The huger reverse current increases the v_{ds1} rising speed, so the needed dead-time for I_R decreases. Therefore, the point where P_{TO} disappears moves left to 200 ns. Since higher voltage ($V_I - V_O$) is applied on L_f at 150 V V_O, even though I_R is larger, i_L rises to 0 A faster during the redundant dead-time compared with 200 V V_O. Hence, higher P_{TO} is generated under 600 ns dead-time at 150 V V_O than at 200 V V_O. Fig. 18 shows the extra losses at 400 V V_I / 150 V V_O / 100 W load. Under a lighter load, I_P decreases as the output current decreases, so the freewheeling current decreases. Since the turn-OFF time ($t_{4a}/t_{4b} - t_1$) of the device increases as I_{OFF} decreases, the redundant dead-time decreases. Therefore, according to (4), E_{RC} decreases. Since I_R is dependent on V_I / V_O as (7), E_{TO} is unchanged. Since $P_{RC} = f_{sw} * E_{RC}$ and $P_{TO} = f_{sw} * E_{TO}$, by contrast, P_{TO} makes a larger influence at 100 W load than 500 W. As a result, DT_O at 100 W load move right to 200 ns.

As shown in Figs. 13, 17, and 18, the effect of the dead-time will change as the operation condition changes. The 150 ns dead-time is the DT_O for 150 V V_O, but causes the highest extra loss at 200 V V_O. The extra loss caused by the dead-time at 150 V V_O / 100 W load under 600 ns exceeds the whole loss at 200 V V_O / 500 W load under DT_{ref}. Therefore, a comprehensive loss evaluation should consider both the operation range and the dead-time. For applications with a wide operation range, the advantages of the high calculation speed and the capacity of batch processing of the proposed model are highlighted.

$$\left[\frac{\mathrm{d}v_{\mathrm{gs1}}}{\mathrm{d}t},\frac{\mathrm{d}i_{\mathrm{g1}}}{\mathrm{d}t},\frac{\mathrm{d}v_{\mathrm{ds1}}}{\mathrm{d}t},\frac{\mathrm{d}i_{\mathrm{d1}}}{\mathrm{d}t},\frac{\mathrm{d}v_{\mathrm{co2}}}{\mathrm{d}t},\frac{\mathrm{d}i_{\mathrm{L}}}{\mathrm{d}t}\right]^{\mathrm{T}}=A_1\left[v_{\mathrm{gs1}},i_{\mathrm{g1}},v_{\mathrm{ds1}},i_{\mathrm{d1}},v_{\mathrm{co2}},i_{\mathrm{L}}\right]^{\mathrm{T}}+B_1$$

$$A_1=\begin{bmatrix} 0,\ \frac{C_{\mathrm{ds1}}+C_{\mathrm{gd1}}}{C_{\mathrm{T}}^2},\ \frac{-C_{\mathrm{gd1}}}{C_{\mathrm{T}}^2R_{\mathrm{on}}},\ \frac{C_{\mathrm{gd1}}}{C_{\mathrm{T}}^2},0,0 \\ -\frac{1}{L_{\mathrm{g1}}+L_{\mathrm{ss1}}},-\frac{R_{\mathrm{g1}}}{L_{\mathrm{g1}}+L_{\mathrm{ss1}}},\ \frac{L_{\mathrm{ss1}}(L_{\mathrm{f}}+L_{\mathrm{p2}})}{((L_{\mathrm{g1}}+L_{\mathrm{ss1}})L_{\mathrm{T}}^2)},\ \frac{L_{\mathrm{ss1}}(L_{\mathrm{f}}R_{\mathrm{p1}}+L_{\mathrm{f}}R_{\mathrm{p2}}+L_{\mathrm{p2}}R_{\mathrm{p1}})}{((L_{\mathrm{g1}}+L_{\mathrm{ss1}})L_{\mathrm{T}}^2)},\ \frac{L_{\mathrm{ss1}}L_{\mathrm{f}}}{((L_{\mathrm{g1}}+L_{\mathrm{ss1}})L_{\mathrm{T}}^2)},\ \frac{L_{\mathrm{ss1}}(L_{\mathrm{p2}}R_{\mathrm{L}}-L_{\mathrm{f}}R_{\mathrm{p2}})}{((L_{\mathrm{g1}}+L_{\mathrm{ss1}})L_{\mathrm{T}}^2)} \\ 0,\ \frac{C_{\mathrm{gd1}}}{C_{\mathrm{T}}^2},\ \frac{-(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})}{C_{\mathrm{T}}^2R_{\mathrm{on}}},\ \frac{(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})}{C_{\mathrm{T}}^2},0,0 \\ 0,0,\ -\frac{L_{\mathrm{f}}+L_{\mathrm{p2}}}{L_{\mathrm{T}}^2},\ -\frac{L_{\mathrm{f}}R_{\mathrm{p1}}+L_{\mathrm{f}}R_{\mathrm{p2}}+L_{\mathrm{p2}}R_{\mathrm{p1}}}{L_{\mathrm{T}}^2},-\frac{L_{\mathrm{f}}}{L_{\mathrm{T}}^2},\ \frac{L_{\mathrm{f}}R_{\mathrm{p2}}-L_{\mathrm{p2}}R_{\mathrm{L}}}{L_{\mathrm{T}}^2} \\ 0,0,0,\frac{1}{C_{\mathrm{oss2}}},0,-\frac{1}{C_{\mathrm{oss2}}} \\ 0,0,\ -\frac{L_{\mathrm{p2}}}{L_{\mathrm{T}}^2},\ \frac{L_{\mathrm{p1}}R_{\mathrm{p2}}-L_{\mathrm{p2}}R_{\mathrm{p1}}}{L_{\mathrm{T}}^2},\ \frac{L_{\mathrm{p1}}}{L_{\mathrm{T}}^2},\ -\frac{L_{\mathrm{p1}}R_{\mathrm{L}}+L_{\mathrm{p2}}R_{\mathrm{L}}+L_{\mathrm{p1}}R_{\mathrm{p2}}}{L_{\mathrm{T}}^2} \end{bmatrix} \tag{T1}$$

$$B_2=\left[0,\frac{-(L_{\mathrm{f}}L_{\mathrm{ss1}}+L_{\mathrm{ss1}}L_{\mathrm{p2}})V_{\mathrm{dc}}+L_{\mathrm{T}}^2V_{\mathrm{goff}}+L_{\mathrm{ss1}}L_{\mathrm{p2}}V_{\mathrm{N}}}{L_{\mathrm{T}}^2(L_{\mathrm{g1}}+L_{\mathrm{ss1}})},0\ ,\frac{(L_{\mathrm{f}}+L_{\mathrm{p2}})V_{\mathrm{dc}}-L_{\mathrm{p2}}V_{\mathrm{N}}}{L_{\mathrm{T}}^2},\ 0,\ \frac{L_{\mathrm{p2}}V_{\mathrm{dc}}-(L_{\mathrm{p1}}+L_{\mathrm{p2}})V_{\mathrm{N}}}{L_{\mathrm{T}}^2}\right]^{\mathrm{T}};$$

$$\left[\frac{dv_{\mathrm{gs1}}}{dt},\frac{di_{\mathrm{g1}}}{dt},\frac{dv_{\mathrm{ds1}}}{dt},\frac{di_{\mathrm{d1}}}{dt},\frac{dv_{\mathrm{co2}}}{dt},\frac{di_{\mathrm{L}}}{dt}\right]^{\mathrm{T}}=A_2\left[v_{\mathrm{gs1}},i_{\mathrm{g1}},v_{\mathrm{ds1}},i_{\mathrm{d1}},v_{\mathrm{co2}},i_{\mathrm{L}}\right]^{\mathrm{T}}+B_2$$

$$A_2=\begin{bmatrix} -\frac{C_{\mathrm{gd1}}g_{\mathrm{m}}}{C_{\mathrm{T}}^2},\ \frac{C_{\mathrm{ds1}}+C_{\mathrm{gd1}}}{C_{\mathrm{T}}^2},0,\ \frac{C_{\mathrm{gd1}}}{C_{\mathrm{T}}^2},0,0 \\ -\frac{1}{L_{\mathrm{g1}}+L_{\mathrm{ss1}}},-\frac{R_{\mathrm{g1}}}{L_{\mathrm{g1}}+L_{\mathrm{ss1}}},\ \frac{L_{\mathrm{ss1}}(L_{\mathrm{f}}+L_{\mathrm{p2}})}{((L_{\mathrm{g1}}+L_{\mathrm{ss1}})L_{\mathrm{T}}^2)},\ \frac{L_{\mathrm{ss1}}(L_{\mathrm{f}}R_{\mathrm{p1}}+L_{\mathrm{f}}R_{\mathrm{p2}}+L_{\mathrm{p2}}R_{\mathrm{p1}})}{((L_{\mathrm{g1}}+L_{\mathrm{ss1}})L_{\mathrm{T}}^2)},\ \frac{L_{\mathrm{ss1}}L_{\mathrm{f}}}{((L_{\mathrm{g1}}+L_{\mathrm{ss1}})L_{\mathrm{T}}^2)},\ \frac{L_{\mathrm{ss1}}(L_{\mathrm{p2}}R_{\mathrm{L}}-L_{\mathrm{f}}R_{\mathrm{p2}})}{((L_{\mathrm{g1}}+L_{\mathrm{ss1}})L_{\mathrm{T}}^2)} \\ -\frac{g_{\mathrm{m}}(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})}{C_{\mathrm{T}}^2},\ \frac{C_{\mathrm{gd1}}}{C_{\mathrm{T}}^2},0,\ \frac{(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})}{C_{\mathrm{T}}^2},0,0 \\ 0,0,\ -\frac{L_{\mathrm{f}}+L_{\mathrm{p2}}}{L_{\mathrm{T}}^2},\ -\frac{L_{\mathrm{f}}R_{\mathrm{p1}}+L_{\mathrm{f}}R_{\mathrm{p2}}+L_{\mathrm{p2}}R_{\mathrm{p1}}}{L_{\mathrm{T}}^2},-\frac{L_{\mathrm{f}}}{L_{\mathrm{T}}^2},\ \frac{L_{\mathrm{f}}R_{\mathrm{p2}}-L_{\mathrm{p2}}R_{\mathrm{L}}}{L_{\mathrm{T}}^2} \\ 0,0,0,\frac{1}{C_{\mathrm{oss2}}},0,-\frac{1}{C_{\mathrm{oss2}}} \\ 0,0,\ -\frac{L_{\mathrm{p2}}}{L_{\mathrm{T}}^2},\ \frac{L_{\mathrm{p1}}R_{\mathrm{p2}}-L_{\mathrm{p2}}R_{\mathrm{p1}}}{L_{\mathrm{T}}^2},\ \frac{L_{\mathrm{p1}}}{L_{\mathrm{T}}^2},\ -\frac{L_{\mathrm{p1}}R_{\mathrm{L}}+L_{\mathrm{p2}}R_{\mathrm{L}}+L_{\mathrm{p1}}R_{\mathrm{p2}}}{L_{\mathrm{T}}^2} \end{bmatrix}$$

$$B_2=\left[\frac{C_{\mathrm{gd1}}V_{\mathrm{th}}g_{\mathrm{m}}}{C_{\mathrm{T}}^2},\frac{-(L_{\mathrm{f}}L_{\mathrm{ss1}}+L_{\mathrm{ss1}}L_{\mathrm{p2}})V_{\mathrm{dc}}+L_{\mathrm{T}}^2V_{\mathrm{goff}}+L_{\mathrm{ss1}}L_{\mathrm{p2}}V_{\mathrm{N}}}{L_{\mathrm{T}}^2(L_{\mathrm{g1}}+L_{\mathrm{ss1}})},\frac{(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})V_{\mathrm{th}}g_{\mathrm{m}}}{C_{\mathrm{T}}^2}\ ,\frac{(L_{\mathrm{f}}+L_{\mathrm{p2}})V_{\mathrm{dc}}-L_{\mathrm{p2}}V_{\mathrm{N}}}{L_{\mathrm{T}}^2},\ 0,\ \frac{L_{\mathrm{p2}}V_{\mathrm{dc}}-(L_{\mathrm{p1}}+L_{\mathrm{p2}})V_{\mathrm{N}}}{L_{\mathrm{T}}^2}\right]^{\mathrm{T}}$$

(T2)

$$\left[\frac{dv_{\mathrm{gs1}}}{dt},\frac{di_{\mathrm{g1}}}{dt},\frac{dv_{\mathrm{ds1}}}{dt},\frac{di_{\mathrm{d1}}}{dt},\frac{di_{\mathrm{L}}}{dt}\right]^{\mathrm{T}}=A_3\left[v_{\mathrm{gs1}},i_{\mathrm{g1}},v_{\mathrm{ds1}},i_{\mathrm{d1}},i_{\mathrm{L}}\right]^{\mathrm{T}}+B_3$$

$$A_3=\begin{bmatrix} -\frac{C_{\mathrm{gd1}}g_{\mathrm{m}}}{C_{\mathrm{T}}^2},\ \frac{C_{\mathrm{ds1}}+C_{\mathrm{gd1}}}{C_{\mathrm{T}}^2},0,\ \frac{C_{\mathrm{gd1}}}{C_{\mathrm{T}}^2},0 \\ -\frac{1}{L_{\mathrm{g1}}+L_{\mathrm{ss1}}},-\frac{R_{\mathrm{g1}}}{L_{\mathrm{g1}}+L_{\mathrm{ss1}}},\ \frac{L_{\mathrm{ss1}}(L_{\mathrm{f}}+L_{\mathrm{p2}})}{((L_{\mathrm{g1}}+L_{\mathrm{ss1}})L_{\mathrm{T}}^2)},\ \frac{L_{\mathrm{ss1}}(L_{\mathrm{f}}R_{\mathrm{p1}}+L_{\mathrm{f}}R_{\mathrm{p2}}+L_{\mathrm{p2}}R_{\mathrm{p1}}+L_{\mathrm{f}}R_{\mathrm{on}})}{((L_{\mathrm{g1}}+L_{\mathrm{ss1}})L_{\mathrm{T}}^2)},\ -\frac{L_{\mathrm{ss1}}(L_{\mathrm{f}}R_{\mathrm{on}}-L_{\mathrm{p2}}R_{\mathrm{L}}+L_{\mathrm{f}}R_{\mathrm{p2}})}{((L_{\mathrm{g1}}+L_{\mathrm{ss1}})L_{\mathrm{T}}^2)} \\ -\frac{g_{\mathrm{m}}(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})}{C_{\mathrm{T}}^2},\ \frac{C_{\mathrm{gd1}}}{C_{\mathrm{T}}^2},0,\ \frac{(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})}{C_{\mathrm{T}}^2},0 \\ 0,0,\ -\frac{L_{\mathrm{f}}+L_{\mathrm{p2}}}{L_{\mathrm{T}}^2},\ -\frac{L_{\mathrm{f}}R_{\mathrm{p1}}+L_{\mathrm{f}}R_{\mathrm{p2}}+L_{\mathrm{p2}}R_{\mathrm{p1}}+L_{\mathrm{f}}R_{\mathrm{on}}}{L_{\mathrm{T}}^2},\ \frac{L_{\mathrm{f}}R_{\mathrm{p2}}-L_{\mathrm{p2}}R_{\mathrm{L}}+L_{\mathrm{f}}R_{\mathrm{on}}}{L_{\mathrm{T}}^2} \\ 0,0,\ -\frac{L_{\mathrm{p2}}}{L_{\mathrm{T}}^2},\ \frac{L_{\mathrm{p1}}R_{\mathrm{p2}}-L_{\mathrm{p2}}R_{\mathrm{p1}}+L_{\mathrm{p1}}R_{\mathrm{on}}}{L_{\mathrm{T}}^2},-\frac{L_{\mathrm{p1}}R_{\mathrm{L}}+L_{\mathrm{p2}}R_{\mathrm{L}}+L_{\mathrm{p1}}R_{\mathrm{p2}}+L_{\mathrm{p1}}R_{\mathrm{on}}}{L_{\mathrm{T}}^2} \end{bmatrix} \tag{T3}$$

$$B_3=\left[\frac{C_{\mathrm{gd1}}V_{\mathrm{th}}g_{\mathrm{m}}}{C_{\mathrm{T}}^2},\frac{-(L_{\mathrm{f}}L_{\mathrm{ss1}}+L_{\mathrm{ss1}}L_{\mathrm{p2}})V_{\mathrm{dc}}+L_{\mathrm{T}}^2V_{\mathrm{goff}}+L_{\mathrm{ss1}}L_{\mathrm{p2}}V_{\mathrm{N}}+L_{\mathrm{f}}L_{\mathrm{ss1}}V_{\mathrm{R}}}{L_{\mathrm{T}}^2(L_{\mathrm{g1}}+L_{\mathrm{ss1}})},\frac{(C_{\mathrm{gd1}}+C_{\mathrm{gs1}})V_{\mathrm{th}}g_{\mathrm{m}}}{C_{\mathrm{T}}^2}\ ,\right.$$
$$\left.\frac{(L_{\mathrm{f}}+L_{\mathrm{p2}})V_{\mathrm{dc}}-L_{\mathrm{p2}}V_{\mathrm{N}}-L_{\mathrm{f}}V_{\mathrm{R}}}{L_{\mathrm{T}}^2},\ \frac{L_{\mathrm{p2}}V_{\mathrm{dc}}+L_{\mathrm{p1}}V_{\mathrm{R}}-(L_{\mathrm{p1}}+L_{\mathrm{p2}})V_{\mathrm{N}}}{L_{\mathrm{T}}^2}\right]^{\mathrm{T}}.$$

VI. Conclusion

This article analyzes the dead-time transient in GaN-based TCM converters and evaluates the dead-time loss theoretically based on an improved GaN HEMT model. To comprehensively analyze the effect of the dead-time, the switching processes under the insufficient and superfluous dead-time are analyzed. By adding the voltage rising/falling time of the gate driver, the dynamic threshold voltage, and the equivalent gate-drain capacitance, the improved GaN HEMT model can more accurately simulate the gate delay time, the SCRC voltage, and the turn-ON process under the insufficient dead-time. As verified by the experiments, the proposed model shows high accuracy in the dead-time loss prediction. As the experimental and the simulated results show, the effect of the dead-time will change as the operation condition changes, so a comprehensive loss evaluation should consider both the operation range and the dead-time. Moreover, the proposed model can also be used to find a dead-time with the lowest comprehensive dead-time loss for a certain operating condition.

Appendix

In Section III, (8)–(15) is derived to describe the equivalent circuits listed in Fig. 4, where $L_{\mathrm{p1}}=L_{\mathrm{t1}}+L_{\mathrm{ss1}}$, $L_{\mathrm{p2}}=L_{\mathrm{t2}}+L_{\mathrm{ss2}}$, and $V_{\mathrm{R}}=-V_{\mathrm{th}}+V_{\mathrm{gOFF}}$

$$v_{gs1}=V_{\mathrm{goff}}-i_{\mathrm{g1}}\cdot R_{\mathrm{g1}}-L_{\mathrm{g1}}\frac{di_{\mathrm{g1}}}{dt}-L_{\mathrm{ss1}}\left(\frac{di_{\mathrm{d1}}}{dt}+\frac{di_{\mathrm{g1}}}{dt}\right) \tag{8}$$

$$i_{\mathrm{g1}}=C_{\mathrm{gs1}}\frac{dv_{\mathrm{gs1}}}{dt}+C_{\mathrm{gd1}}\left(\frac{dv_{\mathrm{gs1}}}{dt}-\frac{dv_{\mathrm{ds1}}}{dt}\right) \tag{9}$$

$$i_{\mathrm{d1}} = \frac{v_{\mathrm{ds1}}}{R_{\mathrm{on}}} + C_{\mathrm{ds1}}\frac{dv_{\mathrm{ds1}}}{dt} + C_{\mathrm{gd1}}\left(\frac{dv_{\mathrm{ds1}}}{dt} - \frac{dv_{\mathrm{gs1}}}{dt}\right) \tag{10}$$

$$V_{\mathrm{dc}} - V_{\mathrm{N}} = v_{\mathrm{ds1}} + L_{\mathrm{p1}}\frac{di_{\mathrm{d1}}}{dt} + i_{\mathrm{L}}\cdot R_{\mathrm{L}} + L_{\mathrm{f}}\frac{di_{\mathrm{L}}}{dt} + i_{\mathrm{d1}}R_{\mathrm{p1}} \tag{11}$$

$$V_{\mathrm{dc}} = v_{\mathrm{ds1}} + v_{\mathrm{co2}} + (L_{\mathrm{p1}} + L_{\mathrm{p2}})\frac{di_{\mathrm{d1}}}{dt} - L_{\mathrm{p2}}\frac{di_{\mathrm{L}}}{dt} + R_{\mathrm{p1}}\cdot i_{\mathrm{d1}} + R_{\mathrm{p2}}\left(i_{\mathrm{d1}} - i_{\mathrm{L}}\right) \tag{12}$$

$$C_{\mathrm{oss2}}\frac{dv_{\mathrm{co2}}}{dt} = i_{\mathrm{d1}} - i_{\mathrm{L}} \tag{13}$$

$$i_{\mathrm{d1}} = g_{\mathrm{m}}(v_{\mathrm{gs1}} - V_{\mathrm{th}}) + C_{\mathrm{ds1}}\frac{dv_{\mathrm{ds1}}}{dt} + C_{\mathrm{gd1}}\left(\frac{dv_{\mathrm{ds1}}}{dt} - \frac{dv_{\mathrm{gs1}}}{dt}\right) \tag{14}$$

$$V_{\mathrm{dc}} = v_{\mathrm{ds1}} + V_{\mathrm{R}} + (L_{\mathrm{p1}} + L_{\mathrm{p2}})\frac{di_{\mathrm{d1}}}{dt} - L_{\mathrm{p2}}\frac{di_{\mathrm{L}}}{dt} + R_{\mathrm{p1}}\cdot i_{\mathrm{d1}} + (R_{\mathrm{on}} + R_{\mathrm{p2}})\left(i_{\mathrm{d1}} - i_{\mathrm{L}}\right). \tag{15}$$

According to (8)–(15), the GaN HEMT model is written into the form of the state (T1)–(T3) shown at the top of the previous page, where: $L_{\mathrm{T}}^2 = L_{\mathrm{p1}}L_{\mathrm{p2}} + L_{\mathrm{p1}}L_{\mathrm{f}} + L_{\mathrm{p2}}L_{\mathrm{f}}$, $C_{\mathrm{T}}^2 = C_{\mathrm{gd1}}C_{\mathrm{gs1}} + C_{\mathrm{gd1}}C_{\mathrm{ds1}} + C_{\mathrm{ds1}}C_{\mathrm{gs1}}$.

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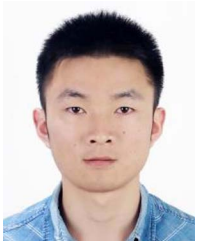

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