An Online DC-Link Capacitance Estimation Method for Motor Drive Systems Based on an Intermittent Reverse-Charging Control Strategy

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***Abstract*—The dc-link capacitor in the three-phase ac–dc–ac motor drive system is a critical component. The degradation of dc-link electrolytic capacitors is a common failure that has a significant impact on system reliability, which can often lead to system breakdown or damage. It is significant to provide monitoring and prognostic techniques for dc-link capacitors to assist in preventive maintenance. To realize online estimation of the dc-link capacitance, a reverse-charging mode of dc-link capacitors is actively introduced during the normal operation, by actively altering the control of the power switches in the converter in an intermittent manner. During the proposed reverse-charging mode, the dc-link capacitor bank is charged by the motor, and the charging current exactly originates from the current in one particular phase, which can be designated and measurable in typical motor drive systems. Based on the reverse-charging mode, the capacitance can be calculated through the voltage rise and charging current. Simulation and experimental tests are implemented to verify the accuracy and feasibility of the proposed method. It is shown that this method is capable of providing online monitoring of dc-link capacitors with high accuracy.**

***Index Terms*—DC-link capacitance, intermittent, motor drive, online monitoring, reverse charging.**

I. Introduction

RELIABILITY of the power electronic converters is one of the most significant challenges in industrial ac motor drives. Converters typically consist of power semiconductor devices and energy storage elements. Capacitors are commonly used as energy storage elements for buffering instantaneous voltage spikes and eliminating harmonics. Three types of capacitors are generally used in power electronic applications, which are electrolytic capacitors (E-Caps), metallized polypropylene film capacitors, and multilayer ceramic capacitors. Aluminum E-Caps are the most popular ones in power electronic circuits, considering their high volumetric efficiency and price/performance ratio [1]. However, in terms of reliability, aluminum E-Caps, when used as dc-link capacitors in the motor drive system, are prone to failure. When failure occurs in capacitors, considering that the function of dc-link capacitors is providing the reactive power compensation and reducing the ripple of the dc-link voltage, the reliability of the converter system is largely affected. In addition, the mitigation of instantaneous impulse voltage is compromised simultaneously, which threatens the power of electronic devices. Therefore, the physical condition of the dc-link capacitors strongly affects the safety and reliability of the motor drive system.

In reality, due to the harsh conditions including the high thermal stress, high switching frequency, and electrical stress in the actual operation process, the dc-link capacitor bank will gradually lose its initial characteristic, through a gradual degradation [2]. The degradation of the dc-link capacitor bank can be due to multiple aging mechanisms as mentioned in the following. In terms of the physical properties of the capacitor, the electrolyte evaporation and oxide-layer deterioration for E-Caps lead to an increase in the equivalent series resistance (ESR) and a decrease in the capacitance values. Overall, aging of dc-link capacitors typically leads to a reduction of capacitance values. Therefore, it is significant to provide monitoring and prognostic techniques for the dc-link capacitor to assist in preventive maintenance.

Recently, online condition monitoring of the dc-link capacitor has attracted strong attention. The ESR and the actual equivalent capacitance C are the most popularly-used aging indicators for monitoring. Generally, capacitors can be considered to be malfunctioning when the ESR increases to twice its original value or the capacitance reduces to 80% of the initial value. Existing monitoring methods are well summarized in [3], [4], and [5]. The previous proposed diagnostics methods used for capacitor deterioration can also be categorized into offline methods, quasi-online methods, and real-online methods.

The offline methods usually directly measure the capacitance and/or the ESR of the dc-link capacitors, which are easy and inexpensive but require system disassembly [6] or modification of the circuit [7]. In addition, signal injection [8] or extra devices [9] are required to extract the ESR or capacitance in the offline state. Overall, the monitoring accuracy of the offline methods is high, but the dc-link capacitors cannot be kept in normal condition for testing. Their application is therefore limited due to these limitations.

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The quasi-online methods can be conducted in specific operation conditions, such as the start-up stages or during the switch-OFF state. Compared with the offline methods, these methods can be implemented conveniently on the system without disassembly. A strategy utilizing the switching conditions is proposed for three-phase ac–dc–ac converters in [10]. Special switching patterns are proposed to acquire the transfer function, as the motor is stopped. In [11], a condition monitoring method for submodule capacitors in modular multilevel converters is proposed. This capacitance is calculated based on the discharging time. In [12], the actively switching state adjustment is implemented when the machine is stopped. During this process, an *LC* resonance is intentionally introduced and the capacitance *C* can be calculated by the resonant current in response. However, the duration of the damped oscillation is dependent on the system parameters, which are variables. Therefore, the sampling accuracy cannot be guaranteed and the estimation precision is affected.

The real-online methods can be implemented during normal operating conditions. A diagnostic method of the ESR is proposed in [13]. An additional designed integrated circuit is required for the measurement of rms. In [14], the capacitance is calculated online through the power stored in the capacitor, by injecting an ac voltage component into the dc link. In [15], a dc sensor is used to obtain the capacitor ripple current. Through the average capacitor power calculated by multiplying the current and voltage, the ESR is estimated. In [16], the control strategy is modified by active controlling of switches, and the short-circuit current and the step voltage in response are used to estimate the ESR. This method can realize the online estimation of capacitor parameters, but the assumption of constant dc-link voltage and phase currents are not reasonable, which causes the estimation precision unsatisfying. In [17], ESR monitoring techniques are used for evaluating the degradation of dc-link capacitors. The capacitance is diagnosed based on lower-frequency current injection and compensated by temperature detection of capacitors. Nevertheless, a controllable grid-side converter is required for the current injection, and the temperature measurement required in this scheme is invasive in nature and may not be feasible in practical application. Overall, in these methods, the accuracy is typically limited for sensorless condition monitoring or extra devices are required to improve accuracy. A capacitance estimation method is proposed based on the artificial neural network (ANN) algorithm in [18]. In [19], the low-frequency impedance is estimated to monitor the health condition. Methods based on the frequency analysis are proposed in [20] and [21]. Two ANNs are used to train the time domain-based and frequency domain-based parameters, respectively. However, the computation burden is heavy for the control system. In [21], a method for condition monitoring of dc-link capacitors based on the ESR is proposed, which can also detect the core temperature through the dc-link capacitance. However, an additional dc-link current sensor is required and the temperature is needed for core temperature calibrating. In [26], the instantaneous dc-link capacitor power is utilized to estimate the capacitance with ignorance of inverter losses. In addition, the power information in the transient condition is difficult to obtain. Lifetime prediction of capacitors is proposed in [28], and the process of nonlinear damage accumulation and capacitance reduction ratio can be obtained. In [29], the dissipation factor is used as an indicator to monitor the condition of the capacitor, which is only suitable for aluminum E-Caps. This method is based on the coupling of dissipation and degradation. With the reconstruction of dc-link current, it is complicated to ensure accuracy. In [30], the braking branch is used to generate the *LCR* response for capacitance estimation. However, the application is limited by the structure and the value of the braking resistor cannot be accurately obtained.

In summary, reliable online condition monitoring of capacitors requires multiple characteristics, including estimation accuracy, the feasibility of normal operating conditions, and simplicity of implementation, which cannot be comprehensively solved in these existing methods.

In this article, a novel quasi-online estimation method for dc-link capacitor monitoring is proposed, which can provide an accurate estimation of the capacitance. The proposed method is based on a novel monitoring mode by altering the control of switching devices in the converter, which is actively inserted into the normal operation intermittently. This new gate drives control mode, namely, the "*reverse-charging mode,*" is proposed in this article. In fact, this monitoring strategy is derived from a "forward-charging mode," which is proposed in [31]. "Forward-charging" means that the discharging of capacitors is actively controlled. However, the discharging leads to the decrease of dc-link voltage, which can trigger the diodes on the rectifier side. Then, the grid side charges the capacitors, which can confuse the identification of voltage increment. Furthermore, for dc voltage supply modes, such as electric vehicles, the forward-charging is absolutely unavailable. To solve this problem, the "reverse-charging mode" is proposed. During the proposed monitoring mode, the stage at which the capacitor bank discharges to supply load while disconnected from the grid is used to extract the capacitance value. The reverse charging generates the rise of dc-link voltage, which can avoid the impact caused by the charging of the grid side.

A permanent magnet synchronous motor (PMSM) is taken as the driven motor in this article as an example, and relevant analysis and research are based on its characteristics. It is worth mentioning that the impact intensity of reverse charging for the application of high-power machines and low-power machines is different. High-power machines are more tolerable and robust.

The article is organized as follows. Section II presents the principle of the proposed online capacitance monitoring method for dc-link capacitors. Section III outlines the feasible regions for operating the proposed method. Section IV describes the duration selection and potential influence of the implementation. In Section V, simulation is presented for preliminary verification and interval design of reverse-charging mode injection. The experimental validation of the proposed scheme is demonstrated in Section VI. In Section VII, the limitation and practical application are discussed. In Section VIII, some conclusions are drawn to summarize this article.

II. Principle of DC-Link Capacitance Estimation

The main concept of the proposed method is to realize the significant increase of the dc-link voltage by intentional

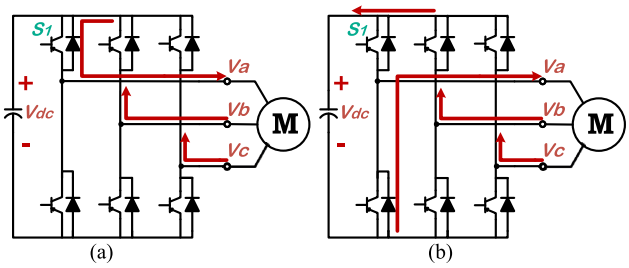

Fig. 1. Reverse-charging process of dc-link capacitor.

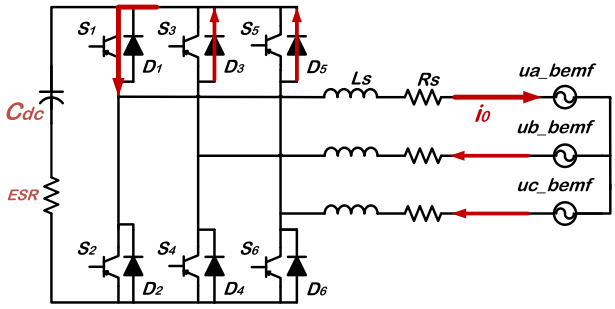

Fig. 2. Conductive path during the ON-state.

reverse-charging mode and convert the unmeasurable dc-link current to the measurable phase current. The normal switching of the power electronics devices is determined by the ideal circuit trajectory tracking of flux linkage. In the proposed method, a short-time active control mode is inserted in the normal control strategy, which is named reverse-charging mode. The purpose of the specific mode is to provide a reverse-charging condition of the dc-link capacitors for monitoring purposes.

A. Reverse Charging Mode

As shown in Fig. 1, when the switch S_1 is turned ON and other switches are OFF, it creates an opportunity for the formation of conduction loops between the phase windings. During the operation of motor drive systems, the terminal voltages of three-phase windings are sinusoidal with a phase difference of 120° due to the rotation. Therefore, due to the voltage potential difference and winding impedance, currents will generate as shown in Fig. 1(a). When the generated currents are sufficient, the controlled switch S_1 is turned OFF to form a complete disconnection among three-phase windings. In this condition, the free-wheeling of residual currents should be accomplished through the antiparallel diodes, as shown in Fig. 1(b). Therefore, the residual currents reversely flow into the dc bus and the dc-link capacitors are charged. In this case, the dc-link capacitance can be estimated based on the measurable charging current and increment of dc-link voltage. Because the charging current is zero at the beginning and the end of the charging process, the voltage variation of the ESR is from zero to zero. Therefore, the impact of the ESR can be ignored from the perspective of the entire process.

The specific implementation steps and corresponding response process are shown as follows.

B. Analysis of the Reverse-Charging Implementation

Assuming that the upper insulated-gate bipolar transistor (IGBT) of Phase A is the controlled switch, the specific reverse-charging mode and response process are demonstrated as follows.

First, the six switching devices are all switched OFF to consume the residual currents, and the residual currents flow into the dc bus through the antiparallel diodes. This process is exactly consistent with the proposed reverse-charging process, but the rise of dc-link voltage is inconspicuous and limited. Therefore, sufficient currents and charging duration are required for a significant voltage increase. In this method, this is achieved in two stages: *the current generation and reverse charging.*

Stage 1: Current generation (When the IGBT S_1 is turned ON)

After the residual currents are completely consumed, due to that all the lower IGBTs of three phases are switched OFF, the dc-link capacitor bank cannot form a closed loop with the phase windings. However, the rotor is still rotating, so the three-phase back EMFs are still induced. When at least one of the back EMFs in Phase B and Phase C is higher than Phase A, one or two loops between phase windings can be generated through the upper antiparallel diodes and IGBT S_1. As shown in Fig. 2, the diodes D_3 and D_5 will be utilized by Phase B and Phase C, respectively. Then, RL zero-state responses are excited. Taking the direction that flows into Phase A as the positive direction, the response current of one loop is shown as follows:

$$i_0 = \frac{U_0}{R_0}\left(1 - e^{-\frac{R_0}{L_0}t}\right) \tag{1}$$

where U_0 represents the potential difference between phases, R_0 is double winding resistance and L_0 is double winding inductance. Generally, considering the value of the resistance and the inductance, $\frac{U_0}{R_0}$ and $\frac{R_0}{L_0}$ are in thousand level. Therefore, the response current will rise rapidly.

Stage 2: Reverse charging (When the IGBT S_1 is switched OFF)

When the response current of Phase A rises to a significant value, the IGBT S_1 is switched OFF. The closed loops are cutoff and the residual currents freewheel through the antiparallel diodes. The current of Phase A is maintained through diode D_2, and the currents of Phase B and Phase C are maintained through diodes D_3 and D_5. As shown in Fig. 3, a current conductive path that connects the dc-link capacitor bank and stator windings is established. Then, the residual currents are forced into the dc bus, which forms the reverse-charging process of the dc-link capacitors. Actually, the process can be considered as a RL nonzero state response. Keeping the reference direction consistent with the previously mentioned, the response current can be expressed as

$$i_1 = \left(I_0 + \frac{U_1}{R_1}\right) e^{-\frac{R_1}{L_1}t} - \frac{U_1}{R_1} \tag{2}$$

where I_0 is the initial current, U_1 represents the potential difference between the dc bus and phases, and R_1 and L_1 are the resistance and inductance in the conductive path, respectively.

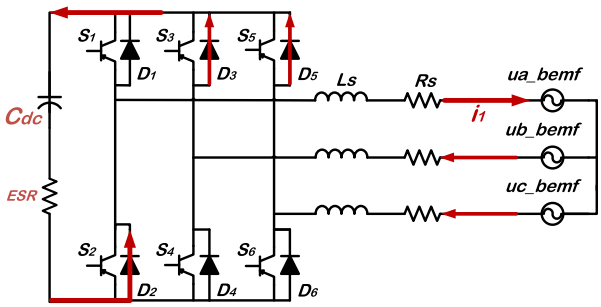

Fig. 3. Conductive path during the OFF state.

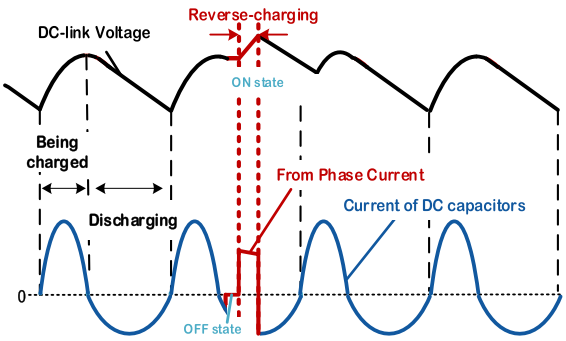

Fig. 4. Reverse-charging process of the dc-link voltage.

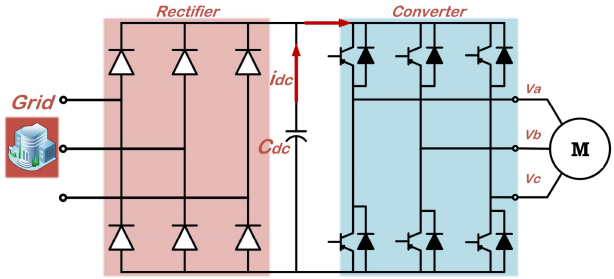

Fig. 5. Structure of the grid-connected motor drive system.

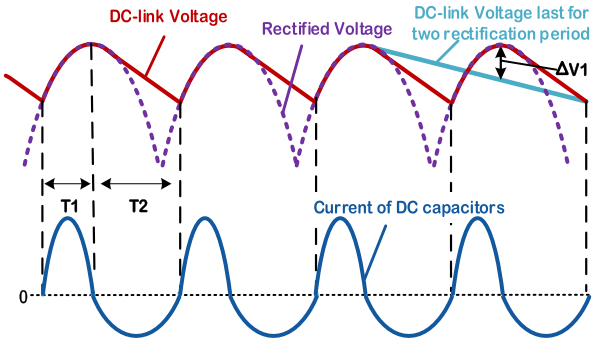

Fig. 6. Fluctuations of the dc-link voltage and current.

From the expression of the current response, it can be seen that the process is the consumption of the initial currents. Before the initial current reaches zero, the dc-link capacitor bank is continuously charged. As a result, the dc-link voltage rises.

During the reverse-charging process, the condition of dc-link voltage is shown in Fig. 4. Flowing into the dc capacitors is the positive direction of the current of dc capacitors. During the reverse-charging stage, the current of dc capacitors is positive, which is actually the current of the specific phase. In normal operation, the dc-link voltage contains two stages: charging and discharging. The reverse charging is conducted during the discharging stage.

Actually, the reverse-charging process essentially converts the mechanical energy of the motor rotation into electrical energy, which is transferred and stored in the dc-link capacitors.

Then, through the adjustable reverse-charging strategy and these corresponding transient response processes, the voltage increase of dc-link capacitors generated by reverse charging can be implemented. Meanwhile, the current of the dc-link capacitor bank is zero at the beginning and end of the reverse charging. Therefore, after an entire control special operation period, the voltage variation caused by the ESR is zero, which means that the impact of ESR can be eliminated during this operation. Therefore, the capacitance can be calculated based on the charging current and increasing voltage.

C. Calculation of DC-Link Capacitance

The reverse-charging stage is used to estimate the capacitance in the proposed method. To calculate the dc-link capacitance, the characteristic equation of the dc-link capacitance is utilized. The estimation is expressed as

$$i_{\mathrm{dc}} = C\frac{dU_{\mathrm{dc}}}{dt} \rightarrow C = \int i_{\mathrm{dc}}\, dt/\Delta U_{\mathrm{dc}} \tag{3}$$

where i_{dc} is the current of the dc-link capacitor bank, and ΔU_{dc} is the total increment of the dc-link voltage.

In this stage, the corresponding charging current is the current of Phase A, which is a quantity being measured in a typical motor control system.

After determining the basic principle of the proposed scheme, there are two essential indicators at the control level: the exact feasible region and the duration of an entire special operation period.

III. Feasible Operating Condition for Reverse Charging Mode

A. Feasible Operating Condition for the DC-Link Voltage

A typical grid-connected motor system driven by a three-phase ac–dc–ac converter is shown in Fig. 5.

The switching devices of the inverter are chosen to be IGBTs. In Fig. 6, the voltage fluctuations and the change of dc-capacitor current flowing direction are shown and a complete fluctuation period can be divided into two stages: T_1 and T_2, which is similar with the demonstration in Section II. The waveform of the grid side rectified voltage is shown in Fig. 6, which is with 6th harmonics. When the grid side rectified voltage is higher than the dc-link voltage, the grid side supplies power to the load and charges the dc-link capacitors simultaneously. This process corresponds to stage T_1. When the rectified grid voltage reaches

the peak, the rectified voltage and dc-link voltage both begin to reduce. The decrease in the waveform of rectified grid voltage is definite and the decrease of dc-link voltage is determined by the value of dc-link capacitance and load condition. Supposing that the capacitors supply power to the load, the performance can be described as follows:

$$\frac{1}{2}C\ \left(U_{\mathrm{dc0}}^2 - U_{\mathrm{dc1}}^2\right) = \int_{t_0}^{t_1} P dt \tag{4}$$

where C is the value of dc-link capacitance, t_0 and t_1 are two points in time, U_{dc0} and U_{dc1} are the dc-link voltage value at t_0 and t_1, and P is the output power of capacitors. Higher power levels of motor drive correspond to a higher value of dc-link capacitance.

In fact, the value of dc capacitance will be matched to the capacity of the motor drive system. Generally speaking, the desired function of dc-link capacitors is to reduce the fluctuation of rectified grid voltage. Therefore, the suitable value of capacitors ensures a slower reduction in the speed of dc-link voltage. Generally, the decrease of the dc-link voltage is slower than the rectified voltage. Because of the unidirectional continuity of the rectifier diode, the dc bus and the grid side will be disconnected and no energy will be transferred to the grid side. In this condition, the dc-link capacitors begin to supply the load. During this stage, the dc-link voltage will be higher than the rectified grid voltage. This process corresponds to stage T_2.

As aforementioned, the rectification devices are usually composed of power semiconductors selected according to the signal single-track pass feature, which ensures that the dc-link capacitors cannot supply power to the grid side reversely during the discharging process. Therefore, during the stage at which the dc-link voltage is higher than rectified grid voltage, the dc-link capacitors supply the load while disconnected from the grid, which indicates that there is electrical isolation between the grid side and the dc bus.

Hence, in the proposed method, to avoid the influence of the grid side voltage and parameter variations, the decrease stage T_2 of the dc-link voltage (or the discharging stage of the dc link capacitor) is chosen to implement the proposed control strategy.

The actual grid side rectified voltage contains fluctuations at a frequency that is six times as high as the fundamental component. But in reality, due to the fluctuation-smoothing function of dc-link capacitors and the conducting voltage of rectifier diodes, the decrease stage of dc-link voltage may last for several rectification periods. As shown in Fig. 6, when $\Delta V1$ is lower than the conducting voltage of rectifier diodes, the charging process will not be enabled. This feature provides convenience to the implementation of the scheme.

In addition, during each cycle of rotation, the condition of three-phase back EMFs changes regularly. The generation of reverse-charging currents can be obtained due to potential differences between phases in particular rotation regions. Therefore, the region should be selected for the current generation.

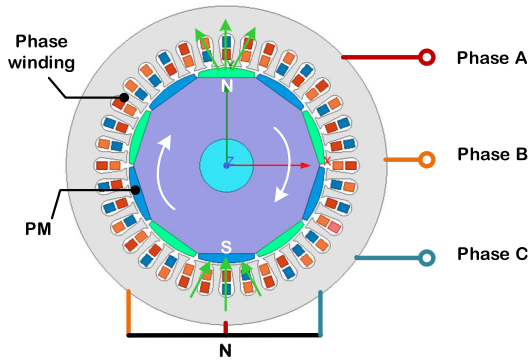

Fig. 7. Model of the PMSM.

B. Feasible Operating Condition During the Normal Period of the Motor

The feasible regions during one cycle of rotation should be selected for effective implementation of the proposed method. For the generation of charging current, it should be guaranteed that at least one of the back EMFs in Phase B and Phase C is higher than Phase A during the operation. In this case, one or two conduction loops between phase windings can be formed through the upper antiparallel diodes and IGBT S_1. Therefore, the regions where the back EMF of Phase A is not the maximum in magnitude are available. When the proposed control strategy is enabled, the original control aiming at stabilizing the operation is adjusted to the intermittent reverse-charging mode. Then, the power supply is stopped, but the motor keeps rotating due to inertia.

As previously mentioned, the PMSM is taken as the driven motor. The PM flux is kept constant regardless of the power supply. Actually, due to the remained rotor magnetic field, the three-phase back EMFs are generated by electromagnetic induction when the rotor keeps rotating. The magnitudes of three-phase back EMFs are determined by the relative positions of the windings and (permanent magnet) PM in each phase. In Fig. 7, the model of a PMSM is shown to demonstrate the mechanism of back EMF generation. For example, when the PM rotates to the position shown in Fig. 7, the back EMF of Phase A reaches its peak. Meanwhile, considering that the three-phase windings are arranged symmetrically, the generated three-phase back EMF waveforms are characterized by the same amplitude and phase differences of 120°. Assuming that the back EMF of Phase A reaches the peak when $\theta = 0°$, the waveforms of the produced three-phase back EMFs based on the rotor position are shown in Fig. 8. So, at each electrical period in a range of 360°, the nonmaximum region of back EMF in Phase A is $60° \leq \theta \leq 300°$, which is labeled in Fig. 8.

As for the selection of the nonmaximum region at the control level, there are two approaches: based on the signals of position sensors and based on the condition of phase currents. On the one hand, typical PMSM drive systems are equipped with position sensors, which support the accurate location determination for stable control. On the other hand, after compensation according to the load condition and winding parameters, the measurable

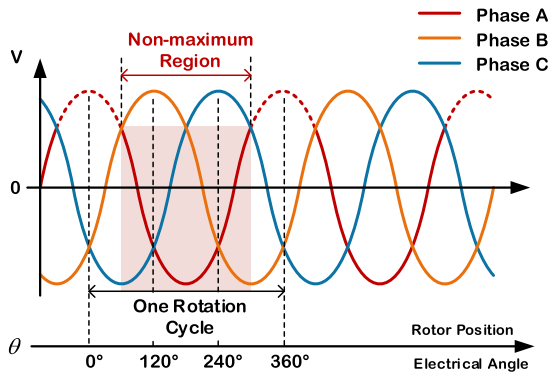

Fig. 8. Feasible region considering the induced back EMFs.

three-phase currents can represent the condition three-phase back EMFs. Therefore, the position selection can be implemented on both sensor-equipped and sensor-less systems.

After the selection of the feasible operating region, the exact inserted position of the reverse-charging strategy can be determined. Nevertheless, before the implementation of this method, the duration of the operating period should be analyzed and set for sufficient voltage increment and minimal negative impact.

IV. Analysis and Selection of the Duration of the Reverse Charging Mode

Considering the estimation accuracy and negative impact of the inserted operation, the duration of an entire reverse-charging period is restricted by the following three aspects:

1) the impact of current rising on IGBT switches and stator windings;
2) the acceptable speed reduction;
3) the required total increment of dc-link voltage for estimation.

On the one hand, the excessive duration of inserted reverse-charging mode will cause excessive speed fluctuation, and the current rising during ON state should be limited under the permissible peak currents of IGBT switches and stator windings. On the other hand, an inadequate reverse-charging operation can result in an insufficient increment of dc-link voltage, which may lead to an inaccurate estimation of the capacitance. Hence, the duration of an entire reverse-charging period should be selected in a reasonable range by analyzing the relevant transition process. Assuming that the total duration of one reverse-charging cycle is T, of which the ON-state duration is t_1 and the OFF-state duration is t_2. In view of the above three influence factors, the following studies are introduced in turn.

A. Peak Limitation of the Response Current

The peak of response is determined by the duration of the ON state in one cycle. As described in Section III, the expressions of response currents in two stages of one reverse-charging cycle are defined, which supports the duration selection for current regulation. The smaller one between the permissible peak currents of IGBT switches and stator windings should be used as the upper limit of the response current. It is worth mentioning that the peak value of motor's rated current is used as the upper limit in the test for the protection of the motor. A specific duration can be calculated by the current limitation and used as the maximum permissible ON-state duration t_1.

B. Speed Reduction During the Reverse-Charging Mode

There are two factors affecting the speed. On the one hand, the power supply is paused and the rotating speed begins to decrease due to the internal friction. On the other hand, electrical energy is generated in the conducting circuits established during the reverse-charging state. Actually, the entire reverse-charging stage is a process that the mechanical energy is converted into electrical energy.

Actually, these two processes are coupled, which is difficult to conduct quantitative analysis respectively. Therefore, the artificial reverse-charging stage is regarded as the operation of generator mode, which is without additional torque excitation.

In generator mode, the speed reduction is determined by the mechanical motion equation of PMSM, which is written as

$$J\frac{d\omega_m}{dt} = T_e + T_L + B\omega_m \tag{5}$$

where T_e represents the electromagnetic torque, T_L is the combined torque of load and static friction, J indicates the nominal rotational inertia, ω_e is the electrical angular velocity, and B is the nominal viscous friction coefficient.

In practice, T_e is the combination of torque produced by the force of the induced stator magnetic field on the PM, which impedes the rotation of the rotor. In this operating mode similar to the generator, T_e can be calculated as follows:

$$T_e = \frac{3}{2}\, p\left[\psi_r i_q + (L_d - L_q)\, i_d i_q\right] \tag{6}$$

where p is the pole pairs, ψ_r is the PM flux, L_d and L_q are the inductance of d- and q-axis, and i_d and i_q are the currents of d- and q-axis. Actually, the expression of T_e is consistent with the motor mode. Therefore, the magnitude of T_e is dependent on the current value. In previous conceptual design, the response current is limited to not exceeding the peak value of motor rated current. Therefore, the theoretical maximum value of T_e is close to the rated load torque of the motor. Based on the worst impact assessment criteria, T_e is treated as the maximum value, which can be replaced by the rated load torque. So, the speed reduction can be calculated by

$$J\frac{d\omega_m}{dt} = T_{L\_\text{rated}} + T_L + B\omega_m. \tag{7}$$

Since the duration is so short that the mechanical speed can be considered unchanged in term $B\omega_m$. Combined with the assumed torque condition, the reverse-charging stage can be regarded as a uniform deceleration process. In one reverse-charging control cycle, the deceleration value can be calculated as

$$\begin{aligned} \alpha &= \left(T_{L\_\text{rated}} + T_L + B\omega_m\right)/J \\ &\Rightarrow \Delta\omega = \alpha\Delta t,\ \Delta t = T = t_1 + t_2 \end{aligned} \tag{8}$$

where α is the deceleration and $\Delta\omega$ represents the speed fluctuation. ω_e is regarded as a constant of the initial speed.

Then, when the entire duration is determined, the maximum speed reduction can be calculated for a reverse-charging control cycle. If the tolerable speed reduction is definite, it can be used to derive the permissible duration of the operating period.

C. Requirement of Sufficient DC-Link Voltage Increment

In terms of priorities, maintaining the safe and reliable operation of the system is the primary premise. Nevertheless, a sufficient increment of dc-link voltage is the guarantee of estimation accuracy. When the voltage increment is sufficient to estimate the capacitance, the shortest duration should be selected for the least impact on the operating stability. In practice, The dc-link voltage increment is dependent on the total integral value of current in the charging stage. Considering that the duration of the current attenuation is determined by the initial value, with a limited peak value of response current, the maximum integral value of current in one reverse-charging cycle is definite. When the tolerable speed reduction is specific, especially at low speed, the entire duration is definite.

Overall, when the limitation of these factors mentioned above is quantified, the maximum duration of the reverse-charging operation is determined. In this condition, maximum dc-link voltage increment should be acquired by optimized operating mode.

V. Simulation Studies on Reverse-Charging Mode

Based on the aforementioned principle, an inverter drive system is established in MATLAB/Simulink for simulation purposes. As aforementioned, high-power machines are more tolerable and feasible. Generally, for the same value of voltage increment, high-power machines require a shorter duration of reverse charging, which is on account of the current limitation and current generation capability. The respective models are simulated for demonstrating the specific implementation.

A. Low-Power Machines

The capacitance and ESR of dc-link capacitors are set as 1000 μF and 0.02 Ω, respectively. For sufficient voltage increment to estimate the dc-link capacitance, it is worth mentioning that an entire implementation period is composed of several reverse-charging control cycles. One reverse-charging control cycle is combined by these two stages: current generation and reverse charging.

Assuming that the direction of flowing into the motor is positive, the simulated three-phase currents in response are shown in Fig. 9. Corresponding to the feasible operating region, the duration of one entire implementation period is 3.33 ms, which is 2/3 of the rotation period. The current of Phase A remains nonzero and the currents of the other two phases are generated when either of the corresponding back EMFs is higher than Phase A. Meanwhile, as demonstrated in Fig. 10, the speed fluctuation is around 100 r/min during one entire implementation period and the increment of dc-link voltage is obvious. As for

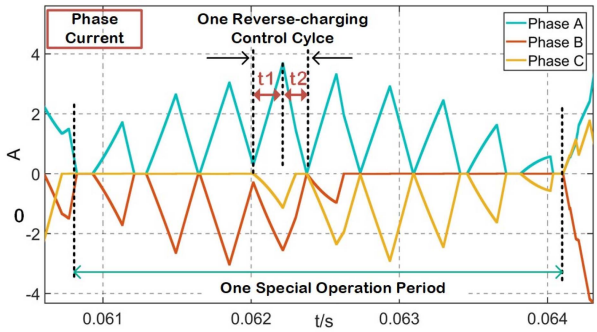

Fig. 9. Three-phase currents during the reverse-charging control.

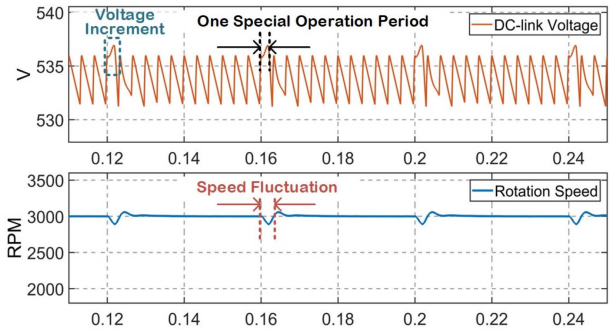

Fig. 10. Condition of voltage increment and speed fluctuation during reverse-charging control.

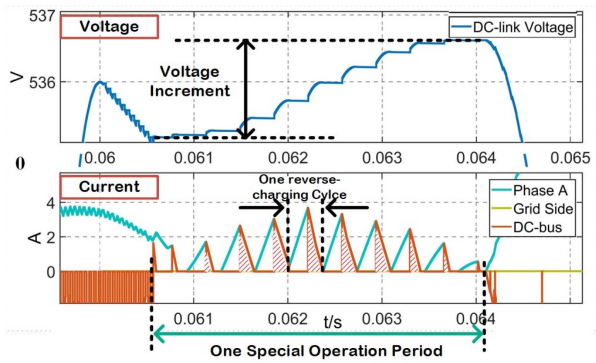

Fig. 11. Reverse charging based on the sufficient current drop.

the condition of dc bus, assuming that the direction of flowing into the dc bus is positive, the result is shown in Fig. 11. A reverse-charging control cycle consists of a rise and fall of phase current. At the current falling stage of Phase A, the current of the dc bus is exactly the same as Phase A, which fits the explained charging process. Each stepwise increment of the dc-link voltage corresponds to the OFF state in each control cycle.

As shown in Fig. 11, the shaded areas should be calculated as the integral quantity of the charging current, and the total increment of dc-link voltage in this entire implementation period is obtained. Therefore, the dc-link capacitance can be

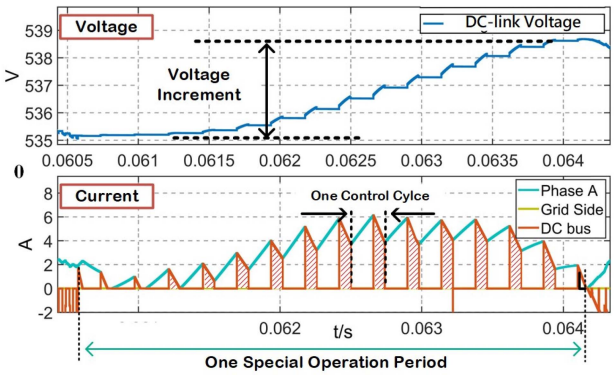

Fig. 12. Reverse charging based on the modified strategy.

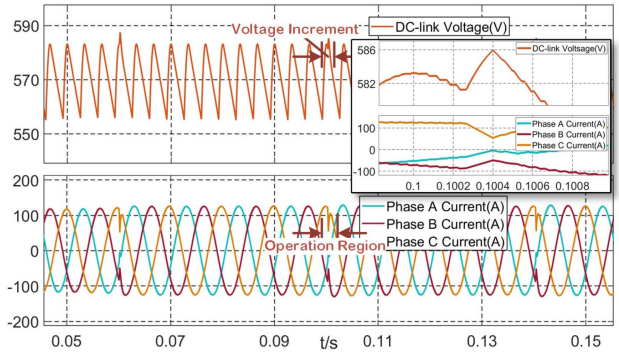

Fig. 13. Reverse charging based on the sufficient current drop.

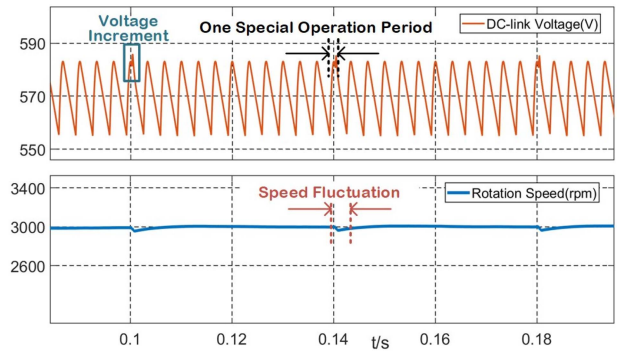

Fig. 14. Condition of voltage increment and speed fluctuation during reverse-charging control.

calculated by

$$C_{\mathrm{dc}} = \sum_{1}^{n} \left(\int i_a dt \right) / \Delta U_{\mathrm{dc}} \tag{9}$$

where n is the number of reverse-charging cycles, i_a is current of Phase A, and ΔU_{dc} is the total increment of the dc-link voltage. When the current of the dc-link capacitor bank is zero, there is no voltage drop across the ESR. So, the dc-link voltage after the current reaches zero is taken as the end value to calculate the increment.

When the capacitance to be estimated is a fixed value, a larger voltage increment is produced by a larger current integral value. As mentioned in Section IV, to obtain the maximum increment of dc-link voltage in a certain operating duration, the operating process should be optimized. As shown in Fig. 12, compared with the control strategy shown in Fig. 11, the OFF state is shortened for more efficient reverse charging. Therefore, the charging current is always kept at a large value. In this operating mode, more reverse-charging cycles can be implemented for larger voltage increments over the same length of duration.

B. High-Power Machines

For comparison, the values of capacitance and ESR of the high-power machine model are consistent with the aforementioned. In addition, the dc-link voltage level is improved for capacity matching. With higher load conditions, three-phase currents exceed 100 A. In addition, the normal operating current limitation is high, which can provide sufficient power to charge the capacitors without intermittent mode. For an equal increment of voltage, the required duration is shorter. In this condition, the duration is shortened as shown in Fig. 13, which is about 0.2 ms. Furthermore, as shown in Fig. 14, due to the larger inertia and shorter operating duration, the speed fluctuation is significantly reduced, which is around 30 r/min. Therefore, the high-power machines provide a more suitable application prospect.

So far, an online dc-link capacitance estimation method based on the intermittent active reverse-charging control strategy for motor drive systems has been accomplished. Low-power and high-power machines are both simulated to demonstrate their applicability. The reverse-charging process is intentionally formed for the increment of dc-link voltage. In summary, the novelties of the proposed method are considered as follows.

1) No additional devices are required.
2) Online estimation is realized.
3) The estimation accuracy is improved.

The improved accuracy is based on the convenience of data monitoring. Due to the countertrend of the voltage rise at the stage in which the dc-link capacitors supply load separately, the voltage increment can be monitored with high accuracy. In addition, as previously mentioned, the reverse-charging current is also a measurable quantity. As for the verification of feasibility and accuracy, the proposed method is implemented through experimental tests. Moreover, in order to demonstrate the feasibility more effectively, a low-power PM motor is used as the test machine.

VI. Experimental Verification

A. Setup of the Test System

To verify the validity of the dc-link capacitance monitoring technique based on an intermittent active reverse-charging strategy, an experimental test is performed on a PMSM drive system. As shown in Fig. 15, The PMSM is fed by a variable frequency drive with configurable dc-link capacitors. The nominal parameters of the test PMSM are shown in Table I. IGBTs are used as switching devices in the three-phase converter. A DSP chip

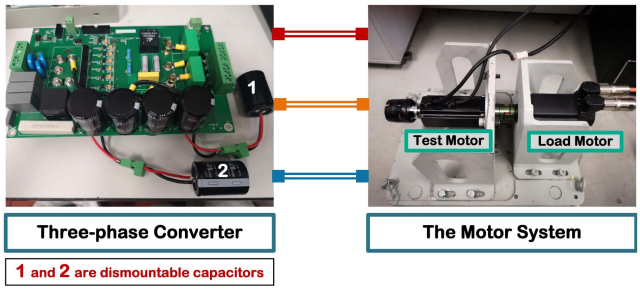

Fig. 15. Test bench for experimental verification.

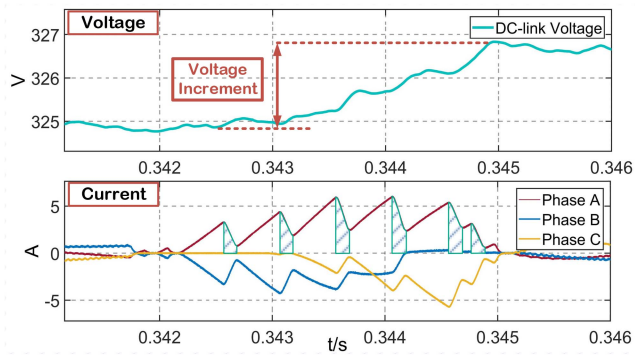

Fig. 16. Waveforms in detail of the experimental result.

TABLE I
SPECIFICATION OF TEST PMSM

Parameters	Values
Rated power	400 W
Rated speed	3000 r/min
Rated voltage (RMS)	220 V
Rated current (RMS)	2.89 A
Permissible current (RMS)	8.67 A
Pole pairs	4
Rated torque	1.17 N·m
Nominal rotational inertia of rotating parts	$2.16*10^{-4}$kg·m^2
Nominal viscous friction coefficient	0.0001

(TMS320F28335) operating at 150 MHz is used to conduct the SVPWM control strategy, of which the switching frequency is 10 kHz. In addition, for detection of the feasible region, the PMSM is equipped with an incremental pulse encoder, of which the type is SBH-1024-2C.

Aluminum E-Caps are used in the configurable dc-link capacitor bank, which is composed of four fixed capacitors and two dismountable capacitors. The type of these capacitors is Black Gate/KMH 1000 μF 450 V. The connection type of the four fixed capacitors is that two capacitors considered as one pair are connected in parallel respectively and the two parallel pairs are connected in series. The dismountable capacitors can be separately attached to the two parallel pairs. Theoretically, the fixed capacitance value is 1000 μF and the reachable value is 1500 μF.

Actually, the reference condition of the nominal capacitance is 25 °C and 120 Hz. But the current during the reverse charging process should be considered as a dc value. Therefore, the test capacitor bank is disassembled and measured using a Hioki 3532 HITESTER *LCR* meter at 20 Hz and 25 °C. The values for conditions whether dismountable capacitors are installed are 1000.5 and 1500.8 μF, which serve as the reference values for two conditions. The instrument accuracy is $\pm 0.06\%$.

B. Implementation of Capacitance Monitoring

Fig. 16 shows the detailed experimental waveforms of the dc-link voltage and three-phase currents, which are based on the voltage source inverter drive system. The operating condition is 100% of rated speed and 20% of rated load. The process of being charged in reverse of the dc-link capacitor bank is demonstrated. There are mainly six active reverse-charging cycles, and the phenomenon of voltage rise occurs in these OFF states, which are shaded. During an intermittent charging process of 3.2 ms, the increment of dc-link voltage is 2 V. Combined with the accumulated integral value of charging current, the estimated dc-link capacitance is 1001.2 μF, which means the error compared with the test value is 0.7 μF.

For the current limitation, the permissible currents of the IGBT switches and stator windings are 20 A and 8.67 A, respectively. The maximum value of the response current is 5.1 A, which is close to the rated peak value and less than these two limits.

As for the speed reduction of the demonstrated case, it can be calculated as

$$\Delta\,\omega_m = \frac{2T_{L\_\text{rated}} + B\omega_m}{J}\,\Delta T \tag{10}$$

where T_{L_rated} is 1.27 N·m, J is $2.16*10^{-4}$ kg·m^2, ω_m is 100 π, B is 0.0001, and ΔT is 0.0032 s.

Then, the speed reduction, in this case, is 35.1 rad/s, which is about 10% of the rated speed. Actually, as mentioned previously, the entire implementation period can be adjusted for variable permissible speed reduction. For low-speed conditions, the duration of reverse charging will be reduced.

In addition, compared with the quasi-online techniques, the proposed reverse charging can be implemented multiple times during the normal operating state. The reprocessing of the results obtained from multiple intermittent tests can eliminate the errors caused by measurement and other factors in signal estimation. To minimize the impact on the operation, the proposed active control mode is intermittently inserted into the normal operation. As shown in Fig. 17, with a 20% rated load, the active reverse-charging control is executed at intervals. Every 60 ms, shortly after the dc-link capacitors begin to supply the load separately, the active reverse-charging control strategy is inserted. For each test condition, the intermittent reverse-charging control strategy is implemented 100 times for adequate data acquisition. Then, all the estimation results of the same condition are averaged as the representative value.

It is worth mentioning that heavier load and higher load current can provide a more distinguishable decrease region of dc-link voltage. Compared with a lighter load, a higher load is

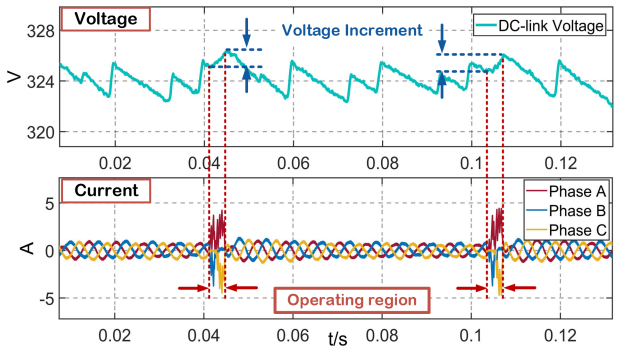

Fig. 17. DC-link voltage and three-phase currents during the test.

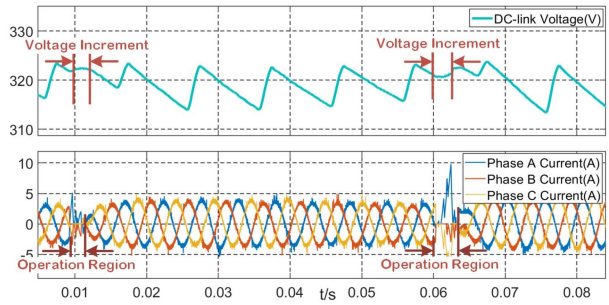

Fig. 18. DC voltage and phase currents during reverse charging in rated load.

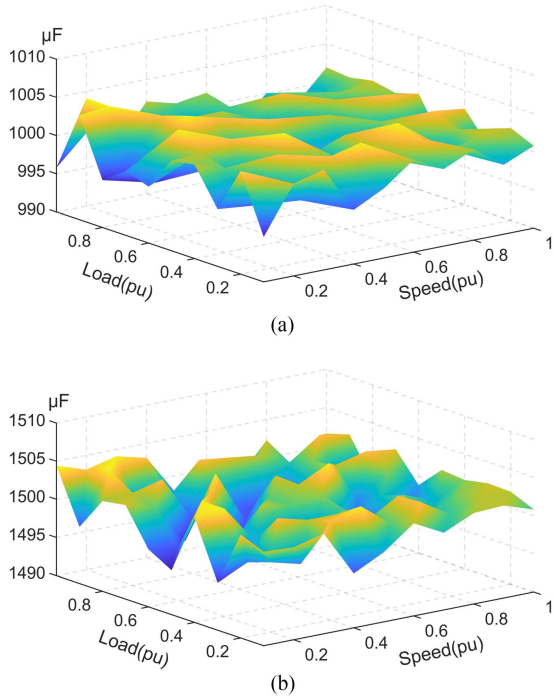

Fig. 19. Estimation results for dc-link capacitance. (a) DC-link capacitance is 1000 μF. (b) DC-link capacitance is 1500 μF.

beneficial for dc voltage measuring and feasible region selection. As the rated load condition is shown in Fig. 18, the extremum difference is larger than that in Fig. 17.

It is worth mentioning that the detected voltage should be filtered by hardware or digital process, which is utilized to eliminate the harmonics. Various conditions under different speeds and loads are tested. The estimation results of the two conditions of capacitance are plotted in Fig. 19. The load condition is varied from 0 to 100% of the rated value in intervals of 10%. The speed condition is varied from 10% to 100% of the rated value in intervals of 10%.

To be specific in terms of implementation, according to the equations of response currents and the empirical conclusion drawn from the experiments, the durations of ON and OFF states in each cycle are 25–30 μs and 10–15 μs respectively, which is dependent on the target value of current. The number of reverse-charging cycles is determined by the entire duration. In these test cases, the duration of an entire special implementation period is adjusted with speed to cope with variable r/min drop limits. For example, the duration is 3 ms and 1.5 ms when the speed is 3000 r/min and 300 r/min, respectively. A shorter duration of the special operation period means a smaller voltage increment. Therefore, as shown in Fig. 19, the estimation errors tend to decrease with the increase in speed. Overall, the maximum errors under all test conditions are less than 0.5%. The rms errors of the two test capacitances are approximately 0.45% and 0.47%.

To sum up, the availability of the proposed method is verified by experimental tests under various operating conditions. The estimation accuracy is outstanding and the implementation is feasible for online monitoring.

VII. Discussion on Practical Application

A. Application Scope

Theoretically, the active reverse-charging control strategy is an intrusive monitoring method. The speed fluctuation is the main negative effect during the operating period. Admittedly, this method is not suitable for high-performance motor drives, which require to achieve accurate reference tracking torque, speed, or position. Nevertheless, compared with other methods like signal injection, the intermittent reverse-charging control is extremely short with minimal impact on the system's normal operation. In addition, the speed fluctuation is slight and the time scale is at the millisecond level. Moreover, the high-power machines will be more tolerable for the reverse-charging mode due to the high current limitation and large inertia. Therefore, this method is feasible in most application scenarios, which is tolerable to the slight and short fluctuation of rotation speed.

B. Analysis of Factors Affecting the Estimation Accuracy

It is worth mentioning that estimation accuracy is affected by measuring precision. Therefore, the ability of typical devices should be investigated. In our controller used for experiments, VSM025A Hall voltage sensor is utilized to measure the dc-link voltage. The precision level declared in the manual is $\pm 0.7\%$, which is common in typical converters. In addition, the current sensor used in the converter is HNC50LA Hall sensor, of which the nominal absolute accuracy is 0.1%. Therefore, based on these conventional measuring devices, the monitoring accuracy of dc-link voltage and current is sufficiently high. Actually, the

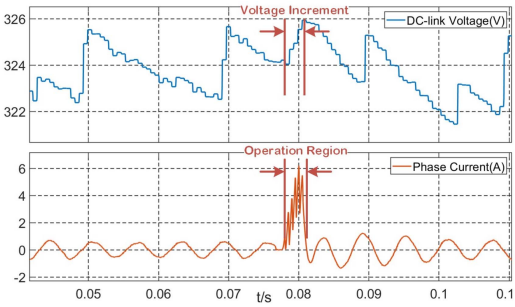

Fig. 20. DC voltage and phase current sampled from the controller.

estimation accuracy is more determined by the sampling frequency, which is dependent on the analog to digital conversion frequency and accuracy. In our test, the frequency of analog to digital conversion is set to 20 kHz, which is accessible in typical converters. The sampling data of dc-link voltage and phase current from the controller is output through the series port, as shown in Fig. 20. The voltage increment and current fluctuation are able to be distinguished. Based on these devices and processing algorithms, the estimation errors are within 0.9%–1%.

VIII. Conclusion

An online dc-link capacitance estimation method for motor drive systems based on intermittent active reverse-charging control strategy has been proposed in this article. By altering the control strategy of the power switches in the inverter, a reverse-charging mode is introduced, where the dc-link capacitors are charged reversely by the motor. Based on the measurable phase current and the increment of the dc-link voltage, the capacitance estimation results can be obtained with high accuracy. With fluctuations in speed during a very short time at millisecond level, the accurate online capacitance estimation can be realized. The implementation of the proposed method is simple and applicable to different operating conditions. Experimental validation shows that the proposed estimation method is accurate during various operating conditions, with a maximum error of 0.5%. Compared to other existing methods, the key features of the proposed method are listed as follows.

1) No additional hardware is required.
2) The scheme can be implemented during normal operations.
3) The estimation accuracy is significantly improved.

The three-phase currents at the inverter output have been utilized to estimate the dc-link current. Based on the analysis of the operating characteristic of capacitors, the discharge duration of the dc-link capacitor has been analyzed for accurate estimation. The impact of the operating frequency and condition of load on the capacitance value of aluminum E-Caps have also been discussed.

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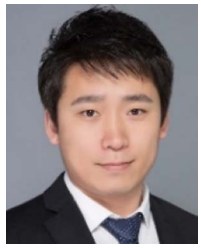

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