A Single-Switch Continuous Input Current Buck–Boost Converter With Noninverted Output Voltage

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***Abstract*—In this article, a single-switch continuous input current (CIC) buck–boost converter with noninverted output voltage is proposed. The proposed converter utilizes capacitor and inductor along with three diodes in conjunction with a quadratic boost converter to adopt its CIC feature. The features of high voltage gain, single active power switch, less ripple CIC, and noninverted output voltage make the proposed converter suitable for renewable and industrial applications. In addition, it provides a wide operating voltage gain with optimum component count, which is higher than the conventional buck–boost converter. Furthermore, it has low voltage stress across the power switch with comparable converters. To elevate the importance of the proposed converter, a detailed comparison analysis has been carried out considering voltage stress, voltage gain, effectiveness index, and component count. The operating principle and steady-state analysis in continuous conduction mode and discontinuous conduction mode of the proposed converter are discussed in detail. To validate the theoretical analysis and performance of the proposed converter, a prototype has been developed and tested in laboratory.**

***Index Terms*—Buck–boost converter, continuous input current (CIC), noninverted output voltage.**

I. Introduction

In THE current scenario, renewable energy resources captivate considerable attention due to issues aroused because of global warming, increase in energy consumption, abatement of fossil fuels, climate changes [1], etc. In general, power electronics equipment has an indispensable role in integrating these renewable energy resources, such as photovoltaic (PV), wind energy, and fuel cells, to the load. In addition, these power electronic equipments are used in many applications, such as battery systems, power factor correction, electric vehicle, portable devices, etc., and maintains the load voltage on account of broad variation in source voltage. In contrast, some applications, such as multifunctional switched mode power supplies, require a varied range of output voltages with respect to constant source at the input end. A dc–dc converter with a wide voltage conversion ratio becomes a promising solution for the aforementioned aspects. Boost and Buck converters are conventional and well-established due to their intelligible and simple structure. On the other hand, these converters are confined to limited voltage conversion ratio requirements in the extremes of desired voltages, low or high. Consequently, to discard these limitations, the voltage multipliers, voltage lift, switched capacitor/switched inductor, and cascading techniques are employed for achieving high voltage gain. Furthermore, interleaved converters are useful in achieving step-down or step-up mode with low ripple current. However, it is adding complication in the converter structure as well as control strategy due to additional switches.

A buck–boost converter benefits in providing both step-up as well as step-down modes in contrast to conventional boost or buck converter. In PV applications, the buck–boost converter faces difficulties in integrating the loads due to its pulsating source current [2], which is not admissible. In addition, the pulsating source current slackens or degrades efficiency, life, and performance of PV and fuel cell [3]. A Cuk converter is derived from a boost converter where the diode is replaced with an inductor-capacitor-diode (LCD) network. It abolishes the indispensable pulsating current and smoothens with the use of an inductor at the input end. An added advantage of continuous output port current, due to the presence of another inductor at the load end, makes the converter more suitable for PV and fuel cell applications. The inverted output voltage which is still present in the converter as a buck–boost converter pertains to some specific applications, such as data transmission, signal generators, etc. However, extra circuitry is needed to invert the voltage polarity in the control loop. To overcome the issue of inverted voltage polarity, a pair of converters is introduced, namely single ended primary inductance converter (SEPIC) and Zeta. The SEPIC converter is a variant of the Cuk converter where the inductor and diode are swapped in the LCD network. However, it attains noninverted output voltage with the expense of absence in continuous output port current. The Zeta converter is derived from a buck-boost converter where the diode is replaced with LCD network. Further, in contrast to the Cuk converter, the Zeta converter achieves noninverted output voltage and continuous output port current with a shortcoming of pulsating input current, which is not agreeable. But, in contrast to the Cuk converter, this converter achieves noninverted output voltage and continuous output port current with a shortcoming

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of pulsating input current, which is not agreeable. In addition, these derived converters have the same voltage conversion ratio as the conventional buck–boost converter, and it may not be suitable for a wide range of operations.

Hence, a quadratic buck–boost converter [4] is presented in the literature, which was developed by integrating two conventional buck–boost converters in a cascade manner utilizing a single switch. This converter facilitates a wide operating range in terms of quadratic gain. However, this converter fails in providing continuous input and output ports current as well as its ability to work in boost mode for $d > 0.5$ because of the voltage stress across diode D_b ($V_{D_b} = V_0 \cdot (1 - 2d/d^2)$). With the inclusion of an additional switch to the aforementioned converter, a modified quadratic buck–boost converter [5] was proposed with the ability to work in boost mode. Perhaps, this converter finds difficulty in providing continuous input and output ports current as the aforementioned converter in [4]. This is due to the floating switches presented in the converter. To preserve the property of continuous input current (CIC) of the converter in [5], a converter in [6] was proposed with reconfiguration of similar component count, which further deviates the voltage gain and gives inverting voltage polarity. The converters presented in [7] and [8] employed capacitors in series with input source reflects output voltage, which makes the converter to achieve quadratic gain with pulsating current due to switched capacitor.

In pursuit of minimizing the switch count, a series of converters with single switch are proposed with elevation of conversion ratio, which resembles conventional buck–boost, Cuk, SEPIC, and Zeta in terms of properties. Converters presented in [9] and [10] achieved twice voltage gain of conventional buck–boost converters along with properties of Zeta converter. However, in [9], the load was tapped across two capacitors, which were connected in series fashion. This increases the output voltage ripple and is not advisable. A quadratic gain-based buck–boost converter was proposed in [11] with a single switch. Furthermore, it derived from a buck–boost converter where the inductor is replaced with switched inductor cell to improve the conversion ratio. In the same fashion, with increment of passive components in switched inductor cell that is integrated in the buck–boost converter, as in [11], was proposed in [12]. Hence, the converter enhances the conversion ratio three times of conventional buck–boost conversion ratio. However, these sets of converters are unable to abolish the difficulties that are present in [5], mainly the CIC.

With the importance of quality of CIC, single switch, and high conversion ratio, a pair of converters was introduced in [13] and [14] with inverting voltage polarity. The converter presented in [13] utilized the Cuk converter as its embodiment. Furthermore, it achieved high gain in step-up mode when compared with the Cuk converter. Similarly, in [14], with inclusion of basic buck, buck–boost, and boost converters, a converter with quadratic gain was proposed. Unlike the aforementioned converters, the SEPIC-based implementation of converter [15] was pertinent in terms of CIC and noninverting voltage polarity.

In this article, the number of energy storage elements of the SEPIC-based converter presented in [15] is minimized. Also, the proposed converter achieves better voltage gain capabilities in both boost as well as buck modes. Furthermore, unique features of the proposed converter, such as noninverting voltage polarity, comparable high gain, less voltage stress, and substantial CIC, are noteworthy to mention. The proposed buck–boost converter configuration is divergent to the conventional buck–boost converter and other presented converters in the literature.

II. Circuit Schematic of the Proposed Converter and its Description

The proposed converter configuration emanates from the traditional quadratic boost converter (QBC) to preserve the abilities in terms of CIC, noninverted output voltage, and wide operating range, which are inevitable shortcomings in the conventional buck–boost converter. As shown in Fig. 1(a), an additional set of passive elements, such as inductor L_c, capacitor C_b, and diodes D_c and D_d, is employed in QBC for acquiring the abilities of buck mode along with the boost mode. QBC comprises of a pair of inductors ($L_a$andL_b), capacitors ($C_a$andC_c), three diodes (D_a, D_b, andD_c), and a power switch (S). In continuous conduction mode (CCM), the proposed configuration shuttles between two operating modes based on the state of power switch ON or OFF over a switching period, as shown in Fig. 2. Furthermore, the steady-state typical waveforms of the proposed converter are shown in Fig. 3.

The following assumptions are made to ease the analysis of the proposed converter in view of operating modes and steady-state analysis.

1) Nonconducting passive devices and switch are shown in light gray color.
2) Voltage across the utilized capacitors is contemplated as constant over a switch cycle due to the enough value of capacitance is used.
3) Power devices are considered as ideal. Thus, the parasitics are neglected.

A. Operation Principle

1) Mode 1 $[t_a - T_b]$*:* This mode commences by switching the power switch S at $t = t_a$ and lasts until $t = t_b$ before entering into the subsequent interval. The equivalent schematic of this mode is shown in Fig. 1(b). During this mode, the diodes ($D_b$andD_d) assist the inductors ($L_a$andL_b) to magnetize by utilizing the input voltage source (V_i) and capacitor (C_a) being in conduction state. In addition, the diode (D_a) at the input end turn into reverse biased by the virtue of voltage (V_{C_a}) across it. The inductor L_c gets magnetized using capacitor C_b with the entitling reverse biased diodes ($D_c$andD_e) where the diodes ($D_c$andD_e) block the voltages of V_{C_b} and $V_{C_c} + V_{C_b}$, respectively. Finally, the capacitor (C_c) alone energizes the load by discharging through it. The voltages across inductor followed by currents through capacitor are expressed in Table I.

2) Mode 2 $[t_b - T_c]$*:* As subsequent mode to the mode1, this mode starts OFF at instant t_b by switching OFF the power switch S lasts until t_c, which becomes starting point to the mode1. The equivalent schematic of this mode is shown in Fig. 1(c) and the current paths are represented as dotted lines. In contrast to the earlier mode, the inductors start discharging in a way to charge

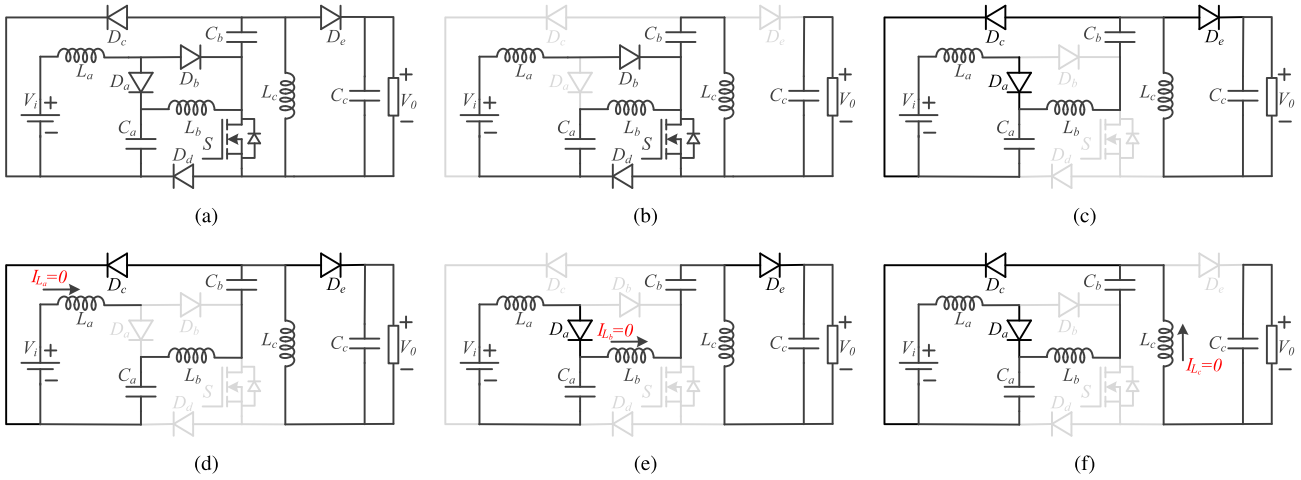

Fig. 1. Equivalent circuits. (a) Proposed converter. (b) ON state. (c) OFF state. (d) DCML_a state. (e) DCML_b state. (f) DCML_c state.

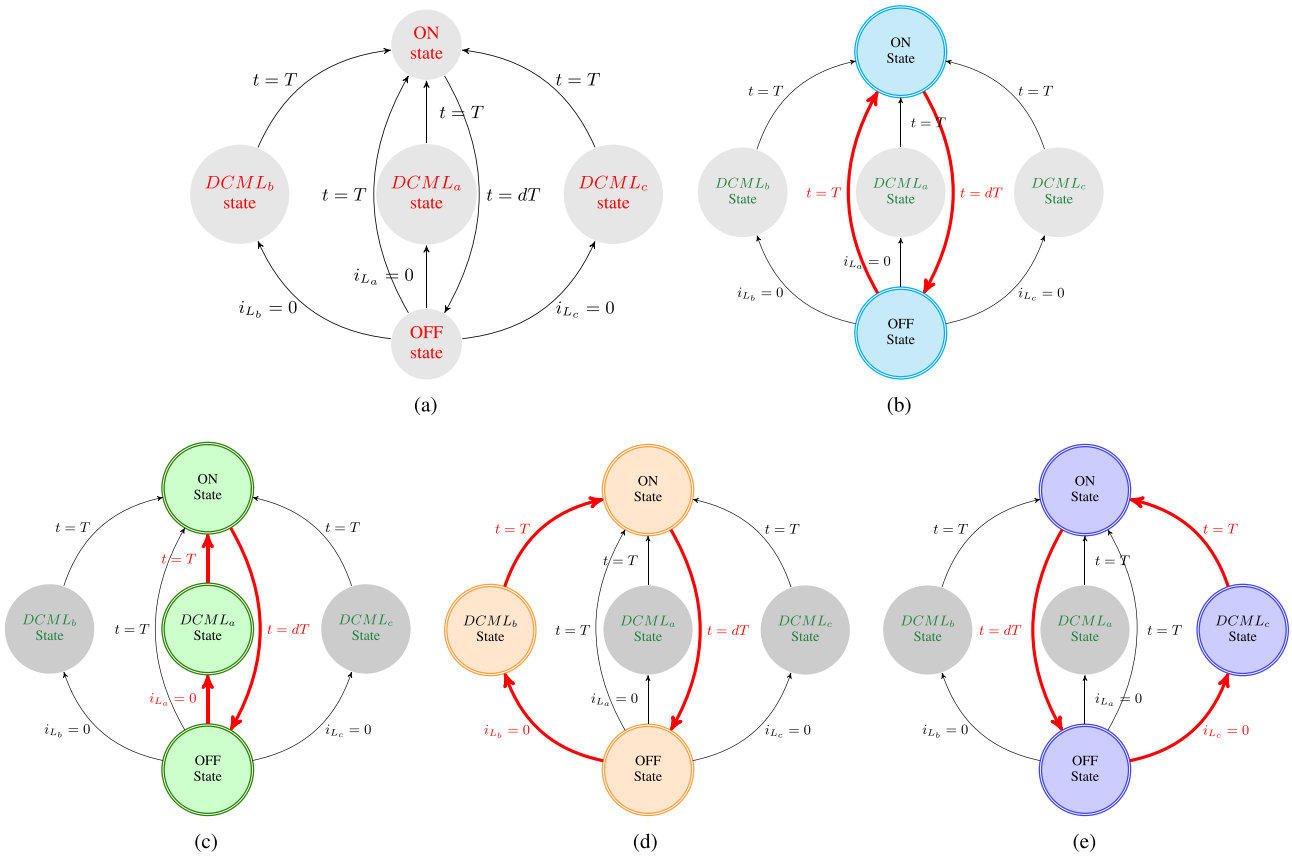

Fig. 2. Conduction mode state diagram of the proposed converter. (a) General representation. (b) CCM. (c) DCML_a. (d) DCML_b. (e) DCML_c.

the capacitors where inductors L_a and L_b and voltage source V_i accompany the capacitor C_a, inductor L_b assists the capacitor C_b, and finally the capacitor C_c charged up by inductor L_c. The posterior energy exchange is through the forward biased diodes (D_a, D_c, and D_e) in addition to reverse biased diodes ($D_b$andD_d). The voltages across inductor followed by currents through capacitor are expressed in Table I.

III. Steady-State Analysis

A. CCM Analysis

1) Voltage Gain: To ease the analysis of voltage gain derivation, it is assumed that the voltage ripple content on the all capacitors is negligible. With this, the voltage across each capacitor can be found by utilizing the volt–second balance principle

TABLE I
PROPOSED CONVERTER STATE EQUATIONS

	$V_{L_a}=L_a\frac{\mathrm{d}i_{L_a}}{\mathrm{d}t}$	$V_{L_b}=L_b\frac{\mathrm{d}i_{L_b}}{\mathrm{d}t}$	$V_{L_c}=L_c\frac{\mathrm{d}i_{L_c}}{\mathrm{d}t}$	$i_{C_a}=C_a\frac{\mathrm{d}v_{C_a}}{\mathrm{d}t}$	$i_{C_b}=C_b\frac{\mathrm{d}v_{C_b}}{\mathrm{d}t}$	$i_{C_c}=C_c\frac{\mathrm{d}v_{C_c}}{\mathrm{d}t}$
ON state (dT)	v_i	v_{C_a}	v_{C_b}	$-i_{L_b}$	$-i_{L_c}$	$-i_0$
OFF state $((1-d)\,T)$	$v_i-v_{C_a}$	$v_{C_a}-v_{C_b}$	$-v_{C_c}$	$i_{L_a}-i_{L_b}$	i_{L_b}	$i_{L_c}-i_0$
DCM$L_a$state (d_xT)	0	$v_{C_a}-v_{C_b}$	$-v_{C_c}$	$-i_{L_b}$	i_{L_b}	$i_{L_c}-i_0$
DCM$L_b$state (d_yT)	$v_i-v_{C_a}$	0	$-v_{C_c}$	$i_{L_a}-i_{L_b}$	0	$i_{L_c}-i_0$
DCM$L_c$state (d_zT)	$v_i-v_{C_a}$	$v_{C_a}-v_{C_b}$	0	$i_{L_a}-i_{L_b}$	i_{L_b}	$-i_0$

TABLE II
VOLTAGE ACROSS THE CAPACITORS AND CURRENT THROUGH THE INDUCTORS

	V_{C_a}	V_{C_b}	V_{C_c}	i_{L_a}	i_{L_b}	i_{L_c}
CCM	$\frac{V_i}{(1-d)}$	$\frac{V_{C_a}}{(1-d)}=\frac{V_i}{(1-d)^2}$	$\frac{dV_{C_b}}{(1-d)}=\frac{dV_i}{(1-d)^3}$	$\frac{i_{L_b}}{(1-d)}=\frac{dI_0}{(1-d)^3}$	$\frac{di_{L_c}}{(1-d)}=\frac{dI_0}{(1-d)^2}$	$\frac{I_0}{(1-d)}$
DCML_a	$\frac{V_i\,(d+d_x)}{d_x}$	$\frac{V_{C_a}}{(1-d)}=\frac{V_i\,(d+d_x)}{d_x\,(1-d)}$	$\frac{dV_{C_b}}{(1-d)}=\frac{V_i d\,(d+d_x)}{d_x\,(1-d)^2}$	$\frac{v_i d\,(d+d_x)}{2L_a f}$	$\frac{di_{L_c}}{(1-d)}=\frac{Q_{L_{a_{\mathrm{OFF}}}}}{T}$	$\frac{I_0}{(1-d)}$
DCML_b	$\frac{V_i}{(1-d)}$	$\frac{V_{C_a}\,(d+d_y)}{d_y}=\frac{V_i\,(d+d_y)}{d_y\,(1-d)}$	$\frac{dV_{C_b}}{(1-d)}=\frac{V_i d\,(d+d_y)}{d_y\,(1-d)^2}$	$\frac{i_{L_b}}{(1-d)}$	$\frac{v_{C_a} d\,(d+d_y)}{2L_b f}$	$\frac{Q_{L_{b_{\mathrm{OFF}}}}}{dT}$
DCML_c	$\frac{V_i}{(1-d)}$	$\frac{V_{C_a}}{(1-d)}=\frac{V_i}{(1-d)^2}$	$\frac{dV_{C_b}}{d_z}=\frac{dV_i}{d_z\,(1-d)^2}$	$\frac{i_{L_b}}{(1-d)}$	$\frac{di_{L_c}}{(1-d)}$	$\frac{v_{C_b} d\,(d+d_z)}{2L_c f}$

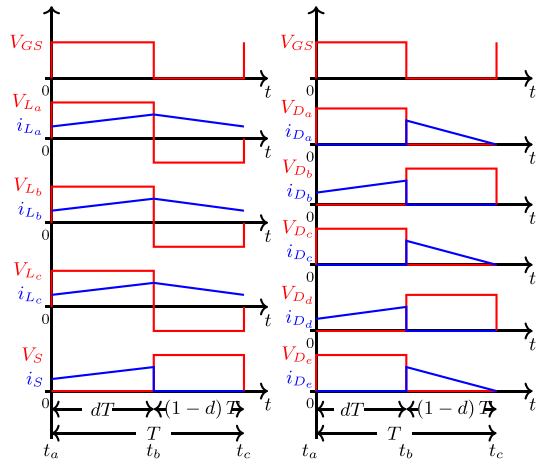

Fig. 3. Key waveforms of the proposed converter during CCM.

on inductors, which is given as

$$\int_{t_a}^{t_b} V_{L_{P\mathrm{ON}}}\mathrm{d}t+\int_{t_b}^{t_c} V_{L_{P\mathrm{OFF}}}\,(1-d)\,t=0, P=a,b,\,\&\,c. \quad (1)$$

By substituting the state equations in Table I into the (1), the capacitor voltages are calculated and presented in Table II.

Finally, the voltage gain of the proposed QBC-based buck–boost converter can be written from Table II as

$$M_{\mathrm{CCM}}=\frac{V_0}{V_i}=\frac{V_{C_c}}{V_i}=\frac{d}{(1-d)^3}. \quad (2)$$

With reference to (2), it can be stated that the presented converter is capable of working in boost mode as well as buck mode with duty ratio boundary of 0.3178.

2) Voltage Stress: From the operating mode in Fig. 1(c), it is discernible that the voltage stress across the switch S can be written as the combination of voltages across the capacitors C_b and C_c as

$$V_{DS}=V_{C_b}+V_0=\frac{V_0}{d}=\frac{V_i}{(1-d)^3}. \quad (3)$$

Similarly, the voltage stress across diodes D_b and D_d can be written as follows:

$$V_{D_b}=V_{C_b}-V_{C_a}=V_0\,(1-d)=\frac{dV_i}{(1-d)^2} \quad (4)$$

$$V_{D_d}=V_{C_c}=V_0=\frac{dV_i}{(1-d)^3}. \quad (5)$$

With the help of operating mode in Fig. 1(b), the remaining diode voltages can be written as follows:

$$V_{D_a}=V_{C_a}=\frac{V_0\,(1-d)^2}{d}=\frac{V_i}{(1-d)} \quad (6)$$

$$V_{D_c}=V_{C_b}=\frac{V_0\,(1-d)}{d}=\frac{V_i}{(1-d)^2} \quad (7)$$

$$V_{D_e}=V_{C_b}+V_0=\frac{V_0}{d}=\frac{V_i}{(1-d)^3}. \quad (8)$$

3) Current Stress: During mode1 means (switch-ON state), the switch current stress can be calculated as summation of three inductor currents: a) I_{L_a}; b) I_{L_b}; and c) I_{L_c}, which are flowing

through switch. The inductor currents can be found using amp–second balance of the capacitor currents during both modes, which is given as

$$\int_{t_a}^{t_b} I_{C_{P\mathrm{ON}}} \mathrm{d}t + \int_{t_b}^{t_c} I_{C_{P\mathrm{OFF}}} (1-d)\, t = 0, P = a, b, \,\&\, c. \quad (9)$$

With the consideration of resistive load, the load current i_0 can be written as V_0/R because the load capacitor C_c is discharging to the load R. Knowing the load current, the inductor currents I_{L_a}, I_{L_b}, and I_{L_c} are calculated with the aid of (9) and Table I and are presented in Table II.

From Table II, the relation between root mean square (rms) switch current and load current can be obtained as

$$I_{S_{\mathrm{rms}}} = (I_{L_a} + I_{L_b} + I_{L_c})\sqrt{d} = \frac{I_0}{(1-d)^3}\sqrt{d}. \quad (10)$$

Since, the inductor L_a current flows through diodes D_a and D_b in successive modes. By utilizing the Table II, the rms current of these diodes can be estimated as

$$I_{D_{a\mathrm{rms}}} = (I_{L_a})\sqrt{1-d} = \frac{dI_0}{(1-d)^3}\sqrt{1-d} \quad (11)$$

$$I_{D_{b\mathrm{rms}}} = (I_{L_a})\sqrt{d} = \frac{dI_0}{(1-d)^3}\sqrt{d}. \quad (12)$$

The rms current of diodes D_c and D_e can be estimated as currents I_{L_b} and I_{L_c}, respectively, flowing through those accordingly during mode2. So,

$$I_{D_{c\mathrm{rms}}} = (I_{L_b})\sqrt{1-d} = \frac{dI_0}{(1-d)^2}\sqrt{1-d} \quad (13)$$

$$I_{D_{e\mathrm{rms}}} = (I_{L_c})\sqrt{1-d} = \frac{I_0}{(1-d)}\sqrt{1-d}. \quad (14)$$

Finally, rms current through D_d can be evaluated as the combination of inductor currents I_{L_a} and I_{L_b} and expressed as

$$I_{D_{d\mathrm{rms}}} = (I_{L_a} + I_{L_b})\sqrt{d} = \frac{(2-d)\,dI_0}{(1-d)^3}\sqrt{d}. \quad (15)$$

B. DCM Analysis

1) DCML_a: This mode arises when the inductor current i_{L_a} becomes zero marked as t_x between the time intervals t_b and t_c shown in Fig. 4 where the diode D_a becomes reverse biased, as shown in Fig. 1(d), and the inductor voltage is also goes to zero. Hence, during the volt–second balance of inductor L_a will be having a time interval d_x instead of $1-d$ and remaining inductors follow the same as CCM. With the evaluation of volt–second balance via Table I, the outcomes are appended in Table II.

The charge balance on the capacitor C_a leads to (16), where the $Q_{L_{a_{\mathrm{OFF}}}}$ represents the charge delivered to the capacitor C_a by inductor L_a before undergoing the DCML_a state.

$$\frac{-i_{L_b}T + Q_{L_{a_{\mathrm{OFF}}}}}{T} = 0. \quad (16)$$

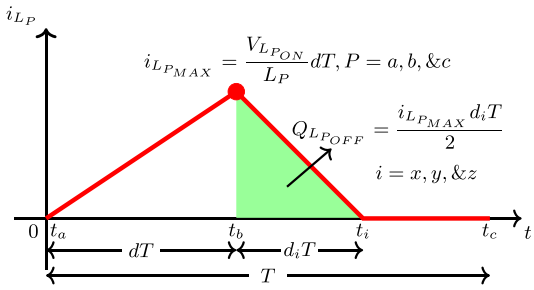

Fig. 4. Generalized discontinuous conduction mode (DCM) inductor current waveform.

By using $Q_{L_{a_{\mathrm{OFF}}}}$ in Fig. 4 and solving (16), the dimensionless parameter K_x can be written as

$$K_x = \frac{2L_a}{RT} = \frac{(1-d)^4 (d_x)^2}{(d+d_x)\,d}. \quad (17)$$

Rearranging the (17) results (18) as a quadratic equation shown as follows:

$$(1-d)^4 (d_x)^2 - K_x d d_x - K_x d^2 = 0. \quad (18)$$

Finding the roots of (18) leads the unknown d_x as

$$d_x = \frac{dK_x \cdot A}{2(1-d)^4}, \quad A = \left(1 + \sqrt{1 + \frac{4(1-d)^4}{K_x}}\right). \quad (19)$$

By replacing the d_x in Table II with (19), the DCML_a of converter states are resulted as follows:

$$\begin{cases} I_{L_a} = \dfrac{V_i d^2 \cdot A^2}{4R(1-d)^4} \\ I_{L_b} = \dfrac{V_i d^2 \cdot A}{2R(1-d)^4} \\ I_{L_c} = \dfrac{V_i dA}{2R\,(1-d)^3} \end{cases} \quad \begin{cases} V_{C_a} = \dfrac{V_i \cdot A}{2} \\ V_{C_b} = \dfrac{V_i \cdot A}{2\,(1-d)} \\ V_{C_c} = \dfrac{V_i dA}{2\,(1-d)^2} \end{cases} . \quad (20)$$

2) DCML_b: As DCML_a, this mode starts with the discontinuity in the inductor current i_{L_b} at time t_y. Furthermore, the diode D_c becomes reverse biased and makes no charging path to the capacitor C_c results i_{C_c} as zero, as shown in Fig. 1(e). As stated in DCML_a, only the volt–second balance of the inductor L_b changes, and the associated state equations and outcomes are furbished in Tables I and II, respectively. The amp–second balance on the capacitor C_b results as follows:

$$\frac{-i_{L_c}dT + Q_{L_{b_{\mathrm{OFF}}}}}{T} = 0. \quad (21)$$

By solving (21), the dimensionless parameter K_y can be obtained as

$$K_y = \frac{2L_b}{RT} = \frac{(1-d)^2 (d_y)^2}{(d+d_y)\,d}. \quad (22)$$

The unknown parameter d_y is obtained by rearranging the abovementioned equation as

$$(1-d)^2 (d_y)^2 - K_y d d_y - K_y d^2 = 0 \quad (23)$$

TABLE III
SUMMARY OF DCM VOLTAGE GAIN

Mode	DCM gain
DCML_a	$M_{\mathrm{DCM}L_a} = \dfrac{V_{C_c}}{V_i} = \dfrac{V_i dA}{2(1-d)^2}$
DCML_b	$M_{\mathrm{DCM}L_b} = \dfrac{V_{C_c}}{V_i} = \dfrac{V_i d \cdot B}{2(1-d)^2}$
DCML_c	$M_{\mathrm{DCM}L_c} = \dfrac{V_{C_c}}{V_i} = \dfrac{V_i d}{(1-d)^2 \cdot \sqrt{K_z}}$

$$d_y = \frac{dK_y \cdot B}{2(1-d)^2}, \quad B = \left(1 + \sqrt{1 + \frac{4(1-d)^2}{K_y}}\right). \tag{24}$$

Substituting the d_y in the expressions stated in Table II, the converter state variables are obtained as follows:

$$\begin{cases} I_{L_a} = \dfrac{V_i d^2 \cdot B^2}{4R(1-d)^4} \\ I_{L_b} = \dfrac{V_i d^2 \cdot B^2}{4R(1-d)^3} \\ I_{L_c} = \dfrac{V_i dB}{2R(1-d)^3} \end{cases} \begin{cases} V_{C_a} = \dfrac{V_i}{(1-d)} \\ V_{C_b} = \dfrac{V_i \cdot B}{2(1-d)} \\ V_{C_c} = \dfrac{V_i d \cdot B}{2(1-d)^2} \end{cases}. \tag{25}$$

3) DCML_c: As shown in Fig. 1(f), the diode D_e becomes reverse biased with the discontinuity of inductor current i_{L_c} at time t_z names the converter operating mode as DCML_c. The steady-state expression of capacitor voltages is obtained with volt–second balance of the inductors utilizing Table I and listed in Table II.

$$\frac{-i_0 T + Q_{L_{c\mathrm{OFF}}}}{T} = 0. \tag{26}$$

Solving the abovementioned equation results the dimensionless parameter K_z as

$$K_z = \frac{2L_c}{RT} = d_z^2. \tag{27}$$

Rearranging the (27) leads to

$$d_z^2 - K_z = 0. \tag{28}$$

Taking the positive root of the quadratic equation (27) gives the d_z as

$$d_z = \sqrt{K_z}. \tag{29}$$

By substituting the d_z in Table II results the average values of converter states in DCML_c as

$$\begin{cases} I_{L_a} = \dfrac{V_i d^2 \left(d + \sqrt{K_z}\right)}{R(1-d)^4 K_z} \\ I_{L_b} = \dfrac{V_i d^2 \left(d + \sqrt{K_z}\right)}{R(1-d)^3 K_z} \\ I_{L_c} = \dfrac{V_i d \left(d + \sqrt{K_z}\right)}{R(1-d)^2 K_z} \end{cases} \begin{cases} V_{C_a} = \dfrac{V_i}{(1-d)} \\ V_{C_b} = \dfrac{V_i}{(1-d)^2} \\ V_{C_c} = \dfrac{V_i d}{(1-d)^2 \cdot \sqrt{K_z}} \end{cases}. \tag{30}$$

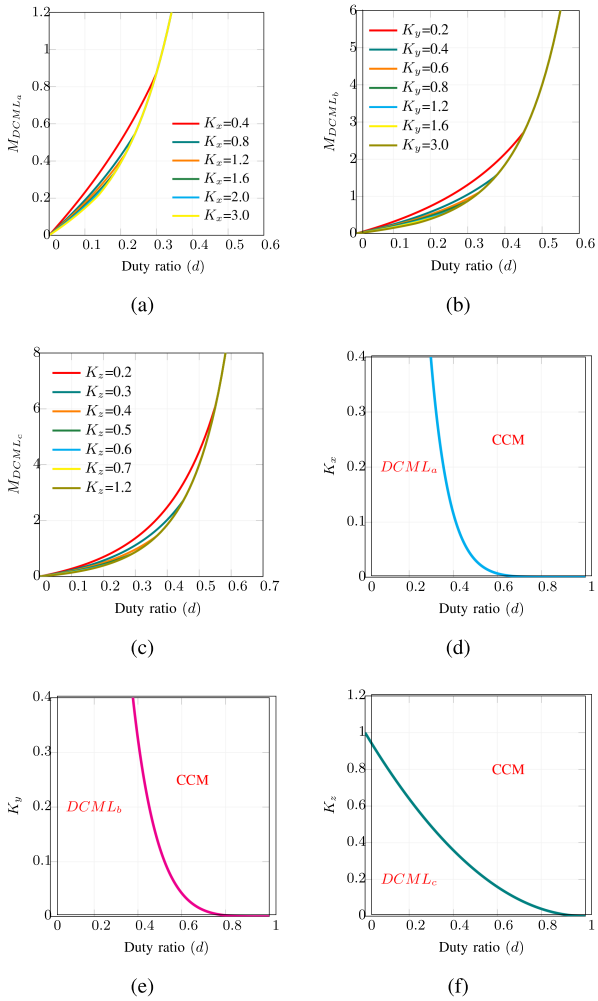

Fig. 5. DCM voltage gain versus duty ratio. (a) DCML_a. (b) DCML_b. (c) DCML_c. Boundary condition between the following terms. (d) CCM and DCML_a. (e) CCM and DCML_b. (f) CCM and DCML_c.

Finally, the voltage gain associated with DCM's are tabulated in Table III and graphically represented in Fig. 5(a)–(c) along with duty cycle, respectively.

C. Boundary Conduction Mode

The boundary conduction mode (BCM) of a converter is when the inductor current touches the zero exactly at the end of switching cycle. For example, as shown in Fig. 4, where the time t_x equals to t_c. Hence, by replacing the d_i, as shown in Fig. 4, with $(1-d)$ in (16), (21), and (28), the boundary condition between the CCM and the DCM's is resulted as given in Table IV. The graphical representation of all the BCM's, i.e., CCM→DCML_a, CCM→DCML_b, and CCM→DCML_c, are shown in Fig. 5(d)–(f).

IV. COMPARISON

A comprehensive comparative investigation of presented converter among other converters is facilitated in Table V to demonstrate its performance in CCM. The investigation considers various parameters, such as voltage gain, components count,

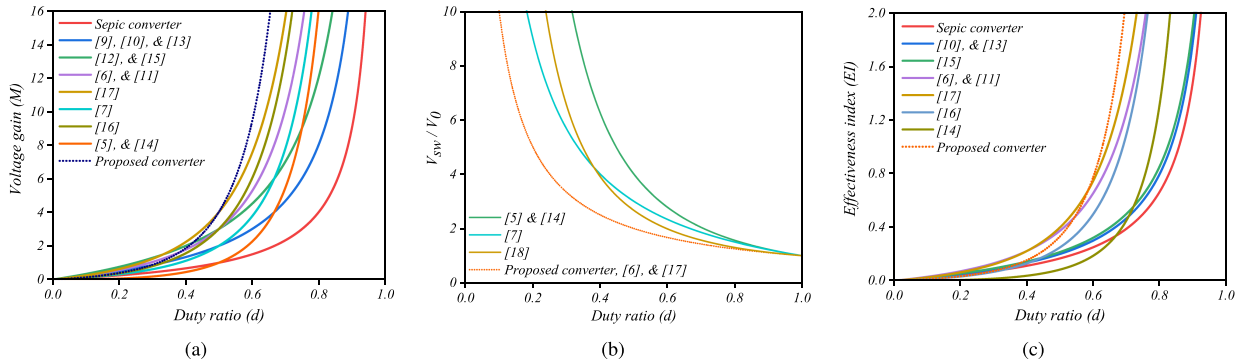

Fig. 6. Comparison of the following terms. (a) Voltage gain versus duty ratio. (b) V_{SW}/V_0 versus duty ratio. (c) EI versus duty ratio.

TABLE IV
CONDITION FOR THE BOUNDARY BETWEEN CCM AND DCM

Transition	Condition
CCM→DCML_a	$K_{a_{critical}} = \dfrac{(1-d)^6}{d}$
CCM→DCML_b	$K_{b_{critical}} = \dfrac{(1-d)^4}{d}$
CCM→DCML_c	$K_{c_{critical}} = (1-d)^2$

voltage stress across switch, output voltage polarity, and input current nature. As illustrated, converters presented in [5] and [12] having a switch in conjunction with input source. Furthermore, in [7], the input source is in conjunction with capacitor and switch, which makes the input current as continuous; but due to capacitive switching, an additional ripple content is injected, which is not admissible. Whereas, the proposed converter and the converters presented in [6], [15], and [14] are employed only an inductor in series with the input source. Hence, it leads to less ripple input source current. The input current ripple is quantified by finding the ripple factor of input current of each converter and given in Table V. The proposed converter is having a ripple factor of 0.057 due to its CIC, as in converter presented in [14]. Furthermore, considering the worst-case duty ratio as 0.8, the maximum voltage gain of the each converter is calculated and tabulated in Table V. It can be seen that the proposed converter delivers a voltage gain of 100, which is too high when compared with its par converters. In the aspects of device count, single switch, and CIC, the proposed converter exhibits noninverting output voltage polarity when compared to remaining converters. Furthermore, the proposed converter and converter presented in [15] exhibit same favorable features. But, the SEPIC-based converter [15] employs more device count when compared with the proposed converter, which leads to increase in size. Finally, the proposed converter is benefited with less switch voltage stress (i.e., duty ratio times) in comparison with its counterpart in [14], as shown in Fig. 6(b).

In addition, a graphical representation of voltage gain comparison with variation of duty cycle among proposed and refereed converters is presented in Fig. 6(a). Furthermore, the quantified voltage stress ratio on switch at a voltage gain of one for the proposed converter and its par converters is given in Table V. From the Table V, it can be seen that the proposed converter is having a reduction of 21.5% voltage stress ratio on switch and noninverted voltage polarity when compared with its par converter in [14]. Furthermore, the converter in [15] is having better reduction in voltage stress ratio with limited maximum voltage gain of 12, which is 12% of the proposed converter maximum voltage gain. In addition, the converter in [15] utilized four inductors and a total component count of 14, which is higher than the proposed converter component count. Basically, the proposed converter provides amenable degree of freedom in terms of duty cycle for high voltage gain in step-up mode instead of going for extreme duty cycles. Furthermore, it exhibits better buck gain when compared with the converters presented in [12] and [15]. Eventually, the presented converter displays remarkable performance with relative converters, as presented in Table V. Finally, an effectiveness index (EI) is utilized to evaluate the power density of the converter, which is illustrated for the proposed converter along with the other converters shown in Fig. 6(c), where EI is the ratio of the voltage gain to the number of utilized elements.

V. EXPERIMENTAL RESULTS

To validate the theoretical analysis provided in the CCM operating mode, a laboratory prototype is developed and tested with 100 W in boost mode and 30 W in buck mode. The component values of inductor and capacitor are tabulated in Table VI along with its design equations where the duty ratio and the ripple current are chosen as 0.5 and 20% of respective inductor current, respectively. Furthermore, the semiconductor components that are utilized to build the converter prototype are detailed in Table VII and its converter part converter presented in [14] are detailed in Table VIII. The experimental verification is done at the full load with input voltage of 30 V, as specified in Table VII.

A texas instruments (TI)-based digital signal processor (DSP) TMS320F28379D is utilized to generate the driving signal to the metal oxide semiconductor field effect transistor (MOSFET) along with the driver circuit associated with the IC TLP350. In addition, voltage and current probes of N2863B and YOKOGAWA 50 MHz/30 ARMS and oscilloscope of DSO-X-2024 A

TABLE V
COMPARISON BETWEEN PROPOSED CONVERTER AND OTHER CONVERTERS

Converter in	Voltage gain	Component count					V_{SW}	V_{SW}/V_{in} @ $M_{CCM}=1$	O/P voltage polarity	CIC	RF @ $M_{CCM}=1$	d @ $M_{CCM}=1$	$M_{CCM_{max}}$ @ $d=0.8$
		S	L	C	D	T							
[5]	$\frac{d^2}{(1-d)^2}$	2	2	2	2	8	$\frac{V_0}{d^2}$	4	Non-inverted	No	1.0033	0.5	16
[6]	$\frac{d(2-d)}{(1-d)^2}$	2	2	2	2	8	$\frac{V_0}{d}$	3.415	Inverted	Yes	0.5041	0.2928	24
[7]	$\frac{d}{(1-d)^2}$	2	2	2	2	8	$\frac{V_0(2-d)}{d}$	4.2369	Inverted	Yes	0.4033	0.3819	20
[16]	$\frac{d(1+d)}{(1-d)^2}$	2	3	4	3	12	$\frac{V_0}{d(1+d)}$	2.2528	Non-inverted	Yes	0.057	0.3333	36
[17]	$\frac{2d}{(1-d)^2}$	2	2	3	3	10	$\frac{V_0}{d}$	3.7327	Inverted	Yes	0.057	0.2679	40
[12]	$\frac{3d}{1-d}$	1	3	5	3	12	$\frac{V_0}{3d}$	1.333	Inverted	No	1.7359	0.25	12
[15]	$\frac{3d}{1-d}$	1	4	6	3	14	$\frac{V_0}{3d}$	1.333	Non-inverted	Yes	0.057	0.25	12
[11]	$\frac{d(2-d)}{(1-d)^2}$	1	2	2	3	8	$\frac{V_0}{d(2-d)}$	2	Inverted	No	1.5578	0.2928	24
[9]	$\frac{2d}{1-d}$	1	2	3	2	8	$\frac{V_0}{2d}$	1.5	Non-inverted	No	1.4177	0.3333	8
[10]	$\frac{2d}{1-d}$	1	3	4	2	10	$\frac{V_0}{2d}$	1.5	Non-inverted	No	1.4177	0.3333	8
[13]	$\frac{2d}{1-d}$	1	3	4	2	10	$\frac{V_0}{2d}$	1.5	Inverted	Yes	0.057	0.3333	8
[14]	$\frac{d^2}{(1-d)^2}$	1	3	3	5	12	$\frac{V_0}{d^2}$	4	Inverted	Yes	0.057	0.5	16
[18]	$\frac{d^2(2-d)}{(1-d)^2}$	1	3	3	5	12	$\frac{V_0}{d^2(2-d)}$	3.24	Inverted	Yes	0.2066	0.445	19.2
Proposed	$\frac{d}{(1-d)^3}$	1	3	5	3	12	$\frac{V_0}{d}$	3.14	Non-inverted	Yes	0.057	0.3178	100

Note: S : Switches; *L* : Inductors; *C* : Capacitors; *D* : Diodes; *T* : Total number of components; RF: Ripple factor.

TABLE VI
INDUCTOR AND CAPACITOR DESIGN VALUES

Parameter	Symbol	Value
Inductors	L_a	$\frac{V_i}{\Delta i_{L_a}} dT_s = \frac{(1-d)^3 V_0}{\Delta i_{L_a} f_s} = 450\mu H$
	L_b	$\frac{V_{C_a}}{\Delta i_{L_b}} dT_s = \frac{(1-d)^2 V_0}{\Delta i_{L_b} f_s} = 1.8mH$
	L_c	$\frac{V_{C_b}}{\Delta i_{L_b}} dT_s = \frac{(1-d) V_0}{\Delta i_{L_c} f_s} = 3.6mH$
Capacitors	C_a	$\frac{Q_{C_a}}{\Delta V_{C_a}} = \frac{V_0 d^2}{2\Delta v_{C_a}(1-d)^2 R f_s} = 47\mu F$
	C_b	$\frac{Q_{C_b}}{\Delta V_{C_b}} = \frac{V_0 d}{2\Delta v_{C_b}(1-d) R f_s} = 47\mu F$
	C_c	$\frac{Q_{C_c}}{\Delta V_{C_c}} = \frac{V_0 d}{\Delta v_{C_c} R f_s} = 100\mu F$

TABLE VII
COMPONENTS AND PARAMETER SPECIFICATIONS OF THE PROPOSED CONVERTER HARDWARE PROTOTYPE

Parameter	Symbol	Details	
		Boost mode	Buck mode
Input voltage	V_i	30V	30V
Output power	P_0	100W	30W
Voltage gain	M	4	0.875
Duty ratio	d	0.5	0.3
Switch	S	IRFP460	
Switching frequency	f	50 kHz	
Diodes	D_a and D_b	NTSV20U100CTG	
	D_c, D_d and D_e	MBR20200CTG	

and APLAB series L3230 power supply are used to perform the experiment and capture the key waveforms of the converter. Furthermore, a TLP350 photocoupler is utilized to drive the MOSFET by generating an isolated driving signal.

The proposed buck–boost converter is tested at a voltage gain of four in boost mode and 0.875 in buck mode with the respected duty ratio d, which is shown in Fig. 5(a). The experimental results of the converter in both boost and buck modes are shown in Fig. 7. It is worthwhile to mention that the experimentally measured and theoretical values are moderately different due to the assumptions considered while carrying out the theoretical analysis.

The input current (current flowing the inductor L_a) and the voltage stress across the power switch are shown in Fig. 7(a), where the average value of current I_{L_a} is recorded as 1.2 A is slightly greater than the theoretical value of average current ($I_{L_a} = 1$ A). Fig. 7(b) shows the current through inductor L_b and the voltage stress on the D_a. It can be seen that the current I_{L_b} is about 0.75 A and the blocking voltage on diode D_a is about 43 V. The blocking voltage on the diode D_b shown in Fig. 7(c) is

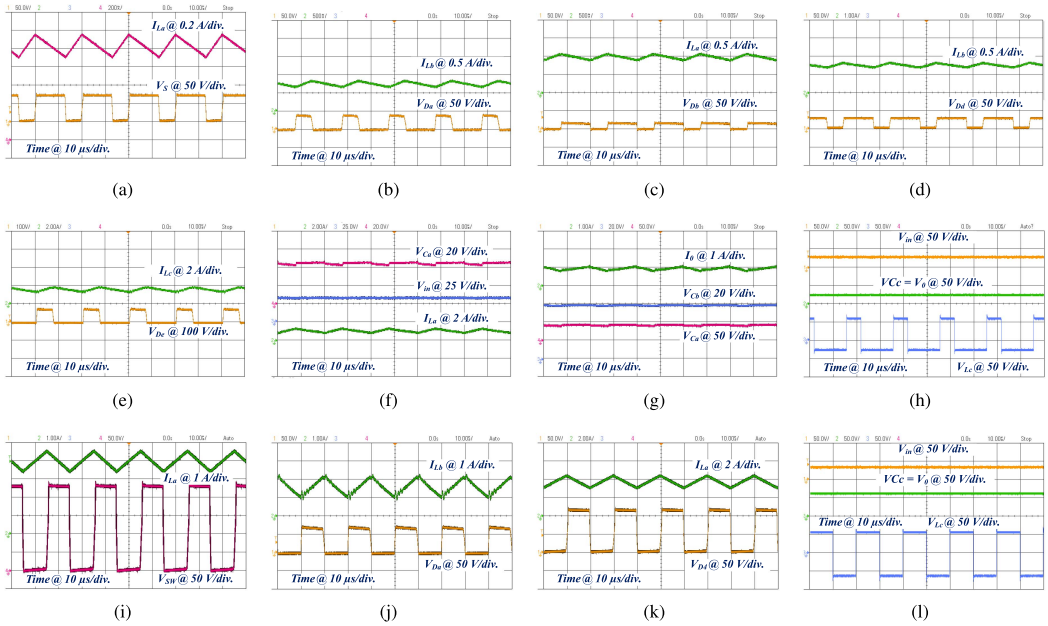

Fig. 7. Experimental results in the Buck mode. (a) I_{L_a} and V_S. (b) I_{L_b} and V_{D_a}. (c) I_{L_a} and V_{D_b}. (d) I_{L_b} and V_{D_d}. (e) I_{L_c} and V_{D_e}. (f) V_{C_a}, V_{in}, and I_{L_b}. (g) I_0, V_{C_a}, and V_{C_b}. (h) V_{in}, V_0, and V_{L_c}. Experimental results in the Boost mode. (i) I_{L_a} and V_{SW}. (j) I_{L_b} and V_{D_a}. (k) I_{L_a} and V_{D_d}. (l) V_{in}, V_0, and V_{L_c}.

TABLE VIII
COMPONENTS AND PARAMETER SPECIFICATIONS OF CONVERTER HARDWARE PROTOTYPE IN [14]

Parameter	Symbol	Details	
		Boost mode	Buck mode
Input voltage	V_i	20V	20V
Output power	P_0	33.75W	1.48W
Voltage gain	M	2.25	0.445
Switch	S	IRFP260N	
Switching frequency	f	40 kHz	
Diodes	D_a -D_e	DSEP8-06A	

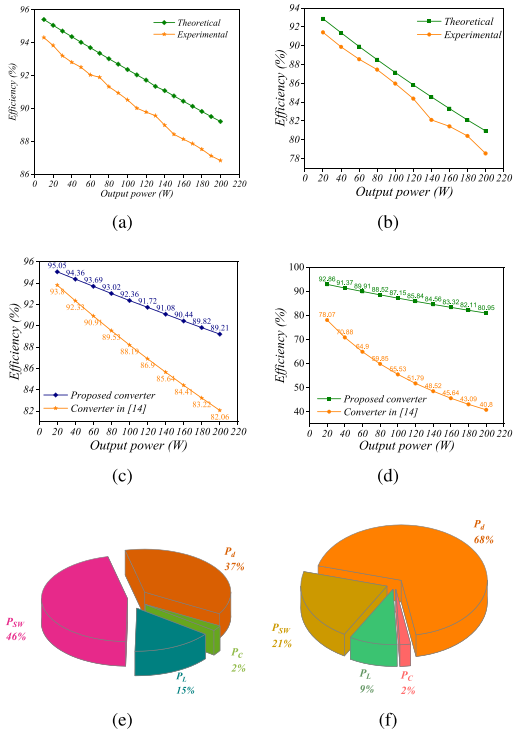

Fig. 8. Comparison of efficiency between theoretical and experimental: (a) Boost mode; (b) Buck mode. Efficiency versus output power: (c) Boost mode; (d) Buck mode. Power loss distribution: (e) Boost mode; (f) Buck mode.

about 20 V, which is approximately equal to the stated theoretical value. Fig. 7(d) shows the voltage stress on the diode D_d, which is about 27 V. The current through the inductor L_c and voltage stress across the diode D_e are shown in Fig. 7(e) with average current of 1.8 A and blocking voltage of 88 V, which are around the theoretical values. The input voltage and voltage across the capacitor C_a along with input current I_{L_a} are shown in Fig. 7(f) where with the applied input voltage of 30 V at the operated duty ratio results the voltage V_{C_a} around 42 V. Furthermore, the intermediate capacitor C_b voltage V_{C_b} is shown in Fig. 7(g) along with output current and voltage V_{C_a}. The voltage across the capacitor is resulted around 60 V, which is in par with the theoretical voltage. Finally, the output voltage $V_0 = V_{C_c}$ and voltage across the inductor V_{L_c} are shown in Fig. 7(h) along with the input voltage. The measured average values of 25.8 V for an input voltage of 30 V is close to the theoretical values presented in Section III. Furthermore, the experimental recorded waveforms of the proposed converter during boost mode are shown in Fig. 7(i)(l), respectively.

Finally, the efficiency of the proposed converter using (31) shown at the top of this page, is compared with its contemporary converter in [14] by varying output power. From Fig. 8(c) and

$$\eta = \frac{1}{1+\frac{r_{DS_{ON}}}{R}\frac{d}{(1-d)^6}+\frac{r_{L_a}}{R}\frac{d^2}{(1-d)^6}+\frac{r_{L_b}}{R}\frac{d^2}{(1-d)^4}+\frac{r_{L_c}}{R}\frac{1}{(1-d)^2}+\frac{\sqrt{d}\left(3d-d^2\right)+\sqrt{1-d}}{(1-d)^3}\frac{V_F}{V_0}+\frac{0.5f_s(t_f+t_r)}{(1-d)^3}+\frac{r_{C_a}}{R}\frac{d^3}{(1-d)^5}+\frac{r_{C_b}}{R}\frac{1}{(1-d)^3}+\frac{r_{C_c}}{R}\frac{1}{1-d}} \times 100\% \quad (31)$$

8(d), it can be seen that the proposed converter delivers better efficiency in both boost and buck modes in comparison with converter in [14] with same number of components. The loss breakdown of the proposed converter in both boost and buck modes is shown in Fig. 8(c) and 8(d), respectively. Furthermore, the efficiency of the proposed converter is measured and compared with theoretical calculations, as shown in Fig. 8(a) and 8(b), for both buck and boost modes of operation.

VI. Conclusion

In this article, a new single-switch CIC nonisolated buck–boost converter with wide voltage conversion ratio and single switch was presented. The steady-state analysis of the converter in both CCM and named DCM's were discussed in detail and presented with respective voltage conversion ratios. In addition, a detailed comparative analysis was done among the proposed and its contemporary converters in voltage gain, voltage stress ratio, and EI aspects. From the comparison, it can be inferred that the proposed converter results better voltage gain with optimum component count as well as lower voltage stress. Furthermore, the EI comparison confirms the prominence of the proposed converter over its contemporary converters. Finally, the prototype of the proposed buck–boost converter was fabricated and tested in laboratory for both buck and boost modes of operation. The experimental results promise the validation of the converter theoretical analysis in CCM.

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