A Method to Derive the Coupling Thermal Resistances at Junction-to-Case Level in Multichip Power Modules

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***Abstract*—A method to derive the junction-to-case level coupling thermal resistances among paralleling chips in the multichip semiconductor power module has been proposed in this article. It is revealed that the traditional structure function methodology (SFM), which is developed for analyzing the self-heating effect of the driving-point chip, cannot be applied directly in the thermal coupling analysis, where the influence of the driving-point chip on the neighboring acceptor chip is concerned. This article shows that by combining the traditional SFM with the frequency-domain analysis (FDA), the effective separation points between the module case and the external cooling setup can be identified in both time and frequency domains, which correspond to the characteristic frequency points in the complex loci of the thermal impedance curves. By extracting the amplitudes at the characteristic frequencies from the complex loci in the FDA, the junction-to-case level coupling thermal resistances can be derived. Both simulation and experimental study have been carried out to verify the concept. The agreement between the two justifies the proposed method.**

***Index Terms*—Junction-to-case level, semiconductor chips, semiconductor power modules, thermal coupling.**

I. Introduction

In POWER electronic applications of the semiconductor chips, such as the insulated-gate bipolar transistors (IGBTs) [1], metal oxide semiconductor field-effect transistors [2], fast recovery diodes (FRDs) [3], and GaN high electron mobility transistors [4], it is a common technology to enclose a number of identical chips in parallel to increase the current rating of single module. With the rapid development of the chip technology, the semiconductor power modules become more and more compact. The shrinking of the packaging size coupled with the growing chip power density may increase the semiconductor chip thermal coupling during operation, which will lead to thermal imbalance or overheating of chips. Thus, it is of practical importance to characterize the thermal coupling behavior among paralleling chips. It is well known that the junction temperature of chips in a multichip power module during operation can be expressed as [5]

$$T_j^n = \sum_{m=1}^{N} P_{\text{loss}}^m \cdot R_{ja}^{n,m} + T_a \tag{1}$$

where N is the total number of chips in consideration. T_j^n and T_a are the junction temperature of chip n ($n = 1 \ldots N$) and the ambient temperature of the cooling boundary condition, respectively. j and a refer to the semiconductor junction and ambient, respectively. P_{loss}^m is the power loss of chip m ($m = 1 \ldots N$). $R_{ja}^{n,n}$ is the junction-to-ambient level self-heating thermal resistance, which characterizes the temperature variation of chip n due to its own power loss. For $m \neq n$, $R_{ja}^{n,m}$ represents the junction-to-ambient level coupling thermal resistance from chip m to n, which characterizes the influence of power loss in the driving-point chip m on the acceptor chip n. The subscript a means that $R_{ja}^{n,n}$ and $R_{ja}^{n,m}$ take the ambient as the temperature reference point. In the field operation of a power module, both $R_{ja}^{n,n}$ and $R_{ja}^{n,m}$ are essential parameters to determine the thermal uniformity characteristic among parallel chips. A number of previous publications have been elaborated to derive and utilize (1), to characterize the thermal resistances from the chip junction to ambient. In [6], the $R_{ja}^{n,n}$ and $R_{ja}^{n,m}$ values for 24 IGBT chips and 12 FRD chips were derived, by assuming a homogeneous heat transfer coefficient at the module baseplate, to emulate the external cooling boundary condition. Yu et al. [7] developed a compact thermal network model by using the simulated $R_{ja}^{n,n}$ and $R_{ja}^{n,m}$ values under constant ambient cooling temperature. In [8], the transient $R_{ja}^{n,n}$ and $R_{ja}^{n,m}$ matrix was tested under constant ambient temperature and reconstructed to produce a multiport thermal coupling model for circuit simulation. A comprehensive test algorithm was also reported in [9] for efficient measurement of the thermal coupling effects on a multichip light-emitting diode module, by taking the constant temperature of the heat sink as reference. It was also shown

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in [10] that the thermal coupling within power modules could influence the lifetime and failure mode during power cycling test. While the previous work gave a comprehensive study of the thermal coupling in multichip modules, the adopted thermal models took the ambient temperature as reference nodes. In other words, the characterization of the modules was strongly dependent on the external cooling boundaries, which could not describe the intrinsic thermal properties of the modules under consideration.

In industrial practice, the semiconductor power modules are usually supplied with their own thermal resistances in the datasheet, which tells the users about the junction-to-case level thermal characteristics. Here, case refers to the surface of the module to be in contact with the external cooling setup. The junction-to-case level thermal resistance is essential as it provides an intrinsic parameter about the thermal performance of the module. Such convention is widely applied to single-chip packaging structures. However, for the multichip module packaging, the thermal resistance value per switch (there are usually several chips connected in parallel for each switch) presents inadequate information. This is mainly due to two reasons. First, the thermal resistance specified per switch cannot disclose the thermal distribution among the paralleling chips. Second, the heat dissipation in a multichip module involves considerable thermal coupling behavior among paralleling chips, which cannot be described by single thermal resistance value. As a matter of fact, the commonly used JEDEC JESD51-14 standard [11] only specifies the measurement method for single chip packaging, without addressing the junction-to-case level thermal resistance measurements in the multichip modules.

To accurately describe the thermal performance of a power module and ensure a fair as well as repeatable comparison among modules from different suppliers, the junction-to-case level thermal resistances can be defined as follows:

$$T_j^n = \sum_{m=1}^{N} P_{\text{loss}}^m \cdot R_{jc}^{n,m} + T_c \tag{2}$$

where $R_{jc}^{n,n}$ $(n = 1 \ldots N)$ is the junction-to-case level self-heating thermal resistance, which characterizes the temperature variation of the chip due to its own power loss at module level. For $m \neq n$, $R_{jc}^{n,m}$ $(m = 1 \ldots N)$ represents the junction-to-case level coupling thermal resistance from chip m to n, which characterizes the influence of power loss in the driving-point chip on the acceptor chip. T_c is the case temperature of the module. The subscript c means that $R_{jc}^{n,n}$ and $R_{jc}^{n,m}$ takes the case temperature as the reference. It has to be clarified that, for the power electronics community, the definition of T_c as well as T_j^n is to some extend ambiguous since the temperature distribution is uneven on either the case surface or the semiconductor chip surface [12]. It is defined in this study that T_c and T_j^n are the average temperature values on the case surface and in the semiconductor active area, respectively.

The definition and derivation of the $R_{jc}^{n,n}$ and $R_{jc}^{n,m}$ are essential. First, instead of the commonly used thermal resistance value per switch in the module datasheet, they differentiate the self-heating and coupling thermal resistances for individual chip inside a switch. In fact, it has already been suggested by researchers that a chip-by-chip thermal test should be performed to fully characterize a multichip module [13]. Second, the elements in the $R_{jc}^{n,m}$ matrix provide direct and essential indication of the potential chip thermal uniformity performance. Third, the derived thermal resistance information is important to establish a junction-to-case level thermal network corresponding to the physical structure of the module packaging itself, with weak dependency on the cooling boundary conditions [14], [15]. The derived thermal network can be used as the intrinsic dataset of the module packaging itself and conveniently connected to external thermal network of the cooling structure, to enable electro-thermal simulation from chip scale to system level [16].

It is well known that $R_{jc}^{n,n}$, which is the self-heating thermal resistance characterizing the thermal response of individual chip to its own power loss, can be derived from the structure function methodology (SFM) [17], [18] based on the assumption of unidirectional thermal propagation. However, $R_{jc}^{n,m}$ $(m \neq n)$, which characterizes the thermal response of individual chip to the power loss of its neighbor, cannot be derived directly from the SFM. This is because the definition of $R_{jc}^{n,m}$ violates the assumption of the SFM that the T_j^n variation of chip n is caused by power loss of itself (P_{loss}^n). The traditional SFM is unsuitable for $R_{jc}^{n,m}$ derivation, which could amount to 21.9% of the $R_{jc}^{n,n}$ in our case and affect the T_j^n evaluation, as shown in (2). It is, thus, essential to develop a proper method for deriving the $R_{jc}^{n,m}$ values, to address the challenge of thermal coupling analysis at junction-to-case level.

The new contribution of this article can be summarized as two parts. On the one hand, the limitation of the SFM for deriving $R_{jc}^{n,m}$ $(m \neq n)$ is revealed with a simple but representative case study, by both simulation and experimental test. On the other hand, a new method based on the combination of SFM and frequency-domain analysis (FDA) is proposed as well as verified. In this new approach, the structure functions and complex loci of the junction-to-ambient self-heating thermal impedances ($Z_{ja}^{n,n}$) with different thermal interface materials (TIMs) are analyzed jointly to determine the separation point between the module case and external cooling setup. By extracting the characteristic excitation frequency at the separation point in the frequency domain, the value of $R_{jc}^{n,m}$ can be derived from the $Z_{ja}^{n,m}$ loci. To verify this method, a simplified IGBT power module is prepared and evaluated. The agreement between the simulation and experiment justifies the proposed method.

II. Modeling and Simulation

As a representative example, the previously reported 3.3-kV/450-A IGBT power module for the high-speed railway traction inverter has been selected, where the detailed internal layout has been elaborated in [19]. The structure, as shown in Fig. 1, represents a simplified version with three IGBT chips and three FRDs chips mounted on one substrate while removing the other substrates, bonding wires, power terminals, gels, and frames of the full module. The six chips are soldered on the AlN substrate with SnPbAg solder. The AlN substrate with copper brazing on both sides is soldered on the AlSiC baseplate with SnPb solder. The baseplate is mounted on the heat sink with

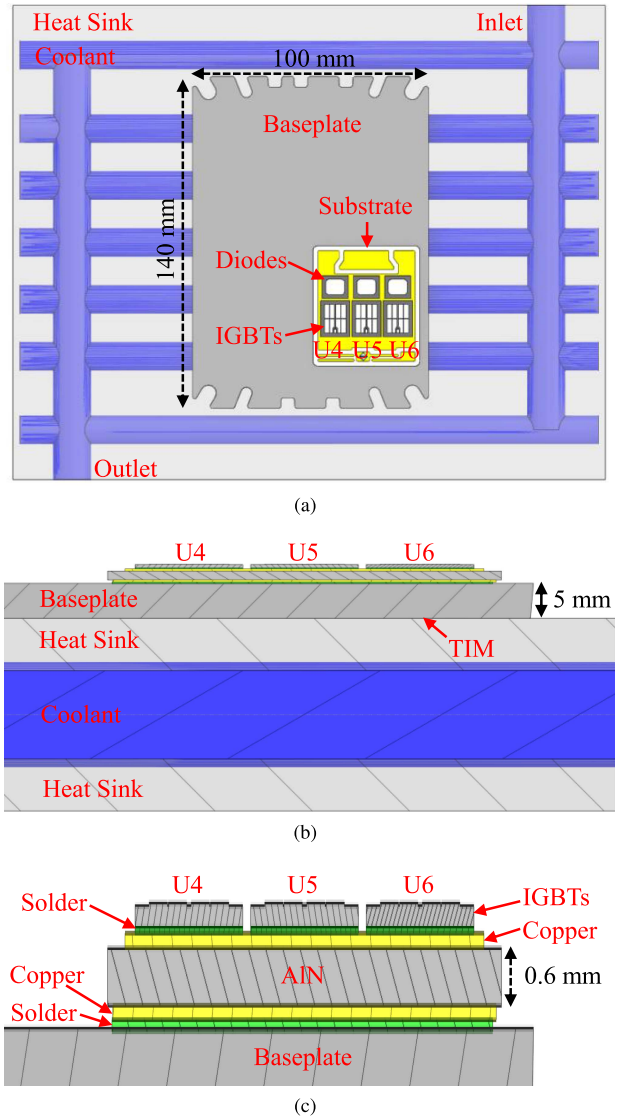


Fig. 1. Simplified module sample and the corresponding cooling structure. (a) Top view. (b) Cross-sectional view. (c) Cross-sectional view from junction to case (not to scale).

screws. To enhance the thermal conduction, a TIM is usually applied between the two. The generated heat is mainly dissipated from the chip junction to the heat sink in the vertical direction. The heat sink is designed according to the fashion as being used in the railcar traction inverters. The three IGBT chips are denoted as $U4$, $U5$, and $U6$, respectively, which form a multichip system in this study. The thermal interaction between any two chips in a multichip system can be investigated in the same fashion as governed by the superposition law specified in (1) and (2). From (1) and (2), by making P^m_{loss} $(m \neq n)$ as 0

$$R^{n,n}_{ja} = \frac{T^{n,n}_j - T_a}{P^n_{\text{loss}}} \tag{3}$$

and

$$R^{n,n}_{jc} = \frac{T^{n,n}_j - T_c}{P^n_{\text{loss}}} \tag{4}$$

where $T^{n,n}_j$ is the steady-state junction temperature of chip n by applying the driving power of P^n_{loss} only. T_a and T_c are the average temperature values at the cooling water inlet interface and the bottom surface of the module baseplate, respectively. $R^{n,n}_{ja}$ and $R^{n,n}_{jc}$ characterize the thermal behavior of the chip n due to the self-heating effect during its operation. The $R^{n,m}_{ja}$ and $R^{n,m}_{jc}$ can be obtained by making P^n_{loss} as 0 $(n \neq m)$ in (1) and (2)

$$R^{n,m}_{ja} = \frac{T^{n,m}_j - T_a}{P^m_{\text{loss}}} \tag{5}$$

and

$$R^{n,m}_{jc} = \frac{T^{n,m}_j - T_c}{P^m_{\text{loss}}} \tag{6}$$

where $T^{n,m}_j$ is the junction temperature of acceptor chip n by applying the heating power of P^m_{loss} on the driving-point chip m. $R^{n,m}_{ja}$ and $R^{n,m}_{jc}$ characterize the coupling effect on chip n from m.

Both $R^{n,n}_{jc}$ and $R^{n,m}_{jc}$ are the inherent parameters to describe the thermal behavior of the chips inside a semiconductor power module, with reference to the T_c of the module itself. Only with the information of both $R^{n,n}_{jc}$ and $R^{n,m}_{jc}$ for each chip can the thermal distribution be predicted by (2), which are essential factors for the long-term reliability design of the power modules. Also, in the scenario of a copack module including both the IGBT and diode chips, the $R^{n,m}_{jc}$ values provide important information about the thermal coupling between these two types of chips, for preventing thermal runaway and optimization of the control algorithm. What is more, the thermal coupling parameters among the chips inside a power module are indispensable parameters for constructing high-fidelity thermal networks, which enable the electrothermal coupling study of the power electronic systems.

The direct implementation of (4) and (6) in the derivation of $R^{n,n}_{jc}$ and $R^{n,m}_{jc}$ is challenging as the determination of T_c in simulation or experimental test is difficult. As an alternative, $R^{n,n}_{jc}$ can be derived by the SFM, described in [18]. To do so, the system, as shown in Fig. 1, is modeled in Ansys Icepak [20], which solves the heat conduction and Navier–Stokes equations by the finite volume method, with consideration of the fluid turbulence. To ensure simulation convergence with the nonlinear and coupled equations, a number of iterations within the solution loop are performed until the self-consistent physical fields are derived. In the simulation of this study, the material properties follow the values, as given in [21]. The power loss is applied to the part of the chip body known as active area, whereas the edge terminal structure is considered as passive. Inside the heat sink, as shown in Fig. 1(b), a type of liquid formed by equal mixture of the ethylene glycol and deionized water is adopted for cooling, with fixed flow rate of 13 L/min and inlet temperature of 35 °C. This resembles the cooling condition in the railway traction inverters.

For $R^{n,n}_{jc}$ derivation, taking chip $U5$ in Fig. 1 as an example, two simulation runs with different types of TIMs can be carried out to derive two junction-to-ambient thermal impedance $(Z^{U5,U5}_{ja})$ curves, which depict the time-dependent variations of $R^{U5,U5}_{ja}$. In each of the simulation runs with Ansys Icepak, a

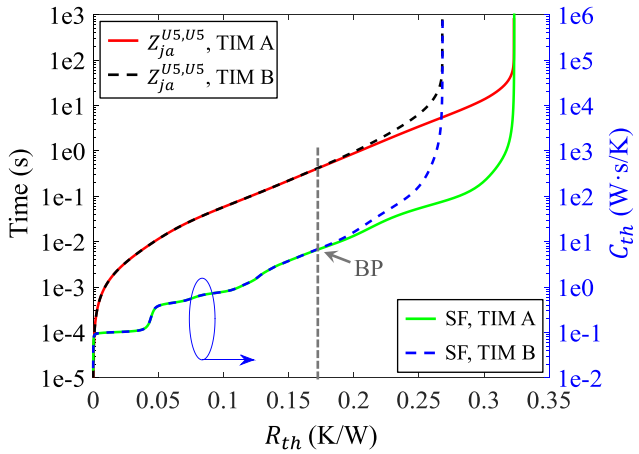


Fig. 2. Simulated $Z_{ja}^{U5,U5}$ curves and the corresponding structure function curves of the chip U5 for two types of TIMs.

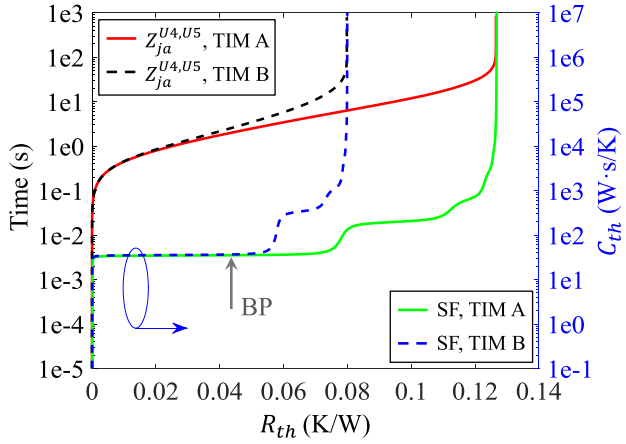


Fig. 3. Simulated $Z_{ja}^{U4,U5}$ curves and the corresponding structure function curves for two types of TIMs.

constant power of P_{loss}^{U5} is applied on chip $U5$, while the time-dependent $T_j^{U5,U5}$ can be recorded. The $T_j^{U5,U5}$ value is time dependent before the steady state because of the thermal capacitances in the subsequent layers of the thermal dissipation path. Using (3), the $Z_{ja}^{U5,U5}$ curves are derived, as shown in Fig. 2. The two curves correspond to two types of TIMs, namely graphite (TIM A) and thermal grease (TIM B), with different thermal conductivities and capacities. Such pair of TIMs are chosen according to the JEDEC JESD51-14 standard, which specifies that a dry (graphite in our case) and a wet (thermal grease in our case) TIM should be used, to ensure a clear separation of the derived thermal impedance curves (see Fig. 2). The methodology described in this article is still valid for other TIM pairs as long as the abovementioned specification is fulfilled. The $Z_{ja}^{U5,U5}$ curves are then transformed into structure function representations, as also shown in Fig. 2, which depict the variation of the cumulative thermal capacitance (C_{th}) with resistance (R_{th}) from the semiconductor junction to the ambient cooling boundary. It can be seen that C_{th} increases with R_{th} until the curves ramp straight upward, representing the external cooling boundaries. The variation of the structure functions reveals the thermal properties of different layers in the thermal dissipation path of the chips. For example, the horizontal section in the $R_{\text{th}} \leq 0.05$ K/W region represents the chip soldering layer [see Fig. 1(c)] where R_{th} increases but C_{th} stays at the same level. The sudden increase of C_{th} in the region of $R_{\text{th}} = 0.05$ K/W depicts the behavior of the top copper layer on the substrate. Since the variation of the structure functions corresponds to the physical structures and material properties of the heat dissipation path, the bifurcation point (BP) of the two sets of structure functions [11] represents an abrupt change of the material properties, which is induced by the different TIM materials used. Thus, the BP is taken as the interface between the power module and the TIMs. The BP in this study is identified as the location where the C_{th} amplitudes of the two structure function curves differ by 2%, given the same R_{th} value. By extracting the thermal resistance value at the BP, the $R_{jc}^{U5,U5}$ value is derived to be 0.170 K/W, as shown in Fig. 2.

Although the abovementioned method has been proven effective in the calculation of $R_{jc}^{n,n}$, it meets inherent difficulty in the derivation of $R_{jc}^{n,m}$ $(m \neq n)$. This is because the SFM is used for analyzing the self-heating effect, where the P_{loss}^{n} on chip n itself is considered. From the definition of $R_{ja}^{n,m}$ and $R_{jc}^{n,m}$ in (5) and (6), in the coupling analysis $(m \neq n)$, chip n is not the driving point where the heating power is applied. Thus, the structure function of $Z_{ja}^{n,m}$ is physically meaningless. What is more, $Z_{ja}^{n,m}$ describes the effect of heat propagation in both the vertical and horizontal directions, which violates the theoretical basis of unidirectional propagation assumption in the SFM. Taking chips $U4$ and $U5$ for example, Fig. 3 shows the simulated $Z_{ja}^{U4,U5}$ curves of the thermal structure in Fig. 1 with the aforementioned two TIMs. In the simulation, only heating power of P_{loss}^{U5} is applied to chip $U5$ while the temperature response of chip $U4$ is recorded to derive the $Z_{ja}^{U4,U5}$ results according to (5). The corresponding structure function curves are also shown in Fig. 3. It can be seen that as the R_{th} increases, C_{th} stays almost at the same level until the two curves branch out directly. The extensive horizontal part and the following section of the structure functions possess little useful information to indicate the interface between the module baseplate and the TIMs. The identified BP point in Fig. 3 cannot be used for indicating the corresponding $R_{jc}^{U4,U5}$ value in this scenario. In other words, the traditional SFM is unsuitable for deriving $R_{jc}^{n,m}$ values.

To solve this problem, a new approach is proposed based on the combination of SFM and the aforementioned FDA. The FDA has been introduced into self-heating characterization of power semiconductor chips for two decades [22]. However, due to the exceptional performance of the SFM in single-chip packaging thermal analysis, FDA is not widely adopted. The frequency-domain representations of the transient $Z_{ja}^{n,n}$ and $Z_{ja}^{n,m}$ curves have also been discussed in a number of literature [23], [24], [25], but the possibility of deriving the $R_{jc}^{n,m}$ values has not been revealed. In this work, we show the potential of utilizing such analysis in deriving the $R_{jc}^{n,m}$ values. The frequency-domain representation of the transient $Z_{ja}^{n,n}$ curves can be obtained by Fourier transformation as [26]

$$Z_{ja}^{n,n}(\omega) = \int_0^{\infty} Z_{ja}^{n,n} e^{-i\omega t} dt \tag{7}$$

where i is the imaginary unit and ω denotes the frequency of excitation. Correspondingly, the frequency-domain representation of the transient $Z_{ja}^{n,m}$ curves can be obtained by Fourier transformation as follows:

$$Z_{ja}^{n,m}(\omega) = \int_0^\infty Z_{ja}^{n,m} e^{-i\omega t} dt \tag{8}$$

$Z_{ja}^{n,n}(\omega)$ and $Z_{ja}^{n,m}(\omega)$ can be expressed as follows:

$$Z_{ja}^{n,n}(\omega) = \text{Real}[Z_{ja}^{n,n}(\omega)] + i\text{Imag}[Z_{ja}^{n,n}(\omega)] \tag{9}$$

and

$$Z_{ja}^{n,m}(\omega) = \text{Real}[Z_{ja}^{n,m}(\omega)] + i\text{Imag}[Z_{ja}^{n,m}(\omega)] \tag{10}$$

where Real and Imag represent the real and imaginary parts, respectively. The abovementioned expression can also be written as follows:

$$Z_{ja}^{n,n}(\omega) = |Z_{ja}^{n,n}(\omega)|e^{i\theta} \tag{11}$$

and

$$Z_{ja}^{n,m}(\omega) = |Z_{ja}^{n,m}(\omega)|e^{i\phi} \tag{12}$$

where $|Z_{ja}^{n,n}(\omega)|$ and $|Z_{ja}^{n,m}(\omega)|$ are the amplitudes of the respective complex thermal impedances. They also equal to $R_{ja}^{n,n}$ and $R_{ja}^{n,m}$ in time domain, respectively. θ and ϕ represent the phase delay angles between temperature and the respective power losses. The abovementioned two equations can be rewritten as follows:

$$Z_{ja}^{n,n}(\omega) = |Z_{ja}^{n,n}(\omega)|\cos\theta + i|Z_{ja}^{n,n}(\omega)|\sin\theta \tag{13}$$

and

$$Z_{ja}^{n,m}(\omega) = |Z_{ja}^{n,m}(\omega)|\cos\phi + i|Z_{ja}^{n,m}(\omega)|\sin\phi \tag{14}$$

which also conform with (9) and (10).

By using (7) to (14), the time-domain thermal impedances can be transformed into the frequency-domain loci, where the responses to periodic power excitations are represented on the complex plane. Taking chips $U4$ and $U5$ as an example, Fig. 4 shows the frequency-domain locus curves of $Z_{ja}^{U5,U5}(\omega)$ and $Z_{ja}^{U4,U5}(\omega)$ by using two types of TIMs from the abovementioned simulation model as well as (3), (5), and (7) to (14). The variations of the imaginary parts are plotted as functions of the real parts, whereas the corresponding frequency points are annotated. The imaginary parts of the frequency-domain thermal impedances are physically related to the thermal capacitances in the thermal dissipation path. They characterize the phase angles of the temperature change compared with the power losses at different ω, which are caused by the thermal capacitances of the thermal dissipation path underneath the chips. The real parts represent the thermal resistances of the underneath thermal dissipation path at different ω.

It can be seen that $Z_{ja}^{U5,U5}(\omega)$ and $Z_{ja}^{U4,U5}(\omega)$ vary with the excitation frequency, showing similar behavior as reported before [23], [24], [25]. The curves occupy all the four quadrants [25] but are mainly located in the second quadrant, where θ and ϕ decrease from 0 to -π/2 as the frequency increases. At zero excitation frequency, the heat generated from chip $U5$ reaches the ambient and the phase delay is zero, which indicates

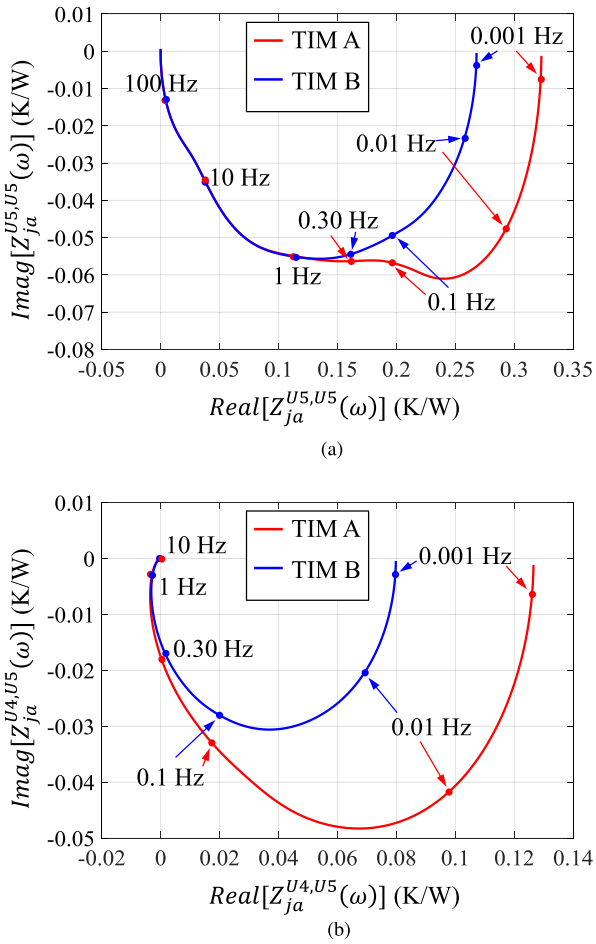


Fig. 4. Simulated $Z_{ja}^{U5,U5}(\omega)$ and $Z_{ja}^{U4,U5}(\omega)$ results in the complex domain. (a) Complex locus representation of $Z_{ja}^{U5,U5}(\omega)$. (b) Complex locus representation of $Z_{ja}^{U4,U5}(\omega)$.

high $|Z_{ja}^{n,n}(\omega)|$ and $|Z_{ja}^{n,m}(\omega)|$ but low θ and ϕ. Thus, the real parts hit the maximum values while the imaginary parts are zero, according to (9), (10), (13), and (14). As the excitation frequency increases, the dissipation path becomes shorter as the heat is stored and released locally by the thermal capacitance, thus $|Z_{ja}^{n,n}(\omega)|$ and $|Z_{ja}^{n,m}(\omega)|$ decrease. Considering the variation trends of the trigonometric functions in the second quadrant, the real parts decrease while the imaginary parts decrease first and then increase toward zero. At high frequency, the heat does not reach the interface between the module case and the external cooling setup, since the two complex loci with different TIMs overlap, implying that they are not affected by the external cooling setup. Thus, there is an characteristic frequency point in between, at which the heat reaches the interface between the module case and the external cooling setup, without crossing it. In this case the heat dissipation will not be affected by the external cooling setup.

In the proposed new approach, the SFM and FDA are combined to take advantages of both the time-domain analysis and FDA. As a first step, the SFM is carried out to determine the value of $R_{jc}^{m,m}$. Then, the FDA is performed to derive the

characteristic frequency that corresponds to the interface between the module case and the external cooling setup. Finally, the $R_{jc}^{n,m}$ value can be obtained in the complex loci of the $Z_{ja}^{n,m}$ curves, as the amplitude at the characteristic frequency point.

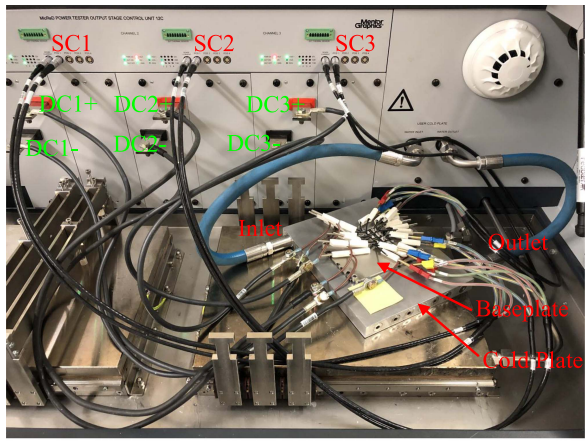
As an example, the abovementioned process can be performed on chips $U4$ and $U5$. It is known from the previous SFM analysis (see Fig. 2) that the $R_{jc}^{U5,U5}$ value is about 0.170 K/W, which corresponds to excitation frequency of 0.30 Hz in Fig. 4. This is also the characteristic frequency at which the periodically generated heat of $U5$ reaches the case surface without being affected by the external cooling condition. Thus, the frequency of 0.30 Hz can be taken as the indication of the boundary between the module case and the external cooling setup. By reading the amplitudes at 0.30 Hz from the two $Z_{ja}^{U4,U5}(\omega)$ curves in Fig. 4(b) and take the average value, $R_{jc}^{U4,U5}$ is obtained as 0.017 K/W. By applying similar approach to other $Z_{ja}^{n,n}(\omega)$ and $Z_{ja}^{n,m}(\omega)$ curves, $R_{jc}^{n,m}(\omega)$ between each pair of chips can be derived.

III. Experimental Verification

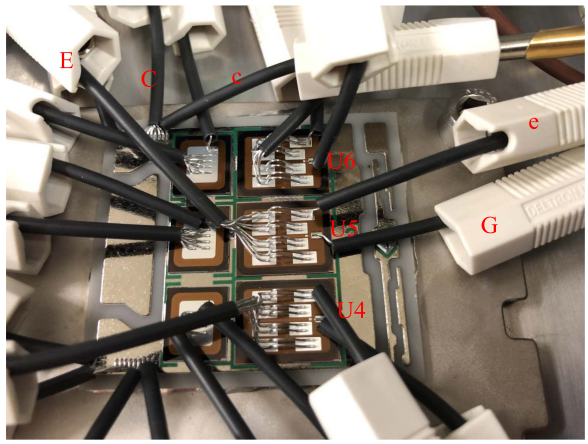
To verify the method experimentally, the module sample as well as cold plate corresponding to the model in Fig. 1 have been built and assembled, as shown in Fig. 5. The module sample is prepared purposely for testing the thermal coupling among the chips. That is, the chips are no longer connected in parallel, but are allocated with separate power, control, and sense bonding wires, to enable independent heating as well as sensing of single chip for the thermal coupling test. For example, the gate (G), auxiliary emitter (e), auxiliary collector (c), power emitter (E), and power collector (C) terminals for the chip $U5$ are annotated in Fig. 5. The bonding wires are protected by the black shrinking tubes while the fast connections with the testing circuit are accomplished by banana plugs. The chips under test are the standard 3.3-kV/75-A IGBTs built in-house. The module is mounted on the heat sink by M6 screws with 5 N · m torque at the four corners, as would be done in the railway traction inverters.

The thermal coupling test is performed with Mentor Graphics MicReD Power Tester [27], setup of which is shown in Fig. 5(a). In the test with three available heating (DC ports) and sense channels (SC ports), one, two, or three chips can be heated at a time by the DC ports, while the thermal responses of all the three are recorded by the SC ports. The SC ports sense the chips' ON-state voltage drop ($V_{\mathrm{ce(on)}}$) values, which are in turn transformed into T_j^n responses by the inversely proportional relationship between the two, as shown by the calibration curve in Fig. 6.

Fig. 7 shows the experimental results of $Z_{ja}^{U5,U5}$ with the two types of TIMs, along with the corresponding structure functions. In the test, a constant power loss of 49 W is applied on chip $U5$ and the time-dependent variation of $T_j^{U5,U5}$ is recorded to derive the $Z_{ja}^{U5,U5}$ according to (3). The same test is repeated for the two types of TIMs. The value of $R_{jc}^{U5,U5}$ can then be derived from the BP of the two $Z_{ja}^{U5,U5}$ curves with different TIMs, as shown



(a)



(b)

Fig. 5. Experimental setup for the thermal measurements. (a) Overall cable connection and module mounting. (b) Detailed bonding wire arrangement and connection.

in Fig. 7. It can be seen that the derived value of 0.178 K/W agrees well with the simulated results, as shown in Fig. 2.

Fig. 8 shows the experimental results of $Z_{ja}^{U4,U5}$ with the two types of TIMs, along with the corresponding structure functions. In the test, a constant power loss of 49 W is applied on chip $U5$ and the time-dependent variation of $T_j^{U4,U5}$ is recorded to derive the $Z_{ja}^{U4,U5}$ according to (5). The same test is repeated for the two types of TIMs. It can be seen that the derived $Z_{ja}^{U4,U5}$ curves agree with the simulation results in Fig. 3. Similar to the simulation results, the experimental $Z_{ja}^{U4,U5}$ curves and the corresponding structure function curves provide little useful information to determine $Z_{jc}^{U4,U5}$.

The experimentally tested $Z_{ja}^{U5,U5}$ and $Z_{ja}^{U4,U5}$ in time domain can be transformed into frequency domain representations by using (7)–(14). The comparison between the derived complex loci of the $Z_{ja}^{U5,U5}$ and $Z_{ja}^{U4,U5}$ with the two types of TIMs is shown in Fig. 9(a) and (b), respectively. By comparing Figs. 4 and 9, it can be seen that the simulation and experimental results reasonably agree with each other. With the similar analysis fashion as in the simulation, the $R_{jc}^{U5,U5}$ value is obtained as 0.178 K/W in the experiments, which corresponds to the excitation frequency

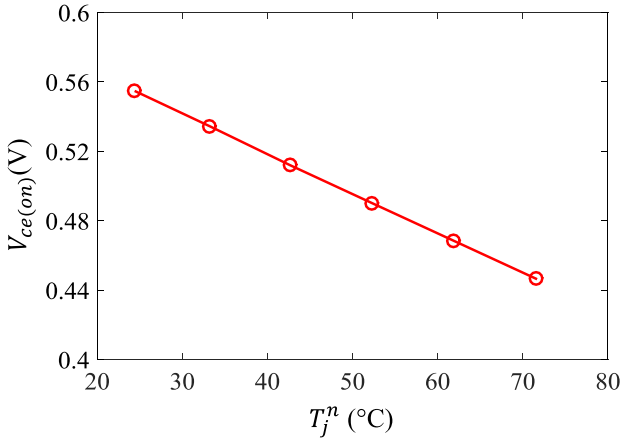


Fig. 6. Calibration curve between $V_{\mathrm{ce(on)}}$ and T_j^n.

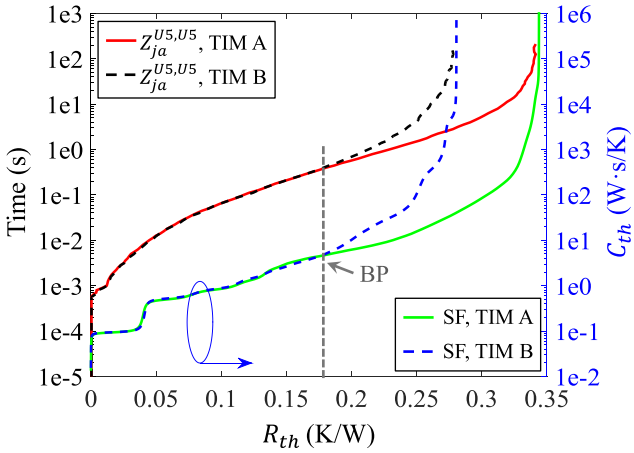


Fig. 7. Experimental results of the $Z_{ja}^{U5,U5}$ curves and the corresponding structure function curves for two types of TIMs.

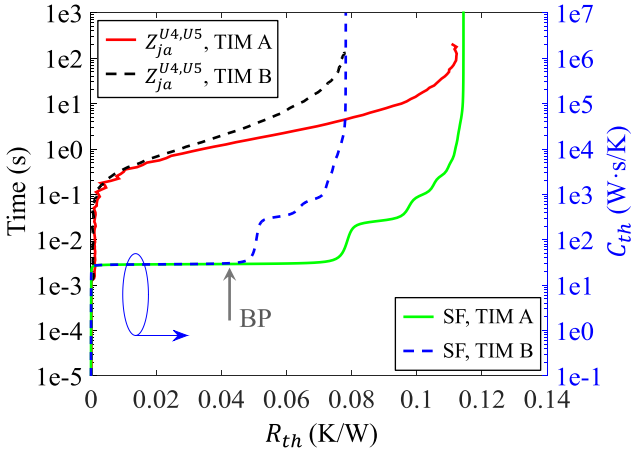
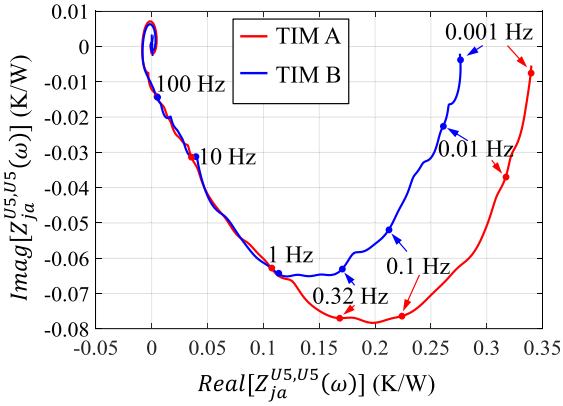
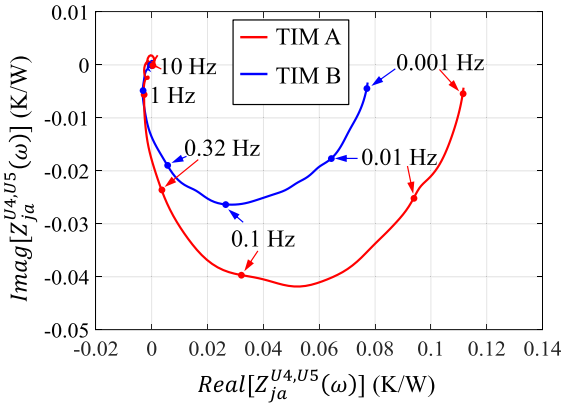


Fig. 8. Experimental results of the $Z_{ja}^{U4,U5}$ curves and the corresponding structure function curves for two types of TIMs.



(a)



(b)

Fig. 9. Experimentally derived $Z_{ja}^{U5,U5}(\omega)$ and $Z_{ja}^{U4,U5}(\omega)$ in the complex domain. (a) Complex locus representation of $Z_{ja}^{U5,U5}(\omega)$. (b) Complex locus representation of $Z_{ja}^{U4,U5}(\omega)$.

TABLE I
$R_{jc}^{n,m}$ AND $R_{jc}^{n,n}$ OF THE PARALLELING CHIPS DERIVED FROM SIMULATION (BLUE) AND EXPERIMENT (GREEN) (UNIT: K/W)

n \ m	$U4$	$U5$	$U6$
$U4$	0.171/0.175	0.017/0.021	0.003/0.002
$U5$	0.018/0.020	0.170/0.178	0.018/0.019
$U6$	0.003/0.003	0.018/0.021	0.173/0.183

of 0.32 Hz in the complex loci, as shown in Fig. 9(a). Thus, the $R_{jc}^{U4,U5}$ value is derived from Fig. 9(b) as 0.021 K/W at 0.32 Hz. The derived value agrees reasonably with the simulation. It is also noted that the identified characteristic frequency in the experiment is slightly higher than the simulation, which could be caused by the limited numerical modeling accuracy or system noise in the testing bench.

The abovementioned derivation process is then repeated between other chip pairs to derive the $R_{jc}^{n,m}$ between each pair of them. Table I compares the numerically and experimentally

derived $R_{jc}^{n,m}$ values among the three chips. The experimental results reasonably agree with the simulated ones. The discrepancy could be caused by the noise during the experimental test, the limited accuracy of the numerical modeling and the fabrication error of the module structure. For example, the baseplate bottom is modeled as flat in the simulation to limit the computational resources required. In reality, the tested module describes an irregular bottom surface profile due to mechanical stress in the soldering process, where the height difference between the peak and valley is around 60 μm.

A number of observations should be noted from Table I. First, the $R_{jc}^{n,n}$ values are different for the three IGBT chips, which is mainly due to the different thermal dissipation structure underneath considering the thermal spreading effect. Second, the matrix is not strictly symmetrical since the $R_{jc}^{n,m}$ and the corresponding $R_{jc}^{m,n}$ values describe slight difference. This can also be attributed to the asymmetrical placement of the chips in the module. Third, the thermal coupling between $U4$ and $U6$ is weaker than other chips pairs, which is mainly due to the fact that they are located further apart. Although $R_{jc}^{U4,U6}$ and $R_{jc}^{U6,U4}$ are relatively small compared with others in the table, they should not be neglected. This is because in practical application where the thermal resistance between module case and the ambient is considered, the coupling effect between $U4$ and $U6$ will still be prominent [16]. Fourth, assuming equal power losses and considering the thermal coupling effect, the T_j^n value calculated by (2) would be about 13.1%, 21.9%, and 13.1% higher for the three chips, respectively, compared with the self-heating alone case. Such imbalance in thermal coupling effect tends to reduce the module-level lifetime expectation [28].

The effectiveness of the derived $R_{jc}^{n,m}$ parameters can be verified by further investigation of the module-level junction-to-case thermal resistance, R_{jc}. For the module, as shown in Fig. 5, which incorporates three IGBT chips, R_{jc} can be calculated as follows:

$$R_{jc} = \frac{T_j - T_c}{P}. \tag{15}$$

Following the common practice of defining R_{jc} from different manufacturers of power modules with multiple paralleling chips, it is calculated as the overall thermal response of the switch (comprised of three chips in this case) to the power loss P. Thus, T_j is taken as the average junction temperature of all the paralleling chips in the switch. In this study, it is taken as the average value of T_j^{U4}, T_j^{U5}, and T_j^{U6}. P is taken as the total power of the paralleling chips. It can be calculated as the sum of P_{loss}^{U4}, P_{loss}^{U5}, and P_{loss}^{U6} in this study. Due to the balanced current sharing among the paralleling chips, it is usually considered that P_{loss}^{U4}, P_{loss}^{U5}, and P_{loss}^{U6} describe equal value. However, the direct determination of R_{jc} via (15) by experiment is challenging, since the measurement of T_c brings considerable uncertainties [29].

The derivation of R_{jc} for the module, as shown in Fig. 5, can be carried out in a number of alternative approaches [13], three of which will be elaborated in the following to compare the results.

Method I: The similar SFM as described previously can be applied to derive R_{jc} from the structure functions of two Z_{ja} curves with different TIMs, which is a common practice of the module manufacturers [30]. Fig. 10(a) shows the experimentally derived Z_{ja} curves of the module consisted of three IGBT chips by using the aforementioned two TIMs. The corresponding structure functions are shown in Fig. 10(b). The BP can be taken as the position of the module case. The cumulative thermal resistance at this point denotes R_{jc}. By locating the BP, the R_{jc} value of the module is obtained from Fig. 10(b) as 0.069 K/W.

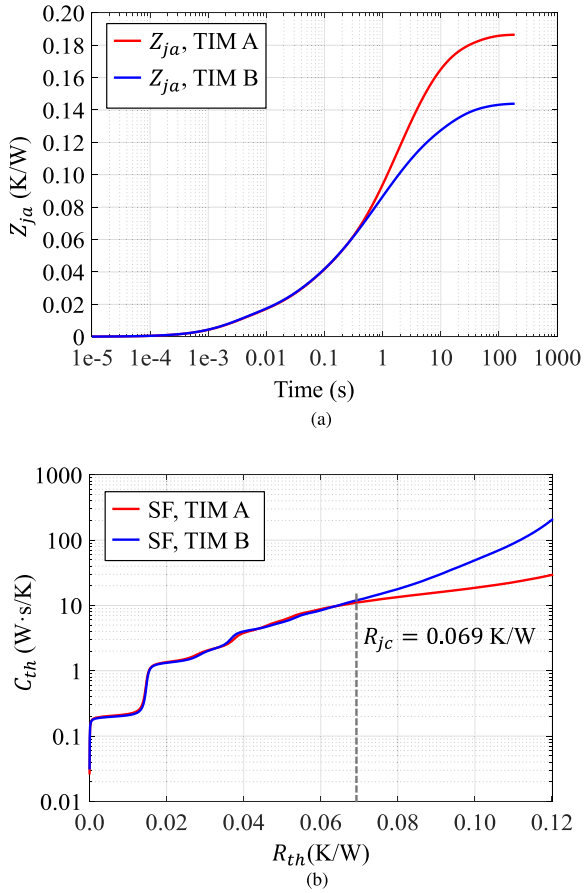


Fig. 10. Experimentally derived Z_{ja} curves and the corresponding structure functions with two types of TIMs for the whole module. (a) Z_{ja} curves. (b) Structure functions of the Z_{ja} curves. The indicated R_{jc} value is also annotated.

Method II: The R_{jc} can be derived from its definition. By taking

$$T_j = \frac{1}{N}\sum_{n=1}^{N} T_j^n \tag{16}$$

and

$$P = \sum_{n=1}^{N} P_{\text{loss}}^n \tag{17}$$

into (15), it is derived

$$R_{jc} = \frac{1}{N \cdot P}\left(\sum_{n=1}^{N} T_j^n - N \cdot T_c\right). \tag{18}$$

Considering the values of P^n_{loss} are usually similar for the paralleling chips and taking (2) into (18), it can be obtained that

$$R_{jc} = \frac{1}{N \cdot N} \sum_{n=1}^{N} \sum_{m=1}^{N} R_{jc}^{n,m}. \tag{19}$$

In the module considered, N equals 3, and the experimental values of $R_{jc}^{n,m}$ are listed in Table I. It can, thus, be calculated from (19) that R_{jc} is also about 0.069 K/W.

Method III: If the coupling effect is neglected ($R_{jc}^{n,m} = 0$ for $m \neq n$), R_{jc} can also be derived from (19) and

$$\frac{1}{R_{jc}} = \sum_{n=1}^{N} \frac{1}{R_{jc}^{n,n}}. \tag{20}$$

By taking the diagonal elements of the experimental results in Table I into (20), R_{jc} is calculated as 0.060 K/W.

It can be seen that the R_{jc} value derived by Method III is about 13.0% lower than the other two methods, due to the ignorance of the coupling effect among the paralleling chips. Method II, by taking the derived $R_{jc}^{n,m}$ values into account, generates similar results as Method I, which is a commonly adopted approach to assess R_{jc} for multichip power modules. Thus, the effectiveness of the proposed method in determining $R_{jc}^{n,m}$ is verified. It should also be noted that the derived $R_{jc}^{n,m}$ matrix contains much more information than the commonly adopted single R_{jc} value in the multichip power module datasheet. The detailed knowledge of the $R_{jc}^{n,m}$ matrix provides sufficient information for assessing the thermal distribution among paralleling chips during operation and preventing thermal imbalances due to module packaging structures. The matrix is also a useful tool to compare modules from different manufacturers for thermal uniformity performance. In addition, the extracted $R_{jc}^{n,m}$ matrix can be adopted in the optimization of the thermal network for the multichip power module. In the process, the matrix can be used as the target when the lumped elements of the network are optimized by numerical iterations [16]. Finally, the derivation method of $R_{jc}^{n,m}$ bears the potential to be considered in the future establishment of industrial standards for assessing power modules with multiple chips in parallel.

IV. Conclusion

A new method to derive the inherent thermal coupling resistances among neighboring chips for the multichip semiconductor power modules has been presented in this article. The method is based on the combination of the traditional time-domain SFM and the FDA. By observing the characteristic excitation frequency at which the periodic heat flow of the chip stays inside the module, the interface between the module case and the external cooling setup can be identified in the complex loci of the junction-to-ambient coupling thermal impedances. Consequently, the junction-to-case level coupling thermal resistance can be obtained at the characteristic frequency. The effectiveness of the method is validated by the agreement between the experimental results and simulation outcome. It is further verified against the incumbent industrial practice in determining the module-level thermal resistance for a multichip power module.

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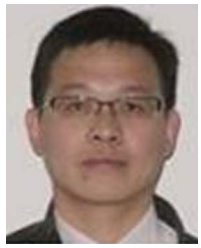

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