A Hybrid Seven-Level Dual-Inverter Scheme With Reduced Switch Count and Increased Linear Modulation Range

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***Abstract*—This work presents a hybrid seven-level dual inverter scheme with increased linear modulation range. The hybrid inverter structure is formed by supplying the load from primary side by using a cascaded structure of a two-level inverter and H-bridge (HB) and secondary side of the load is supplied by a floating-capacitor-fed two-level inverter. The combination of primary two-level space vector structure (SVS) with secondary two-level SVS and primary three-level SVS of HB form a seven-level SVS that can further be extended to an eight-level hexagonal SVS. This structure then reduced to a 12-sided eight-level SVS to avoid exceeding motor phase voltage rating. Subsequently by using this eight-level SVS in an unique pulsewidth modulation mode, the proposed topology can increase the modulation range linearly from $0.577V_{\rm dc}$ to $0.637V_{\rm dc}$ peak phase fundamental voltage for any load power factor (pf), where dc-link voltage is $V_{\rm dc}$. An 11% increase in modulation range ($0.637V_{\rm dc}/0.577V_{\rm dc}$) is possible devoid of lower order harmonics (predominantly 5th, 7th, 11th, 13th, etc.) in phase voltage for unity pf load in comparison to the conventional six-step operation of two-level and multilevel hexagonal SVS. To balance HB capacitors voltages in this work, a concept of indirect space vector redundancy is used. The efficacy of the proposed inverter scheme is verified through various experimental results at different steady-state and transient conditions.**

***Index Terms*—Induction motor (IM) drive, pulsewidth modulation (PWM), seven-level inverter, space vector structure (SVS).**

I. Introduction

In LAST few years, high power medium-voltage multilevel inverters (MLIs) gained popularity in many applications such as motor drives, traction, distributed generations, HVdc, EV, etc. MLIs offer better harmonic performance, less dv/dt stress across load terminals, better operation with reduced sized filters, etc. There are a few MLI topologies, which become popular in the last decade, such as, neutral point clamp (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) [1], [2]. These topologies suffer from several shortcomings such as neutral point voltage fluctuations, higher floating capacitors count, and too many isolated power supplies. These are greatly minimized by using modular and hybrid MLI structures.

Among several MLIs, the dual-inverter (DI) scheme supplying the stator windings terminals from either end of an open-end winding induction motor (OEWIM) possesses many advantages compared to single-sided MLI feeding star-connected load [3], [4], [5], [6], [7]. Here, the primary-side and secondary-side inverter can be powered in three ways: by using two isolated dc links, a single common dc link, a single dc link, and a floating capacitor. However, the DI with a single dc link configuration has become widely accepted. It can increase the phase voltage levels with reduced switch count apart from higher reliable, and fault-tolerant operations [4], [5], [16], [18]. In the case of DI topology, the primary inverter of a hexagonal voltage space vector structure (SVS) of radius $V_{\rm dc}$ can form a combined multilevel hexagonal SVS of radius $V_{\rm dc}$ utilizing the secondary floating capacitor-fed inverter. Any hexagonal SVS achieves a maximum peak phase fundamental voltage of $0.637V_{\rm dc}$, while the inverter produces six-step output voltages [8]. However, the conventional space vector (SV) pulsewidth modulation (PWM) operation can yield only $0.577V_{\rm dc}$ peak phase fundamental voltage in the highest linear modulation range (LMR), defined by the inscribed circle of radius $0.866V_{\rm dc}$ within the hexagonal SVS of radius $V_{\rm dc}$. Several overmodulation strategies are discussed in the literature to increase the peak phase fundamental [8], [9], [10]. A PWM strategy to increase modulation range (MR) till $0.637V_{\rm dc}$ peak fundamental is proposed for any *n*-level diode clamped inverter [9]. Although it can achieve full modulation index besides dc-link capacitors balancing, lower order harmonics start to appear above $0.6062V_{\rm dc}$ peak phase fundamental. An inscribed polygonal-boundary compression technique was proposed to seamlessly extend MR till $0.6062V_{\rm dc}$ peak phase fundamental for a three-level diode clamped inverter with a better harmonic performance [10].

Recently, different hybrid MLI topologies discussed in literatures to eliminate lower order harmonics while extending the MR linearly [11], [12], [13], [14], [15], [16]. It will

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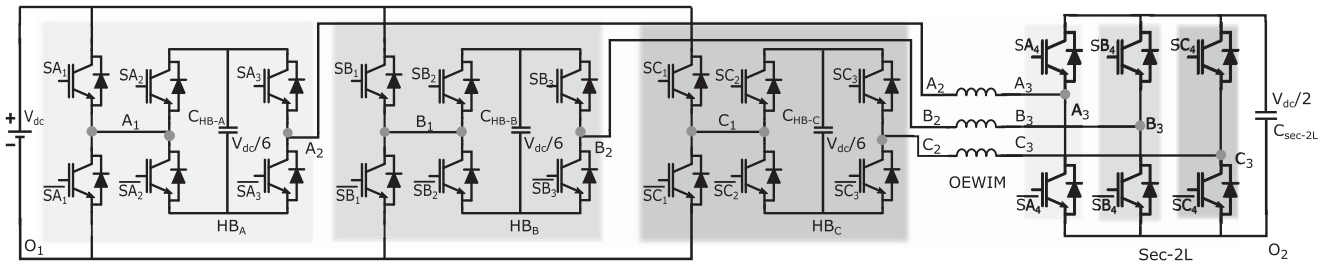

Fig. 1. Power circuit of the proposed seven-level inverter supplying an OEWIM load.

eventually mitigate low frequency torque pulsation of a motor at the overmodulation region (from $0.577V_{\rm dc}$ to $0.637V_{\rm dc}$ peak phase fundamental). A five-level inverter scheme formed by cascading a two-level inverter and two three-level HB with 30 switches is proposed in [11] for the first time to increase the LMR till $0.63V_{\rm dc}$. This topology uses a square-wave offset-added PWM algorithm to balance HB capacitor voltages. Another two five-level inverters, boosting their voltage levels to 7 for increasing LMR till $0.615V_{\rm dc}$, are proposed with fewer switches in [12] and [13]. The authors in [14] proposed a similar seven-level inverter with a distinct dynamic offset-added PWM technique for balancing floating capacitor voltages at extended MR. The aforementioned seven-level topologies have $V_{\rm dc}/4$ voltage division between two-pole voltage levels. However, the seven-level inverter topology with $V_{\rm dc}/6$ level division proposed in [15] can operate in nine-level mode to extend LMR till $0.607V_{\rm dc}$ peak phase fundamental for a unity power factor (upf) load. Recently, a seven-level hybrid clamped converter with boosted nine-level operation is proposed in [17]. It can achieve a maximum peak phase fundamental of $0.634V_{\rm dc}$ using 36 switches. A five-level inverter scheme with extended LMR till full base speed ($0.637V_{\rm dc}$, peak phase fundamental) is also proposed in literature [16]. As reported in [11], a similar hybrid MLI topology can extend the LMR for a seven-level counterpart only up to $0.625V_{\rm dc}$. Several polygonal voltage SV schemes are also investigated in works of literature to eliminate lower order harmonics selectively in extended MR [19], [20], [21]. Though more harmonics can be eliminated from the phase voltage with the increase in polygon sides, these topologies suffer from complex implementation.

A hybrid seven-level DI topology is presented in this article with extended LMR till 0.637Vdc peak phase fundamental, and it eliminates all lower order harmonics (5th, 7th, 11th, 13th, etc.). The proposed inverter circuit comprises a dc-link-fed two-level inverter cascaded with a three-level H Bridge (HB) on the primary side, whereas the secondary side has a floating capacitor-fed two-level inverter. The proposed seven-level DI power circuit is almost the same as the five-level counterpart of previous work, which underutilized its three-level HB as a two-level SVS [11], [16]. Nonetheless, the present article fully exploits the three-level SVS of HB to generate a combined seven-level SVS that can boost SV voltages levels to eight level. But, this SVS lacks direct SV redundancy, as seen in the previous article [16]. Hence, balancing of HB capacitors voltages becomes crucial, predominantly under upf load operation ([19]). However, this work proposes an innovative way to balance all the capacitors by incorporating the idea of indirect SV redundancy, as discussed in Section III. It facilitates improved harmonic performance and lower dv/dt stress across the motor phase compared to the five-level work proposed in [16]. Further, hardware experimental results are discussed in Section V to validate this proposed inverter scheme.

II. Proposed Inverter Scheme

A. Power Circuit Configuration

The proposed inverter circuit configuration powering an OEWIM load is illustrated in Fig. 1. The primary side of the stator winding of OEWIM is formed by cascading a capacitor-fed three-level HB with a dc-link-fed two-level inverter, whereas the secondary side is only supplied by a capacitor-fed two-level inverter. The primary two-level inverter is powered by dc link of voltage $V_{\rm dc}$, while the nominal voltage of the HB capacitors ($C_{{\rm HB}-x}$,where $x = A, B, C$ phase) and secondary two-level common capacitor ($C_{\rm sec}$) are controlled at $V_{\rm dc}/6$ and $V_{\rm dc}/2$, respectively. Each phase of the inverter have four pairs of complementary switches—$Sx1, Sx1'$; $Sx2, Sx2'$; $Sx3, Sx3'$; $Sx4, Sx4'$, where $x = A, B, C$ phase. The switches in the primary two-level block voltage $V_{\rm dc}$, the HB switches block only voltage $V_{\rm dc}/6$, and the secondary two-level switches block voltage $V_{\rm dc}/2$. On the primary side, the two-level inverter can generate pole voltage levels of 0 and $V_{\rm dc}$, and the HB can produce three-pole voltage levels of $-V_{\rm dc}/6$, 0, and $V_{\rm dc}/6$. On the secondary side, the capacitor-fed two-level inverter can have 0 and $V_{\rm dc}/2$ pole voltage levels. Hence, from Fig. 1, the phase voltage equations seen across the stator windings of the OEWIM can be written as follows:

$$V_{A2A3} = V_{A1O1} + V_{A2A1} - V_{A3O2} + V_{O1O2} \quad (1)$$

$$V_{B2B3} = V_{B1O1} + V_{B2B1} - V_{B3O2} + V_{O1O2} \quad (2)$$

$$V_{C2C3} = V_{C1O1} + V_{C2C1} - V_{C3O2} + V_{O1O2} \quad (3)$$

where V_{A1O1}, V_{B1O1}, and V_{C1O1} are the pole voltages of primary two-level inverter; V_{A2A1}, V_{B2B1}, and V_{C2C1} are the pole voltages of primary-side HB; V_{A3O2}, V_{B3O2}, and V_{C3O2} denote the pole voltages of secondary two-level inverter; and V_{O1O2} is the common-mode voltage.

B. Formation of SVS

It is possible to construct the SVS of the inverter scheme by combining the primary two-level SVS, the primary three-level

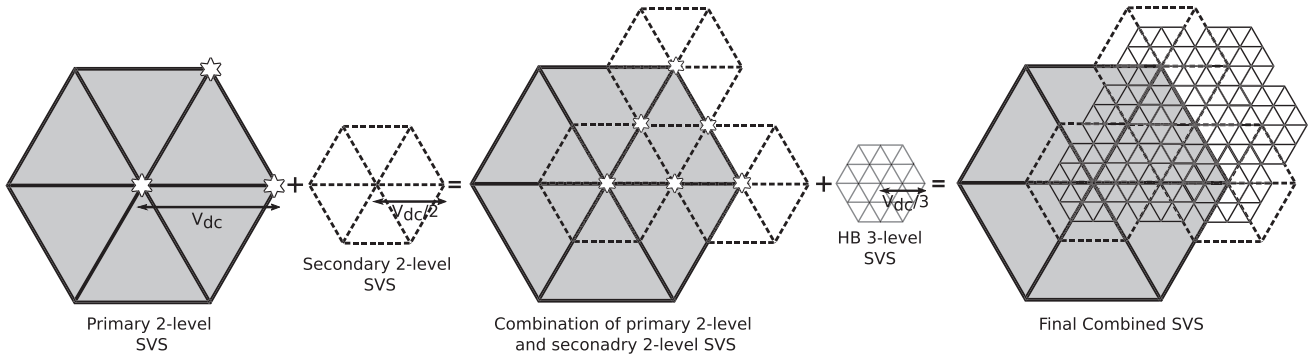

Fig. 2. Steps to form the proposed combined SVS.

HB SVS, and the secondary two-level SVS (see Fig. 2). The primary two-level hexagonal SVS has a radius of $V_{\rm dc}$, whereas the secondary two-level hexagonal SVS has a radius of $V_{\rm dc}/2$. The two-level HBs from A, B, and C phases form a three-level hexagonal SVS of radius $V_{\rm dc}/3$. To synthesize the proposed SVS, first, the secondary two-level hexagon is superimposed on the vector points (VPs) of the primary two-level hexagon, which will create a three-level SVS. Subsequently, the star-marked VPs of the generated three-level hexagonal SVS of radius $V_{\rm dc}$ are overlapped by the three-level HB SVS of radius $V_{\rm dc}/3$. Consequently, a seven-level SVS of radius $V_{\rm dc}$ is developed that can then be extended to an eight-level SVS by adding or subtracting the three-level HB pole voltages from the two-level primary and secondary inverter pole voltages. This unique feature of the proposed SVS aids in increasing the modulation index from $0.577V_{\rm dc}$ to $0.637V_{\rm dc}$ peak phase fundamental by utilizing the eight-level SVPs along with seven-level SVPs. It is crucial to ensure that the capacitor voltages are balanced when increasing the MR. The capacitor voltage balancing is achieved by using a unique indirect SV redundancies of the VPs in the SVS, which will be discussed in the next section. Therefore, the phase voltages can become devoid of lower order harmonics at the maximum MR. Equations (4)–(7) represent the voltage SVs of primary two-level($\overrightarrow{V_{SV1}}$), secondary two-level($\overrightarrow{V_{SV2}}$), three-level HB($\overrightarrow{V_{SV3}}$), and combined inverter scheme ($\overrightarrow{V_{\rm SV}}$).

$$\overrightarrow{V_{SV1}} = V_{A1O1} + V_{B1O1}e^{j2\pi/3} + V_{C1O1}e^{j4\pi/3} \quad (4)$$

$$\overrightarrow{V_{SV2}} = V_{A3O2} + V_{B3O2}e^{j2\pi/3} + V_{C3O2}e^{j4\pi/3} \quad (5)$$

$$\overrightarrow{V_{SV3}} = V_{A2A1} + V_{B2B1}e^{j2\pi/3} + V_{C2C1}e^{j4\pi/3} \quad (6)$$

$$\overrightarrow{V_{SV}} = \overrightarrow{V_{SV1}} - \overrightarrow{V_{SV2}} + \overrightarrow{V_{SV3}}. \quad (7)$$

The proposed combined SVS is shown in Fig. 3. The dotted line is the boundary of a hexagonal SVS of radius $V_{\rm dc}$. The inscribed circle of radius $OR_1 = 0.866V_{\rm dc}$ within this hexagon, denotes the boundary of LMR of the inverter in seven-level mode operation. However, while extending the modulation index, the reference voltage SV have to follow the circular trajectory of radius $OR_2 = 0.955V_{\rm dc}$, to yield $0.637V_{\rm dc}$ peak phase($= (2/3) * 0.955V_{\rm dc} = 0.637V_{\rm dc}$) fundamental across load. To switch averages along this circular trajectory in sector-I, eight-level VPs along straight line B_1C_1 must be applied, along with seven-level VPs along straight line AD. Since the application of eight-level

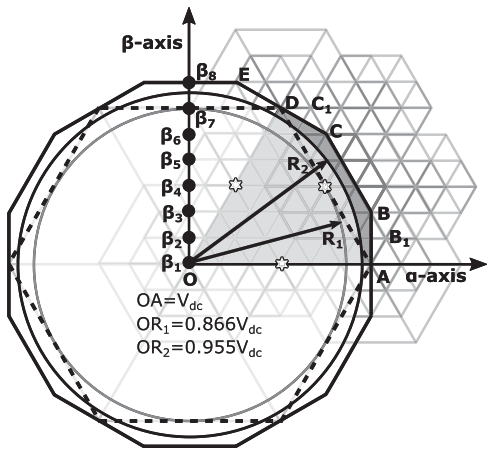

Fig. 3. Generated combined SVS of the proposed Inverter scheme for 0 to 60° sector.

VP B_1 exceeds the machine phase voltage rating of $(2/3)V_{\rm dc}$, the SV trajectory is modified to ABCD for sector-I. Whenever vector $\overrightarrow{OB_1}$ is needed to be applied, $\overrightarrow{OA}$ and $\overrightarrow{OB}$ vectors are summed up in a ratio of x_1 and x_2 to get resultant $\overrightarrow{OB_1}(=x_1.\overrightarrow{OA} + x_2.\overrightarrow{OB})$. The calculated value of x_1 and x_2 would be 0.5833 and 0.5. Furthermore, to generate the eight-level VPs, the HB $V_{\rm dc}/6$ capacitors are used, and they discharge by carrying the load current at an extreme MR. In this work, all the HB capacitors are balanced strategically to achieve a maximum peak phase fundamental of $0.637V_{\rm dc}$ across phases without any lower order harmonics. The following section describes the balancing scheme of all the capacitors of the inverter.

III. Operation of the Proposed Inverter Scheme

A. Capacitor Balancing Strategy Till Seven-Level Mode

As discussed in the previous section, the proposed inverter scheme utilized the three-level HB SV such a way that combined seven-level SVS can be generated. However, the generated seven-level SV points lack direct opposing vector redundancy, as seen in [5]. In the present case, to balance an HB capacitor while generating a particular VP, other phase HB capacitors will also be disturbed (charged or discharged) unlike the existing work. For example, three direct redundancies are observed to generate SVP V_1 [$V_{\rm dc}$/6, 0, 0]. First, zero vector [0,0,0] from

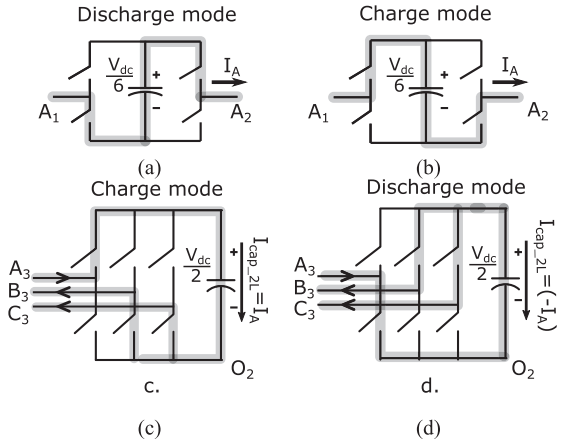

Fig. 4. (a) and (b) Voltage status of A-phase HB capacitor while applying HB vector $[V_{\rm dc}/6, 0, 0]$ and $[-V_{\rm dc}/6, 0, 0]$, respectively. (c) and (d) Voltage status secondary two-level capacitor for two-level vector state $[V_{\rm dc}/2, 0, 0]$ and $[0, V_{\rm dc}/2, V_{\rm dc}/2]$, respectively.

TABLE I
DIFFERENT COMBINATIONS OF HB SV FOR A, B, AND C PHASES

	A	B	C		A	B	C
1	Vdc/6	0	0	2	Vdc/6	-Vdc/6	-Vdc/6
	0	-Vdc/6	-Vdc/6		0	Vdc/6	Vdc/6
	-Vdc/6	Vdc/6	Vdc/6		-Vdc/6	0	0
3	0	Vdc/6	0	4	-Vdc/6	Vdc/6	-Vdc/6
	-Vdc/6	0	-Vdc/6		Vdc/6	0	Vdc/6
	Vdc/6	0	Vdc/6		0	-Vdc/6	0
5	0	0	Vdc/6	6	-Vdc/6	-Vdc/6	Vdc/6
	-Vdc/6	-Vdc/6	0		Vdc/6	Vdc/6	0
	Vdc/6	Vdc/6	-Vdc/6		0	0	-Vdc/6
7	Vdc/6	-Vdc/6	0	8	Vdc/6	0	-Vdc/6
	0	Vdc/6	-Vdc/6		0	-Vdc/6	Vdc/6
	-Vdc/6	0	Vdc/6		-Vdc/6	Vdc/6	0

the primary and secondary two-level can be applied along with HB vector $[V_{\rm dc}/6, 0, 0]$ (see Fig. 4(a)). The second option is to apply zero vector [0,0,0] from primary two-level, vector $[0, V_{\rm dc}/2, V_{\rm dc}/2]$ (see Fig. 4(d)) from secondary two-level and vector $[-V_{\rm dc}/6, V_{\rm dc}/6, V_{\rm dc}/6]$ from HB. Third, one can apply vector $[V_{\rm dc}, 0, 0]$ from primary two-level, vector $[V_{\rm dc}/2, 0, 0]$ from secondary two-level and vector $[-V_{\rm dc}/6, V_{\rm dc}/6, V_{\rm dc}/6]$ from HB. It is noticeable that even though the A-phase HB capacitor can be balanced, the C and B phases capacitor eventually became disturbed due to the aforementioned redundancies.

However, one can find out that the HB vector state $[V_{\rm dc}/6, 0, 0]$ can be modified equivalently to the vector state $[0, -V_{\rm dc}/6, -V_{\rm dc}/6]$ by subtracting a common mode $V_{\rm dc}/6$ from each phase. Both the vector states $[V_{\rm dc}/6, 0, 0]$ and $[0, -V_{\rm dc}/6, -V_{\rm dc}/6]$ would result in a similar phase voltage. The vector state $[0, -V_{\rm dc}/6, -V_{\rm dc}/6]$ is capable of balancing B and C phase capacitor voltages, which got disturbed while balancing $C_{{\rm HB}_A}$. This vector state will not affect the balanced $C_{{\rm HB}_A}$. It is thus easy to infer that if the HB vector states, $[V_{\rm dc}/6, 0, 0]$, $[0, -V_{\rm dc}/6, -V_{\rm dc}/6]$, and $[-V_{\rm dc}/6, V_{\rm dc}/6, V_{\rm dc}/6]$ are applied for a third of SVP dwell time in a sampling period, all the HB capacitor voltages will be balanced. This phenomenon is termed the concept of indirect SV redundancy. Table I lists all the possible triplet combinations of HB SV to generate a specific SVP from the proposed inverter scheme.

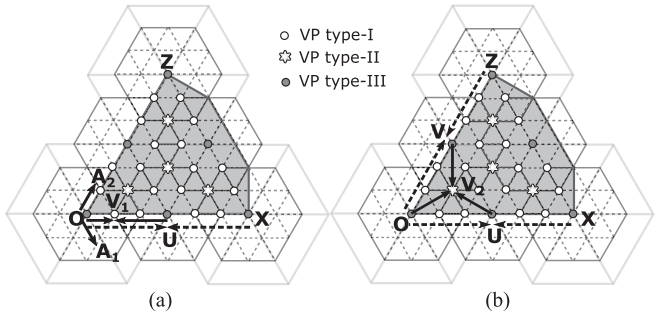

Fig. 5. SV redundancy of vectors $\overrightarrow{OV_1}[V_{\rm dc}/6, 0, 0]$ and $\overrightarrow{OV_2}[V_{\rm dc}/3, V_{\rm dc}/6, 0]$. (a) HB SV combination-1. (b) HB SV combination-8.

The proposed SVS can have three different VPs combinations (see Fig. 5). VP type-I refers to VPs that utilize HB SV combinations 1–6. The HB SV combinations 7 and 8 are used to produce VP type-II. The type-III VPs, generated by primary two-level and secondary two-level SV combinations exclude HB SV combinations. Fig. 5 also shows the SV combination for two vector $\overrightarrow{OV_1}$ and $\overrightarrow{OV_2}$. In this case, the $\overrightarrow{OV_1}$ uses the HB combination-1, while the $\overrightarrow{OV_2}$ uses the HB combination-8. So far, the aforementioned discussions ensure that all HB capacitors voltages can be balanced in each sampling cycle. Additionally, using the opposing vector concept, the secondary two-level common capacitor $C_{\rm sec}$ voltage can easily be regulated for every SVP. As seen in Fig. 5(a), for the generation of $\overrightarrow{OV_1}$, the opposite two-level SV $\overrightarrow{OU}$ and $\overrightarrow{XU}$ along A-phase, can be used. The A-phase current regulates the $C_{\rm sec}$ capacitor voltage in this case. Similarly, while generating vector $\overrightarrow{OV_2}$, along with opposite vector pair $\overrightarrow{OU}$ and $\overrightarrow{ZV}$, another opposite vector pair $\overrightarrow{OV}$ and $\overrightarrow{ZV}$ would be used. The vector pair $\overrightarrow{OV}$ and $\overrightarrow{ZV}$ will balance $C_{\rm sec}$ through the C-phase current. Thus, until the seven-level mode of operation of the proposed inverter scheme, all capacitor voltages can remain within a predefined hysteresis band.

B. Capacitor Balancing Strategy at Eight-Level Mode

Up until now, it is determined that the proposed inverter scheme has to utilize the eight-level voltage potentials along the trapezoidal boundary to extend the peak phase fundamental voltage. PWM switching of eight-level VPs and seven-level VPs helps eliminate lower order harmonics from phase voltage compared to the six-step operation mode of the MLI at extended LMR. However, balancing the capacitor voltages for the eight-level VPs would not be straightforward, as seen in the case of VPs below seven-level. In Fig. 6 and Table II, SV redundancies for eight-level VPs (M_1, M_2, M_3, M_4) are shown. In case for generation of eight-level VP M_1, three-level HB vectors $\overrightarrow{XM_1}$ $(0, V_{\rm dc}/6, -V_{\rm dc}/6)$, $\overrightarrow{PM_1}$ $(-V_{\rm dc}/6, 0, V_{\rm dc}/6)$, and $\overrightarrow{N_3M_1}$ $(V_{\rm dc}/6, -V_{\rm dc}/6, 0)$ can be used. All three HB vectors will have a balancing effect on each phase HB capacitors voltages if applied for an equal duration. However, while generating VP $\overrightarrow{M_1}$, secondary 2-level vectors $\overrightarrow{XN_3}$ $(V_{\rm dc}/2, 0, V_{\rm dc}/2)$, $\overrightarrow{ZN_3}$ $(0, V_{\rm dc}/2, 0)$ along the B-phase and $\overrightarrow{XP}$ $(0, 0, V_{\rm dc}/2)$ along the C phase are applied. Although, the opposite two-level vectors

TABLE II
SV REDUNDANCIES FOR EIGHT-LEVEL VPS

Eight-level VPs	Primary two-level SV	Secondary two-level SV	Three-level HB SV	Effect on C_{sec}	Effect on C_{HB}
M1 [7Vdc/6,Vdc/3,0]	[Vdc,0,0]	[0,0,0]	[0,Vdc/6,-Vdc/6]	N	IB (D) and IC (C)
	[Vdc,0,0]	[0,0,Vdc/2]	[-Vdc/6,0,Vdc/6]	$I_C(*)$	I_A (C) and I_C (D)
	[Vdc,0,0]	[Vdc/2,0,Vdc/2]	[Vdc/6,-Vdc/6,0]	I_B	I_A (D) and I_B (C)
	[Vdc,Vdc,0]	[0,Vdc/2,0]	[Vdc/6,-Vdc/6,0]	I_B	I_A (D) and I_B (C)
M2 [7Vdc/6,Vdc/2,0]	[Vdc,0,0]	[0,0,Vdc/2]	[-Vdc/6,Vdc/6,Vdc/6]	I_C(*)	I_A (C) and I_B (D) and I_C (D)
	[Vdc,0,0]	[Vdc/2,0,Vdc/2]	[Vdc/6,0,0]≡[0,-Vdc/6,-Vdc/6]	I_B	I_A (D) / I_B (C) and I_C (C)
	[Vdc,Vdc,0]	[0,Vdc/2,0]	[Vdc/6,0,0]≡[0,-Vdc/6,-Vdc/6]	I_B	I_A (D) / I_B (C) and I_C (C)
M3 [7Vdc/6,2Vdc/3,0]	[Vdc,0,0]	[Vdc/2,0,Vdc/2]	[Vdc/6,Vdc/6,0]≡[0,0,-Vdc/6]	I_B	I_A (D) and I_B (D) / I_C (C)
	[Vdc,Vdc,0]	[0,Vdc/2,0]	[Vdc/6,Vdc/6,0]≡[0,0,-Vdc/6]	I_B	I_A (D) and I_B (D) / I_C (C)
	[Vdc,Vdc,0]	[0,Vdc/2,Vdc/2]	[-Vdc/6,-Vdc/6,Vdc/6]	I_A(*)	I_A (C) and I_B (C) and I_C (D)
M4 [7Vdc/6,5Vdc/6,0]	[Vdc,0,0]	[Vdc/2,0,Vdc/2]	[0,Vdc/6,-Vdc/6]	I_B	I_B (D) and I_C (C)
	[Vdc,Vdc,0]	[0,0,0]	[Vdc/6,-Vdc/6,0]	N	I_A (D) and I_B (C)
	[Vdc,Vdc,0]	[0,Vdc/2,0]	[0,Vdc/6,-Vdc/6]	I_B	I_B (D) and I_C (C)
	[Vdc,Vdc,0]	[0,Vdc/2,Vdc/2]	[-Vdc/6,0,Vdc/6]	I_A(*)	I_A (C) and I_C (D)

Note: The charging and discharging status of HB capacitors for positive phase currents defined by "C" and "D" respectively.

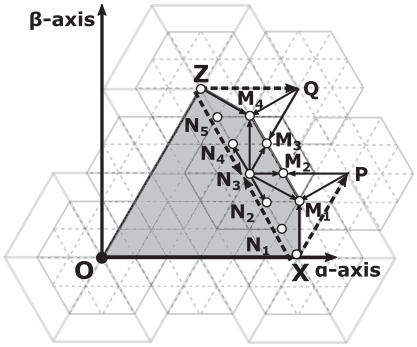

Fig. 6. SV redundancy for an eight-level VPs.

$\overrightarrow{XN_3}$ and $\overrightarrow{ZN_3}$ have a balancing effect on C_{sec} using the B-phase current, vector $\overrightarrow{ZN_3}$ is a nonredundant. Hence, C_{sec} will discharge by carrying a C-phase current. Similarly, for VP M_2, secondary two-level vector XP, and for VPs M_3, M_4 two-level vector $\overrightarrow{ZQ}$ along A-phase would be utilized to generate three-level HB SV further. Thus, the common secondary capacitor C_{sec} will discharge due to nonredundant vectors $\overrightarrow{XP}$ and $\overrightarrow{ZQ}$ in sector-I of the proposed SVS while extending the peak phase fundamental. The C_{sec} voltage will discharge more in case of upf load operation of the inverter [18]. In Table II, respective charging or discharging currents [depending on load power factor (pf)] through the secondary C_{sec} capacitor are given for eight-level VP redundancies in sector-1. At extended MR, to yield a peak phase fundamental of $0.637V_{\text{dc}}$, C_{sec} must remain balanced so that other HB capacitors voltages remain at nominal values. The following equations illustrate the charging status of the common secondary capacitor C_{sec} for the eight-level VPs in sector-I.

Instantaneous discharging energies at eight-level VPs for specific HB vectors

$$\begin{aligned}
E_{D/M_1}(t) &= (V_{\text{dc}}/2).I_C(t).(d_{M_1}(t)/3), \text{when } PM_1 \text{ applied}\\
E_{D/M_2}(t) &= (V_{\text{dc}}/2).I_C(t).(d_{M_2}(t)/3), \text{when } PM_2 \text{ applied}\\
E_{D/M_3}(t) &= (V_{\text{dc}}/2).I_A(t).(d_{M_3}(t)/3), \text{when } QM_3 \text{ applied}\\
E_{D/M_4}(t) &= (V_{\text{dc}}/2).I_A(t).(d_{M_4}(t)/3), \text{when } QM_4 \text{ applied.}
\end{aligned} \tag{8}$$

Instantaneous charging energies at eight-level VPs for specific HB vectors

$$\begin{aligned}
E_{C/M_1}(t) &= (V_{\text{dc}}/2).I_B(t).(d_{M_1}(t)/3), \text{when } N_3M_1 \text{ applied}\\
E_{C/M_2}(t) &= (V_{\text{dc}}/2).I_B(t).(2d_{M_2}(t)/3), \text{when } N_3M_2 \text{ and}\\
&\qquad \text{summation of } (N_3M_3 + N_3N_2) \text{ applied}\\
E_{C/M_3}(t) &= (V_{\text{dc}}/2).I_B(t).(2d_{M_3}(t)/3), \text{when } N_3M_3 \text{ and}\\
&\qquad \text{summation of } (N_3M_2 + N_3N_4) \text{ applied}\\
E_{C/M_4}(t) &= (V_{\text{dc}}/2).I_B(t).(d_{M_4}(t)/3), \text{when } N_3M_4 \text{ applied.}
\end{aligned} \tag{9}$$

Charging of C_{sec} can also be done at seven-level VPs $(N_1, N_2, N_3, N_4, N_5)$ along XZ line as

$$\begin{aligned}
E_{C/p}(t) &= (V_{\text{dc}}/2).I_B(t).(2d_p(t)/3),\\
&\qquad \text{where } p = N_1, N_2, N_4, N_5\\
E_{C/N_3}(t) &= (V_{\text{dc}}/2).I_B(t).d_{N_3}(t).
\end{aligned} \tag{10}$$

In the aforementioned equations, $E_{D/M_x}(x = 1, 2, 3, 4)$ defines the energy discharged and $E_{C/M_x}(x = 1, 2, 3, 4)$ defines charging energy while eight-level VPs are applied. The corresponding timing durations for which C_{sec} discharges are third of eight-level VP dwell time $d_{M_x}(x = 1, 2, 3, 4)$ since for other two HB vector combination C_{sec} may charge or get bypassed. Therefore, charging of C_{sec} can be done at seven-level as well as eight-level VPs as described by (9) and (10). The B-phase current is only responsible for charging the C_{sec} capacitor in sector-I. Further, it can be proved that in the trapezoidal region XM_1M_4ZX, the total energy discharged from C_{sec} always would be less than equal to total possible charging energy for C_{sec} (in case of upf load operation in ideal condition, $E_{D/\text{total}} = E_{C/\text{total}}$, whereas for any other pf, $E_{D/\text{total}} < E_{C/\text{total}}$). Hence, the MR can be increased linearly through PWM operation till peak phase fundamental of $0.637V_{\text{dc}}$ without any presence of lower order harmonics since all the capacitors are balanced irrespective of load pf.

$$E_{D/\text{total}} \leq E_{C/\text{total}-8\text{levelVPs}} + E_{C/\text{total}-7\text{levelVPs}}. \tag{11}$$

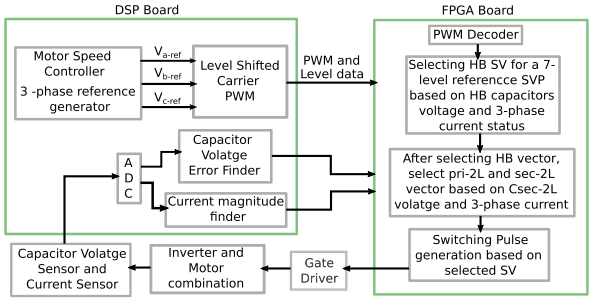

Fig. 7. Controller diagram and flowchart of the proposed scheme.

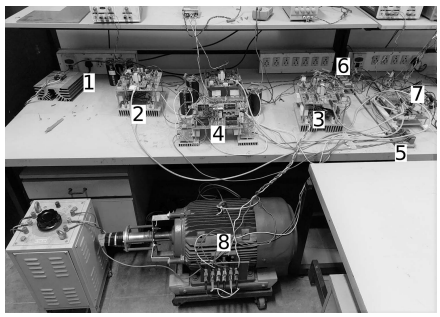

Fig. 8. Hardware prototype of the proposed seven-level inverter. 1) DC link. 2) Primary two-level inverter. 3) Secondary two-level inverter. 4) Three-level HBs. 5) Current sensor. 6) Voltage sensor. 7) DSP FPGA controller. 8) OEWIM.

IV. Hardware Implementation

The experimental prototype of the proposed inverter scheme has been developed in the Lab. TI TMS320F28335 is used in conjunction with the Spartan XC3S200 FPGA platform to implement capacitor balancing logic and consequent PWM signal generation. The DSP ADC measures capacitor voltages, phase current magnitudes, and directions and determines whether the capacitors are overcharged or undercharged and the maximum deviated HB phase. The DSP will also generate PWM signal and level data. These information are then transmitted to the FPGA to generate a set of switching signals accordingly for the gate driver board based on a lookup table. The controller diagram of the proposed inverter scheme is shown in Fig. 7. The switch complements each other with a dead time of $1.5\ \mu$s.

An OEWIM of 200 V, 50 Hz, 4-pole, 5-kW rating has been used to showcase experimental validation in steady state (open-loop *V/f* control) and transient state (closed-loop rotor field oriented control) conditions (see Fig. 8). The power switches used in the inverter circuit are SKM100GB12T4 for primary and secondary two-level and IRF240 N for HBs. For the duration of the experiment, the inverter setup is linked to a 200-V dc source. Accordingly, the nominal voltage of C_{sec} and C_{HB} capacitors must be regulated at 100 and 33.33 V, respectively. Over the entire fundamental frequency range, the sampling frequency of the inverter is kept at around 2 kHz. To design capacitors value keeping a 5% margin of error around the nominal value, $C = I_P/(f_s * \delta V)$ is used, where I_P is peak phase current, f_s is 2 kHz, and δV is an acceptable margin of error in capacitor voltage. In this case, C_{sec} and C_{HB} values are calculated as equal to 0.5 and 1.5 mF, respectively. However, in light of laboratory availability, C_{sec} and C_{HB} values are considered 2.2 mF.

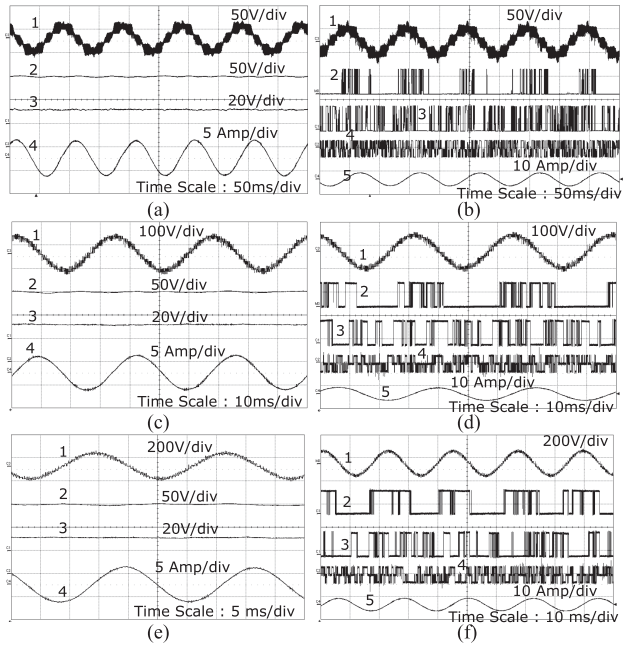

Fig. 9. Steady-state *V/f* operation results. (a) and (b) 10 Hz, (c) and (d) 30 Hz, and (e) and (f) 45 Hz. Traces in (a), (c), and (d):- 1) Phase voltage(V_{A2A3}); 2) secondary C_{sec} capacitor voltage; 3) A-phase C_{HB} capacitor voltage; 4) phase current (5 A/div). Traces in (b), (d), and (f):- 1) phase voltage (V_{A2A3}); 2) primary two-level pole voltage (V_{A1O1}) (200 V/div); 3) secondary two-level pole voltage (V_{A3O2}) (100 V/div); 4) three-level HB pole voltage (V_{A2A1}) (100 V/div); and 5) phase current (10 A/div).

V. Experimental Results

A. Inverter Operation Upto Seven-Level Mode

The proposed inverter scheme operates till seven-level mode for peak phase fundamental less than $0.577V_{\text{dc}}$. The motor is run at different frequencies in steady-state under open-loop *V/f* speed control mode (see Fig. 9). In Fig. 9(a), (c), and (e), motor A phase voltage, current and voltage status of C_{sec} and C_{HB} capacitors are shown. For all three frequencies—10, 30, and 45 Hz, the voltages of the capacitors are regulated perfectly around nominal values of 100 and 33.33 V, respectively for C_{sec} and C_{HB}. On the other hand, Fig. 9(b), (d), and (f) depict A-phase pole voltage waveforms of primary two-level, secondary two-level, and three-level HB for 10, 30, and 45 Hz, respectively. Out of these three pole voltages, three-level HB has the highest switching transitions. The reason is full utilization of HB SV level as compared to previous work [16], [22]. Although it may increase switching loss, low-voltage MOSFETs are being used to compensate it.

It is possible to validate the dynamic performance of the proposed inverter scheme by reversing the speed from -35 to +35 Hz under field-oriented control [see Fig. 10(a) and (b)]. It corresponds to the sudden loading of the inverter. The torque component of the motor current I_{sq} increases instantaneously with the speed change command's initiation, hits the peak value, and settles as soon as the motor speed reaches a steady state. During this transition mode, the magnetizing component of the motor current I_{sd} remain constant without any coupling effect with I_{sq}. As shown in Fig. 10(b), the voltage of both C_{sec} and C_{HB} capacitors is also strictly controlled when speed is reversed.

TABLE III
COMPARISON OF THE PROPOSED WORK WITH EXISTING INVERTER SCHEMES WITH EXTENDED LMR

Inverter scheme	Device count	Capacitor count	Maximum linear modulation range(LMR)
Five-level inverter with extended LMR [16]	Vdc-6, Vdc/4-12, Vdc/2-6	Vdc/2-1, Vdc/4-3	0.637Vdc peak phase fundamental irrespective of load pf.
Nine-level inverter with extended LMR [15]	Vdc/2-12, Vdc/6-12	Vdc/2-2, Vdc/6-3	0.607Vdc peak phase fundamental irrespective of load pf. Full dc bus utilization is not possible.
Ten-level inverter with extended LMR [22]	Vdc-6, Vdc/2-6, Vdc/4-12, Vdc/8-12	Vdc/2-1, Vdc/4-3, Vdc/8-3	0.637Vdc peak phase fundamental irrespective of load pf.
Seven-level hybrid clamped inverter with boosted Nine-level [17]	Vdc/3-24, Vdc/6-12	Vdc/3-6, Vdc/6-3	0.634Vdc peak phase fundamental irrespective of load pf. Full dc bus utilization is not possible.
Proposed 7-level inverter with extended LMR	Vdc-6, Vdc/2-6, Vdc/6-12	Vdc/2-1, Vdc/6-3	0.637Vdc peak phase fundamental irrespective of load pf.

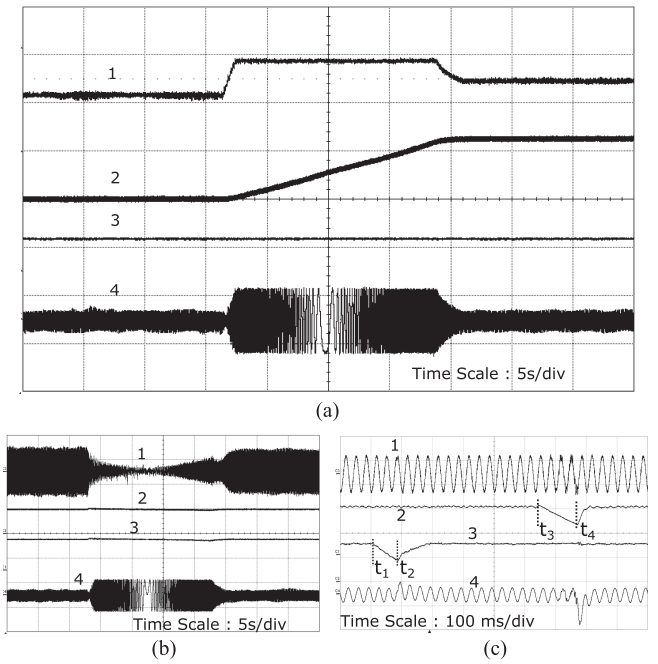

Fig. 10. (a) and (b) Field-oriented control results for speed reversal from -35 to +35 Hz. Traces in (a):- 1) I_{sq} torque producing component of stator current (10 A/div); 2) speed reversal from -35 Hz to +35 Hz (40 Hz/div); 3) I_{sd} magnetizing flux producing component of stator current (1.5 A); and 4) stator current (10 A/div). Traces in (b):- 1) phase voltage (100 V/div); 2) secondary common C_{sec} capacitor (100 V/div); 3) A-phase C_{HB} capacitor (50 V/div); and 4) stator current (10 A/div). (c) Independent control of C_{sec} and C_{HB} capacitor :- 1) phase voltage (100 V/div); 2) C_{sec} voltage (100 V/div); 3) A-phase C_{HB} capacitor voltage (20 V/div); and 4) Phase Current (10 A/div).

Furthermore, Fig. 10(c) proves the feasibility and robustness of the proposed capacitor balancing algorithm. In trace 10.(c)-3, A-phase HB capacitor voltage controller is disabled at t_1 instant. Therefore, it starts to discharge after t_1 and charged back to a nominal value after t_2 timing instant when the controller is enabled again. Similarly, C_{sec} capacitor started to discharge after t_3 and charged back to nominal voltage after t_4, respectively, after disabling and enabling secondary two-level capacitor controller. It is also worthy to note that capacitors controllers are independent from each other in the sense that deviation in C_{HB} does not affect C_{sec} and vice versa.

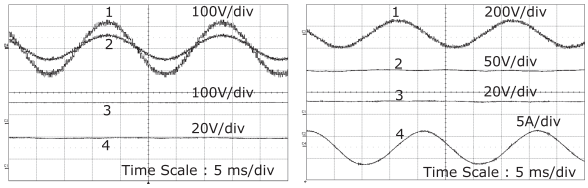

Fig. 11. Eight level mode operation of the proposed inverter scheme at steady state. (a) Resistive load (upf). Traces—1) phase voltage(V_{A2A3}); 2) phase current; 3) C_{HB} capacitor voltage; and 4) C_{sec} capacitor voltage. (b) Motor load (lagging pf). Traces—1) phase voltage (V_{A2A3}); 2) C_{sec} capacitor voltage; 3) C_{HB} capacitor voltage; and 4) phase current.

B. Inverter Operation at Eight-Level Mode

As proposed, the main objective of this work to increase the MR till peak phase fundamental of $0.637V_{\text{dc}}$ (50 Hz operation in case of *V/f*) devoid of lower order harmonics across the phase. When the inverter reaches its peak phase fundamental of $0.577V_{\text{dc}}$ (over 45 Hz in case of *V/f* operation), it begins to operate in eight-level PWM mode, as shown in Figs. 11 and 12. A resistive load of 50Ω in each phase is connected to verify upf load operation at an increased MR (0.637, peak phase fundamental) [see Fig. 11(a)]. A steady-state *V/f* operation at 50 Hz for the OEWIM load is shown in Fig. 11(b). All the capacitors voltages are maintained at nominal values in both lagging and upf mode. It validates the proposed indirect SV redundancy algorithm even at an extended modulation region. Thenceforth, a comparison of the proposed inverter scheme at extreme MR with the conventional six-step mode of operation is depicted in Fig. 12. In Fig. 12(a) and (d) (traces 1 and 2), α- and β-axes projections of the phase voltage are shown along with phase current (trace-3). These projections construct circular SV trajectory [see Fig. 12(b)] for the proposed modulation scheme and hexagonal SV trajectory [see Fig. 12(e)] for the six-step mode of operation. Therefore, while operating in the proposed eight-level mode, all lower order harmonics are eliminated from phase voltage [see Fig. 12(c)], whereas conventional six-step mode operation retains all lower order harmonics in phase voltage [see Fig. 12(f)]. Thus, the proposed inverter scheme can extend the MR till $0.637V_{\text{dc}}$ peak phase fundamental without the presence of any lower order harmonics irrespective of load pf.

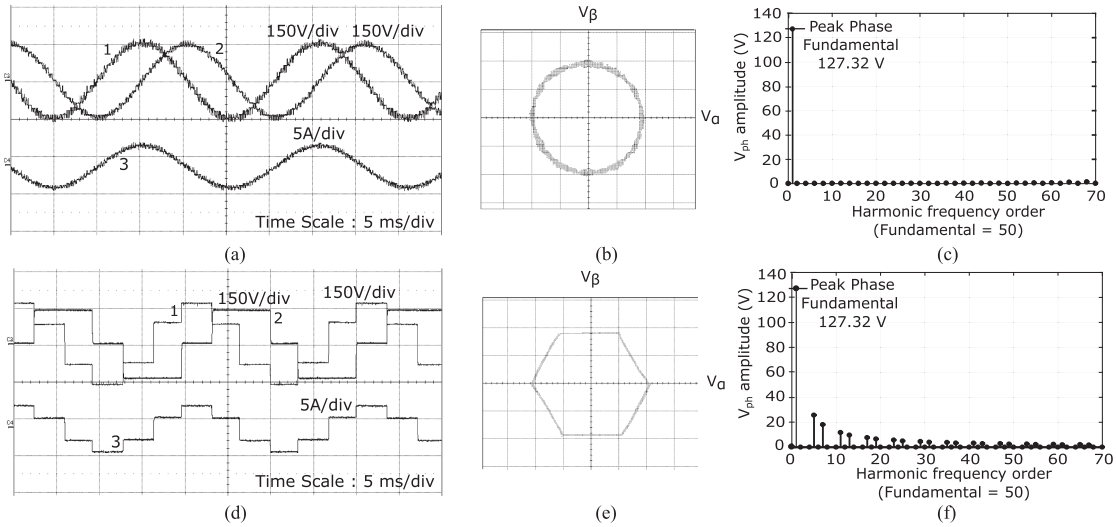

Fig. 12. Operation of the proposed inverter scheme at extreme MR ($0.637V_{\rm dc}$ peak phase fundamental) for resistive load (upf). (a) Proposed eight-level mode operation (peak phase fundamental $0.637V_{\rm dc}$) and (d) conventional six-step mode (peak phase fundamental $0.637V_{\rm dc}$)—1) α-axis projection of phase voltage; 2) β-axis projection of phase voltage; 3) phase current. (b) and (e) SV trajectory of phase voltage for proposed eight-level 50-Hz operation and conventional six-step 50-Hz operation, respectively. (c) and (f) Comparison of harmonic frequency spectrum of phase voltage waveform for proposed eight-level 50-Hz operation and conventional six-step 50-Hz operation, respectively.

VI. Comparison Study in Terms of Increasing LMR

A comparison of the proposed work with the latest works is shown in Table III. The comparison is made in respect of increasing the LMR till $0.637V_{\rm dc}$ peak phase fundamental for different MLI topologies. In previous works, extension in LMR till 0.637Vdc peak phase fundamental is done for a five-level [16] and a ten-level inverter [22]. However, these two inverters underutilized the HB capacitors, since only two SV levels of the HB are utilized instead of 3 SV levels (which is described in Section III). The authors in [15] show a seven-level inverter with an extended nine-level mode, which can increase the LMR only up to $0.607V_{\rm dc}$. A seven-level hybrid clamped inverter with boosted nine-level extends the LMR till $0.634V_{\rm dc}$. Since for upf load, capacitor balancing is critical, as explained in [18], maximum extension in LMR is measured for the upf load. The proposed seven-level hybrid inverter scheme can extend the LMR till the maximum possible peak phase fundamental $0.637V_{\rm dc}$ for upf load.

VII. Conclusion

This article describes the linear extension of MR for a hybrid seven-level inverter. The proposed seven-level inverter forms an open-end winding topology where primary side is comprised of a two-level inverter and a three-level HB in cascade and secondary side is supplied by a common floating capacitor-fed two-level inverter. This power circuit generates a 12-sided eight-level SVS compared to hexagonal voltage SVS of the conventional scheme by full utilization of HB SV levels. Using this proposed SVS, the MR in the proposed scheme can be extended by increasing the radius of the inscribed circular voltage SV. A concept of indirect SV redundancy is employed here to balance the HB capacitor voltages. The experimental results for different steady-state and transient conditions proves the validity of this inverter scheme. The following points highlight the key aspects of the proposed inverter scheme.

1) It increases the MR linearly from $0.577V_{\rm dc}$ to $0.637V_{\rm dc}$ peak phase fundamental, first time for a seven-level inverter.

2) Due to PWM operation at extended modulation region, all lower order harmonics can be eliminated from the phase voltages as compared to conventional methods.

3) The proposed inverter scheme can be helpful during intermittent voltage drops in the dc link, as it can provide an 11% ($0.637V_{\rm dc}/0.577V_{\rm dc}$) extension in phase voltage amplitude.

4) This topology is capable of extending MR up to $0.637V_{\rm dc}$ peak phase fundamental irrespective of any load pf.

References

[1] S. Kouro et al., "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[2] J. I. Leon, S. Vazquez, and L. G. Franquelo, "Multilevel converters: Control and modulation techniques for their operation and industrial applications," *Proc. IEEE*, vol. 105, no. 11, pp. 2066–2081, Nov. 2017.

[3] M. R. Baiju, K. K. Mohapatra, R. S. Kanchan, and K. Gopakumar, "A dual two-level inverter scheme with common mode voltage elimination for an induction motor drive," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 794–805, May 2004.

[4] S. Chowdhury, P. W. Wheeler, C. Patel, and C. Gerada, "A multilevel converter with a floating bridge for open-end winding motor drive applications," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5366–5375, Sep. 2016.

[5] M. G. Majumder, A. K. Yadav, K. Gopakumar, K. Raj R., U. Loganathan, and L. G. Franquelo, "A 5-Level inverter scheme using single DC link with reduced number of floating capacitors and switches for open-end IM drives," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 960–968, Feb. 2020.

[6] Y. Oto, T. Noguchi, T. Sasaya, T. Yamada, and R. Kazaoka, "Space vector modulation of dual-inverter system focusing on improvement of multilevel voltage waveforms," *IEEE Trans. Ind. Electron.*, vol. 66, no. 12, pp. 9139–9148, Dec. 2019.

[7] C. Perera, G. J. Kish, and J. Salmon, "Decoupled floating capacitor voltage control of a dual inverter drive for an open-ended winding induction motor," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7305–7316, Jul. 2020.

[8] R. Kanchan, K. Gopakumar, and R. Kennel, "Synchronised carrier-based SVPWM signal generation scheme for the entire modulation range extending up to six-step mode using the sampled amplitudes of reference phase voltages," *IET Elect. Power Appl.*, vol. 1, no. 3, pp. 407–415, May 2007.
[9] S. Busquets-Monge, R. Maheshwari, and S. Munk-Nielsen, "Overmodulation of n-level three-leg DC–AC diode-clamped converters with comprehensive capacitor voltage balance," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1872–1883, May 2013.
[10] F. Guo et al., "An overmodulation algorithm with neutral-point voltage balancing for three-level converters in high-speed aerospace drives," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 2021–2032, Feb. 2022, doi: 10.1109/TPEL.2021.3105752.
[11] A. R. S, S. Pramanick, R. S. Kaarthik, K. Gopakumar, and F. Blaabjerg, "Extending the linear modulation range to the full base speed using a single DC-Link multilevel inverter with capacitor-fed H-bridges for IM drives," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5450–5458, Jul. 2017.
[12] T. Abhilash, K. Annamalai, and S. V. Tirumala, "A seven-level VSI with a front-end cascaded three-level inverter and flying-capacitor-fed H-bridge," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 6073–6088, Nov./Dec. 2019.
[13] H. Yu, B. Chen, W. Yao, and Z. Lu, "Hybrid seven-level converter based on T-type converter and H-bridge cascaded under SPWM and SVM," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 689–702, Jan. 2018.
[14] T. T. Davis and A. Dey, "Enhanced floating capacitor voltage balancing schemes for single-source seven-level inverters with capacitor fed H-bridge units," *IEEE Trans. Ind. Electron.*, vol. 67, no. 8, pp. 6227–6236, Aug. 2020.
[15] T. T. Davis, T. Joseph, and A. Dey, "A capacitor voltage balancing scheme for single-source fed switch optimized three-phase nine-level inverter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 5, pp. 3652–3661, May 2021.
[16] M. G. Majumder, R. Rakesh, M. Imthias, K. Gopakumar, U. Loganathan, and W. Jarzyna, "Extending the linear modulation range to full base speed independent of load power factor for a multilevel inverter fed IM drive," *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9143–9152, Nov. 2020.
[17] H. Tian, L. Ding, and Y. W. Li, "Boosting nine-level operation of seven-level hybrid-clamped (7L-HC) converter," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6265–6270, Jun. 2022.
[18] S. Pal et al., "A cascaded nine-level inverter topology with T-type and H-bridge with increased DC-Bus utilization," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 285–294, Jan. 2021.
[19] S. Pramanick, N. Azeez, R. S. Kaarthik, K. Gopakumar, and C. Cecati, "Low-order harmonic suppression for open-end winding IM with dodecagonal space vector using a single dc-link supply," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5340–5347, Sep. 2015.
[20] M. Boby, A. R. S. K. Gopakumar, L. Umanand, F. Blaabjerg, and S. Bhattacharya, "A low-order harmonic elimination scheme for induction motor drives using a multilevel octadecagonal space vector structure with a single DC source," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2430–2437, Mar. 2018.
[21] R. R. K. R. Ramachandran, A. K. Yadav, K. Gopakumar, L. Umanand, and K. Matsuse, "A switched capacitive filter-based harmonic elimination technique by generating a 30-Sided voltage space vector structure for IM drive," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2402–2410, Mar. 2020.
[22] S. Pal et al., "A ten level inverter fed drive scheme with extended linear modulation range," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12261–12269, Dec. 2022.

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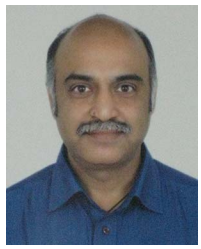

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