A High Power Density Wide Range DC–DC Converter for Universal Electric Vehicle Charging

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***Abstract*—This article presents a single stage isolated bidirectional DC–DC converter comprising of LCL-T resonant network for universal electric vehicle (EV) charging. Fixed frequency operation along with phase-shift control enables easier design of passive components, while achieving high efficiency across wide output voltage range. Furthermore, to increase the switching frequency and consequently the power density, gallium nitride (GaN) switches are explored in the proposed solution. In order to facilitate use of commercially available 650 V GaN transistors, a multi-level inverter and a reconfigurable rectifier architecture is utilized along with LCL-T resonant network, accommodating an input voltage of 800 V, generated from an universal three phase ac input supply, and an output voltage ranging from 150 V to 950 V catering to large variation of battery voltages from different vehicle manufacturers. The constant input voltage-to-output current gain property of LCL-T network, along with an efficient phase-shift modulation proposed in this paper enable soft switching of all transistors with minimum circulating currents over constant current (CC), constant power (CP), and constant voltage (CV) modes of battery charging. Experimental results are provided for a single-phase DC–DC converter prototype utilizing 650 V GaN transistors operating from an 800 V DC bus and providing a very wide output voltage from 150 V to 950 V at 6.6 kW maximum power at a constant switching frequency of 500 kHz. The prototype achieves two peak efficiency points of 98.2% and maintains $>$ 97% efficiency across the entire output voltage range at a power density of 120 W/in^3 (7.3 kW/L).**

***Index Terms*—Charging stations, current source converter, efficiency optimized phase-shift control, fixed frequency control, gallium nitride (GaN), LCL-T resonant converter, on-board charger, universal electric vehicle (EV) charging.**

I. Introduction

With increased proliferation and penetration of electric vehicles (EV) in automotive industry, importance of charging infrastructure grows and the demand of higher efficiency and power density increases. Furthermore, with increasing demand of fast charging to alleviate range anxiety and reduced charging time, the peak power demand for the charging facility has increased [1], [2]. A conventional two-stage ac–dc power delivery architecture for on board or off board battery charging is shown in Fig. 1 with a front-end PFC stage followed by an isolated dc–dc charging converter. To support higher power demand for fast charging, generally three phase 480 V ac input is being used with a front end PFC stage providing regulated or semi regulated 800 V bus [3], [4]. Typically, the forthcoming trend is to move up to 22 kW charging converters utilizing three phase interleaved dc–dc stages, hence requiring 6.6–7.2 kW power from a single phase dc–dc converter. For off-board charging station applications, two mainstream charging connector protocols are CHArge de MOve (CHAdeMO) and combined charging system (CCS) catering to different ranges of battery voltage levels. Usually, CHAdeMO covers relatively low voltage battery up to 500 V, and CCS covers relatively high voltage battery up to 950 V [4], [5], [6]. In order to be compatible with all EVs adapting either CHAdeMO or CCS, it is required to develop a universal EV charger that covers an extremely wide range of the battery voltage. DC/DC converter for the universal charger needs to achieve high efficiency over the entire output voltage range. Similarly for on board charging, to keep up with operating voltage ranges of low voltage (LV) and high voltage (HV) batteries from original equipment manufacturers (OEMs), a very wide output voltage range operation of 150–950 V needs to be covered using the dc–dc stage with high efficiency, imposing significant challenges in the converter topology selection and modulation [7].

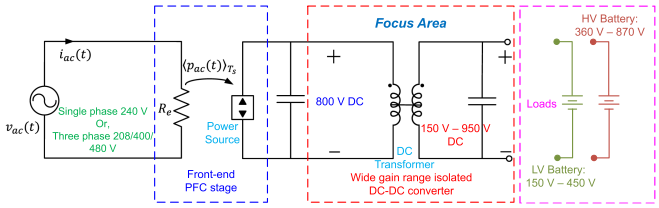

Fig. 1. Conceptual representation of a conventional two-stage ac–dc power delivery architecture for on board or off board EV charging, comprising a single-phase or, three-phase universal input front-end PFC stage followed by an isolated wide gain range dc–dc stage.

Another important consideration to this end, is the emergence of wide band gap (WBG) semiconductors. Fundamentally due to reduced reverse recovery charge and higher electron mobility, gallium nitride (GaN) and silicon carbide (SiC) based transistors enable bidirectional operation and significantly higher switching frequency and efficiency compared to their Si based counterparts [8]. Although there are 1.2 kV SiC transistors commercially available [9], GaN power transistors are still restricted to 650 V [10]. Hence, in order to leverage the superior switching performance of GaN power transistors from the 800 V PFC bus,

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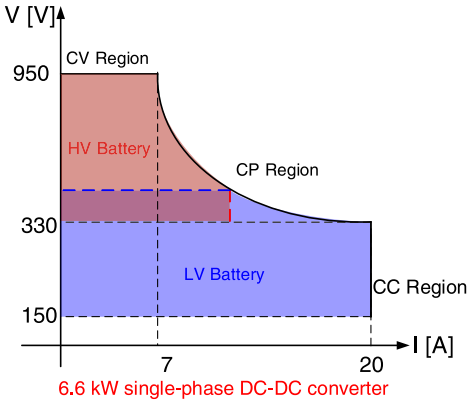


Fig. 2. Typical charging profile of a single phase dc–dc converter for EV charging applications encompassing entire voltage ranges of commercially available LV and HV batteries.

catering to an output voltage range of 150–950 V, multilevel switching circuits need to be considered.

Traditionally, series resonant converter or CLLC resonant converters have been the topologies under consideration in various charging applications due to their inherent capabilities of achieving soft-switching to minimize switching losses and allow high-frequency operation while maintaining high conversion efficiencies [11], [12], [13]. However, the major challenges with traditional resonant converter approaches like SRC or CLLC resonant tanks is their steep efficiency fall-offs when operated across wide gain ranges [14], [15]. To achieve wider gain range with reduced circulating currents and zero voltage switching (ZVS) several approaches have been identified in literature. Some of them use variable frequency control [16], while some adopt PWM control using introduction of boosting periods for standard SRC converters [4], [13].

An interesting alternative to traditionally used resonant converter topologies is a class of resonant networks known as immittance resonant converters [17]. These networks provide constant input voltage-to-output current gain making battery charging in constant current (CC) mode very efficient with wide output voltage variation. For constant power (CP) and constant voltage (CV) mode of operation, variations of such immittance networks have been proposed in literature [18], [19]. However, deployment of such immittance resonant topologies for higher power battery charging applications remain unexplored, where additional components can be detrimental to increased power density requirements. To address the questions regarding design, modulation, and performance of immittance network based resonant converters for EV charging applications, this article focuses on the charging profile shown in Fig. 2. It should be noted how, the intended output voltage range of the dc–dc converter spans from 150 to 950 V, with a maximum current of 20 A for LV batteries and 10 A for HV batteries. To deal with the wide variety of battery voltages from OEMs, the proposed solution aims to find a single, efficient dc–dc converter topology to cover the entire output voltage range.

The rest of this article is organized as follows: Section II discusses the multilevel inverter and reconfigurable rectifier approach to leverage the use of 650 V GaN transistors for the charging profile shown in Fig. 2. In this section, the fundamentals of a three element immittance network, known as the LCL-T network is revisited along with the derivation of its dc gain under synchronous rectification [20], [21]. Next, a phase-shift based, fixed frequency three-level modulation strategy is discussed in Section III. This novel modulation strategy, when applied to LCL-T immittance network, enables regulation of output current over CP and CV modes of charging, while maintaining ZVS of all transistors. This fixed frequency modulation strategy allows for optimized magnetics design and ease of control even at lighter loads. Section IV provides specific design considerations and component selection for a prototype converter adhering to the charging specifications of Fig. 2. In Section V, experimental results are provided for a GaN based isolated bidirectional dc–dc converter operating at 500 kHz fixed switching frequency across the entire load profile for a 6.6 kW charging converter. This converter achieves a power density of $120\,\mathrm{W/in^3}$ or, 7.3 kW/L with a peak efficiency of 98.2%. The experimental prototype is also capable of maintaining $>97\%$ efficiency throughout the entire output voltage range. Finally, Section VI concludes this article.

II. Topology Overview

Fig. 3 shows the circuit diagram of the proposed LCL-T network based isolated dc–dc converter for EV charging. In order to utilize 650 V GaN transistors from an 800 V input voltage, some form of multilevel inverter architecture is necessary. There are many inverter architectures such as flying capacitor multilevel (FCML) [22], neutral-point clamped (NPC) [23] or stacked half bridge (SHB) [24], which serve essentially the same purpose of reducing the voltage stress on the transistors. In comparison to FCML or NPC inverters, SHB inverters offer capacitors with reduced RMS current stress. Furthermore, the frequency multiplication effect offered by FCML or NPC circuit is not a necessary requirement for GaN based approaches as the transistors can switch relatively fast in soft switching applications and further increase in effective frequency can result in higher ac resistances of magnetic components. Hence, the SHB architecture is chosen for the inverter side. At the rectifier side two different approaches are adopted to cover low voltage and high voltage batteries. In Fig. 3(a) for the LV battery, where charging current requirement is high, two half bridges are connected in parallel to realize a full bridge (FB) rectifier, while for the HV battery, as shown in Fig. 3(b), the half bridges are stacked in a voltage doubler fashion. This reconfiguration can be easily achieved using dc relays, which does not add significant additional cost, but enables much better volt–ampere (VA) utilization of the switching transistors.

At the heart of this dc–dc converter is the LCL-T immittance network [17], [18], [21]. It consists of two resonant inductors: L_1, L_2 and a resonant capacitor: C along with an isolation transformer having primary to secondary turns ratio of $n:1$. It is interesting to note that the transformer magnetizing inductance

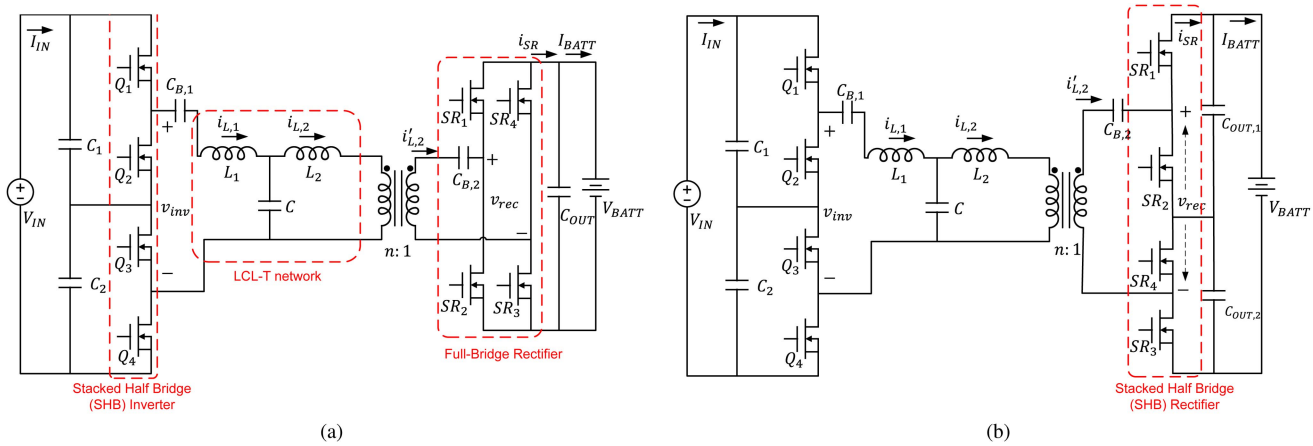


Fig. 3. Schematic of LCL-T resonant network based wide range isolated bidirectional resonant dc–dc converter with (a) full-bridge (FB) rectifier for LV battery charging and (b) stacked half–bridge (SHB) rectifier or, voltage doubler rectifier for HV battery charging. In both cases the primary side uses a SHB inverter with a constant input voltage of $V_{IN} = 800$ V provided from a front-end universal input three-phase power factor correction (PFC) stage.

can be infinitely large (subsequently very small magnetizing current), relieving it from storing any energy, which will result in a gapless transformer increasing it's efficiency and power density. Since the resonant network does not offer any series capacitors, two dc blocking capacitors are added at the inverter and rectifier side to prevent flux walking or saturation from any dc voltage being applied to the transformer. Although the "T" network shown in Fig. 3 is reminiscent of a multiple element resonant network [25], the constraints associated with immittance design make both inductances of L_1 and L_2 to be same and capacitor C resonate with them at the switching frequency [17]. Resulting in

$$L_1 = L_2 = L; C = \frac{1}{4\pi^2 f_s^2 L}. \tag{1}$$

With such a relation between the resonant components, under the sinusoidal approximation [26], a linear circuit approximation of the network can be obtained as shown in Fig. 4(a). In this linear approximation, the inverter port is modeled as a CV source with an amplitude equal to fundamental harmonic of the square wave inverter voltage shown in Fig. 4(b): $\hat{V}_{\text{inv,fund}} = \frac{2V_{IN}}{\pi}\angle 0$. It is interesting to note that the inductive impedances can be modeled as jX, whereas the capacitor simply resonates with the inductor offering an impedance of $-jX$ in the equivalent circuit approximation. Under synchronous rectification, where the rectifier transistors are switched as diodes, synchronized with the zero crossing of the transformer secondary current, the transformer along with the rectifier switches can be modeled as a resistor with $R_r = \frac{8n^2 V_{\text{BATT}}}{\pi^2 I_{\text{BATT}}}$ for a FB rectifier and $R_r = \frac{4n^2 V_{\text{BATT}}}{\pi^2 I_{\text{BATT}}}$ for a SHB rectifier [26], [27]. Now, the linear circuit depicted in Fig. 4(a) can be solved for the inductor currents $i_{L,1}$ and $i_{L,2}$. First, the input impedance seen from the inverter terminal can be found as

$$Z_{in} = jX + (-jX||(jX + R_r)) = \frac{X^2}{R_r}. \tag{2}$$

From (2), it is clear that the input impedance of the "T" network is purely resistive under synchronous rectification, which will result in an inductor current $\hat{I}_{L,1}$ in phase with the voltage $\hat{V}_{\text{inv}}$. Next, from the current divider in Fig. 4(a), inductor current $\hat{I}_{L,2}$ can be found from $\hat{I}_{L,1}$ as

$$\hat{I}_{L,1} = \frac{2V_{IN}R_r}{\pi X^2}\angle 0$$
$$\hat{I}_{L,2} = \hat{I}_{L,1}\frac{-jX}{R_r} = \frac{2V_{IN}}{\pi X}\angle -\frac{\pi}{2}. \tag{3}$$

Finally, once the inductor current $\hat{I}_{L,2}$ is determined, the dc output current for FB rectifier and SHB rectifier can be found from rectification and averaging of the secondary side transformer current $i'_{L,2}$

$$I_{\text{BATT},FB} = \langle i_{SR}\rangle = \frac{2n}{\pi}|\hat{I}_{L,2}| = \frac{4nV_{IN}}{\pi^2 X}$$
$$I_{\text{BATT},SHB} = \langle i_{SR}\rangle = \frac{n}{\pi}|\hat{I}_{L,2}| = \frac{2nV_{IN}}{\pi^2 X} \tag{4}$$

where i_{SR} indicates the rectified current $i'_{L,2}$ as shown in Fig. 3. From (3) and (4), a few important conclusions can be drawn. First, under synchronous rectification, the dc output current of the LCL-T network is independent of the output voltage [17]. Furthermore, the phase of the rectifier side inductor current $\hat{I}'_{L,2}$ is also fixed with output voltage variation and it lags the inverter excitation by a constant phase-shift of $\pi/2$. This feature of the resonant network is highlighted in Fig. 4(b), where the rectifier switching lags the inverter switching by a fixed time interval $T_s/4$. Hence, performing synchronous rectification for this topology is also simpler without the requirement of high bandwidth current sensing compared to other resonant approaches. This unique feature resulting in constant input voltage-to-output current gain with resistive input impedance (resulting in reduced circulating currents) enables high efficiency operation of the resonant network in CC mode of battery charging. However, the charging regions in CP and CV modes indicated in Fig. 2 need further attention. To address the issue of charging with reduced output current over these modes, the following section will aim to develop a modulation strategy, which enables soft switching of transistors along with relatively small circulating current across CP and CV modes of battery charging.

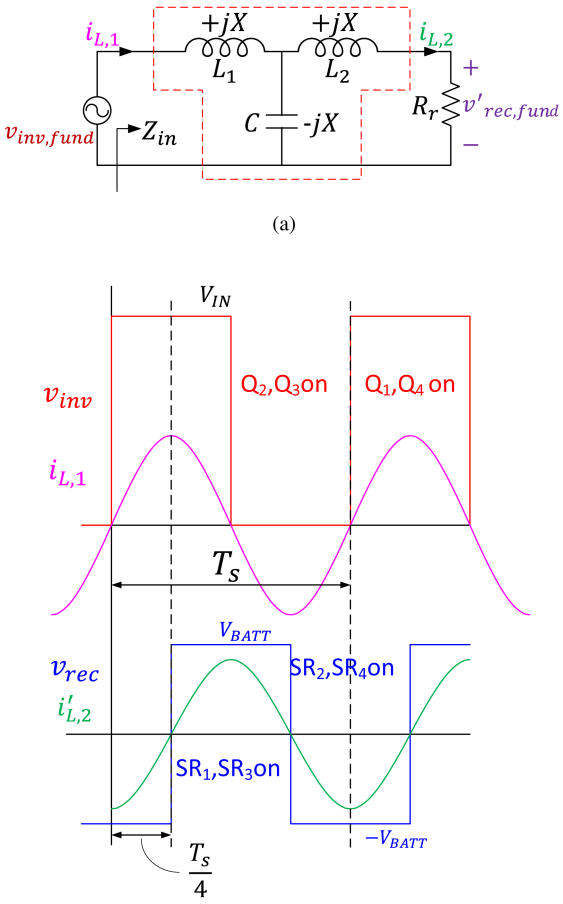


Fig. 4. (a) Equivalent circuit of LCL-T resonant dc–dc converter shown in Fig. 3 under Fundamental Harmonic Approximation and (b) Theoretical switching waveforms at inverter and rectifier nodes along with inductor currents utilizing synchronous rectification for FB rectifier mode of operation.

III. Phase-Shift Modulation for Wide Gain Range

In order to facilitate CP and CV mode of battery charging, the output current from the resonant converter need to be reduced as seen from the V-I profile of Fig. 2. For the LCL-T network based resonant converter discussed in the previous section, the dc output current is directly proportional to the excitation at the input of the resonant tank. The effect of input excitation on the output current is illustrated in (4) as well. Where the output charging current is directly proportional to the amplitude of inverter voltage excitation $|\hat{V}_{\text{inv,fund}}| = \frac{2V_{IN}}{\pi}$. Hence, it is intuitive to explore reduction of the inverter input voltage excitation for controlling the output current in CP and CV charging modes.

A. Three-Level Inverter Modulation

In the conventional two-level inverter modulation described in Fig. 4(b), transistors Q_1, Q_4 are gated together, whereas transistors Q_2, Q_3 are gated in a complimentary fashion to Q_1 and Q_4. This modulation generates the maximum amplitude of inverter voltage : $|\hat{V}_{\text{inv,fund}}|_{\max} = \frac{2V_{\text{IN}}}{\pi}$. This will consequently result in maximum charging current at the output. However, if the gate signals of Q_1 and Q_4 are phase-shifted with respect

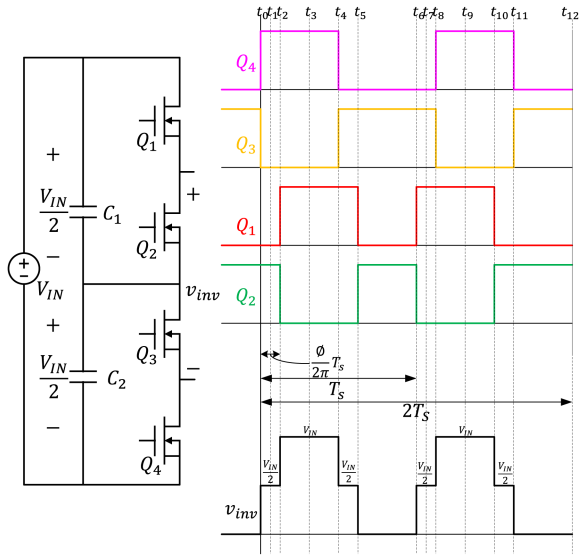


Fig. 5. Three-level inverter input voltage synthesized using phase-shifted modulation of the SHB inverter along with period doubling feature to ensure balanced current stress among all inverter transistors.

to each other, the SHB inverter can be used to generate output voltage as illustrated in Fig. 5 [24].

For such a three-level modulation, where during time interval $t_0 - t_2$ in Fig. 5, transistors Q_4 and Q_2 conduct together, a voltage level of $\frac{V_{\text{IN}}}{2}$ can be generated at the inverter output terminals. This interval is defined as $\frac{\phi}{2\pi}T_s$. During time interval of $t_2 - t_4$, V_{IN} voltage is generated by simultaneous gating of Q_1 and Q_4, followed by another $\frac{V_{\text{IN}}}{2}$ interval during $t_4 - t_5$, where Q_1 and Q_3 are turned ON together. Finally during $t_5 - t_6$ both Q_2 and Q_3 are turned ON to generate a voltage level of 0. Furthermore, to balance the current stress between all the switching transistors, the leading and lagging transistors among Q_1 and Q_4 are swapped in every alternate switching cycles [24], i.e., if in the first switching cycle, Q_4 gate signal leads Q_1, in the next cycle Q_1 gate signal will lead Q_4 by the same time, as illustrated in Fig. 5. Hence, although the transistors switch with a switching frequency of $f_s = 1/T_s$, the current carried by the transistors have an effective switching frequency of $f_s/2$ [24]. As the inverter output voltage v_{inv} is periodic with a frequency of f_s, Fig. 6 shows the three-level inverter voltage along with it's first harmonic. By calculating the Fourier series of the three-level switched waveform v_{inv} shown in Fig. 6, the first harmonic excitation voltage and subsequently under synchronous rectification, the dc output charging current from the LCL-T resonant converter can be found as

$$\hat{V}_{\text{inv,fund}} = \frac{2\cos\left(\frac{\phi}{2}\right)V_{\text{IN}}}{\pi}\angle -\frac{\phi}{2}$$

$$I_{\text{BATT,FB}} = \frac{4n\cos\left(\frac{\phi}{2}\right)V_{\text{IN}}}{\pi^2 X}$$

$$I_{\text{BATT,SHB}} = \frac{2n\cos\left(\frac{\phi}{2}\right)V_{\text{IN}}}{\pi^2 X}. \quad (5)$$

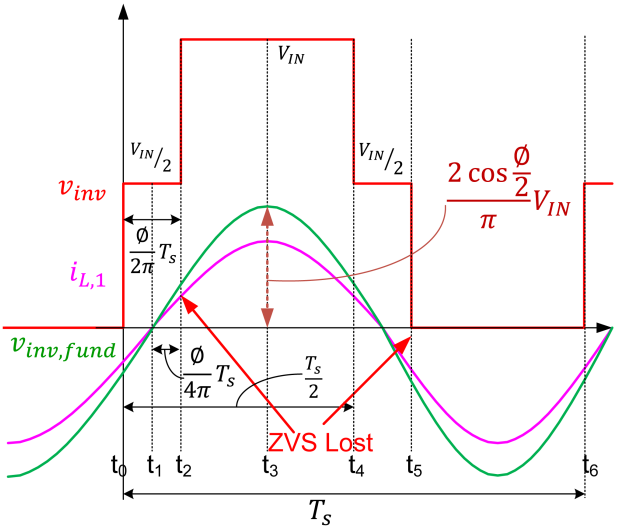


Fig. 6. Three-level inverter voltage and it's fundamental harmonic component $v_{\text{inv,fund}}$. Use of synchronous rectification results in $i_{L,1}$ and $v_{\text{inv,fund}}$ being in phase. Consequently loss of ZVS transitions occur at time instants t_2 and t_5.

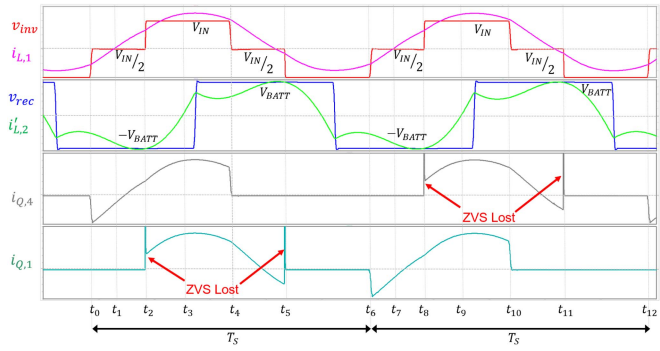


Fig. 7. Simulation waveforms illustrating effect of three-level inverter modulation with synchronous rectification. Although, control over output current is achieved along with balanced current stress of inverter transistors, ZVS is lost at $f_s/2$ frequency for every switching device.

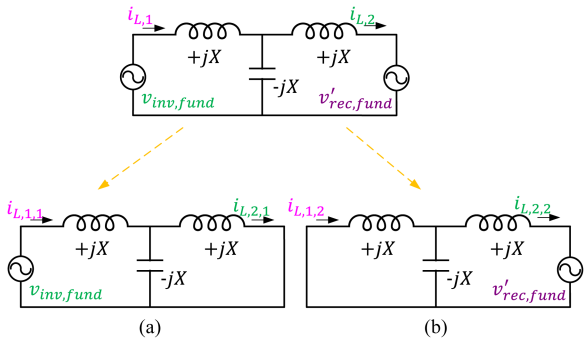


Fig. 8. Application of superposition theorem under active rectification on LCL-T resonant network. Under fundamental harmonic approximation, a linear circuit with two active sources can be used. Inductor currents $i_{L,1}$ and $i_{L,2}$ are independently solved when (a) only inverter source is active and (b) only rectifier source is active. Then, total currents can be obtained by simple phasor addition.

It should be noted how the same proportionality factor or, voltage-to-current gain between inverter voltage amplitude and output current in (4) is present in (5) as well. Hence, using the three-level inverter modulation, it is relatively easy to regulate the output current using the dc battery current expressions of (5). The control variable ϕ, which essentially dictates the amount of time spent in the voltage level $\frac{V_{\text{IN}}}{2}$ at the inverter switching node, controls the output current. However, as indicated earlier, under synchronous rectification, the inverter input impedance is purely resistive [see (2)]. Hence, under the inverter excitaion expressed in (5), the inductor current $i_{L,1}$ can be solved as

$$\hat{I}_{L,1} = \frac{2\cos\left(\frac{\phi}{2}\right)V_{\text{IN}}R_r}{\pi X^2}\angle -\frac{\phi}{2}. \tag{6}$$

Due to such resistive loading of the inverter, as shown in Fig. 6, the inductor current $i_{L,1}$ has a zero crossing at the time instant t_1, where $t_1 - t_0 = \frac{\phi}{4\pi}T_s$. As a consequence, in Fig. 6, although the switching transitions at time t_0 and t_4 can maintain ZVS for transistors Q_4 and Q_3, respectively, during the switching transitions at t_2 and t_5, the inductor current polarity is incorrect to achieve ZVS and transistors Q_1 and Q_2 turns ON under hard switching. In the next switching period, transistors Q_4 and Q_3 turns ON under hard switching conditions at timing instants t_8 and t_{11} as the relative phases between Q_4 and Q_1 are swapped in the next switching cycle (see Fig. 5). The loss of ZVS is further illustrated using simulated waveforms shown in Fig. 7. First, it is interesting to note how use of period doubling modulation explained in Fig. 5, makes RMS current stress in all the transistors well balanced and the effective switching frequency of the transistor currents become $f_s/2$. Furthermore, it is also shown how during switching transitions at timing instants t_2, t_5, t_8, and t_{11} transistors turn ON with hard switching. This prompts further adjustments in modulation scheme to enable ZVS for all transistors. As synchronous rectification will always result in resistive inverter input impedance, active rectification is explored next, to alleviate the hard switching issues with three-level inverter modulation. The main purpose of rectifier side control will be aimed at simultaneous power flow control and complete soft switching of the transistors.

B. Active Rectification for Complete Inverter ZVS

Using three-level inverter modulation, the control law derived in (5) provides an effective way to control the dc output current of LCL-T resonant network. But, in order to achieve ZVS at all switching transitions, active rectification strategies are explored in this section. With active rectification, the linear equivalent circuit used for analysis of the resonant network shown in Fig. 4(a) needs modification. As under fundamental approximation the rectifier port can not be simply modeled as a resistor anymore. Instead, as shown in Fig. 8, now the rectifier port reflected through the transformer can be modeled as an independent voltage source marked as $v'_{\text{rec,fund}}$. Next, to solve for the currents $i_{L,1}$ and $i_{L,2}$ using the linear circuit of Fig. 8, method of superposition can be applied. In Fig. 8(a) only the inverter source is active, and similarly in Fig. 8(b) only the source

at the rectifier port is active. From Fig. 8(a)

$$\hat{I}_{L,1,1} = \frac{\hat{V}_{\text{inv,fund}}}{jX + (-jX||jX)} = 0$$

$$\hat{I}_{L,2,1} = \frac{\hat{V}_{\text{inv,fund}}}{jX}. \tag{7}$$

Similarly from Fig. 8(b)

$$\hat{I}_{L,1,2} = -\frac{\hat{V}_{\text{rec,fund}}}{jX}$$

$$\hat{I}_{L,2,2} = \frac{\hat{V}_{\text{rec,fund}}}{jX + (-jX||jX)} = 0. \tag{8}$$

Finally, using superposition

$$\hat{I}_{L,1} = \hat{I}_{L,1,1} + \hat{I}_{L,1,2} = -\frac{\hat{V}_{\text{rec,fund}}}{jX} = \frac{\hat{V}_{\text{rec,fund}}}{X}\angle\frac{\pi}{2}$$

$$\hat{I}_{L,2} = \hat{I}_{L,2,1} + \hat{I}_{L,2,2} = \frac{\hat{V}_{\text{inv,fund}}}{jX} = \frac{\hat{V}_{\text{inv,fund}}}{X}\angle -\frac{\pi}{2}. \tag{9}$$

From (7) to (9), it can be found that both magnitude and phase of inductor current $i_{L,1}$ is only dependent on $v'_{\text{rec,fund}}$ and similarly inductor current $i_{L,2}$ (magnitude and phase) depends only on $v_{\text{inv,fund}}$. Utilizing this unique feature of the "T" network, the hard switching issue at the inverter side can be addressed using the following argument. Application of three-level switching with a controllable phase-shift ϕ at the inverter side results in a phase of $-\frac{\phi}{2}$ with respect to time t_0 for $v_{\text{inv,fund}}$ [see (5)]. In order to achieve ZVS of all inverter transitions, the required phase of inductor current i_{L1} is $-\phi$, where the second and final inverter switching event occurs, providing the correct polarity of inductor current to achieve ZVS (see Fig. 6). Since the inductor current $\hat{I}_{L,1}$ leads rectifier fundamental voltage $v'_{\text{rec,fund}}$ by a phase angle $\frac{\pi}{2}$ [see (9)], the required phase of rectifier voltage $\hat{V}'_{\text{rec,fund}}$ is $\pi/2 + \phi$ with respect to time t_0, in order to ensure ZVS of all inverter transistors. On the other hand, for the rectifier side inductor current $i_{L,2}$, which lags fundamental of the inverter voltage by $\frac{\pi}{2}$ [see (9)], the zero crossing of $\hat{I}'_{L,2}$ is at $\frac{\phi+\pi}{2}$. Hence, delaying the rectifier transitions until any point before $\pi + \frac{\phi}{2}$ automatically ensures ZVS of rectifier transistors as well. To summarize, the objective of achieving complete ZVS of all transistors can be met by synthesizing a rectifier fundamental voltage that lags the inverter fundamental voltage $\hat{V}_{\text{inv,fund}}$ by $\frac{\pi+\phi}{2}$ (and lags the inductor current $\hat{I}_{L,2}$ by $\frac{\phi}{2}$). However, this fundamental voltage can be synthesized using both two-level and three-level switching of rectifier transistors. The next section will discuss the relative merits and demerits associated with these two approaches.

C. Two-Level and Three-Level Active Rectification

Fig. 9 shows two different modulation approaches using active rectification, with an example FB rectifier. Application of SHB rectifier will result in half the excitation at $v'_{\text{rec,fund}}$ port in Fig. 8 compared to full bridge rectification and the dc component in the rectifier voltage ($V_{\text{BATT}}/2$) will be applied across capacitor $C_{B,2}$. Consequently, the magnitude of inductor current $i_{L,1}$ will

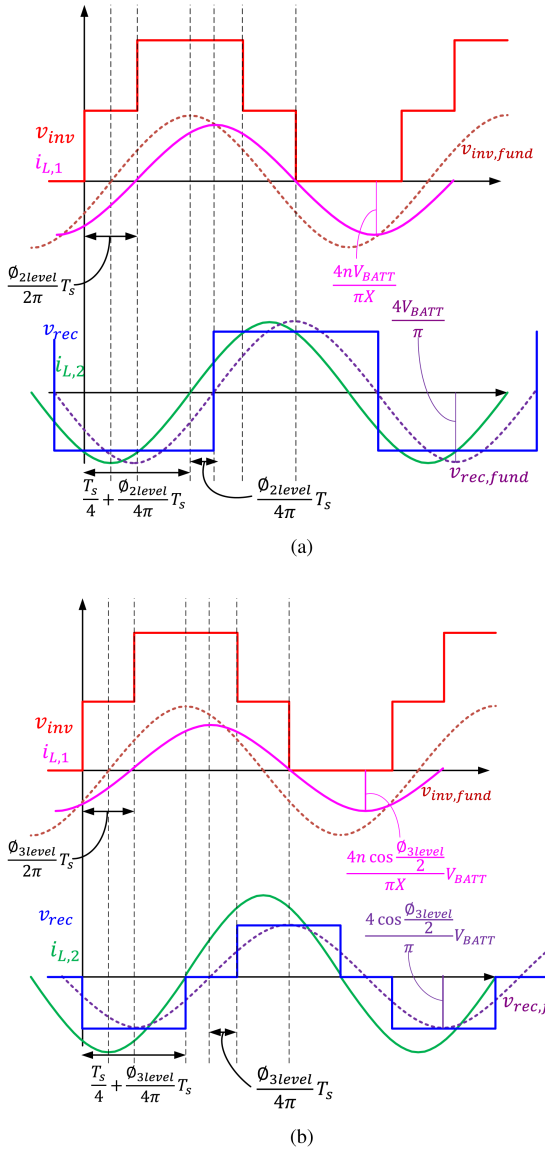


Fig. 9. Inverter and rectifier switching node voltages with their fundamental harmonic components along with inductor currents $i_{L,1}$ and $i_{L,2}$ using exemplary FB rectifier configuration at same output power P_{BATT} for: (a) Two-level active rectification approach, which results in larger $i_{L,1}$ current amplitude and (b) Three-level active rectifier operation with reduced control effort ($\phi_{3\text{level}} < \phi_{2\text{level}}$) resulting in larger amplitude of $i_{L,2}$ but reduced amplitude of $i_{L,1}$.

be reduced by half under SHB rectification, but the rectifier side inductor current $i_{i_{L,2}}$ remains the same as it is only dictated by applied voltage at the inverter port [see (9)]. Under both two-level and three-level rectifier modulation schemes, inverter side is switched using three-levels and the fundamental harmonic of rectifier side voltage lags the fundamental component of inverter side voltage by $\frac{\pi+\phi}{2}$. Hence, the inverter side inductor current now lags the inverter voltage by $\frac{\phi}{2}$, which results in ZVS of all switching transitions at the inverter. However, now the circulating currents in the resonant network have increased, as both inverter and rectifier deviates from ideal resistive behavior. It should also be noted that in a practical scenario, to charge

and discharge the output capacitance of the switching nodes, the fundamental of the rectifier switching node voltage needs to lag slightly more to provide sufficient inductive energy at all switching transitions ensuring the inverter side inductor current lags the inverter voltage by an angle greater than $\frac{\phi}{2}$. Hence, the choice of two-level or, three-level rectifier switching has additional impact on the conduction losses and when selected appropriately for a given application, it can help mitigating the circulating energy and associated conduction losses in the system. As can be seen from the FB rectification example in Fig. 9(a), when two-level switching is performed at the rectifier side, the fundamental voltage amplitudes can be computed as

$$\begin{aligned}\hat{V}_{\text{inv,fund,2level}} &= \frac{2\cos\left(\frac{\phi_{\text{2level}}}{2}\right)}{\pi} V_{IN}\angle -\frac{\phi_{\text{2level}}}{2}\\ \hat{V}_{\text{rec,fund,FB,2level}} &= \frac{4}{\pi} V_{\text{BATT}}\angle -\left(\frac{\pi}{2}+\phi_{\text{2level}}\right)\\ \hat{V}_{\text{rec,fund,SHB,2level}} &= \frac{2}{\pi} V_{\text{BATT}}\angle -\left(\frac{\pi}{2}+\phi_{\text{2level}}\right)\end{aligned} \tag{10}$$

and subsequently the currents are given by

$$\begin{aligned}\hat{I}_{\text{L,1,FB,2level}} &= \frac{4n}{\pi X} V_{\text{BATT}}\angle -\phi_{\text{2level}}\\ \hat{I}_{\text{L,1,SHB,2level}} &= \frac{2n}{\pi X} V_{\text{BATT}}\angle -\phi_{\text{2level}}\\ \hat{I}_{L,2,\text{2level}} &= \frac{2\cos\left(\frac{\phi_{\text{2level}}}{2}\right)}{\pi X} V_{\text{IN}}\angle -\frac{\pi+\phi_{\text{2level}}}{2}.\end{aligned} \tag{11}$$

Similarly from three-level FB rectification example shown in Fig. 9(b), the voltages under three-level rectification can be described as

$$\begin{aligned}\hat{V}_{\text{inv,fund,3level}} &= \frac{2\cos\left(\frac{\phi_{\text{3level}}}{2}\right)}{\pi} V_{IN}\angle -\frac{\phi_{\text{3level}}}{2}\\ \hat{V}_{\text{rec,fund,FB,3level}} &= \frac{4\cos\left(\frac{\phi_{\text{3level}}}{2}\right)}{\pi} V_{\text{BATT}}\angle -\left(\frac{\pi}{2}+\phi_{\text{3level}}\right)\\ \hat{V}_{\text{rec,fund,SHB,3level}} &= \frac{2\cos\left(\frac{\phi_{\text{3level}}}{2}\right)}{\pi} V_{\text{BATT}}\angle -\left(\frac{\pi}{2}+\phi_{\text{3level}}\right).\end{aligned} \tag{12}$$

and currents

$$\begin{aligned}\hat{I}_{L,1,FB,\text{3level}} &= \frac{4n\cos\left(\frac{\phi_{\text{3level}}}{2}\right)}{\pi X} V_{\text{BATT}}\angle -\phi_{\text{3level}}\\ \hat{I}_{L,1,SHB,3level} &= \frac{2n\cos\left(\frac{\phi_{\text{3level}}}{2}\right)}{\pi X} V_{\text{BATT}}\angle -\phi_{\text{3level}}\\ \hat{I}_{L,2,\text{3level}} &= \frac{2\cos\left(\frac{\phi_{\text{3level}}}{2}\right)}{\pi X} V_{IN}\angle -\frac{\pi+\phi_{\text{3level}}}{2}\end{aligned} \tag{13}$$

From (11) and (13), it is obvious that although both two-level and three-level switching at rectifier side can achieve soft switching of all transistors (by virtue of achieving the required phase-shift between inductor current $i_{L,1}$ and inverter voltage $v_{\text{inv,fund}}$), the circulating energy, especially for the inverter side inductor can

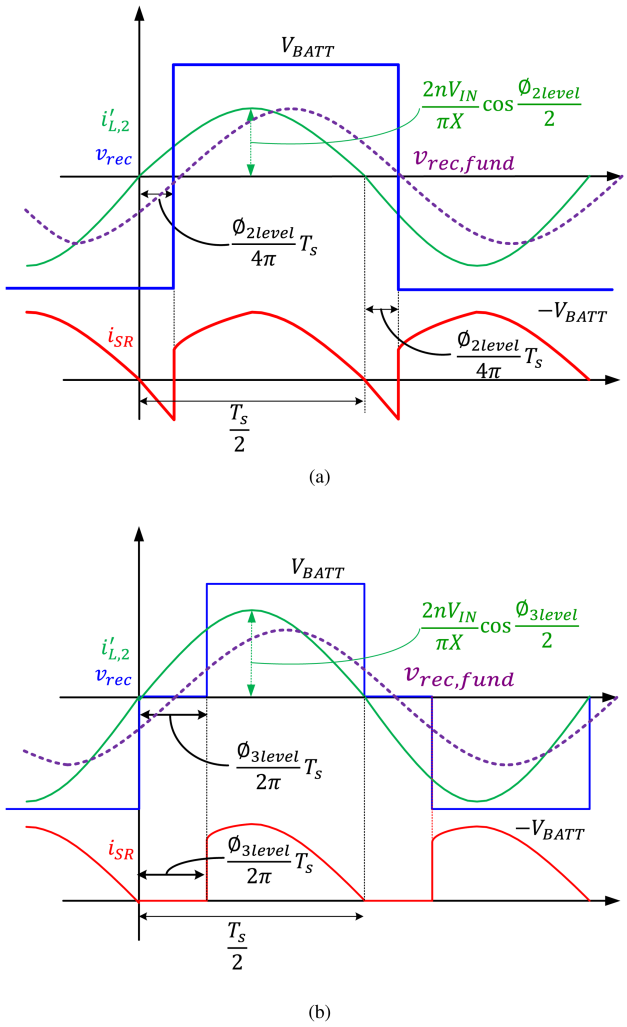


Fig. 10. Averaging of rectified transformer secondary current i_{SR} to derive dc output current I_{BATT} for (a) two-level rectifier operation and (b) three-level rectifier operation using FB rectifier as an example.

be quite different for the two cases. Furthermore, the relation of dc output current and the phase-shift control variable is also different for the two types of active rectification. Fig. 10(a) shows the rectified output current for a full bridge rectifier under two-level rectification. Where the dc output current is the averaged value of i_{SR}. As indicated earlier, for a voltage doubler or SHB rectifier, the dc output current will be reduced by half. Following averaging of i_{SR}, resultant expressions for dc output current for a FB and SHB rectifier can be found as

$$\begin{aligned}I_{\text{BATT},FB,\text{2level}} &= \frac{1}{\pi}\int_{\frac{\phi_{\text{2level}}}{2}}^{\pi+\frac{\phi_{\text{2level}}}{2}} \frac{2nV_{IN}}{\pi X}\cos\left(\frac{\phi_{\text{2level}}}{2}\right)\sin\theta d\theta\\ &= \frac{4n\cos^2\left(\frac{\phi_{\text{2level}}}{2}\right)}{\pi^2 X} V_{\text{IN}}\\ I_{\text{BATT,SHB,2level}} &= \frac{2n\cos^2\left(\frac{\phi_{\text{2level}}}{2}\right)}{\pi^2 X} V_{\text{IN}}\end{aligned} \tag{14}$$

According to similar arguments of averaging, for three-level rectification and corresponding rectified current indicated in

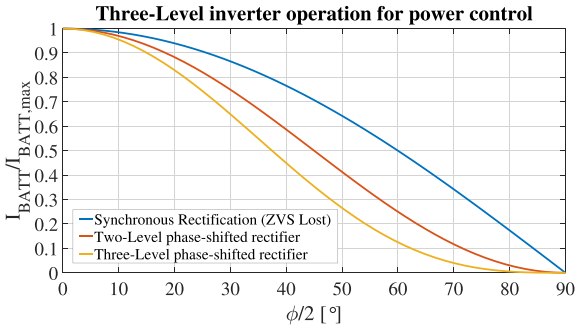


Fig. 11. Required phase-shift to reduce the output current from maximum achievable limit to any possible desired level using three different control approaches. Out of the two soft-switching active rectification approaches, three-level rectifier modulation results in reduced control action compared to two-level active rectification for the same desired output current level.

Fig. 10(b) for a FB rectifier, the dc output currents for both FB and SHB rectifier can be calculated as

$$I_{\text{BATT,FB,3level}} = \frac{1}{\pi}\int_{\phi_{3\text{level}}}^{\pi} \frac{2nV_{IN}}{\pi X}\cos\left(\frac{\phi_{3\text{level}}}{2}\right)\sin\theta d\theta$$
$$= \frac{4n\cos^3\left(\frac{\phi_{3\text{level}}}{2}\right)}{\pi^2 X}V_{\text{IN}}$$
$$I_{\text{BATT},SHB,\text{3level}} = \frac{2n\cos^3\left(\frac{\phi_{3\text{level}}}{2}\right)}{\pi^2 X}V_{\text{IN}} \quad (15)$$

From (14) and (15), it should be observed that different amount of control effort ϕ is required to maintain the same dc output current under two-level and three-level rectifier switching. Comparison of control efforts for three-level inverter modulation with synchronous rectification [see (5)], which results in loss of ZVS and the two different (two-level and three-level) active rectifier modulation approaches discussed above, both of which results in complete ZVS, is shown in Fig. 11. Here, $I_{\text{BATT,max}}$ refers to maximum achievable battery output current in either FB or SHB rectifier mode, described by (4). It should be noted that the proposed phase-shift based modulation approach can only result in reduction of output current and theoretically the output current can be reduced all the way to 0 by applying $\phi = 180^\circ$ as shown in Fig. 11. It is also important to observe that using the proposed modulation strategy can result in complete ZVS until very light load operation of the converter, while operating at fixed switching frequency alleviating any thermal or EMI limits. Furthermore, as ZVS is achieved using resonant inductor currents, unlike LLC converter, the RMS value of circulating currents to achieve ZVS reduces with load [see (13)]. This feature results in smaller conduction losses at lighter loads compared to converters, where magnetizing current is used to ensure ZVS and the associated conduction losses, remain constant at reduced loads, for a particular voltage gain. Since both of the active rectifier approaches result in complete ZVS, to compare the two-level and three-level solution, a conduction loss based figure of merit needs to be considered. Generally, in resonant converters, quality factor of capacitors is much higher than the quality factor of the inductors, hence, reducing inductive energy storage results in improved converter efficiency [20]. Given essentially sinusoidal currents in the inductors and transistors, and assuming similar inductor quality factors for given magnetics technology, the stored energy in the inductors can be a suitable metric to compare the conduction losses in the two different kind of active rectification approaches [28], which is defined as:

$$E = \frac{L}{2}\left[|\hat{I}_{L,1}|^2 + |\hat{I}_{L,2}|^2\right]. \quad (16)$$

Following the rationale of minimizing circulating energy in the resonant network, for a given converter specification, the figure of merit in (16) can be used to compare the two rectifier modulation approaches for efficiency optimization. This will be further addressed in the following section using a design example. The load specifications for this design example will follow the battery charging profile of Fig. 2.

TABLE I
WIDE GAIN RANGE ISOLATED DC–DC CONVERTER SPECIFICATIONS

Input Voltage (V_{IN})	800 V
Output Voltage (V_{BATT})	150 V–950 V
Maximum output power ($P_{\text{BATT,max}}$)	6.6 kW
Maximum Battery current ($I_{\text{BATT,max}}$)	20 A
Switching frequency (f_s)	500 kHz
GaN Transistors	GS66516T–650 V, 25 mΩ

IV. DESIGN CONSIDERATIONS

In this section, a design procedure for determining the reactive components and transformer turns ratio of the LCL-T resonant converter will be outlined for an universal EV charger. The specifications of such a dc–dc converter is outlined in Table I conforming to the charging profile depicted in Fig. 2. As mentioned earlier, the GaN transistors chosen are GaN System's 650 V, 25 mΩ GS66516 T device [29].

Several design considerations were involved in picking the converter switching frequency (f_s), such as size of magnetic components, ac losses in them and residual switching losses in transistors. For state-of-the-art magnetic technologies using soft ferrite magnetic cores and PCB windings with GaN transistors, beyond 500 kHz there is diminishing point of return in the power density. Increasing switching frequency above 500 kHz does not help in reducing size as the components become thermally limited but compromises converter efficiency. Since the converter operates with an input voltage of 800 V, and caters to output voltage of 150–950 V the need of SHBs at input and reconfigurable rectifier at output is justified. As the proposed topology is theoretically capable of maintaining ZVS down to no load using phase-shift control, the reconfiguration can be performed using dc relays as shown in Fig. 12(a) by reducing the load power down to zero, before mode change, alleviating the need of any complex topology morphing strategies [15]. There are many commercially available dc relays that are routinely used for precharging of PFC bus capacitors. Hence, adding three additional relays does not impact the reliability of the system, especially as they do not need to switch any current and

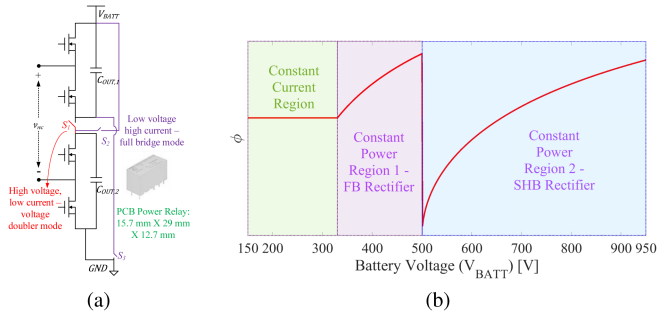


Fig. 12. (a) Practical implementation of the reconfigurable rectifier using dc relays and (b) Visualization of control variable ϕ with variable battery voltage V_{BATT}. For specifications outlined in Table I, in FB rectifier mode, the converter always requires a finite positive phase-shift. However, ϕ is reduced to zero right after the rectifier is morphed to SHB from FB to maintain battery current at $I_{\text{BATT,SHB,max}}$.

works just like a mechanical contactor in the proposed converter. Furthermore, these relays are very small in size, as can be seen from an example off-the-shelf relay shown in Fig. 12(a), and does not compromise the power density. Since, the charging profile requires a maximum output current of 20 A and CP operation over the entire output voltage range of 330–950 V, the output voltage where the rectifier is configured from a full bridge to a SHB is important in determining the maximum current requirement from the resonant network. For 650 V GaN transistors in a soft-switched application, having 500 V blocking voltage gives 77% utilization of transistors and is well in accordance with industry standard of 80% blocking voltage. Hence, the rectifier is reconfigured at $V_{\text{BATT}} = 500$ V. With the rectifier reconfiguration decided from transistor blocking voltage, the maximum required currents in FB and SHB rectifier modes are given by

$$I_{\text{BATT,FB,max}} = 20 \text{ A}; I_{\text{BATT,SHB,max}} = \frac{6600}{500} = 13.2 \text{ A}. \quad (17)$$

According to (4), the maximum output current is determined by the reactance of the inductors L_1, L_2, the transformer turns ratio and the input voltage. As the output current can always be reduced according to (14) or (15), using phase-shifted inverter and rectifier modulation discussed in Section III, the passive components need to be designed for the maximum required battery current, which requires

$$X = \min\left(\frac{4nV_{IN}}{\pi^2 I_{\text{BATT,FB,max}}}, \frac{2nV_{IN}}{\pi^2 I_{\text{BATT,SHB,max}}}\right). \quad (18)$$

From (17) and (18), it is clear that since the required maximum current in SHB rectifier mode is more than twice larger compared to the maximum current required in FB rectifier mode ($I_{\text{BATT,FB,max}} < 2I_{\text{BATT,SHB,max}}$), for the given specifications and chosen device blocking voltage, choice of reactance X is dictated by $I_{\text{BATT,SHB,max}}$. Hence, in the given charging profile of Fig. 2 during the LV battery CC mode, a constant phase-shift ($\phi > 0$) will be required to maintain the current at $I_{\text{BATT}} = 20$ A, as the choice of $\phi = 0$ will result in $I_{\text{BATT}} = 2I_{\text{BATT,SHB,max}} = 26.4$ A current. This control strategy is illustrated in Fig. 12(b), where for battery voltages lower than 330 V a constant finite phase-shift needs to be applied and right after the rectifier is reconfigured in the SHB mode, the phase-shift can be reduced to $\phi = 0$. Thereafter as voltage increases and current drops, phase-shift can be increased. The choice of transformer turns ratio is dictated by available transistor and magnetics technology to maximize converter efficiency by minimization of conduction losses. Multiple choices were considered and finally $n = 2$ was chosen for this application. Further considerations regarding turns ratio optimization is beyond the scope of this article. As a dc blocking capacitor is present in series with both primary and secondary windings of the transformer, there are no additional impact of the SHB inverter and reconfigurable rectifier on the transformer design. After n is picked, with a switching frequency of $f_s = 500$ kHz the inductors and capacitors can be selected from (1) and (18)

$$X = \frac{2nV_{\text{IN}}}{\pi^2 I_{\text{BATT,SHB,max}}} = 24.56\Omega$$
$$L_1 = L_2 = L = \frac{X}{2\pi f_s} = 7.8\mu\text{H}$$
$$C = \frac{1}{2\pi f_s X} = 13\text{nF}. \quad (19)$$

With the design of the components finalized, the type of rectifier side modulation that yields highest performance need to be determined next. To demonstrate the tradeoffs associated with two-level and three-level rectifier switching, Fig. 13 shows the control action, and resultant peak inductor currents while operating across the entire battery voltage range ($V_{\text{BATT}} = 150 - 950$ V). First, in Fig. 13(a), the required phase-shift is shown to regulate the output current at the desired level. It should be noted that for $V_{\text{BATT}} = 150 - 330$ V the applied phase-shift is constant for CC charging. As predicted from (14), (15), and Fig. 11, the required phase-shift is larger for two-level active rectifier modulation to maintain the same battery current. Next, from Fig. 13(b) and (c), it should be observed that although $\hat{i}_{L,1}$ has a consistently lower peak and RMS value for three-level modulation, $\hat{i}_{L,2}$ shows a completely opposite trend from $i_{L,1}$. Hence, to determine which modulation results in lower circulating energy and consequently conduction losses, the figure of merit described in (16) is used next. Using (14)–(16) and the final component design equations expressed in (19), the following ratio of inductive energy storage can be derived

$$\left.\frac{E_{3\text{level}}}{E_{2\text{level}}}\right|_{FB} = \left(\frac{I_{\text{BATT}}}{2I_{\text{BATT,SHB,max}}}\right)^{\frac{2}{3}} \frac{\frac{1}{4n^2} + \frac{V_{\text{BATT}}^2}{V_{\text{IN}}^2}}{\frac{1}{4n^2}\frac{I_{\text{BATT}}}{2I_{\text{BATT,SHB,max}}} + \frac{V_{\text{BATT}}^2}{V_{\text{IN}}^2}}$$
$$\left.\frac{E_{3\text{level}}}{E_{2\text{level}}}\right|_{SHB} = \left(\frac{I_{\text{BATT}}}{I_{\text{BATT,SHB,max}}}\right)^{\frac{2}{3}} \frac{\frac{1}{n^2} + \frac{V_{\text{BATT}}^2}{V_{IN}^2}}{\frac{1}{n^2}\frac{I_{\text{BATT}}}{I_{\text{BATT,SHB,max}}} + \frac{V_{\text{BATT}}^2}{V_{\text{IN}}^2}}. \quad (20)$$

Using the ratio of the energy stored in the resonant tank, the correct modulation strategy should be picked for any given application. In this particular case, as illustrated in Fig. 14, the three-level rectifier modulation always offers lower energy storage compared to two-level modulation for all the desired

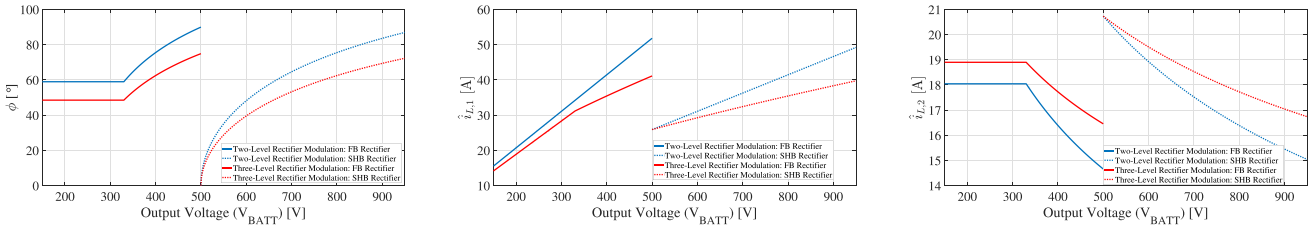


Fig. 13. Comparison of two-level and three-level active rectifier operation across the entire output voltage level of the proposed converter. (a) Different phase-shifts required to operate in CC and CP modes and regulation of output current, (b) peak current in inductor L_1 and (c) peak current in inductor L_2 are plotted for the two alternate rectifier control strategies.

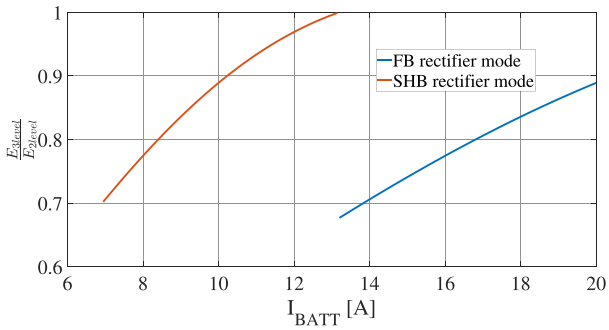


Fig. 14. Evaluation of figure of merit described in (16) across the entire battery current range in CC and CP mode of operation demonstrating superiority of three-level rectifier switching in reducing circulating energy and consequently the conduction losses for the specifications summarized in Table I while delivering same output power.

charging current levels in CC and CP modes. Hence, the three-level phase-shift based rectifier modulation is picked for experimental evaluation, which is likely to offer reduced reactive power flow for a given load and result in more efficient, power dense operation of the resonant converter. In order to regulate the charging currents using a low bandwidth P–I compensator, the plant transfer function can be derived by ignoring the resonant converter dynamics from (15) as [19]

$$G_{\hat{i}_{\text{BATT,FB}},\hat{\phi}} = \frac{\partial I_{\text{BATT,FB}}}{\partial \phi} = -\frac{6n\cos\left(\frac{\phi}{2}\right)\sin\phi V_{\text{IN}}}{\pi^2 X}$$

$$G_{\hat{i}_{\text{BATT,SHB}},\hat{\phi}} = \frac{\partial I_{\text{BATT,SHB}}}{\partial \phi} = -\frac{3n\cos\left(\frac{\phi}{2}\right)\sin\phi V_{\text{IN}}}{\pi^2 X}. \quad (21)$$

As the controller bandwidth need not be very high for EV charging applications, a simple P–I compensator is sufficient to regulate the output current.

V. Prototype Design and Experimental Results

Following the design procedure described in the previous section, a hardware prototype was built to verify the effectiveness of the proposed topology and control for the wide gain range specified in Table I. To enhance power density and

TABLE II
Details of Ceramic Capacitors in the Prototype DC–DC Converter

Resonant capacitor C	16 X KEMET CKC21C143KJGLCAUTO
DC blocking capacitors C_{B1}, C_{B2}	2 X TDK B58035U5106M001
DC link capacitors $C_1, C_2, C_{OUT,1}, C_{OUT,2}$	4 X TDK B58033I7106M001

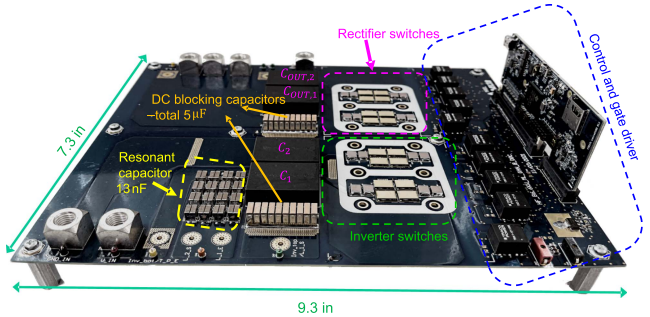


Fig. 15. Photograph of the power board excluding heat sink and magnetic components. The transistors (2 transistors in every switch position), ceramic capacitors used for various purposes and controller part is marked in the photograph along with the dimension of the PCB.

take advantage of the high frequency switching, the capacitors in the circuit were all implemented using ceramic technology and the magnetic components were constructed using planar cores and PCB wingdings. The details of the ceramic capacitors used in the prototype are tabulated in Table II. A photograph of the power board with all components except the magnetic parts is shown in Fig. 15.

It should be noted that for this prototype two GaN transistors are connected in parallel for every switch position. Furthermore, the resonant capacitor C is constructed using 16 discrete 13 nF capacitors, with 4 of them connected in series and 4 such series connected sets connected in parallel. This matrix connection of capacitors is necessary to accommodate severe degradation of ac voltage rating in ceramic capacitors at high frequencies. For the dc blocking capacitors, dc bias characteristics were of particular significance, as at rated dc bias capacitance C_{B1} and C_{B2} needs to be significantly larger than the resonant capacitor C, to ensure proper operation of the converter. In this regard, TDK's Ceralink capacitors with high RMS current rating and

TABLE III
DETAILS OF PLANAR MAGNETIC COMPONENTS IN THE CONVERTER PROTOTYPE. ALL MAGNETIC CORES WERE BUILT USING TDK'S N49 MATERIAL

	PCB Stackup	Windings	Core Geometry	Airgap
L_1	4 layers 4 oz	4 turns	3 X EILP 43 (43.2 mm X 83.7 mm X 13.6 mm)	2 mm
L_2	4 layers 4 oz	4 turns	2 X EILP 43 (43.2 mm X 55.8 mm X 13.6 mm)	1.4 mm
Tfo.	12 layers 4 oz	8 pri. 4 sec.	3 X EILP 43 (43.2 mm X 83.7 mm X 13.6 mm)	0 mm

maximum achievable capacitance at rated dc bias are the most suitable candidate for practical implementation of C_{B1} and C_{B2}. Texas Instrument's TMS320D28379D C2000 control card is used to implement the phase-shifted gate signals with high resolution.

For design of magnetic components a multiobjective loss optimization is used to determine the core geometry, number of turns and PCB construction details (copper thickness, number of layers, and number of turns in each layer) [30]. Dowell's equations [31] are used for winding loss modelling and iGSE [32] method is utilized for core loss modeling. Finally, the optimized designs are simulated using Ansys Maxwell 3D software to estimate losses with relatively high degree of accuracy. The final construction details off all three magnetic components are tabulated in Table III. Inductor L_1 is constructed with a larger core geometry to withstand larger current stress compared to L_2 as indicated in Fig. 13. Furthermore, the transformer is constructed with no airgap and fully interleaved windings to minimize winding losses. It should be noted that even with a very high magnetizing inductance, this topology is capable of achieving complete ZVS, which is an advantage of the proposed topology over conventional SRC or CLLC converters. The planar transformer was characterized using a HP4194 A impedance analyzer. Measured value of magnetizing inductance from primary side was 725 μ H, which is almost 100 times larger than the resonant inductances designed in (19). Measured leakage inductance from primary side was 860 nH due to fully interleaved nature of the planar transformer. The total magnetics volume in the prototype is 130 cm^3. Photograph of the final assembled prototype is shown in Fig. 16. Attention has been given in packaging of the magnetic components along with the heat sink for the transistors. The finished height of the prototype is 25.4 mm or 1 in including the heat sink. Discarding the control and gate driver portion of the prototype, the power stage achieves a power density of 120 W/in^3 (7.3 kW/L).

Next, experimentally measured results are provided across the entire output voltage range using the prototype converter. Fig. 17 shows the measured waveforms of inverter side switch node voltage (v_{inv}), inductor current i_{L1}, rectifier switch node voltage (v_{rec}), inductor current i_{L2} and dc link capacitor voltages for FB rectifier operation with $V_{\text{BATT}} \leq 500$ V. Fig. 17(a) shows operation at 270 V battery voltage with 20 A current at CC mode, and Fig. 17(b) and (c) shows operation in CP mode with $V_{\text{BATT}} = 350$ V and 450 V, respectively.

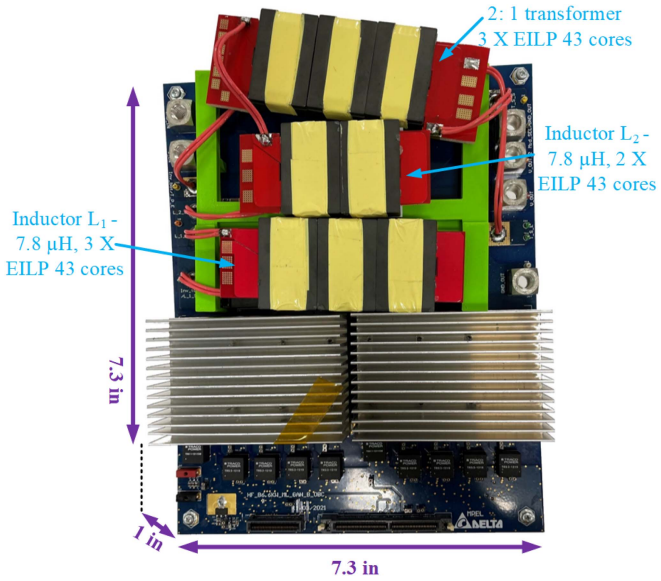
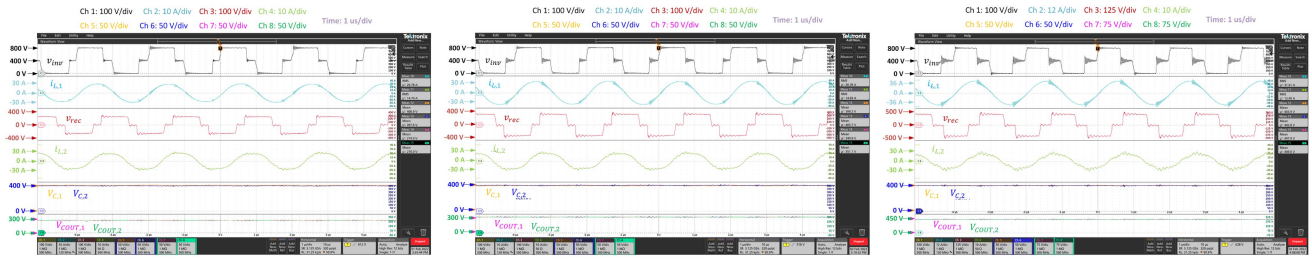


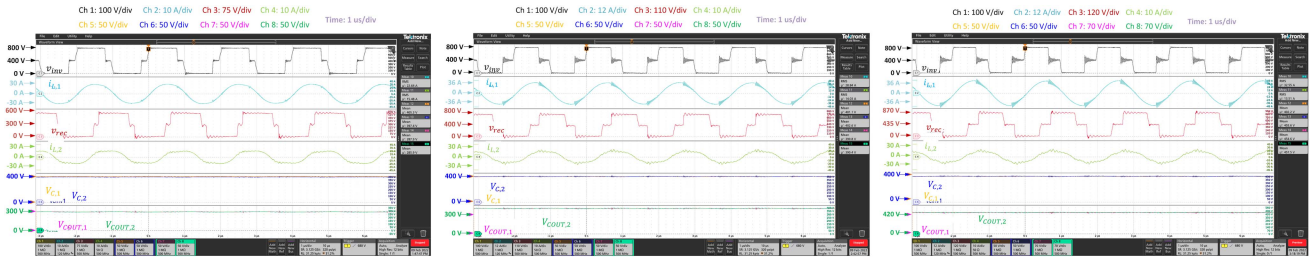
Fig. 16. Assembly of the converter prototype with magnetic components marked. Area of the main power components excluding the controller and gate driver parts is highlighted. This area is used for power density calculation.

It is important to observe how three-level modulation at both inverter and rectifier with phase-shift (ϕ) as the control variable is being used to reduce the output current in CP mode of operation. The waveforms illustrate ZVS turn-ON of all semiconductor components validating the proposed modulation strategy. In the inductor currents additional ringing is observed as a result of parasitic capacitances associated with PCB based windings with large overlap between turns due to their planar nature. It is also important to observe that with larger applied phase-shift [see Fig. 17(c)], the turn-OFFcurrents in the transistors increase, resulting in larger dv/dt and larger ringing associated with parasitic capacitances. In the FB rectifier mode, the rectifier switch node voltage is bipolar and furthermore, the measured voltage on the stacked capacitors at the inverter side indicate how they are always balanced at 400 V. In Fig. 18, all the experimentally measured waveforms are presented for SHB rectifier operation for three different output voltages operating in CP mode. Hence, compared to FB rectifier mode, the rectifier switching node voltage now becomes unipolar. Similar to the FB battery mode, here also three-level phase-shifted modulation is utilized to reduce output battery current. As indicated in Fig. 12(b), in SHB rectifier mode, the required phase-shift is smaller than FB rectifier mode. This is also visible in Fig. 18(a) for $V_{\text{BATT}} = 570$ V. In this case the applied phase-shift is relatively small, which results in lower circulating currents and higher efficiency. For Fig. 18(b) and (c), the output voltage is 770 and 910 V, respectively, with application of larger phase-shifts. Furthermore, it is also interesting to note that even during SHB rectifier mode, both inverter side and rectifier side stacked capacitor voltages are balanced to the same value. The balancing of stacked capacitor voltages require very slow active control. The details of the balancing technique is outside the scope of this article and can be found in existing literature [24], [37].



(a) (b) (c)

Fig. 17. Key measured waveforms for Low Voltage Battery operation using FB rectifier in CC and CP mode for (a) $V_{\mathrm{BATT}} = 270$ V, $I_{\mathrm{BATT}} = 20$ A, (b) $V_{\mathrm{BATT}} = 350$ V, $I_{\mathrm{BATT}} = 19$ A and (c) $V_{\mathrm{BATT}} = 450$ V, $I_{\mathrm{BATT}} = 14.7$ A.



(a) (b) (c)

Fig. 18. Key measured waveforms for High Voltage Battery operation using SHB rectifier in CP mode for (a) $V_{\mathrm{BATT}} = 570$ V, $I_{\mathrm{BATT}} = 11.6$ A, (b) $V_{\mathrm{BATT}} = 770$ V, $I_{\mathrm{BATT}} = 8.6$ A and (c) $V_{\mathrm{BATT}} = 900$ V, $I_{\mathrm{BATT}} = 7.33$ A.

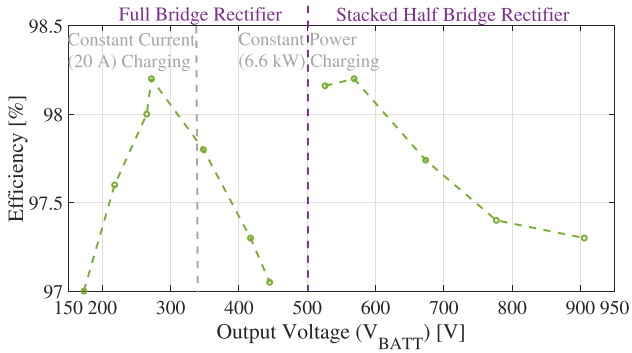
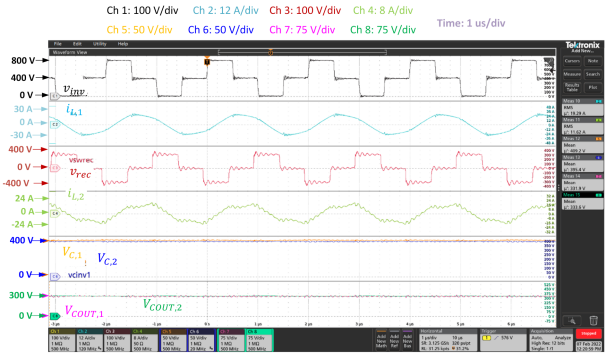


Fig. 19. Measured efficiency of the converter across entire output voltage range in CC and CP modes.

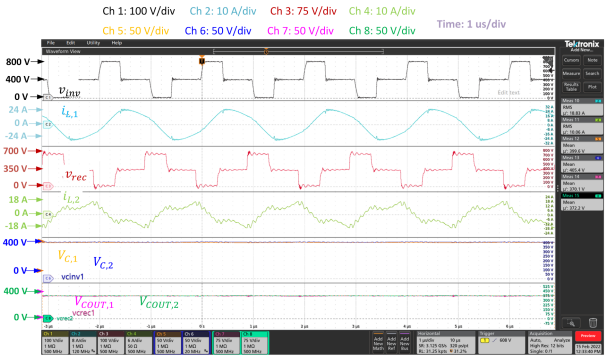
Finally, Fig. 19 shows the experimentally measured efficiency of the prototype converter across the entire output voltage range, operating at the envelop of the load profile shown in Fig. 2. First, in FB rectifier mode, while performing CC charging, efficiency of the converter drops as output power is limited by the current. The peak efficiency occurs at the boundary of CC and CP modes. In the CP mode, as output voltage increases, larger phase-shift is required to achieve battery current reduction, which also results in reduced efficiency due to increased reactive energy in the resonant tank. Once the transition from FB rectifier to SHB rectifier occurs (at $V_{\mathrm{BATT}} = 500$ V), the efficiency is increased, as applied phase-shift is relatively small [see Fig. 12(b)]. At $V_{\mathrm{BATT}} = 570$ V, the peak efficiency of 98.2% is achieved at full output power of 6.6 kW. It should be noted from Figs. 12(b) and 19 that in spite of a smaller applied phase-shift at $V_{\mathrm{BATT}} = 525$ V compared to $V_{\mathrm{BATT}} = 570$ V, the efficiency remains practically the same at both operating points. This phenomenon can be attributed to the contrasting trends in $\hat{I}_{L,1}$ and $\hat{I}_{L,2}$ with increased applied phase-shift. With smaller applied phase-shift, although inductor L_1 has lower peak and RMS current, the current stress on L_2 and transformer increases (see Fig. 13) for same output power transfer. Thereafter, the efficiency starts to drop similar to FB rectifier mode, as dc output current is reduced when battery voltage is increased by application of larger phase-shift. Here, the losses in inductor L_1 becomes dominant. Despite of such increased conduction losses with applied phase-shift, using the proposed circuit topology and fixed frequency phase-shift control, the converter always achieves $> 97\%$ efficiency for the entire output voltage range of 150–950 V, which exceeds the performance of existing charging converters operating with much lower power density and output voltage range [4], [33]. A detailed comparison with several recently proposed OBC systems with the proposed technology is highlighted in Table IV . As the proposed converter operates with fixed frequency phase-shift modulation, this approach is more suitable for high frequency converters, where variable frequency modulation techniques cause additional losses and gate driving challenges. The effectiveness of the proposed modulation strategy in Section III is also prevalent at lighter loads as it allows to maintain ZVS of all transistors across entire load range all the way down to no load. First, light load operation is experimentally illustrated in Fig. 20 using the prototype converter. Where the converter is operated with 1 kW output power for $V_{\mathrm{BATT}} = 330$ V in Fig. 20(a) with FB

TABLE IV
COMPARISON OF PROPOSED LCL-T PROTOTYPE CONVERTER WITH A FEW RECENTLY EVALUATED WIDE RANGE DC–DC CONVERTERS

	Topology	Charging Profile	Switch Type	Switch utilization V_{DS}/V_{rated}	Modulation Technique	Switching frequency	Power Density	Peak Efficiency	Gain Range	Efficiency at Full Load
[13]	Series Resonant	CC CP CV	650 V GaN	0.3-0.72	Frequency and PWM	150-190 kHz	1 kW/L	98.1%	2.4X	94.8-98.1%
[4]	Series Resonant	CC CP CV	1200 V SiC	0.17-0.79	PWM	65 kHz	1.4 kW/L	98.5%	4.75X	96-98.5%
[33]	CLLC	CC CP CV	1200 V SiC 650 V GaN	0.38-0.75	No control DCX mode	500 kHz	8 kW/L	97.8%	1X	97.3-97.8%
[34]	PSFB	CV	1200 V SiC	0.33	Phase-Shift	200 kHz	>5 kW/L	96.5%	1X	96.5%
[35]	Hybrid LLC	CC CV	600 V GaN	0.67	Frequency	75-300 kHz	4 kW/L	98.5%	1.67X	96.2-98.5%
[36]	DAB	CP CV	1200 V SiC	0.21-0.32	PWM and Phase-Shift	500 kHz	5.44 kW/L	98%	1.5X	96-98%
This Work	**Multi-Level LCL-T**	**CC CP CV**	**650 V GaN**	**0.23-0.77**	**Phase-Shift**	**500 kHz**	**7.3 kW/L**	**98.2%**	**6X**	**97-98.2%**

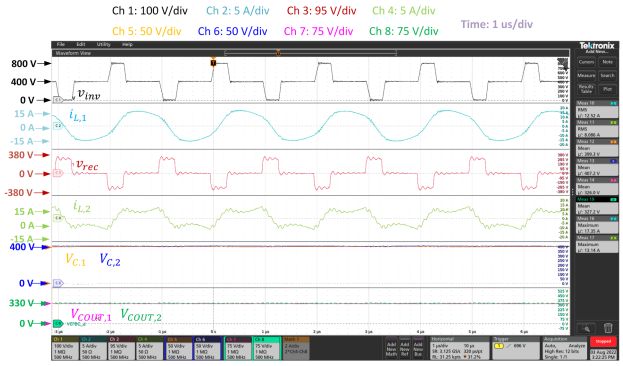


(a)

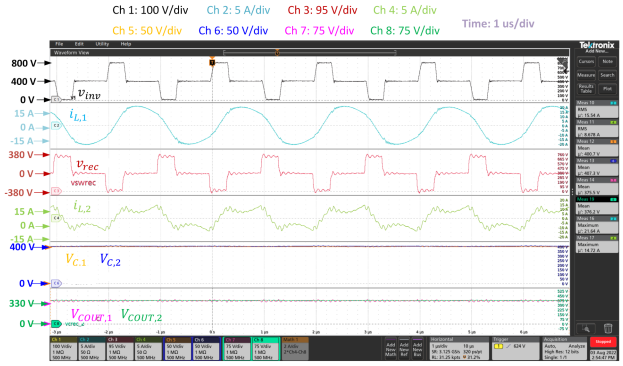


(b)

Fig. 20. Key measured waveforms of the dc–dc converter prototype at light load for: (a) $V_{\mathrm{BATT}} = 330$ V, $I_{\mathrm{BATT}} = 3$ A and $P_{\mathrm{BATT}} = 1$ kW in FB rectifier mode and (b) $V_{\mathrm{BATT}} = 740$ V, $I_{\mathrm{BATT}} = 1.35$ A and $P_{\mathrm{BATT}} = 1$ kW in SHB rectifier mode.



(a)



(b)

Fig. 21. Effectiveness of proposed converter and modulation strategy to eliminate burst mode operation, being verified using key measured waveforms, while delivering 1% of rated power at: (a) $V_{\mathrm{BATT}} = 330$ V, $I_{\mathrm{BATT}} = 0.2$ A and $P_{\mathrm{BATT}} = 66$ W in FB rectifier mode and (b) $V_{\mathrm{BATT}} = 741$ V, $I_{\mathrm{BATT}} = 0.1$ A and $P_{\mathrm{BATT}} = 74$ W in SHB rectifier mode.

rectifier and $V_{\mathrm{BATT}} = 740$ V in Fig. 20(b) with SHB rectifier. It should be noted how large phase-shifts are applied to reduce the output current and power. Furthermore, the superiority of the converter is experimentally verified with continuous operation at practically zero load as illustrated in Fig. 21. With FB rectifier in Fig. 21(a), the battery charging current is reduced to $I_{\mathrm{BATT}} = 0.2$ A at $V_{\mathrm{BATT}} = 330$ V and using the SHB rectifier, Fig. 21(b) shows operation at $V_{\mathrm{BATT}} = 740$ V and $I_{\mathrm{BATT}} = 0.1$ A. The converter is still capable of maintaining ZVS at 1% of the

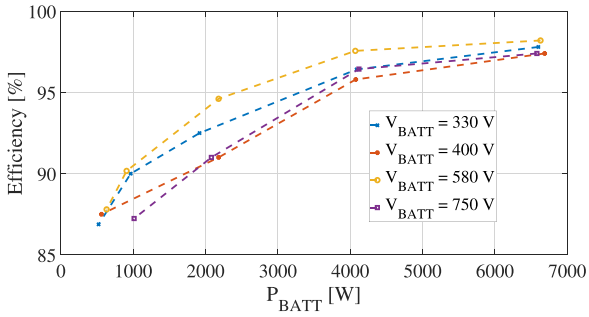


Fig. 22. Measured efficiency of the prototype dc–dc converter across wide load range for different output voltages (CV mode) when the converter is operated in both FB and SHB rectifier mode.

converter's rated power. Finally, Fig. 22 shows experimentally measured efficiency for different output voltages across entire output power range. Experimental measurements show an efficiency of $> 88\%$ can be maintained up to 1 kW output power for all the output voltages. This emphasizes that, it is possible to reduce or eliminate the need of burst mode operation using the proposed topology and control, which can reduce the size of output capacitor, make the converter more power dense and use the dc relays simply as mechanical contactors for rectifier reconfiguration.

VI. Conclusion

This article presents a high frequency phase-shift controlled immittance network based LCL-T resonant converter utilized in a wide output voltage range dc–dc stage for universal EV battery charging. Use of 650 V GaN transistors is explored to achieve 500 kHz fixed switching frequency operation from 800 V PFC bus and delivering 150–950 V output, compatible with both LV and HV batteries. A novel phase-shift based three-level modulation technique is proposed in this article, which in conjunction with the LCL-T resonant network enables wide output voltage and output power profile without loss of ZVS across the entire operating range of the dc–dc converter. Use of a reconfigurable rectifier allows for two high efficiency points for LV and HV batteries. To demonstrate the capabilities of the proposed concepts an experimental prototype is constructed using planar magnetics with PCB windings achieving $120\,\mathrm{W/in^3}$ power density. The measured converter efficiency achieves a peak of 98.2% and maintains fairly flat efficiency profile, with $> 97\%$ efficiency across the whole output voltage range. Improved light load operation is also demonstrated for the proposed converter reducing or completely eliminating the need for burst mode control. Therefore, the proposed converter and control can be considered as a strong candidate for universal EV charger applications.

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