Letters

A 434-MHz Bootstrap Rectifier With Dynamic V_{TH} Compensation for Wireless Biomedical Implants

Muhammad Abrar Akram, *Member, IEEE*, and Sohmyung Ha, *Senior Member, IEEE*

***Abstract*—This letter presents a fully differential CMOS bootstrap rectifier with an effective dynamic threshold voltage (i.e., V_{TH}) compensation (DVC). The bootstrapping circuit for DVC, which consists of a dynamically biased transistor, a series resistor, and a parallel capacitor, dynamically generates a compensation voltage for the main rectifying pass transistors only when the V_{TH} compensation is required. It significantly increases the proposed rectifier's power conversion efficiency (PCE) compared to other bootstrap rectifiers. The proposed rectifier operates at an industrial, scientific, and medical (ISM) band frequency of 434 MHz, and it is fabricated in a 0.18-μm CMOS process together with two conventional bootstrap rectifiers for performance comparison. Measurement results validate that the proposed rectifier outperforms the conventional bootstrap rectifiers in terms of the output dc voltage level, voltage conversion ratio, and PCE. The proposed rectifier attains a peak PCE of 71% at a load resistor of 3 kΩ and an operating frequency of 434 MHz.**

***Index Terms*—Bootstrapping technique, power conversion efficiency (PCE), RF–dc converter, RF energy harvesting, threshold cancellation, wireless power transfer (WPT).**

I. Introduction

IMPLANTABLE medical devices (IMDs) have been increasingly utilized in medical diagnostics and treatments [1]. Among several powering methods of IMDs, electromagnetic wireless power transfer (WPT) has become one of the most desirable power transmission techniques as it removes the requirement of batteries and subcutaneous wiring, circumventing the risk of infection associated with them [2], [3]. However, to meet the stringent and variable power budgets of IMDs, the WPT requires an efficient ac-to-dc conversion with high power conversion efficiency (PCE) and high voltage conversion ratio (VCR) [2], [4]. It poses tough challenges to the design of rectifiers, which convert the ac power of the receiver (RX) antenna to dc power for the load circuits.

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Muhammad Abrar Akram is with the New York University Abu Dhabi, Abu Dhabi 129188, United Arab Emirates (e-mail: abrarakram@nyu.edu).

Sohmyung Ha is with the New York University Abu Dhabi, Abu Dhabi 129188, United Arab Emirates, and also with the New York University, New York, NY 10003 USA (e-mail: sohmyung@nyu.edu).

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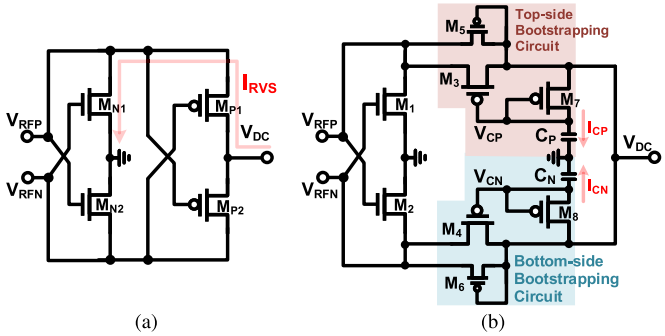

Fig. 1. Circuit diagrams of the following rectifiers. (a) FCC rectifier. (b) Bootstrap rectifier [8].

Conventionally, rectifiers using diodes or diode-connected transistors (DCTs) have been utilized, but they suffer from a large threshold voltage (i.e., V_{TH}) drop, which lowers the output dc voltage (i.e., V_{DC}) and the PCE, particularly at low input power conditions [5]. Schottky diodes with lower V_{TH} have been used but require additional fabrication steps. Hence, they are rarely offered in standard CMOS processes. The fully cross-coupled (FCC) rectifier [6] shown in Fig. 1(a) can effectively compensate for the V_{TH} drops of the rectifying transistors and achieves high-peak PCEs. It is because all the transistors are dynamically biased by the differential input signals (V_{RFP} and V_{RFN}). However, its performance degrades at high-input levels because of the large reverse leakage currents [I_{RVS} shown in Fig. 1(a)]. These reverse currents are caused by simultaneous turning-ON of the PMOS and NMOS transistors during the transition between the turning-ON and turning-OFF periods. I_{RVS} becomes much worse as the radio-frequency (RF) input increases, degrading the PCE significantly. Consequently, the FCC rectifier operates efficiently only within a limited optimal range of the input power [2], [3], [7].

Compared to the FCC rectifier, the bootstrap rectifier shown in Fig. 1(b) offers a better V_{TH} compensation without suffering from the reverse leakage issue [8]. In this rectifier, V_{TH} of the main conducting transistors M_3 and M_4 are compensated by the charging voltages V_{CP} and V_{CN}, respectively. V_{CP} and V_{CN} are kept constant no matter the swing of V_{RFP} and V_{RFN} when the amplitude of V_{RFP} and V_{RFN} does not vary. Thus, this bootstrapping method is categorized into static V_{TH}

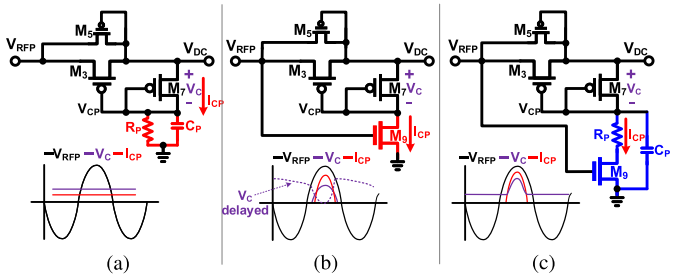

Fig. 2. Bootstrapping circuits of existing and proposed bootstrap rectifiers with waveforms of major signals for V_{TH} compensation. (a) Work in [9]. (b) Work in [10]. (c) Proposed work.

compensation (SVC). The top-side main conducting transistor M_3 turns OFF when $V_{\text{RFP}} < V_{\text{DC}} + (|V_{\text{TH},P3}| - |V_{\text{TH},P7}|)$. When $|V_{\text{TH},P3}| > |V_{\text{TH},P7}|$, M_3 turns OFF as soon as V_{RFP} drops below V_{DC}, so much less reverse current is incurred than the FCC rectifier [2]. Due to its lower leakage currents, the PCE of the bootstrap rectifier does not drop with the increase of input power compared to the FCC rectifier. However, the PCE performance of this bootstrap rectifier is compromised by the charge saturation issue of bootstrap capacitors C_P and C_N. When C_P is fully charged, I_{CP} hardly flows through M_7, making V_{SG} of M_7 much smaller than V_{TH} of M_3. This discrepancy gets worse at high operating frequencies due to parasitic capacitors associated with transistor's terminals, inevitably lowering the V_{DC} and also the PCE. It makes the work in [8] unsuitable for biomedical implants because of their high operating frequency.

To address this issue, we propose a bootstrap rectifier with a new bootstrapping circuit for dynamic threshold voltage (V_{TH}) compensation (DVC). The new bootstrapping circuit significantly enhances the PCE and VCR while operating at high frequency.

The rest of this letter is organized as follows. Section II discusses and compares existing bootstrapping circuits for V_{TH} compensation along with the proposed one. The proposed rectifier is presented more in detail in Section III. The measurement results are demonstrated in Section IV. Finally, Section V concludes this letter.

II. Comparison of V_{TH} Compensation Techniques in Bootstrap Rectifiers

Fig. 2 compares two existing and the proposed V_{TH} compensation circuits of bootstrap rectifiers. The charge saturation problem of [8] was resolved in [9] by inserting a resistor (R_P) in parallel with C_P, as shown in Fig. 2(a). The constant current (I_{CP}) through M_7 and R_P makes V_{SG} of M_7 approximately similar to V_{TH} of M_3. This is also an SVC method as the compensation voltage V_C is constant due to the continuous current flow (I_{CP}), as shown in the bottom side of Fig. 1(a). However, this continuous current itself is extra static power consumption, which degrades the PCE of the rectifier. To reduce this excess current consumption, the rectifier in [10] uses a DVC technique, as shown in Fig. 2(b). Here, an NMOS transistor (i.e., M_9) is added as a dynamic current source, replacing C_P and R_P used in [8] and [9]. During the positive cycle of V_{RFP}, M_9 turns ON by V_{RFP}. This creates I_{CP} flowing through M_7 and forms a dynamically biased current path. I_{CP} flow makes the V_C positive to compensate the V_{TH} of M_3, as shown in the bottom side of Fig. 2(b). As shown in the figure, I_{CP} is generated when needed only, unlike [9]. Consequently, this DVC technique improves the PCE as compared to SVC-based works [8], [9]. However, this DVC technique is affected by the ON-resistance of M_9, because the overall resistance of dynamically biased current path is mainly set by the ON-resistance of M_9, which changes widely due to its gate voltage, the RF input (V_{RFP}). For the cases where V_{RFP} is large, the ON-resistance of M_9 may become too small. Such a wide variation of M_9 ON-resistance and overall resistance of the current path makes it difficult to achieve DVC over a wide range of the input signal. Moreover, the compensating voltage V_C in [10] is required to swing too widely at the given operating frequency of 434 MHz, as shown in Fig. 2(b). Due to that, V_C fails to follow the change of input V_{RmFP} and gets delayed, as shown by the dotted V_C line in the bottom side of Fig. 2(b). This delay in V_C opens the main conducting transistor at the wrong timings, which adversely affects the V_{TH} compensation, thus degrading the V_{DC} level and the PCE at high frequencies.

In order to resolve the shortcomings of charge saturation in [8], excess current consumption in [9], and ON-resistance variations and delay of V_C in [10], we propose a new DVC technique using a dynamically biased transistor M_9 with a series resistor R_P and a parallel capacitor C_P, as shown in Fig. 2(c). In the proposed technique, M_9 forms a dynamically biased current path with R_P and M_7. Without R_P, the overall resistance of the current path is mainly determined by the ON-resistance of M_9, which may adversely affect the DVC and PCE especially at high V_{RFP}[10]. By adding the series resistor R_P, the ON-resistance of the dynamically biased current path is limited at high V_{RFP}. In addition, C_P maintains a baseline voltage level of V_{CP}, limiting its voltage swing much smaller than that in [10]. Altogether, an efficient DVC of the main conducting transistor M_3 is achieved. As shown in the bottom side of Fig. 2(c), during the positive cycle of V_{RFP}, M_9 dynamically turns ON that allows the I_{CP} to flow through M_7 making V_C positive. I_{CP} flowing through M_7 decides $V_{SG,M7}$ to compensate $V_{\text{TH},M3}$. Contrarily, during the negative cycle of V_{RFP}, M_9 is OFF and I_{CP} does not flow, returning V_C to the baseline voltage maintained by C_P, as shown in the bottom side of Fig. 2(c). Due to this baseline voltage, V_C does not swing largely, unlike [10], so it can move faster with a shorter delay at high frequencies. With this proposed DVC technique, V_C is applied only when V_{TH} compensation is required. Otherwise, the level of V_C is kept at a baseline level. Thus, the proposed rectifier operates well even at high frequencies and improves the V_{DC}, PCE, and VCR compared to [10].

Fig. 3 shows a PCE comparison of the proposed rectifier and the DVC bootstrap rectifier in [10] for a frequency range from 1 to 434 MHz while driving R_L of 10 k Ω. To perform these simulations, we utilized the same sizes of the transistors as reported in [10]. In the proposed rectifier (as shown in Fig. 5), the size of main path transistors M_1–M_4 is 10/0.18 μ m. The DCTs, i.e., (M_5, M_6) and (M_7, M_8), have the sizes of 1/0.18 and 2.5/0.18 μm, respectively. The dynamically biased transistors

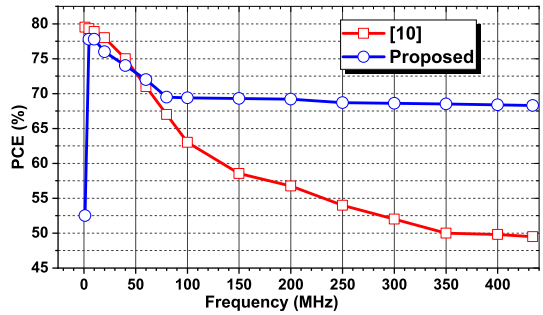

Fig. 3. Simulated PCE of the DVC bootstrap rectifier in [10] and the proposed rectifier over frequency from 1 to 434 MHz at $R_L = 10$ kΩ.

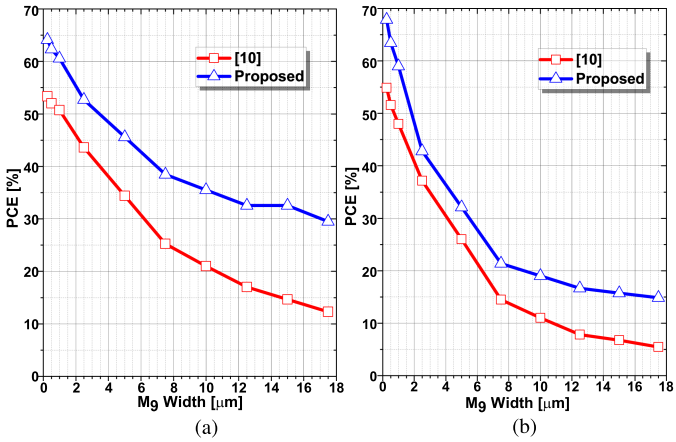

Fig. 4. Simulated PCE comparison between bootstrap rectifier [10] and the proposed rectifier by varying the width of M_9 at (a) $R_L = 3$ kΩ; and (b) $R_L = 10$ kΩ.

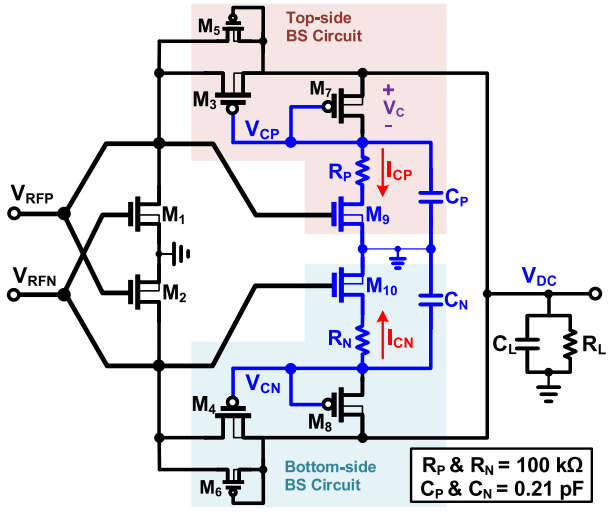

Fig. 5. Circuit schematic of the proposed rectifier.

M_9 and M_{10} have the size of 1/20 μm. R_P and R_N are set to 100 kΩ, and C_P and C_N are set to 0.21 pF. As shown in Fig. 3, Cho et al. [10] performed better up to 60 MHz of frequency. However, above that frequency, the delay effect starts dominating and adversely affecting the DVC, consequently lowering the PCE. In contrast, the proposed rectifier with the proposed DVC technique maintains its PCE performance over a much wider frequency range up to 434 MHz, as shown in Fig. 3.

Fig. 4 shows simulated PCEs of the rectifier of [10] and the proposed one by varying the M_9 dimension for two different load conditions at a fixed V_{RFP} amplitude of 2 V. As shown in the figure, as M_9's width is increased, the PCE of the rectifier of [10] drops more quickly as compared to that of the proposed rectifier. It is because the overall resistance of the dynamically biased current path becomes too small as M_9's width is increased. By increasing the width of M_9, the current through M_9 (I_{CP}) is increased and incurs unnecessarily large voltage drop (V_C) across M_7. It adversely affects the PCE of the rectifier [10]. Contrarily, in the proposed rectifier, the series resistor R_P limits the minimum resistance of the dynamic current path. It results in better PCE even at large dimensions of M_9, as shown in Fig. 4.

III. Proposed Bootstrap Rectifier

Fig. 5 shows the overall circuit diagram of the proposed bootstrap rectifier. The proposed rectifier consists of two cross-coupled NMOS transistors (i.e., M_1 and M_2) and two PMOS transistors (i.e., M_3 and M_4) to provide main conduction paths from the differential input to the output load at V_{DC}. These main path transistors should be large enough to have low ON-resistance and small enough not to disturb the *LC* resonant tank, which is placed just before the rectifier. Hence, M_1–M_4 are carefully sized as 10/0.18 μm. Transistors M_3 and M_4 are equipped with bootstrapping circuits for DVC. The top-side circuit consists of transistors M_3, M_5, M_7, and M_9, a resistor R_P, and a capacitor C_P, while M_4, M_6, M_8, M_{10}, R_N, and C_N constitute the bottom-side one.

The operation of the proposed rectifier is described as follows. Because of the symmetric structure, only the top-side circuit's operation is explained. Initially, the DCT M_5 turns ON first, forming an auxiliary current-conduction path to V_{DC}. This increases V_{DC} and charges C_P through another DCT M_7 to the levels given as follows:

$$V_{DC} \cong \hat{V}_{RFP} - |V_{TH,M5}| \tag{1}$$

$$V_{CP} \cong V_{DC} - |V_{TH,M7}| \cong \hat{V}_{RFP} - 2|V_{TH,M5/M7}|. \tag{2}$$

Thus, V_{SG} of M_3 ($V_{SG,M3}$) is $\hat{V}_{RFP} - V_{CP} = 2|V_{TH,M5/M7}|$. As $2|V_{TH,M5/M7}| > V_{TH,M3}$, M_3 is pushed into the triode region, and V_{DC} and V_{CP} are more charged now mainly by M_3 until V_{CP} becomes $\hat{V}_{RFP} - V_{TH,M3}$. Therefore, at the steady state, V_{DC} finally reaches as follows:

$$V_{DC} \cong \hat{V}_{RFP} - |V_{TH,M3}| + |V_{TH,M7}|. \tag{3}$$

This means that M_3 behaves as a diode with a minimal threshold voltage of $|V_{TH,M3}| - |V_{TH,M7}|$. As described in Section II, M_9 dynamically turns ON during the positive cycle of V_{RFP} in the proposed configuration, providing a current (I_{CP}) flowing through M_7. I_{CP} decides $V_{SG,M7}$ to compensate $V_{TH,M3}$ by making V_C positive. Since I_{CP} flows only when M_9 turns ON, V_C changes only to follow V_{RFP} when it needs to compensate $V_{TH,M3}$, achieving an energy-efficient DVC. Similarly, during

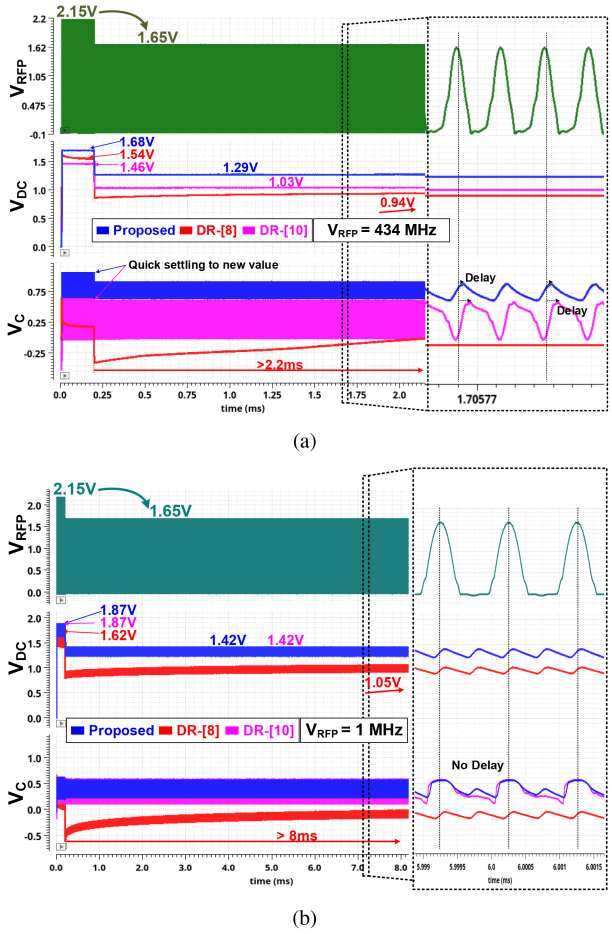

Fig. 6. Simulated main signal waveforms of DR-[8], DR-[10], and the proposed rectifier when the input $V_{\mathrm{RF}P}$ amplitude is reduced by 0.5 V (from 2.15 to 1.65 V) while driving $R_L = 10$ kΩ. The input frequency is set to (a) 434; and (b) 1 MHz.

the negative cycle, I_{CN} flows only when M_{10} turns ON to compensate $V_{\mathrm{TH},M4}$. This V_{TH} compensation significantly improves the overall PCE of the proposed rectifier.

To evaluate the performance of the proposed rectifier in comparison with existing bootstrap rectifiers, we designed and fabricated the two bootstrap rectifiers in [8] and [10] along with the proposed one. These design references [8] and [10] are termed as DR-[8] and DR-[10] onwards in this letter.

Fig. 6(a) compares simulated major signal waveforms of DR-[8], DR-[10], and the proposed rectifier at 434- and 1-MHz RF input. Here, the amplitude of the input signal ($V_{\mathrm{RF}P}$ and $V_{\mathrm{RF}N}$) is reduced from 2.15 to 1.65 V while driving R_{LOAD} of 10 kΩ. As shown in Fig. 6(a), when $\hat{V}_{\mathrm{RF}P} = 2.15$ V, the proposed rectifier supplies V_{DC} of 1.68 V as compared to 1.54 and 1.46 V of DR-[8] and DR-[10], respectively. In this state, the peak VCR of the proposed rectifier is 78.1%, while that of DR-[8] and DR-[10] are 71.6% and 68%, respectively. When the $V_{\mathrm{RF}P}$ amplitude is reduced by 0.5 V, the V_{TH} compensating voltage V_C of DR-[10] and the proposed rectifier adapt quickly to new levels. However, due to the charge saturation issue, it takes more than 2.2 ms for V_C of DR-[8] to settle down to a new level for the new $V_{\mathrm{RF}P}$ amplitude. This long response time should be even worse in [8]

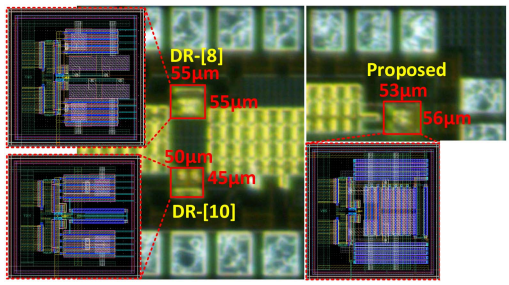

Fig. 7. Die micrographs and layouts of the proposed rectifier and the two reference rectifiers (i.e., DR-[8] and DR-[10]) implemented after [8] and [10].

because C_P used in [8] is 50 pF, which is 50 times larger than that of DR-[8]. Contrarily, in DR-[10], V_C does not correctly follow the $V_{\mathrm{RF}P}$, but it gets delayed. This delay is quite large, as shown in Fig. 6(a). Because of the delay, V_C is even near to its minimum when the input $V_{\mathrm{RF}P}$ is high, and it is high when $V_{\mathrm{RF}P}$ is low, causing a reverse current through the pass transistors, and thus degrading the PCE of DR-[10] at high frequency. Unlike DR-[10], V_C in the proposed rectifier follows the $V_{\mathrm{RF}P}$ well with a slight delay only, as shown in Fig. 6(a). It is because V_C swing is limited by a baseline voltage level V_{CP}, maintained by C_P. By doing so, the proposed rectifier can achieve better DVC of the main conducting transistor even at a higher frequency, i.e., 434 MHz. With the proposed DVC, the proposed rectifier maintains the peak VCR of 78.13% even after the amplitude change, but the VCR performance of DR-[10] is degraded by 6% (from 68% to 62%) due to the change of $V_{\mathrm{RF}P}$ amplitude.

To further evaluate performance of the proposed and reference rectifiers (i.e., DR-[8] and DR[10]), the same simulations were performed at 1-MHz $V_{\mathrm{RF}P}$. Fig. 6(b) shows that the proposed rectifier and DR-[10] exhibit almost the same performance at 1-MHz $V_{\mathrm{RF}P}$. As shown in the figure, V_C of DR-[10] correctly follows the $V_{\mathrm{RF}P}$ and performs reliable DVC at 1-MHz operating frequency. Simulation results in Fig. 6 confirm that the performance of DR-[10] is degraded at high frequencies, while the proposed rectifier achieves the same better performance at high-frequency ranges.

IV. Measurement Results

The proposed rectifier was designed and fabricated in a 180-nm standard CMOS process along with the two reference rectifiers. Fig. 7 shows die micrographs and layouts of the proposed rectifier and DR-[8] and DR-[10], which are designed after [8] and [10]. All the rectifiers are designed with the same size of transistors, but with different bootstrapping circuits, as discussed in Sections II and III. As shown in Fig. 7, the proposed rectifier and DR-[8] occupy an active area of 0.003 mm^2, while DR-[10] occupies 0.0023 mm^2. Each rectifier is connected to an on-chip load capacitor C_L of 32 pF. We measured the standard performance metrics of rectifiers, i.e., peak V_{DC}, VCR, and PCE, with an input signal at 434 MHz.

Fig. 8 compares the V_{DC} level of the proposed rectifier with DR-[8] and DR-[10] when $\hat{V}_{\mathrm{RF}P}$ is increased from 0 to 1 V. As shown in the figure, the proposed rectifier supplies a peak V_{DC} of

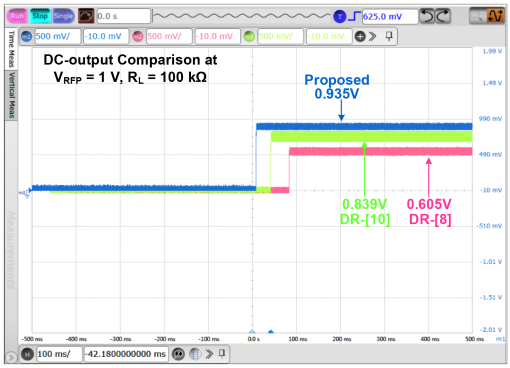

Fig. 8. Oscilloscope capture of V_{DC} of the proposed and reference rectifiers.

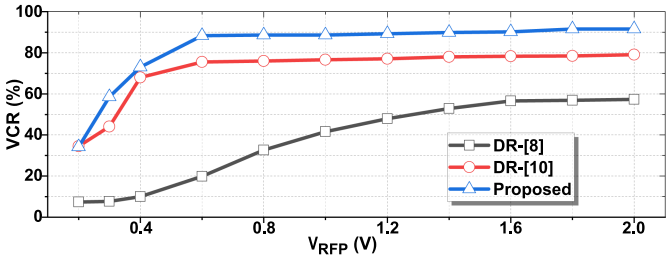

Fig. 9. Measured VCR of the proposed and reference rectifiers, i.e., DR-[8] and DR-[10], over input voltage amplitude.

0.935 V, which is 330 and 96 mV higher than that of DR-[8] and DR-[10], respectively.Higher V_{DC} of the proposed rectifier than its counterparts inevitably results in higher VCR. Fig. 9 shows measured VCRs of DR-[8], DR-[10], and the proposed rectifier for variable input amplitudes from 0.2 to 2.0 V at a fixed R_L of 100 kΩ. As shown in the figure, the proposed rectifier achieves a peak VCR of 91% at $\hat{V}_{RFP}$ of 2 V, while DR-[10] and DR-[8] achieve 79% and 58%, respectively.

To measure the PCE of the rectifiers, the measurement setup shown in Fig. 10 is used. Fig. 10(a) shows the measurement setup picture with test equipments, and the configuration diagram of the PCE measurement setup is shown in Fig. 10(b). An RF signal generator (Keysight N5181B) generates a single-ended 434-MHz RF signal (RF_{IN}), which is converted into a differential signal by a wideband balun transformer (Mini Circuits TC1-1-13MA+). The balun transformer provides the floating differential inputs (i.e., V_{RFP} and V_{RFN}) to the rectifiers. Two resistors of 1 kΩ are connected between the two output ports of the balun and the two input ports of the rectifier, respectively, to measure the input current to the rectifier. Active differential probes (Keysight N2751 A) are used to measure the voltage drop across resistors. Dividing this voltage drop by 1 kΩ provides the input current (i.e., I_{IN}) to the rectifier. Thus, the input current (i.e., I_{IN}) and the input power (i.e., P_{IN}) to the rectifier are calculated as

$$I_{IN}(t) = \frac{V_A(t) - V_B(t)}{R_{INT}} \tag{4}$$

$$P_{IN} = \int_0^T V_B(t) \times I_{IN}(t)\mathrm{d}t. \tag{5}$$

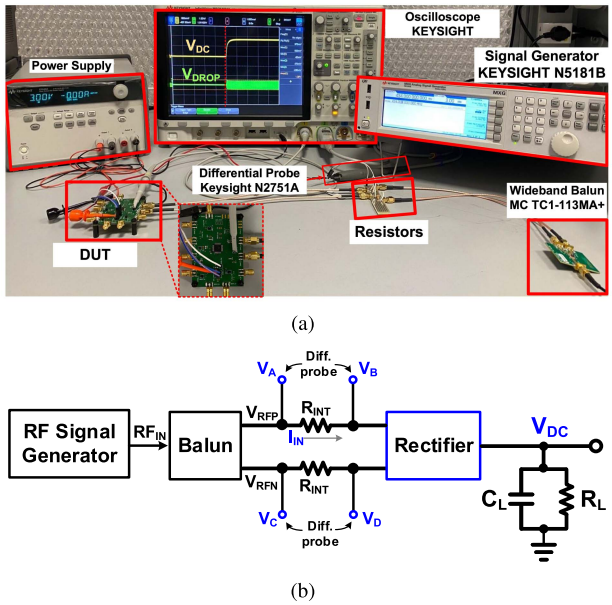

Fig. 10. (a) Picture of the PCE measurement setup. (b) Configuration diagram of the PCE measurement setup.

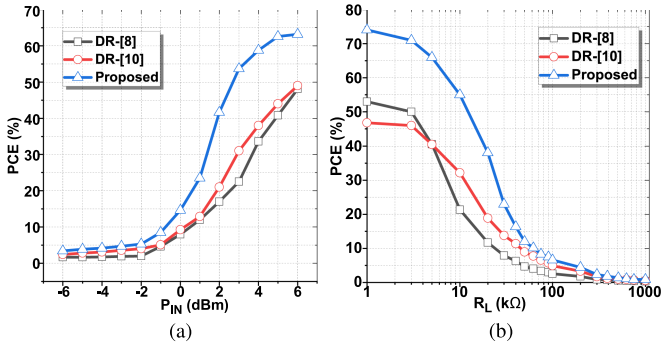

Fig. 11. Measured PCE of the proposed and reference rectifiers (i.e., DR-[8] and DR-[10]) for the following. (a) Variable input power from −6 to 6 dBm at a fixed R_L of 10 kΩ. (b) Variable load resistors from 1 kΩ to 1 MΩ at a fixed input power of 3 dBm.

The output power is calculated as the time integral of the squared V_{DC} divided by R_L and the integration time.

Measured PCE performance of DR-[8], DR-[10], and the proposed rectifier are shown in Fig. 11. Fig. 11(a) shows the measured PCE over a variable input power range from −6 to 6 dBm when the load resistor R_L is fixed at 10 kΩ. At 3-dBm input power, the proposed rectifier achieves a PCE of 54%, much higher than 31% and 22.5% PCEs of DR-[10] and DR-[8], respectively. Fig. 11(b) exhibits the measured PCE over a variable load resistor R_L range from 1 to 1 MΩ when the input power is fixed at 3 dBm. As shown in the figure, the proposed rectifier achieves a PCE of 71% at $R_L = 3$ kΩ, while DR-[8] and DR-[10] achieve 50% and 46% PCEs, respectively. The PCE measurements confirm that the proposed rectifier outperforms the reference rectifiers DR-[8] and DR-[10] by achieving higher PCEs over a variable input power range and a variable output load range.

TABLE I
PERFORMANCE COMPARISON OF THE PROPOSED RECTIFIER WITH STATE-OF-THE-ART RECTIFIERS

	Proposed	**Luo and Liu [5]**	**Kotani et al. [6]**	**Li et al. [7]**
Process (nm)	180	180	180	65
Type/topology	Passive/BS[1]	Passive/VM[2]	Passive/FCC[3]	Passive/FCC[3]
No. of stages	1	3	1	3
Frequency (MHz)	433.92	402	500	200
R_L (kΩ)	1–1000	30	10	3
P_{IN} range (dBm)	From −6 to 6	From −11 to −1	From −35 to 0	From −7 to 7
*Max PCE (%)	71 at 3 kΩ P_{IN} = 3 dBm	31.9 at 30 kΩ P_{IN} = −1dBm	35** at 10 kΩ P_{IN} = −1dBm	64.4 at 3 kΩ P_{IN} = 2.05dBm
Active area (mm^2)	0.003	1.440	0.013	0.384

*PCE measurements are performed without using impedance matching networks in the proposed and reference rectifiers.
[1]Bootstrapped; [2]voltage multiplier; [3]fully cross-coupled; and [4]simulated
**Performance checked at 500 MHz for comparison.

Table I compares the proposed rectifier with different architecture rectifiers operating at similar frequency ranges. Rectifiers in [5] and [7] occupy a large active area, it is because these rectifiers are composed of three stages. As given the table, the proposed rectifier outperforms its existing counterparts in terms of the PCE while occupying a minimum active area.

V. CONCLUSION

A fully differential CMOS rectifier with a new bootstrapping circuit was presented in this letter. The proposed bootstrapping circuit, consisting of a dynamically biased transistor, a series resistor, and a parallel capacitor, performed DVC well even at 434 MHz and improved the overall PCE. The proposed rectifier was cofabricated with two state-of-the-art reference bootstrap rectifiers. The measurement results confirmed that the proposed rectifier outperformed its counterparts.

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