Stability Effect of Load Converter on Source Converter in a Cascaded Buck Converter

Xi Zhang, *Member, IEEE*, Tianshi Wang, Han Bao, *Member, IEEE*, Yihua Hu, *Senior Member, IEEE*, and Bocheng Bao, *Member, IEEE*

***Abstract*—In a cascaded power converter, the input current ripple of load converter is fed forward to the output capacitor of source converter and results in reshaping the output capacitor current and output voltage ripples of source converter. To investigate the stability effect of feedforward current ripple of load converter on source converter, a cascaded power converter comprising two peak-voltage-ripple controlled buck converters is taken as an example. First, the stability effects of chosen circuit parameters of the source converter in cascaded operation and standalone operation are demonstrated and compared. Second, by describing three switching state sequences induced by the feedforward current ripple, a discrete-time map model is established for the cascaded power converter. Based on the map model, the instability mechanism of source converter with the variations of the circuit parameters is thereby expounded, and the stability boundaries are obtained in the circuit parameter planes. The results show that the stability effects of the circuit parameters of source converter with feedforward current ripple are essentially different from those in the standalone operation. The theoretical analyses are verified by the simulation results and experimental results.**

***Index Terms*—Cascaded buck converter, discrete-time map model, feedforward current ripple, load converter, ripple-based control, source converter, stability effect.**

I. Introduction

DUE to its high efficiency, high flexibility, and high power density, the dc distributed power system has been widely used in various applications [1], such as data centers [2], telecom systems [3], electric vehicles [4], renewable energy systems [5], [6], etc. In a dc distributed power system, the cascaded connection is a universal connection method. A typical structure of the cascaded power converter is shown in Fig. 1. The input voltage of the load converter is supplied by the output voltage of the source converter, whereas the output current of the source converter is determined by the input current of the load converter [7]. As a result, the interaction between the source converter and the load converter significantly affects the dynamic characteristics of the cascaded power converter. Typically, the source and load converters are properly designed to be individually stable, but the cascaded power converter composed of them may be unstable [8].

In order to investigate the stability effect of interaction between the source converter and load converter on the cascaded power converter, an impedance-based analysis method was initially proposed by Middlebrook in 1976 and a criterion for evaluating the stability of the cascaded power converter was thereby given, i.e., Middlebrook Criterion [9]. According to the criterion, if the source and load converters are stable individually, and the ratio of the output impedance of the source converter to the input impedance of the load converter (equivalent to the minor loop gain of the cascaded power system) meets the Nyquist criterion, the cascaded power converter is stable. Subsequently, many improved impedance-based stability criteria were proposed to reduce the conservativeness of the Middlebrook Criterion [10] and to meet the stability requirements of the cascaded power system in different applications [11], [12], [13], [14], [15]. In addition, a tightly regulated load converter in the cascaded power converter shows a constant power (CPL) characteristic. This can cause the negative impedance instability in the feeder converter [16]. Therefore, the stability analysis of the converters feeding the CPL has also attracted much attention recently [17], [18], [19], [20], [21]. These results are helpful for us to understand the operation mechanism of the cascaded power converter and to design the cascaded power system with stable and excellent dynamic performance.

However, the impedance-based stability criteria based on the state-space average modeling usually ignore the switching ripples in the cascaded power converter [22]. Thus, even if the impedance-based criteria can be satisfied, the fast-scale instabilities or even the slow-scale instabilities occur in the cascaded power converter [8], [23]. Besides, although simplifying the load converter into a CPL is convenient for the stability analysis of the cascaded converter, the simplification is only effective within a reasonable frequency range and an input voltage span [17]. And, this simplification also ignores the effect of the switching ripple of the load converter.

The instability (such as fast-scale instability) associated with the switching ripple has been widely studied in the switching

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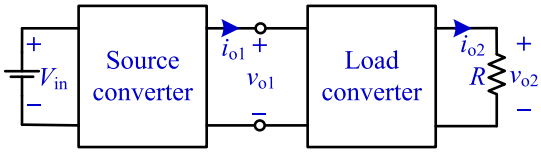

Fig. 1. Typical structure of the cascaded power converter.

converters with resistive load (i.e., in standalone operation) [24], [25], [26], [27], [28], [29], [30], but little attention has been paid on the cascaded converters. Recently, with consideration of the switching ripple interaction between the source converter and the load converter, the stability issue of the cascaded power converters was discussed in [31]. It is pointed out that under the switching ripple interaction, the cascaded power converter can be unstable even if it has been shown to be stable under the impedance-based criterion. Moreover, under the effect of the switching ripples, a standalone unstable source converter can be stabilized by cascading a proper load converter [32]. When the source and load converters have different switching frequencies, the beat frequency oscillation can be introduced by the switching ripple interaction in the cascaded power converter [33]. The results from these academic achievements conflict with the previous understanding and indicate that the switching ripple interaction significantly affect the dynamic characteristics of the cascaded power converter. However, the results in [31] and [32] are only for the case that the duty cycle of the source converter is greater than that of the load converter or otherwise. As a result, the stability effect of the load converter on the source converter in [31] is essentially different from that in [32]. Besides, for the source converter with voltage-mode control [31] or current-mode control [32], the output voltage ripple in the control loop can be attenuated by the compensator. That is, if the feedback gain of the compensator is very small, the voltage ripple in the control loop may be very small. Thus, the stability effect of the feedforward switching ripple of the load converter on the control loop of the source converter can be eliminated by reducing the feedback gain of compensator.

In contrast to the voltage-mode control and current-mode control, the ripple-based control techniques directly use the switching ripple (such as output voltage ripple [34], [35], capacitor current ripple [36], or their combination [29], [37]) at the output of the converter for the output voltage regulation and show fast load transient performance. Thus, the switching ripple is not attenuated by the compensator. When the ripple-based control is used, the stability of the control loop of the source converter is more susceptible to the feedforward switching ripple of the load converter. However, to the authors' knowledge, no literature has reported on this case. Considering that the cascaded buck converters are typical topologies in distributed power system [8], [31], [32], [35], a cascaded power converter comprising two buck converters with ripple-based control is chosen as an example to fully investigate the stability effect of the load converter on the source converter. Then, other three cases that the source and load converters with different switching frequency, the source converter with different controls and topologies are further discussed.

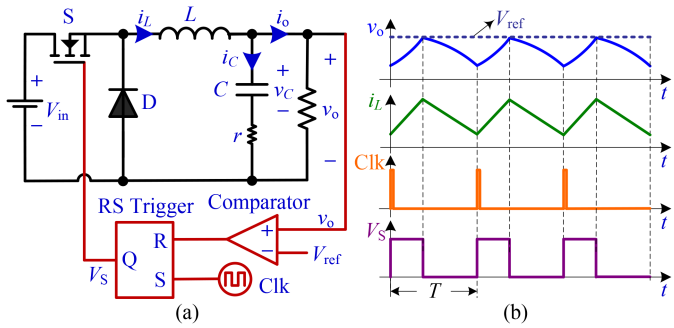

Fig. 2. PVR controlled buck converter. (a) Schematic diagram. (b) Main steady-state waveforms.

The rest of this article is organized as follows. Section II describes the cascaded power converter comprising two buck converters with ripple-based control, and reveals the stability effects of the concerned circuit parameters on the source converter with the feedforward current ripple of the load converter. In Section III, a discrete-time map model is established through describing the three state sequences of the cascaded power converter. Section IV gives the stability boundaries for dividing the stable and unstable regions in the circuit parameter planes based on the stability analyses. In Section V, other three cases are discussed. In Section VI, a hardware experimental prototype is implemented to verify the theoretical analyses and PSIM circuit simulations. Finally, Section VII concludes this article.

II. Stability Effects of Circuit Parameters Under Feedforward Current Ripple

In the ripple-based controls, the peak-voltage-ripple (PVR) control is a basic ripple-based control with a constant switching frequency and simple control circuit [38]. For convenience, the cascaded power converter comprising two PVR controlled buck converter is chosen.

A. Cascaded Power Converter and Operation Waveforms

Before analyzing the cascaded power converter, the operational principle of PVR controlled buck converter is briefly introduced. The schematic diagram and main steady-state waveforms of PVR controlled buck converter are shown in Fig. 2(a) and (b), respectively.

In Fig. 2(a), the output voltage v_o is sensed and then compared with the reference voltage V_{ref} through the comparator. In Fig. 2(b), the steady-state waveforms of output voltage v_o, inductor current i_L, clock signal Clk, and control signal V_S are shown, respectively. At the beginning of each clock period, the switch S is turned ON, and the output voltage v_o and inductor current i_L begin to increase. When the output voltage v_o increases to the reference voltage V_{ref}, the switch S is turned OFF and the diode D is turned ON, and v_o and i_L begin to decrease. Thus, the switching condition can be written as

$$v_o - V_{ref} = 0 \tag{1}$$

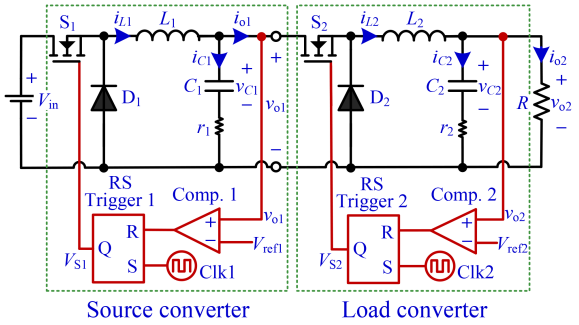

Fig. 3. Cascaded power converter comprising two PVR controlled buck converters.

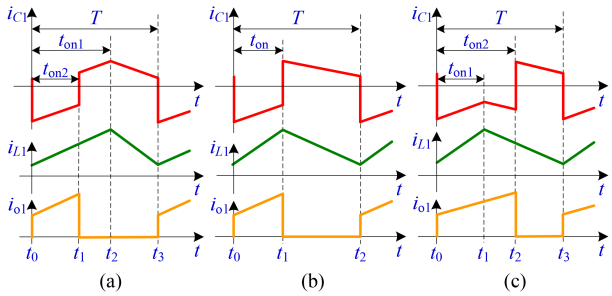

Fig. 4. Operation waveforms of the output capacitor current i_{C1}, inductor current i_{L1}, and output current i_{o1} in the source converter. (a) $D_1 > D_2$. (b) $D_1 = D_2$. (c) $D_1 < D_2$.

The cascaded power converter comprising two PVR controlled buck converters is shown in Fig. 3. Here, i_{o1} and v_{o1} are the output current and output voltage of the source converter or the input current and input voltage of the load converter, respectively. In the source converter, according to Kirchhoff's current law, the output capacitor current i_{C1} of the source converter is equal to the difference between the inductor current i_{L1} and the load current i_{o1}, i.e., $i_{C1} = i_{L1} - i_{o1}$. In other words, the input current ripple of the load converter is fed forward to the output capacitor of the source converter, resulting in that the operation waveform of the output capacitor of the source converter is reshaped.

According to the duty cycle relationships between the source converter and the load converter, the output capacitor current of the source converter has three kinds of operation waveforms, as shown in Fig. 4, where t_{on1} and t_{on2} are the on-time intervals of the source converter and load converter, respectively, T is the switching cycle of the source and load converters. The output voltage ripple $\Delta v_o = \Delta v_C + r i_C$, where Δv_C is the output capacitor voltage ripple. It is used to regulate the output voltage and can greatly affect the stability of PVR controlled buck converter. Note that the duty cycles of the source and load converters are defined as $D_1 = V_{o1}/V_{in}$ and $D_2 = V_{o2}/V_{o1}$, where V_{o1} and V_{o2} are the average output voltages of the source and load converters in the steady state, respectively.

B. Effects of the Concerned Circuit Parameters

The stability effect of the load converter on the source converter can be studied by investigating the stability effects of the correlative circuit parameters with consideration of the feedforward current ripple of the load converter. According to the result given in [38], when operating in the continuous conduction mode (CCM), the PVR controlled buck converter with resistive load (i.e., in standalone operation) is stable if the condition

$$\frac{rC}{T} > 0.5 + \frac{D^2}{1-2D} \text{and} D < 0.5 \tag{2}$$

is satisfied. Here, r and C are the equivalent series resistance (ESR) and capacitance of output capacitor, T is the switching cycle, and D is the duty cycle. Obviously, the stability condition (2) also reflects the effects of the circuit parameters on the stability of the converter. From (2), the stable operation range of the PVR controlled buck converter in the standalone operation is enlarged by decreasing the duty cycle D or increasing the ratio of the output capacitor time constant rC to the switching period T.

Based on the condition (2), the typical circuit parameters for the PVR controlled buck converter in standalone operation are chosen in Table I. To keep the output power the same, $R = 3.6\ \Omega$ is chosen for $V_{ref} = 3$ V and $R = 19.6\ \Omega$ is chosen for $V_{ref} = 7$ V. Thus, when $V_{ref} = 3$ V, the duty cycle $D = V_{ref}/V_{in} = 0.25$ satisfies the condition (2), whereas when $V_{ref} = 7$ V, $D = 0.58$ dissatisfies the condition (2). With the circuit parameters in Table I, the PSIM simulation waveforms of the PVR controlled buck converter under $V_{ref} = 3$ V and 7 V are shown in Fig. 5(a1) and (b1), where Δv_o, i_L, and V_S are the output voltage ripple, inductor current, and control signal, respectively. When $V_{ref} = 3$ V, the PVR controlled buck converter operates in the stable period-1 state, as shown in Fig. 5(a1), whereas when $V_{ref} = 7$ V, the converter operates in the unstable state, as shown in Fig. 5(b1). Obviously, the condition (2) can effectively predict the stability of PVR controlled buck converter in the standalone operation. Remarkably, the period-1 state indicates that the cycle of the operation waveforms is the same as the clock cycle, and the periodic-N state means that the cycle of the operation waveforms is the same as the N-fold clock cycle.

As a comparison, the circuit parameters of the cascaded power converter in Fig. 3 are chosen in Table II, where the load resistance R is chosen as $0.4\ \Omega$ to keep the output power the same with that in Fig. 5(a1) and (b1). With the circuit parameters in Table II, the simulation waveforms of the source converter for $V_{ref1} = 3$ V and 7 V are shown in Fig. 5(a2) and (b2), respectively, where Δv_{o1}, i_{L1}, and V_{S1} are the output voltage ripple, inductor current, and control signal of the source converter, respectively, and V_{S2}

TABLE I
CIRCUIT PARAMETERS FOR THE PVR CONTROLLED BUCK CONVERTER

Symbols	Physical Significations	Values
V_{in}	Input voltage	12 V
L	Inductance	120 μH
C	Output capacitance	470 μF
r	Output capacitor ESR	50 mΩ
V_{ref}	Reference voltage	3 V/7 V
f_S	Switching frequency	100 kHz
R	Load resistance	3.6 Ω/19.6 Ω

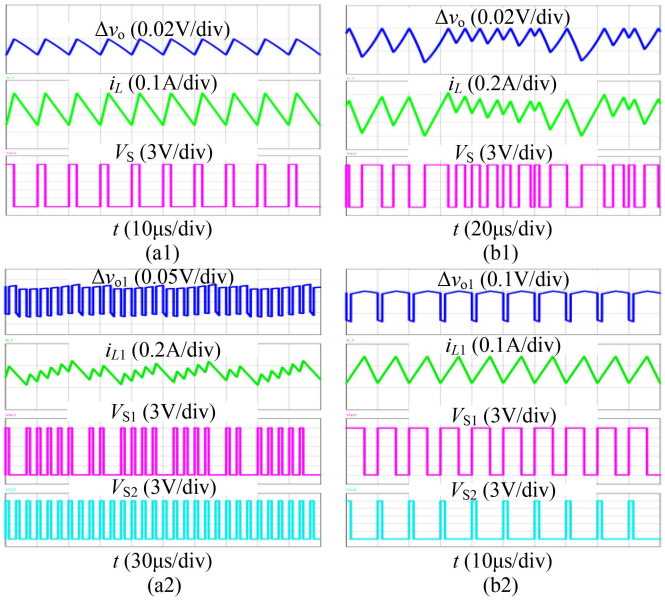

Fig. 5. PSIM simulation waveforms for different reference voltages of V_{ref1}, where (a1) and (b1) stand for the PVR controlled buck converter in the standalone operation, and (a2) and (b2) stand for the PVR controlled buck converter in the cascaded operation. (a) $V_{\mathrm{ref1}} = 3$ V. (b) $V_{\mathrm{ref1}} = 7$ V.

TABLE II
CIRCUIT PARAMETERS FOR THE CASCADED POWER CONVERTER

Symbols	Physical Significations	Values
V_{in}	Input voltage	12 V
L_1, L_2	Inductance	120 μH, 120 μH
C_1, C_2	Output capacitance	470 μF, 470 μF
r_1, r_2	Output capacitor ESR	50 mΩ, 20 mΩ
V_{ref1}, V_{ref2}	Reference voltage	3 V/7 V, 1 V
f_{S1}, f_{S2}	Switching frequency	100 kHz
R	Load resistance	0.4 Ω

is the control signal of the load converter. As can be seen, the source converter operates in the unstable state when $V_{\mathrm{ref1}} = 3$ V and in the stable period-1 state when $V_{\mathrm{ref1}} = 7$ V. Obviously, the simulation results in Fig. 5(a2) and (b2) are contrary to the prediction of the condition (2). It should be emphasized that as observed from Fig. 5(a2) and (b2), the load converter always operates in the stable state.

Furthermore, the stability effect of the ratio of the output capacitor time constant to the switching cycle, i.e., $r_1 C_1/T$, on the source converter is investigated by fixing C_1 and T and adjusting r_1. With the circuit parameters in Table II and $V_{\mathrm{ref1}} = 8$ V, the PSIM simulation waveforms of the source converter for $r_1 = 15$ mΩ and 24 mΩ are shown in Fig. 6(a) and (b), respectively. As can be observed, the source converter operates in the stable period-1 state when $r_1 = 15$ mΩ, whereas the source converter operates in the unstable period-2 state when $r_1 = 24$ mΩ. The simulation results in Fig. 6 are also contrary to the prediction of the condition (2).

In addition, with the circuit parameters in Table II and $V_{\mathrm{ref1}} = 8$ V, the PSIM simulation waveforms of the source converter for

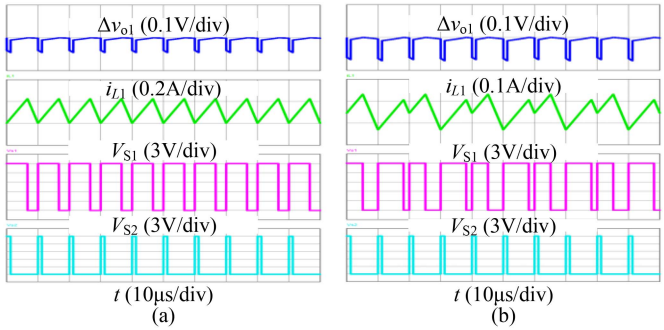

Fig. 6. PSIM simulation waveforms for different values of the output capacitor ESR r_1. (a) $r_1 = 15$ mΩ. (b) $r_1 = 24$ mΩ.

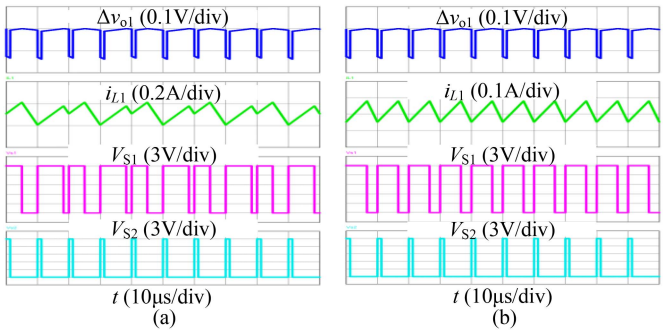

Fig. 7. PSIM simulation waveforms for different inductances of L_1. (a) $L_1 = 195$ μH. (b) $L_1 = 210$ μH.

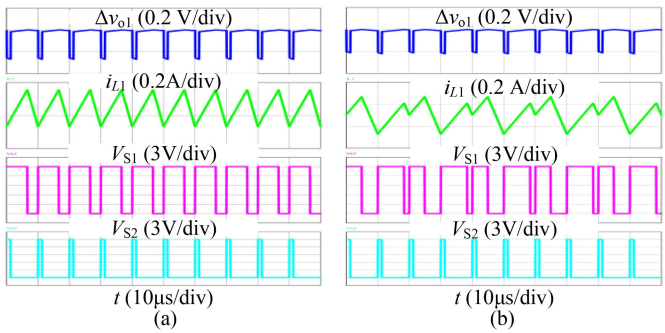

Fig. 8. PSIM simulation waveforms for different load resistances of R. (a) $R = 0.2$ Ω. (b) $R = 0.25$ Ω.

different inductances of L_1 and different load resistances of R are shown in Figs. 7 and 8, respectively. When $L_1 = 195$ μH or $R = 0.25$ Ω, the source converter operates in the unstable period-2 state, as shown in Fig. 7(a) or Fig. 8(b), whereas when $L_1 = 210$ μH or $R = 0.2$ Ω, the source converter operates in the stable period-1 state, as shown in Fig. 7(b) or Fig. 8(a). Obviously, the simulation results in Figs. 7 and 8 do not agree with the condition (2).

In conclusion, the stable regions of the reference voltage V_{ref1}, output capacitor ESR r_1, inductance L_1, and load resistance R are greatly changed by the feedforward current ripple of the load converter. In other words, the stability of the source converter is significantly affected by the feedforward ripple of the load converter in the cascaded power converter.

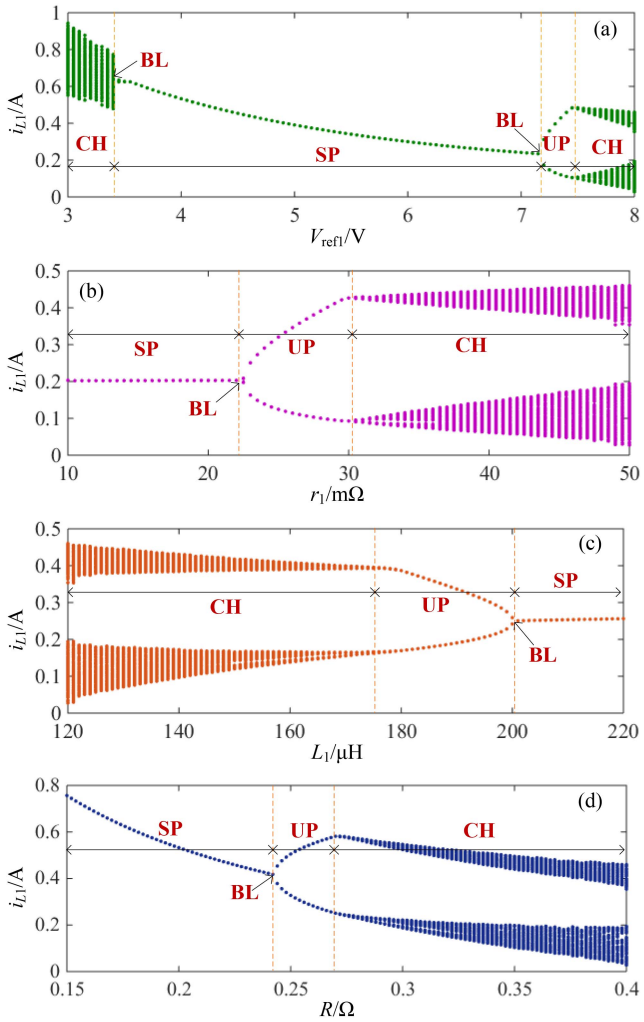

Fig. 9. Bifurcation diagrams of the inductor current i_{L1} with respect to the concerned circuit parameters. (a) $V_{\rm ref1} \in [3\ {\rm V}, 8\ {\rm V}]$. (b) $r_1 \in [10\ {\rm m\Omega}, 50\ {\rm m\Omega}]$. (c) $L_1 \in [120\ \mu{\rm H}, 220\ \mu{\rm H}]$. (d) $R \in [0.15\ \Omega, 0.4\ \Omega]$.

C. Circuit Parameter-Related Bifurcation Analyses

In this section, the bifurcation analyses are carried out to demonstrate the dynamical behaviors of the source converter with the variations of $V_{\rm ref1}$, r_1, L_1, and R. Based on the data acquired from PSIM circuit simulations, the bifurcation diagrams of the inductor current i_{L1} with respect to $V_{\rm ref1}$, r_1, L_1, and R are depicted using MATLAB software tool and their results are shown in Fig. 9(a)–(d), where SP, UP, CH, and BL represent the stable period-1, unstable period-N ($N \geq 2$), chaos, and instability borderline, respectively. It should be emphasized that the load converter is always in the stable period-1 state in Fig. 9(a)–(d).

As shown in Fig. 9(a), when increasing $V_{\rm ref1}$ from 3 to 8 V, i.e., the duty cycle D_1 from 0.25 to 0.67 and D_2 from 0.125 to 0.33, the motion orbit of the source converter mutates from chaos to period-1 via border-collision bifurcation at $V_{\rm ref1} = 3.45$ V, then to period-2 via period-doubling bifurcation at $V_{\rm ref1} = 7.15$ V, and finally to chaos via border-collision bifurcation at $V_{\rm ref1} = 7.45$ V. At the first bifurcation point $V_{\rm ref1} = 3.45$ V, the duty cycles of the source and load converters are $D_1 = 0.28$ and $D_2 = 0.29$. At the second bifurcation point $V_{\rm ref1} = 7.15$ V, they are $D_1 = 0.6$ and $D_2 = 0.12$. According to the condition (2), when the converter operates in the standalone operation, its stable operation range is enlarged with the decrease of the duty cycle. However, when the converter operates in the cascaded operation, its stable operation range is narrowed with the decrease of the duty cycle.

As shown in Fig. 9(b), when increasing r_1 from 10 to 50 mΩ, the motion orbit of the source converter alters from period-1 to period-2 at $r_1 = 22$ mΩ via period-doubling bifurcation, and ultimately to chaos at $r_1 = 30$ mΩ via border-collision bifurcation. According to the condition (2), when the PVR controlled buck converter operates in the standalone operation, its stable operation range is enlarged with the increase of the output capacitor ESR. However, when the converter operates in the cascaded operation, its stable operation range is narrowed with the increase of the output capacitor ESR.

Finally, as shown in Fig. 9(c) and (d), when increasing L_1 from 120 to 220 μH or decreasing R from 0.4 to 0.15 Ω, the motion orbit of the source converter changes from chaos to period-2 at $L_1 = 123.4$ μH or $R = 0.27$ Ω via border-collision bifurcation, then to period-1 at $L_1 = 151$ μH or $R = 0.24$ Ω via inverse period-doubling bifurcation. According to the condition (2), when the PVR controlled buck converter operates in the standalone operation, its stability is independent of the inductance and load resistance. However, when the PVR controlled buck converter is used as the source converter of the cascaded power converter, its stable operation range is enlarged with the increase of L_1 or the decrease of R.

III. Discrete-Time Map Model and Jacobi Matrix

In this section, we establish a discrete-time map model for the cascaded power converter and derive its Jacobian matrix at an invariant point.

A. State Equation and Switching State Sequences

To predict the effects of switching ripple on the stability of the dc–dc switching converter, many models have been explored. These models fall into two main categories. One is the improved small-signal model [24], [25], [26], [27], [28]. With such the improved models, frequency-domain analysis methods, such as the Bode diagram, can be used for the stability analysis. Another is the discrete-time map model [8], [29], [30], [39], [40]. Based on these discrete-time map models, time-domain analysis methods, such as the eigenvalues of the Jacobi matrix, can be used for the stability analysis. In general, when the circuit parameters vary widely, the discrete-time map model can accurately predict the nonlinear dynamical behaviors of the converter [29]. Therefore, the discrete-time map model is adopted in this article.

Within the range of circuit parameters concerned in this article, the source converter and the load converter are always in CCM. There are four possible switching states based on the states of switch $\rm S_{\it i}$ and diode $\rm D_{\it i}$ ($i = 1, 2$), which are expressed as follows.

Switching state 1: $\rm S_1$ is ON, $\rm D_1$ is OFF; $\rm S_2$ is ON, $\rm D_2$ is OFF
Switching state 2: $\rm S_1$ is ON, $\rm D_1$ is OFF; $\rm S_2$ is OFF, $\rm D_2$ is ON
Switching state 3: $\rm S_1$ is OFF, $\rm D_1$ is ON; $\rm S_2$ is ON, $\rm D_2$ is OFF

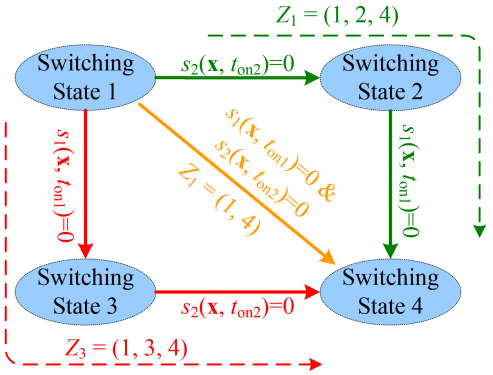

Fig. 10. Three switching state sequences suitable for discrete-time modeling of the cascaded power converter.

Switching state 4: S_1 is OFF, D_1 is ON; S_2 is OFF, D_2 is ON

Accordingly, the state equation for the mth (m = 1, 2, 3, 4) switching state can be written as

$$\dot{\mathbf{x}}(t) = \mathbf{A}_m\mathbf{x}(t) + \mathbf{B}_m \tag{3}$$

where $\mathbf{x}(t) = [i_{L1}\ v_{C1}\ i_{L2}\ v_{C2}]^{\mathrm{T}}$ is the state variable vector, $\mathbf{A}_m$ and $\mathbf{B}_m$ are the parameter matrix and input matrix, respectively. The expressions of $\mathbf{A}_m$ and $\mathbf{B}_m$ are given as follows:

$$\mathbf{A}_1 = \mathbf{A}_3 = \begin{bmatrix} -r_1/L_1 & -1/L_1 & r_1/L_1 & 0 \\ 1/C_1 & 0 & -1/C_1 & 0 \\ r_1/L_2 & 1/L_2 & -(r_1+\kappa r_2)/L_2 & -\kappa/L_2 \\ 0 & 0 & (R-\kappa r_2)/RC_2 & -\kappa/RC_2 \end{bmatrix}$$

$$\mathbf{A}_2 = \mathbf{A}_4 = \begin{bmatrix} -r_1/L_1 & -1/L_1 & 0 & 0 \\ 1/C_1 & 0 & 0 & 0 \\ 0 & 0 & -\kappa r_2/L_2 & -\kappa/L_2 \\ 0 & 0 & (R-\kappa r_2)/RC_2 & -\kappa/RC_2 \end{bmatrix}$$

$$\mathbf{B}_1 = \mathbf{B}_2 = \begin{bmatrix} V_{\mathrm{in}}/L_1 & 0 & 0 & 0 \end{bmatrix}^{\mathrm{T}},\ \mathbf{B}_3 = \mathbf{B}_4 = \begin{bmatrix} 0 & 0 & 0 & 0 \end{bmatrix}^{\mathrm{T}},$$

$\kappa = R/(R+r_2)$.

With the switching condition (1), the switching function for the cascaded power converter can be written as

$$s(\mathbf{x}, t_{oni}) = v_{oi} - V_{refi} \tag{4}$$

where $t_{on\,i}$ can be obtained by solving $s(\cdot) = 0$.

As one can see from Fig. 4, there are three possible switching state sequences for (4) during a switching cycle in the steady state, as shown in Fig. 10. The three switching state sequences can be described as follows.

If $t_{on1} > t_{on2}$, the switching states evolve from $1 \to 2 \to 4$. Such a case is denoted as $Z_1 = (1, 2, 4)$.

If $t_{on1} = t_{on2}$, the switching states evolve from $1 \to 4$. Such a case is denoted as $Z_2 = (1, 4)$.

If $t_{on1} < t_{on2}$, the switching states evolve from $1 \to 3 \to 4$. Such a case is denoted as $Z_3 = (1, 3, 4)$.

Thus, according to the abovementioned three switching state sequences, a discrete-time map model can be established for the cascaded power converter.

B. Discrete-Time Map Model

Referring to the work in [39] and [40], the local map $\mathbf{P}_m$ from the initial value $\mathbf{x}(t_{m-1})$ to the final value $\mathbf{x}(t_m)$ in the mth switching sate can be expressed as

$$\mathbf{P}_m : \mathbf{x}(t_{m-1}) \to \mathbf{x}(t_m) := \phi_m(\tau_m)\mathbf{x}(t_{m-1}) + \psi_m(\tau_m)\mathbf{B}_m \tag{5}$$

where

$\tau_m = t_m - t_{m-1}$, $\phi_m(\tau_m) = \mathrm{e}^{\mathbf{A}_m\tau_m}$, and $\psi_m(\tau_m) = \int_0^{\tau_m} \mathrm{e}^{\mathbf{A}_m\xi}\mathrm{d}\xi$.

Since $\mathbf{A}_m$ is invertible, $\psi_m(\tau_m)$ can be further written as

$$\psi_m(\tau_m) = \mathbf{A}_m^{-1}(\phi_m(\tau_m) - \mathbf{I}). \tag{6}$$

Define $\mathbf{x}_n = \mathbf{x}(nT)$ and $\mathbf{x}_{n+1} = \mathbf{x}((n+1)T)$. If there are K switching states in the nth switching cycle, the map from $\mathbf{x}_n$ to $\mathbf{x}_{n+1}$ can be described as

$$\mathbf{x}_{n+1} = f(\mathbf{x}_n) = \mathbf{\Phi}(\tau)\mathbf{x}_n + \mathbf{\Psi}(\tau) \tag{7}$$

where

$$\mathbf{\Phi}(\tau) = \prod_{m=K}^{1} \phi_m(\tau_m)$$

$$\mathbf{\Psi}(\tau) = \sum_{j=1}^{K-1}\left[\left(\prod_{m=K}^{j+1}\phi_m(\tau_m)\right)\psi_j(\tau_j)\mathbf{B}_j\right] + \psi_K(\tau_K)\mathbf{B}_K.$$

Due to three switching state sequences during a switching cycle, the discrete-time map model of the cascaded power converter is composed of three maps from $\mathbf{x}_n$ to $\mathbf{x}_{n+1}$.

For the switching state sequence Z_1, the map from $\mathbf{x}_n$ to $\mathbf{x}_{n+1}$ is yielded as

$$\mathbf{x}_{n+1} = f_1(\mathbf{x}_n) = \mathbf{\Phi}_1(\tau)\mathbf{x}_n + \mathbf{\Psi}_1(\tau) \tag{8}$$

where $\tau_1 = t_{on2}$, $\tau_2 = t_{on1} - t_{on2}$, and $\tau_4 = T - t_{on1}$. The on-time intervals t_{on2} and t_{on1} can be obtained by solving the following equations:

$$s_1(\mathbf{x}_n, t_{on2}) = v_{o2} - V_{ref2} = \mathbf{K}_1\mathbf{x}(t_1) - V_{ref2} = 0 \tag{9a}$$

$$s_2(\mathbf{x}(t_1), t_{on1}) = v_{o1} - V_{ref1} = \mathbf{K}_2\mathbf{x}(t_2) - V_{ref1} = 0 \tag{9b}$$

where $\mathbf{K}_1 = [0\ 0\ \kappa r_2\ \kappa]$ and $\mathbf{K}_2 = [r_1\ 1\ 0\ 0]$.

For the switching state sequence Z_2, the map from $\mathbf{x}_n$ to $\mathbf{x}_{n+1}$ is yielded as

$$\mathbf{x}_{n+1} = f_2(\mathbf{x}_n) = \mathbf{\Phi}_2(\tau)\mathbf{x}_n + \mathbf{\Psi}_2(\tau) \tag{10}$$

where $\tau_1 = t_{on1} = t_{on2}$ and $\tau_4 = T - t_{on1} = T - t_{on2}$. The on-time interval t_{on1} or t_{on2} can be yielded from the following equation:

$$s_1(\mathbf{x}_n, t_{on1}) = v_{o1} - V_{ref1} = \mathbf{K}_3\mathbf{x}(t_1) - V_{ref1} = 0 \tag{11a}$$

or

$$s_2(\mathbf{x}_n, t_{on2}) = v_{o2} - V_{ref2} = \mathbf{K}_1\mathbf{x}(t_1) - V_{ref2} = 0 \tag{11b}$$

where $\mathbf{K}_3 = [r_1\ 1\ -r_1\ 0]$.

For the switching state sequence Z_3, the map from $\mathbf{x}_n$ to $\mathbf{x}_{n+1}$ is written as

$$\mathbf{x}_{n+1} = f_3(\mathbf{x}_n) = \mathbf{\Phi}_3(\tau)\mathbf{x}_n + \mathbf{\Psi}_3(\tau) \tag{12}$$

where $\tau_1 = t_{\text{on1}}$, $\tau_3 = t_{\text{on2}} - t_{\text{on1}}$, and $\tau_4 = T - t_{\text{on2}}$. The on-time intervals t_{on1} and t_{on2} can be solved from the following equations:

$$s_1(\mathbf{x}_n, t_{\text{on1}}) = v_{\text{o1}} - V_{\text{ref1}} = \mathbf{K}_3\mathbf{x}(t_1) - V_{\text{ref1}} = 0 \tag{13a}$$

$$s_2(\mathbf{x}(t_1), t_{\text{on2}}) = v_{\text{o2}} - V_{\text{ref2}} = \mathbf{K}_1\mathbf{x}(t_2) - V_{\text{ref2}} = 0. \tag{13b}$$

Consequently, the discrete-time map model of the cascaded power converter can be derived as

$$\mathbf{x}_{n+1} = \begin{cases} f_1(\mathbf{x}_n) & t_{\text{on1}} > t_{\text{on2}} \\ f_2(\mathbf{x}_n) & t_{\text{on1}} = t_{\text{on2}} \\ f_3(\mathbf{x}_n) & t_{\text{on1}} < t_{\text{on2}} \end{cases} \tag{14}$$

where $f_1(\mathbf{x}_n)$, $f_2(\mathbf{x}_n)$, and $f_3(\mathbf{x}_n)$ are expressed by (8), (10), and (12), respectively.

C. Jacobi Matrix at the Invariant Point

The stability of a discrete-time map model can be studied using its invariant point. Define the invariant point of the cascaded power converter as $\mathbf{X}_{\text{Q}} = [I_{L1}\ V_{C1}\ I_{L2}\ V_{C2}]^{\text{T}}$. With the discrete-time map model (14), the steady-state solution of the state variables can be obtained by putting $\mathbf{x}_{n+1} = \mathbf{x}_n = \mathbf{X}_{\text{Q}}$. When operating in the steady state, the output capacitor voltages of the source and load converters are equal to their output voltages, i.e., $V_{C1} = V_{\text{o1}}$ and $V_{C2} = V_{\text{o2}}$. Therefore, we have

$$V_{\text{o}i} = V_{\text{ref}i},\ I_{L2} = V_{\text{o2}}/R,\ I_{L1} = D_2 I_{L2}.$$

The Jacobi matrix $\mathbf{J}$ of the discrete-time map model (14) evaluated at the invariant point $\mathbf{X}_{\text{Q}}$ can be described by

$$\mathbf{J}(\mathbf{X}_{\text{Q}}) = \mathbf{\Phi}(\tau) - \frac{\partial f}{\partial \mathbf{t}}\left(\frac{\partial \mathbf{s}}{\partial \mathbf{t}}\right)^{-1}\left(\frac{\partial \mathbf{s}}{\partial \mathbf{x}_n}\right). \tag{15}$$

Here, $\mathbf{s} = [s_1(\cdot)\, s_2(\cdot) \cdots s_{K-1}(\cdot)]^{\text{T}}$ is the vector of the switching function, and $\mathbf{t} = [t_1\ t_2 \cdots t_{K-1}]^{\text{T}}$ is the vector of the switching instant. Moreover, the three partial derivative matrixes in (15) can be expressed as

$$\frac{\partial f}{\partial \mathbf{t}} = \begin{bmatrix} \frac{\partial f}{\partial t_1} \\ \frac{\partial f}{\partial t_2} \\ \vdots \\ \frac{\partial f}{\partial t_{K-1}} \end{bmatrix}^{\text{T}},$$

$$\frac{\partial \mathbf{s}}{\partial \mathbf{t}} = \begin{bmatrix} \frac{\partial s_1}{\partial t_1} & \frac{\partial s_1}{\partial t_2} & \cdots & \frac{\partial s_1}{\partial t_{K-1}} \\ \frac{\partial s_2}{\partial t_1} & \frac{\partial s_2}{\partial t_2} & \cdots & \frac{\partial s_2}{\partial t_{K-1}} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{\partial s_{K-1}}{\partial t_1} & \frac{\partial s_{K-1}}{\partial t_2} & \cdots & \frac{\partial s_{K-1}}{\partial t_{K-1}} \end{bmatrix},$$

$$\frac{\partial \mathbf{s}}{\partial \mathbf{x}_n} = \begin{bmatrix} \frac{\partial s_1}{\partial \mathbf{x}_n} & \frac{\partial s_2}{\partial \mathbf{x}_n} & \cdots & \frac{\partial s_{K-1}}{\partial \mathbf{x}_n} \end{bmatrix}.$$

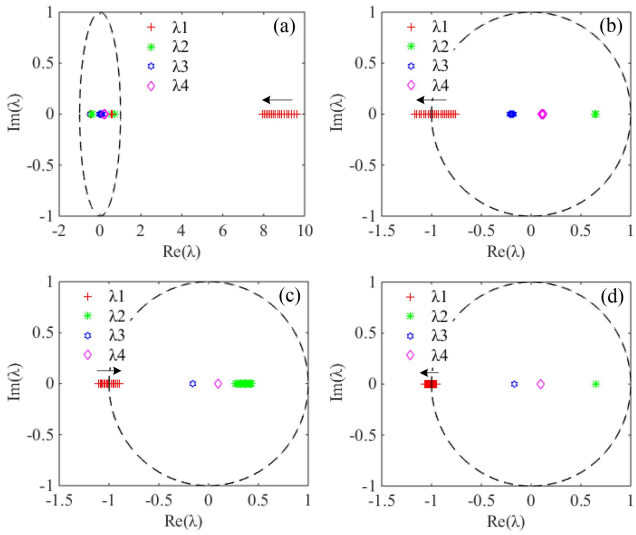

Fig. 11. Loci of the eigenvalues with respect to the three concerned circuit parameters. (a) $V_{\text{ref1}} \in$ [3.3 V, 4 V]. (b) $V_{\text{ref1}} \in$ [6.5 V, 7.5 V]. (c) $r_1 \in$ [19 mΩ, 26 mΩ]. (d) $L_1 \in$ [190 μH, 216 μH].

The elements of the Jacobi matrix for three switching state sequences are given in the Appendix.

IV. Stability Analysis and Stability Boundaries

This section performs the stability analysis and derives the stability boundaries for the cascaded power converter. Furthermore, the transient performance of the presented work is compared with that of the works in the existing literature.

A. Stability Analysis

The stability analysis of the cascaded power converter can be performed by detecting the eigenvalues of the Jacobi matrix (15) at the invariant point $\mathbf{X}_{\text{Q}}$. The eigenvalues can be solved from the following characteristic equation:

$$\det\left(\lambda\mathbf{I} - \mathbf{J}(\mathbf{X}_{\text{Q}})\right) = 0. \tag{16}$$

Here, three concerned circuit parameters V_{ref1}, r_1, and L_1 are chosen to carry out the stability analysis. Based on (15) and (16), the loci of four eigenvalues (λ_1, λ_2, λ_3, λ_4) with respect to V_{ref1}, r_1, and L_1 are numerically depicted, as shown in Fig. 11(a)–(d). Note that to cover the inductor current ripple effect of the source converter, the abovementioned invariant point is modified as $\mathbf{X}_{\text{Q}} = [I_{L1}{+}0.5\Delta i_L\ V_{C1}\ I_{L2}\ V_{C2}]^{\text{T}}$. Therefore, the eigenvalues for V_{ref1}, r_1, and L_1 are listed in Tables III, IV, and V, respectively.

As V_{ref1} increases from 3.3 to 4 V, the eigenvalue λ_1 jumps into the unit circle and the eigenvalues λ_2, λ_3, and λ_4 are always inside the unit circle, leading to the occurrence of the border-collision bifurcation, as shown in Fig. 11(a). As V_{ref1} increases from 6.5 to 7.5 V or L_1 increases from 190 to 216 μH, λ_1 leaves the unit circle via -1 and λ_2, λ_3, λ_4 are always inside the unit circle, resulting in the occurrence of the reverse period-doubling bifurcation, as shown in Fig. 11(b) and (d), respectively. Meanwhile, as r_1 increases from 19 to 26 mΩ, λ_1 enters into the unit circle via -1 and λ_2, λ_3, λ_4 are always

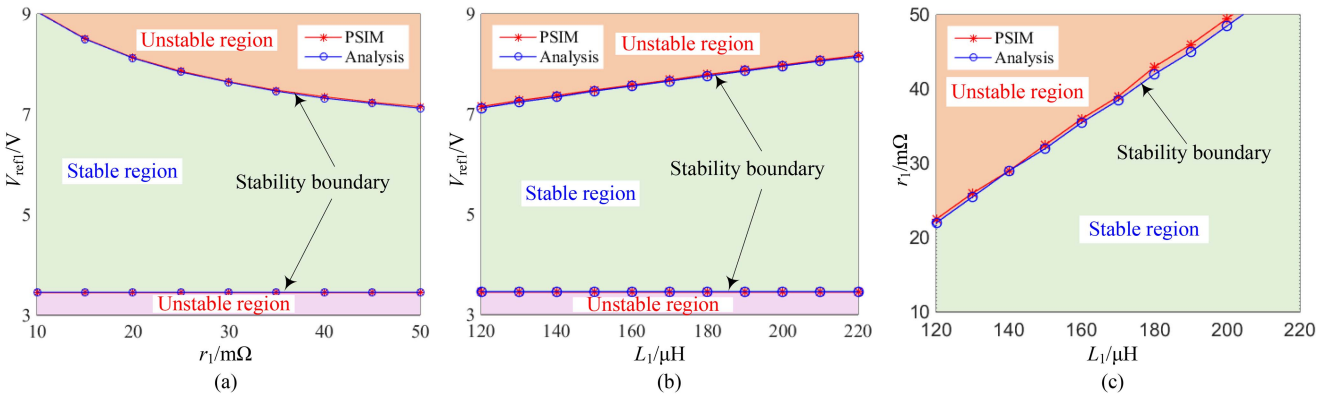

Fig. 12. Stability boundaries in the circuit parameter planes, where the circuit parameters are listed in Table II and $V_{\rm ref1} = 8$ V. (a) In the r_1 - $V_{\rm ref1}$ plane. (b) In the L_1 - $V_{\rm ref1}$ plane. (c) In the L_1 - r_1 plane.

TABLE III
EIGENVALUES FOR THE REFERENCE VOLTAGE $V_{\rm REF1}$

$V_{\rm ref1}$ (V)	Eigenvalues (λ_1, λ_2, λ_3, λ_4)	Module (Max)	Stability
3.4	(8.482, 0.713, −0.467, 0.218)	8.482	Unstable
3.46	(7.946, 0.714, −0.456, 0.214)	7.946	Unstable
3.47	(−0.454, 0.551, 0.101, 0.215)	0.551	Stable
3.5	(−0.449, 0.553, 0.093, 0.213)	0.553	Stable
7.1	(−0.990, 0.649, −0.191, 0.110)	0.990	Stable
7.2	(−1.033, 0.650, −0.188, 0.108)	1.033	Unstable
7.3	(−1.078, 0.652, −0.185, 0.107)	1.078	Unstable

TABLE IV
EIGENVALUES FOR THE OUTPUT CAPACITOR ESR r_1

r_1 (mΩ)	Eigenvalues (λ_1, λ_2, λ_3, λ_4)	Module (Max)	Stability
20	(−0.929, 0.297, −0.162, 0.093)	0.929	Stable
22.1	(−0.998, 0.350, −0.162, 0.093)	0.998	Stable
22.2	(−1.001, 0.352, −0.162, 0.093)	1.001	Unstable
23	(−1.024, 0.370, −0.162, 0.094)	1.024	Unstable
25	(−1.078, 0.410, −0.163, 0.094)	1.078	Unstable

TABLE V
EIGENVALUES FOR THE INDUCTANCE L_1

L_1 (μH)	Eigenvalues (λ_1, λ_2, λ_3, λ_4)	Module (Max)	Stability
202	(−1.011, 0.650, −0.168, 0.097)	1.011	Unstable
204	(−1.002, 0.649, −0.168, 0.097)	1.0018	Unstable
204.4	(−1.000, 0.649, −0.168, 0.097)	1.000	Critical
205	(−0.997, 0.649, −0.168, 0.097)	0.997	Stable
208	(−0.984, 0.649, −0.168, 0.097)	0.984	Stable

inside the unit circle, leading to the occurrence of the forward period-doubling bifurcation, as shown in Fig. 11(c). Thus, the instability of the cascaded power converter is caused by the border-collision bifurcation or period-doubling bifurcation.

B. Stability Boundaries

Based on the aforementioned eigenvalue analyses, the stability boundaries for dividing the stable and unstable regions are presented in the r_1-$V_{\rm ref1}$ plane, L_1-$V_{\rm ref1}$ plane, and L_1-r_1 plane, as depicted in Fig. 12(a)–(c). These boundaries are consistent with the results obtained from the PSIM circuit simulations.

When $V_{\rm ref1} < 3.45$ V, there yields $D_1 < D_2$, the source converter is always in the unstable state, as shown in Fig. 12(a) and (b); when $V_{\rm ref1} > 3.45$ V, there yields $D_1 > D_2$, the stable region of the source converter is enlarged with the decrease of the output capacitor ESR r_1 or the increase of the inductance L_1, as shown in Fig. 12(a)–(c). Thus, the qualitative conclusions are obtained as follows. If the duty cycle of the load converter is greater than that of the source converter, the source converter always operates in an unstable state and its stability is not affected by inductance and output capacitor ESR of the source converter. Otherwise, it is in stable state and its stability can be improved by decreasing the output capacitor ESR or increasing the inductance value of the source converter. These qualitative conclusions are helpful for the key circuit parameters selection to ensure the stable operation of the cascaded power converter. For example, an output capacitor with small ESR is more benefit to the stable operation of the source converter with ripple-based control in the cascaded power converter.

Besides, a novel extended-frequency small-signal model is proposed in [31], which can effectively predict the effects of switching ripple interaction on the stability of the cascaded converter in frequency domain. And, the modeling method in [31] can be applied to the cascaded converter in this article, deserving further research.

C. Comparison of Transient Performance

Recently, some novel control techniques have been proposed to improve the transient performance of the converter [41], [42], [43], [44], [45], [46]. A comparison of the presented work with the works in the existing literature is performed and shown in Table VI. To accurately compare the transient performance of the control schemes in Table VI, a figure of merit (FOM) is defined as

$$\text{FOM} = \frac{\Delta I_{\rm o}}{(t_{\rm up} + t_{\rm down}) \times (V_{\rm ov} + V_{\rm un}) \times f_{\rm S} \times \sqrt{C/L}} \quad (17)$$

TABLE VI
COMPARISON OF THIS WORK WITH OTHERS' WORKS

References	[41]	[42]	[43]	[44]	[45]	[46]	This work
Control scheme	VMC with HFFT	RBAOT	ADP and ANN	Alternative control	Improved optimum-damping control	HHFMC	PVR control
Analog/Digital	Analog	Analog	Digital	Digital	Analog	Digital	Analog
Sensing current	No	No	Yes	Yes	Yes	No	No
Input voltage (V)	2.7-4.2	5-18	42	3.3	2.8-4.0	30	5-7
Output voltage (V)	1.0-2.5	0.8-5	-	1.8	1.4-2.5	15	1.0-2.0
Output inductance (μH)	2.2	4.7	5630	0.8	2.2	10000	2.2
Output capacitance (μF)	10	10	5	100	10	1000	50
Line regulation	0.13%	-	-	-	0.14%	0.008%	0.06%
Load regulation	0.444%	-	-	-	-	0.0667%	0.16%
Switching frequency (MHz)	2.5	1	0.01	0.9	1	-	1
Load current step (mA)	500	400	800	300	550	1350	430
Settling time of step up/down (μs)	4.5/4.5	5/5	-/3000	0.3/0.3	1.8/1.8	-	1.5/3.2
Undershoot/Overshoot voltage (mV)	27/30	17/35	-/2000	300/400	45/40	520/30	40/45
Controller Complexity	Middle	Middle	Complex	Middle	Middle	Middle	Simple
FOM	0.182	0.544	-	0.079	0.843	-	0.226

where $t_{\rm up}$ and $t_{\rm down}$ indicate the settling time of the load step up and down, respectively, $V_{\rm ov}$ and $V_{\rm un}$ represent the overshoot and undershoot voltage, respectively. The definition of (17) is based on the fact that the switching frequency $f_{\rm S}$, output inductance L, and output capacitance C are the key circuit parameters for the transient performance, whereas the setting time and overshoot /undershoot voltage are the important indicators of the transient performance [44], [45]. Therefore, the converter possesses nice transient performance when high switching frequency, small output inductance, or large output capacitance is utilized. Under the same load current step, the short recovery time and small overshoot/undershoot voltage indicate that the converter has high indicators of the transient performance. In brief, the larger the FOM value is, the better the transient performance of the converter is under a specific control scheme.

It should be noticed that among these control schemes in Table VI, the transient performance of the PVR control in this article is not optimal, but the PVR control circuit is the simplest. Thus, using the PVR control is especially convenient to study the feedforward current effect of load converter on the stability of source converter in the cascaded converter.

V. DISCUSSIONS OF THE OTHER THREE CASES

In order to illustrate the generality of the stability effect of the load converter on the source converter, the other three cases are discussed in this section.

A. Load Converter With High Switching Frequency

In many applications (e.g., the power system of computer), to achieve small output voltage ripple and fast transient response, the load converter typically operates at higher switching frequency than the source converter [47]. Here, two cases ($f_{\rm S2} = 2f_{\rm S1}$ and $f_{\rm S2} = 4f_{\rm S1}$) are considered to show the stability effects of load converter with high switching frequency on the source converter. With the circuit parameters listed in Table II, the bifurcation diagrams of inductor current i_{L1} with respect to $V_{\rm ref1}$ for $f_{\rm S2} = 2f_{\rm S1}$ and $f_{\rm S2} = 4f_{\rm S1}$ are shown in Fig. 13(a) and (b).

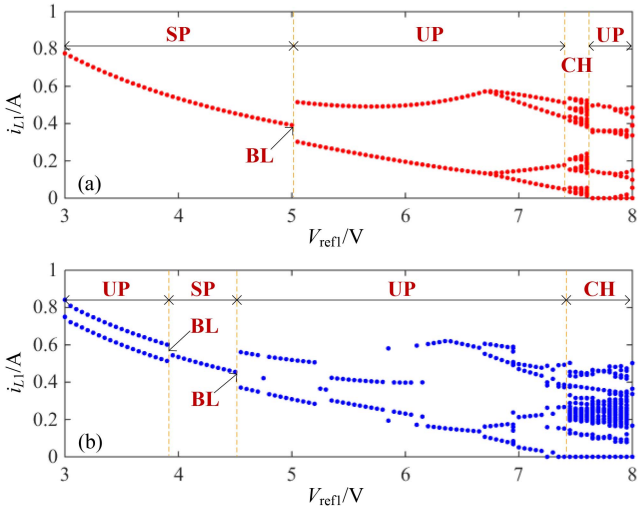

Fig. 13. Bifurcation diagrams of the inductor current i_{L1} with respect to reference voltage $V_{\rm ref1}$ when the load converter with higher switching frequency than that of the source converter. (a) $f_{\rm S2} = 200$ kHz. (b) $f_{\rm S2} = 400$ kHz.

As shown in Fig. 13(a), increasing $V_{\rm ref1}$ from 3 to 8 V, the motion orbit of the source converter mutates from period-1 to unstable period-N ($N \geq 2$) at $V_{\rm ref1} = 5.05$ V, then to chaos at $V_{\rm ref1} = 7.45$ V, and finally to unstable period-N ($N \geq 2$) at $V_{\rm ref1} = 7.6$ V. Similarly, as shown in Fig. 13(b), increasing $V_{\rm ref1}$ from 3 to 8 V, the motion orbit of the source converter mutates from unstable period-2 to period-1 at $V_{\rm ref1} = 3.9$ V, then to unstable period-N ($N \geq 2$) at $V_{\rm ref1} = 4.55$ V, and finally to chaos at $V_{\rm ref1} = 7.45$ V. Note that these state transitions are all caused by the border-collision bifurcation.

From the result in Fig. 13 and the stability condition in (2), it can be concluded that when the source and load converters have different switching frequencies, the stability of the source converter is also affected by the feedforward current ripple of the load converter. Compared Fig. 13 with Fig. 9(a), the stability

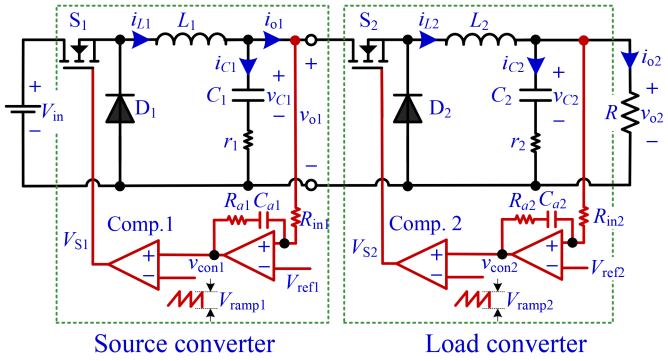

Fig. 14. Cascaded power converter comprising two PI controlled buck converters.

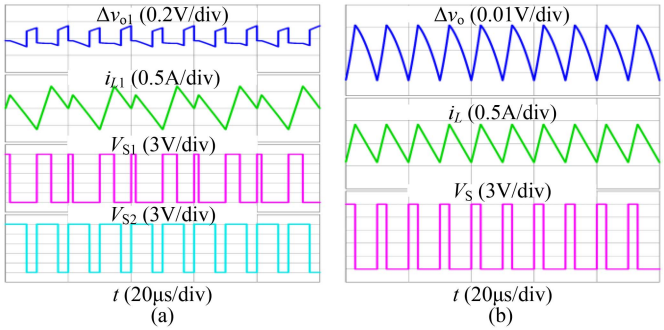

Fig. 15. PSIM simulation waveforms of the PI controlled buck converter. (a) In the cascaded operation. (b) In the standalone operation.

effect of the load converter is affected by the switching frequency relationship between the source converter and load converter. Besides, the case can be further discussed [47] if the ratio of the switching frequency of the load converter to that of the source converter is an arbitrary integer. Otherwise, the source converter is unable to operate in the normal period-1 state, and even has the beat frequency oscillation [33]. Thus, the stability of the cascaded converter needs to be redefined [22].

B. Source Converter With Other Control

To explore the stability effects of the load converter on the source converter with other control techniques, the source converter with PI control is considered. A cascaded power converter comprising two PI controlled buck converters is shown in Fig. 14, where $g_i = R_{ai}/R_{\mathrm{in}i}$ and $\tau_i = R_{ai}C_{ai}$ are the feedback gain and time constant of the PI controller, respectively. Correspondingly, the circuit parameters are set as $V_{\mathrm{in}} = 12$ V, $L_1 = L_2 = 30\,\mu$H, $C_1 = C_2 = 220\,\mu$F, $r_1 = r_2 = 30\,\mathrm{m}\Omega$, $R = 0.4\,\Omega$, $V_{\mathrm{ramp1}} = V_{\mathrm{ramp2}} = 2$ V, $R_{\mathrm{in1}} = R_{\mathrm{in2}} = 2\,\mathrm{k}\Omega$, $R_{a1} = R_{a2} = 40\,\mathrm{k}\Omega$, $C_{a1} = C_{a2} = 10$ nF, $f_{\mathrm{S1}} = f_{\mathrm{S2}} = 100$ kHz, $V_{\mathrm{ref1}} = 3.6$, and $V_{\mathrm{ref2}} = 2.4$ V. With these circuit parameters, the simulation waveforms of Δv_{o1}, i_{L1}, V_{S1}, and V_{S2} are shown in Fig. 15(a), respectively. As a contrast, the simulation waveforms of Δv_{o}, i_L, and V_{S} for the PI controlled buck converter in the standalone operation are shown in Fig. 15(b). Note that the circuit parameters are the same in Fig. 15(a) and (b), except that the load resistance R is set to 0.9 Ω to maintain the same output power. Meanwhile, to avoid

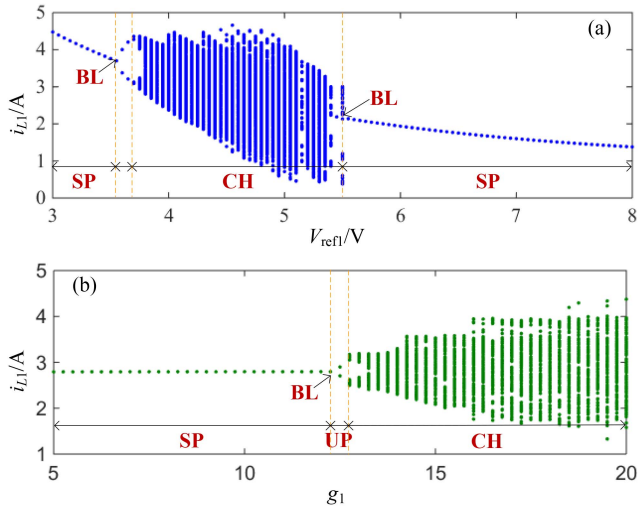

Fig. 16. Bifurcation diagrams of the inductor current i_{L1}. (a) With respect to V_{ref1}. (b) With respect to g_1.

the high-frequency oscillation caused by the slope of the control signal approaching that of the ramp, an RS trigger is connected at the output terminal of the comparator in the simulation circuit. From Fig. 15(a) and (b), the PI controlled buck converter feeding resistive load is stable, but feeding the load converter is unstable.

Furthermore, when V_{ref1} increases from 3 to 8 V, the bifurcation diagram of the inductor current i_{L1} with respect to V_{ref1} is depicted in Fig. 16(a). It can be observed that the motion orbit of the source converter alters from period-1 to period-2 at $V_{\mathrm{ref1}} = 3.55$ V via period-doubling bifurcation, to chaos at $V_{\mathrm{ref1}} = 3.7$ V and ultimately back to period-1 at $V_{\mathrm{ref1}} = 5.5$ V all via border-collision bifurcations. However, when V_{ref1} increases from 3 to 8 V, the PI controlled buck converter in the standalone operation always operates in the stable period-1 state. It indicates that the stability of the source converter with the PI control is also affected by the feedforward ripple of the load converter.

Besides, the stability effect of the feedback gain of the PI compensator on the source converter is also considered. With $V_{\mathrm{ref1}} = 4$ V and the other circuit parameters used in Fig. 16(a), the bifurcation diagram of the inductor current i_{L1} with respect to g_1 is depicted in Fig. 16(b). With g_1 increasing, the motion orbit of the source converter alters from period-1 to period-2 at $g_1 = 12.25$ and to chaos at $g_1 = 12.75$ all via period-doubling bifurcations. It means that the stability effect of the load converter is related to the feedback gain of the source converter. In other words, with the decrease of g_1, the stability effect of the load converter is weakened. Note that when g_1 changes from 5 to 20, the source converter with resistive load is always in the stable state.

To demonstrate the limitations of the impedance-based stability criteria in predicting the stability associated with the switching ripple, the impedance-based stability analysis is carried out for the cascaded power converter comprising two PI controlled buck converters. The closed-loop output impedances of the source converter (without load R) $Z_{\mathrm{oc\_S}}(s)$ and the input impedance of the load converter (with load R) $Z_{\mathrm{inc\_L}}(s)$ are

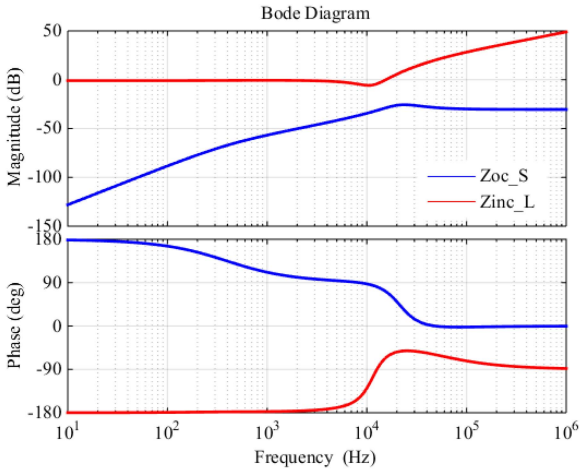

Fig. 17. Bode diagrams of $Z_{\text{oc\_S}}(s)$ and $Z_{\text{inc\_L}}(s)$ of the cascaded power converter comprising two PI controlled buck converters.

written by referring to Li et al. [31] as

$$Z_{\text{oc\_S}}(s) = \frac{Z_{\text{oo\_S}}(s)}{1 + T_1(s)} \tag{18}$$

$$Z_{\text{inc\_L}}(s) = \frac{1}{\frac{1}{Z_{\text{ino\_L}}(s)}\frac{1}{1+T_2(s)} - \frac{D_2^2}{R}\frac{T_2(s)}{1+T_2(s)}} \tag{19}$$

where $Z_{\text{oo\_S}}(s)$ and $T_1(s)$ are the open-loop output impedance and loop gain of the source converter, respectively, $Z_{\text{ino\_L}}(s)$ and $T_2(s)$ are the open-loop input impedance and loop gain of the load converter, respectively.

The expressions of $Z_{\text{oo\_S}}(s)$, $Z_{\text{ino\_L}}(s)$, and $T_i(s)$ $(i = 1, 2)$ can be derived by referring to Li et al. [31] as

$$Z_{\text{oo\_S}}(s) = \frac{s^2 L_1 r_1 C_1 + sL_1}{s^2 L_1 C_1 + s r_1 C_1 + 1} \tag{20}$$

$$Z_{\text{ino\_L}}(s) = \frac{R}{D_2^2}\frac{s^2 L_2 C_2 + s(r_2 C_2 + L_2/R) + 1}{sRC_2 + 1} \tag{21}$$

$$T_i(s) = G_{\text{vd}i} G_{\text{c}i} G_{\text{m}i} H_i \tag{22}$$

where

$$G_{\text{vd}i} = \frac{V_{\text{in}i}(s r_i C_i + 1)}{(s^2 L_i C_i + s r_i C_i + 1) + sL_i(s r_i C_i + 1)/R}$$

$$G_{ci} = g_i\left(1 + \frac{1}{s\tau_i}\right),\ G_{\text{m}i} = \frac{1}{V_{\text{ramp}i}},\ H_i = 1.$$

Note that $V_{\text{in1}} = V_{\text{in}}$ and $R \to \infty$ for $G_{\text{vd1}}(s)$, and $V_{\text{in2}} = V_{\text{ref1}}$ for $G_{\text{vd2}}(s)$.

Based on (18)–(22) and the circuit parameters used in Fig. 15(a), the Bode diagrams of $Z_{\text{oc\_S}}(s)$ and $Z_{\text{inc\_L}}(s)$ are plotted in Fig. 17, respectively. In Fig. 17, $Z_{\text{oc\_S}}(s)$ does not intersect $Z_{\text{inc\_L}}(s)$ over the entire frequency range, indicating that the cascaded power converter comprising two PI controlled buck converters should be stable [9]. However, the converter is actually unstable, as shown in Fig. 15(a). Therefore, it can be concluded that the impedance-based stability criteria fail to predict the stability related to the switching ripple in the cascaded power converter.

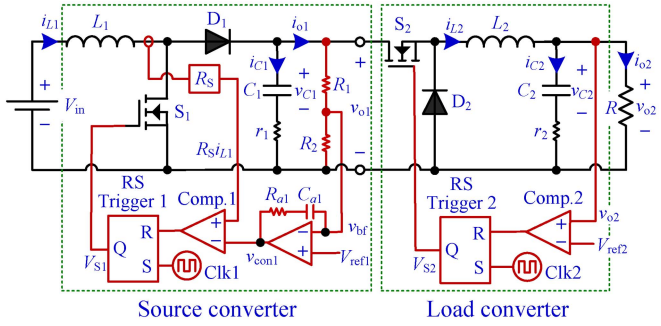

Fig. 18. PCM controlled boost converter loaded by the PVR controlled buck converter.

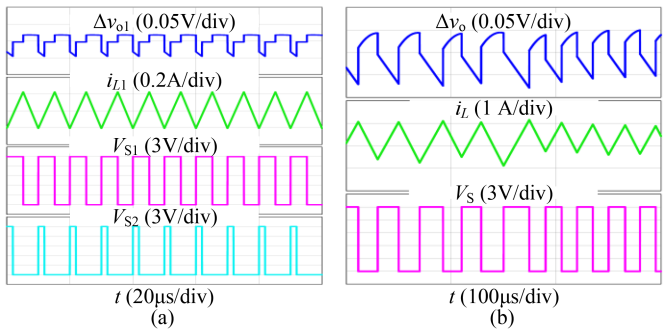

Fig. 19. PSIM simulation waveforms of the PCM controlled boost converter. (a) In the cascaded operation. (b) In the standalone operation.

C. Source Converter With Other Topologies

In order to explore the stability effects of the load converter on the source converter with other topologies, the cascade of boost converter and buck converter is considered and shown in Fig. 18. The boost converter uses peak-current-mode (PCM) control, the buck converter uses PVR control, and the outer voltage loop of PCM control uses PI compensator with $g = R_{a1}/R_2$ and $\tau = R_{a1}C_{a1}$. The circuit parameters for the cascaded converter in Fig. 18 are chosen as $V_{\text{in}} = 5$ V, $L_1 = L_2 = 60$ μH, $C_1 = C_2 = 470$ μF, $r_1 = r_2 = 20$ mΩ, $R = 1$ Ω, $R_1 = R_2 = 2$ kΩ, $R_{a1} = 20$ kΩ, $C_{a1} = 50$ nF, $f_{\text{S1}} = f_{\text{S2}} = 100$ kHz, $V_{\text{ref1}} = 5.2$ V, and $V_{\text{ref2}} = 2$ V. With the chosen circuit parameters, the simulation waveforms of Δv_{o1}, i_{L1}, V_{S1}, and V_{S2} are shown in Fig. 19(a), respectively. As a contrast, the simulation waveforms of Δv_{o}, i_L, and V_{S} for the PCM controlled boost converter feeding resistive load are shown in Fig. 19(b). Similarly, the circuit parameters are the same in Fig. 19(a) and (b), except that the load resistance R is set to 6.76 Ω to maintain the same output power. From Fig. 19(a) and (b), the PCM controlled boost converter feeding resistive load (in standalone operation) is unstable, but feeding the converter (in cascaded operation) is stable.

Furthermore, when V_{ref1} increases from 3 to 7 V, the bifurcation diagram of the inductor current i_{L1} with respect to V_{ref1} is depicted in Fig. 20(a). It is noted that according to the circuit parameters of divider in Fig. 18, one has $v_{\text{bf}} = 0.5v_{\text{o1}}$. Therefore, with V_{ref1} varying from 3 to 7 V, v_{o1} varies from 6 to 14 V. Observed from Fig. 20(a), the motion orbit of the source converter alters from chaos to period-1 at $V_{\text{ref1}} = 3.45$

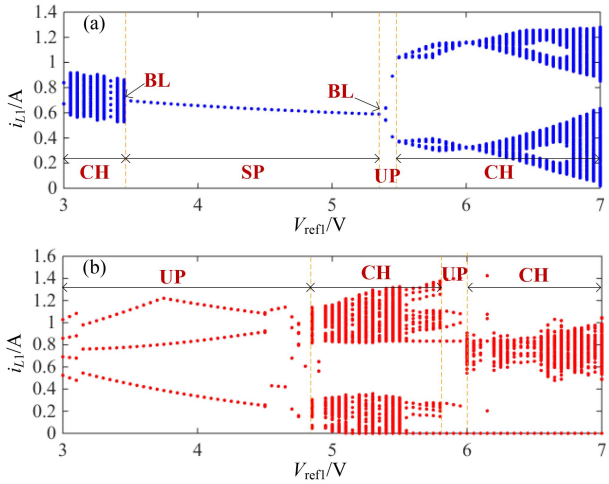

Fig. 20. Bifurcation diagram of the inductor current i_{L1} with respect to V_{ref1} in PCM controlled boost converter. (a) Loaded by PVR controlled buck converter. (b) Loaded by CPL.

V, to period-2 at $V_{\mathrm{ref1}} = 5.35$ V, and ultimately to chaos at $V_{\mathrm{ref1}} = 5.5$ V all via border-collision bifurcations. However, when V_{ref1} increases from 3 to 7 V, the PCM controlled boost converter feeding resistive load always operates in the unstable state. This demonstrates that the stability of the PCM controlled boost converter in the cascaded operation is indeed changed by the feedforward current ripple of the load converter, which is also different from that in the standalone operation.

As a comparison, the PVR controlled buck converter in Fig. 18 is replaced by CPL ($P = 4$ W, equal to the output power of the PVR controlled buck converter), and the corresponding bifurcation diagram is shown in Fig. 20(b). It is noted that the CPL used in Fig. 20(b) is an ideal one and is expressed as $i_{\mathrm{o1}} = P/v_{\mathrm{o1}}$ [20], where i_{o1} is the current through the CPL and v_{o1} is the output voltage of the source converter. From the expression ($i_{\mathrm{o1}} = P/v_{\mathrm{o1}}$), the current ripple through CPL is caused by the output voltage ripple, which is fed forward to the source converter. However, the ripple is generally very small and different from the current ripple fed forward by the load converter. By comparing Fig. 20(a) and (b), simplifying the load converter to CPL cannot predict the stability effect of the feedforward ripple of the load converter on the source converter. Thus, the CPL tends to cause the converter to operate in the unstable state.

It is emphasized that all three cases discussed in this section can be investigated by establishing the discrete-time map model and deriving the corresponding Jacobi matrix. The analysis process can be referred to Sections III and IV.

VI. Experimental Verifications

To verify the stability effects of the key circuit parameters on the source converter, an experimental prototype is fabricated based on the schematic diagram shown in Fig. 3. The photograph of the experimental prototype is shown in Fig. 21, where IRF540 MOSFET switch, MBR2045CT diode, LM319 comparator, and MCP1407 driver are employed, and the RS trigger is implemented by the OR gate provided by 74HC02.

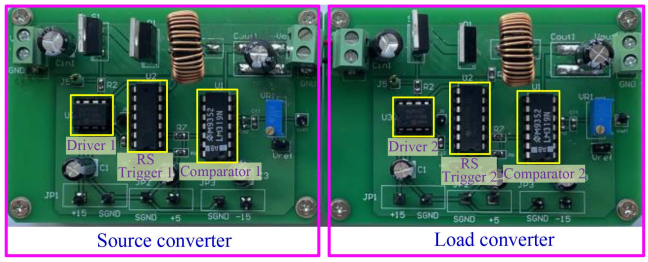

Fig. 21. Experimental prototype photograph of the cascaded power converter comprising two PVR controlled buck converters.

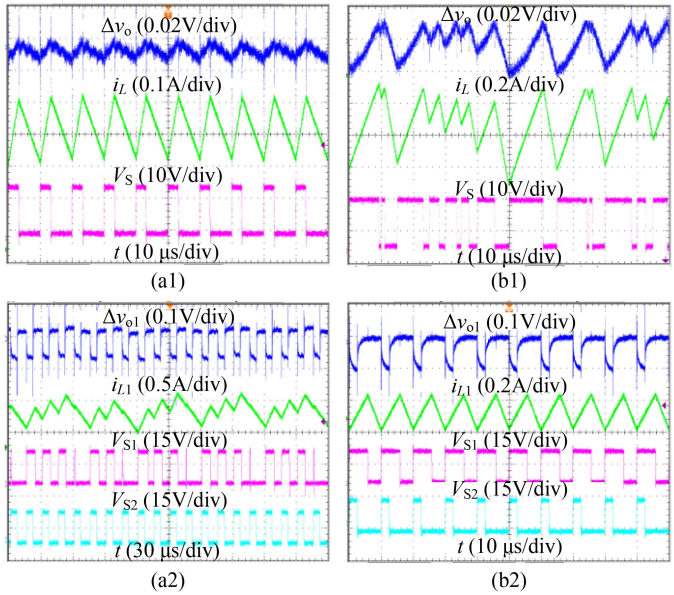

Fig. 22. Experimental waveforms for different reference voltages of V_{ref1}, where (a1) and (b1) stand for PVR controlled buck converter in the standalone operation, and (a2) and (b2) stand for PVR controlled buck converter in the cascaded operation. (a) $V_{\mathrm{ref1}} = 3$ V. (b) $V_{\mathrm{ref1}} = 7$ V.

With the circuit parameters used in Fig. 5, the corresponding experimental results are shown in Fig. 22. As shown in Fig. 22(a1) and (b1), the PVR controlled buck converter operates in the stable period-1 state when $V_{\mathrm{ref}} = 3$ V and in the unstable state when $V_{\mathrm{ref}} = 7$ V. On the contrary, as shown in Fig. 22(a2) and (b2), the source converter operates in the unstable state when $V_{\mathrm{ref1}} = 3$ V and in the stable period-1 when $V_{\mathrm{ref1}} = 7$ V.

Similarly, with the circuit parameters used in Figs. 6–8, the experimental results for different output capacitor ESRs of r_1, different inductances of L_1, and different load resistances of R are shown in Figs. 23 –25, respectively. The results illustrate that the source converter operates in the stable period-1 state when using small output capacitor ESR r_1 or large inductance L_1 or small load resistance R, otherwise it operates in the unstable period-2 state when using large output capacitor ESR r_1 or small inductance L_1 or large load resistance R.

Obviously, the experimental results are consistent with the PSIM circuit simulation results. Besides, the circuit parameters used in Fig. 22(a), Fig. 23(b), and Fig. 24(a) are all located in the unstable region in Fig. 12, whereas the circuit parameters used in Fig. 22(b), Fig. 23(a), and Fig. 24(b) are all located in

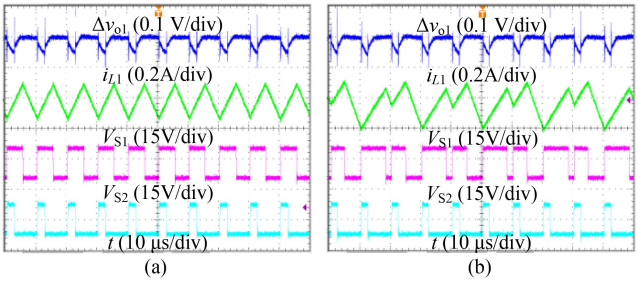

Fig. 23. Experimental waveforms for different values of the output capacitor ESR r_1. (a) $r_1 = 15$ mΩ. (b) $r_1 = 24$ mΩ.

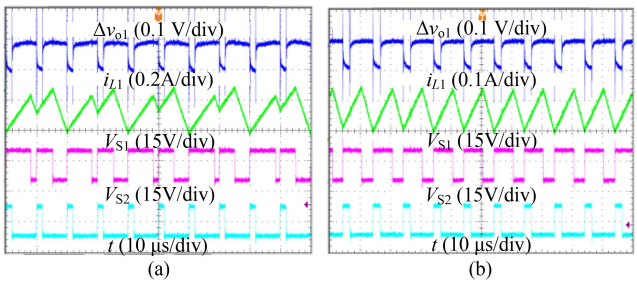

Fig. 24. Experimental waveforms for different inductances of L_1. (a) $L_1 = 195$ μH. (b) $L_1 = 210$ μH.

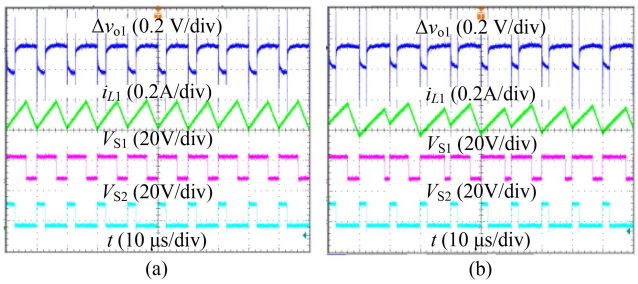

Fig. 25. Experimental waveforms for different load resistances of R. (a) $R = 0.2$ Ω. (b) $R = 0.25$ Ω.

the stable region in Fig. 12. In this way, the correctness of the stability analyses is verified.

Furthermore, to demonstrate the transient performance of the PVR controlled buck converter, the circuit parameters in Fig. 2(a) are chosen as $V_{\rm in} = 5$ V, $L = 2.2$ μH, $C = 50$ μF, $r = 40$ mΩ, $V_{\rm o} = 1.8$ V, and $f_{\rm S} = 1$ MHz. The experimental waveforms for the load step up ($I_{\rm o}$ changing from 480 to 910 mA) and load step down ($I_{\rm o}$ changing from 910 to 480 mA) are shown in Fig. 26(a) and (b), respectively.

As shown in Fig. 26(a), when the load current $I_{\rm o}$ changes from 480 to 910 mA, the settling time and undershoot voltage are 1.5 μs and 40 mV, respectively. As shown in Fig. 26(b), when $I_{\rm o}$ changes from 910 to 480 mA, the settling time and undershoot voltage are 3.2 μs and 45 mV, respectively. The experimental waveforms in Fig. 26 indicate that the PVR controlled buck converter has fast transient response.

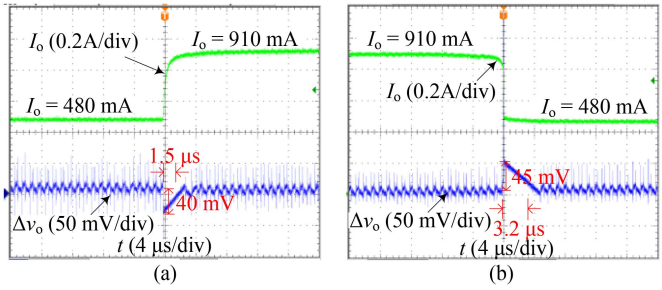

Fig. 26. Experimental waveforms for load step up/down. (a) $I_{\rm o}$: 480 mA → 910 mA. (b) $I_{\rm o}$: 910 mA → 480 mA.

VII. Conclusion

In this article, a cascaded power converter comprising two PVR controlled buck converters is taken as an example to fully investigate the stability effects of the load converter on the source converter. Under the feedforward current ripple of the load converter, the stability effects of the main circuit parameters in the source converter are completely different from those in the standalone operation. To investigate the stability effects theoretically, a discrete-time map model with three switching state sequences was established for the cascaded power converter and its Jacobi matrix at the invariant point was derived. With the Jacobi matrix, the eigenvalue analyses with the variation of the reference voltage, inductance, and output capacitor ESR were carried out, and the stability boundaries for dividing the stable region and unstable region in the circuit parameter planes were given thereafter. The results indicated that if the duty cycle of the load converter is greater than that of the source converter, the source converter is always in the unstable state; otherwise, it is in the stable state and its stable operation range is enlarged with the increase of the inductance or decrease of the output capacitor ESR and load resistance. Furthermore, other three cases, including the load converter with high switching frequency and the source converter with other control techniques and topologies, are discussed. It showed that the stability effect of the load converter is also related to the frequency relationship between the source converter and load converter, and the control techniques and topologies of the source converter. Finally, the experimental results verified the theoretical analyses and simulation results. These results in this article provide more accurate information for choosing circuit parameters, which can be used as an effective candidate to the existing impedance-based stability criterion.

Appendix

For the switching state sequence $Z_1 = (1, 2, 4)$, the elements of the Jacobi matrix can be written as

$$\partial f_1/\partial t_1 = \phi_4(\tau_4)\phi_2(\tau_2)\left(\mathbf{A}_1\mathbf{P}_1 + \mathbf{B}_1 - \mathbf{A}_2\mathbf{P}_1 - \mathbf{B}_2\right)$$

$$\partial f_1/\partial t_2 = \phi_4(\tau_4)\left(\mathbf{A}_2(\mathbf{P}_2 \circ \mathbf{P}_1) + \mathbf{B}_2 - \mathbf{A}_4(\mathbf{P}_2 \circ \mathbf{P}_1) - \mathbf{B}_4\right)$$

$$\partial s_1/\partial t_1 = \mathbf{K}_1\left(\mathbf{A}_1\mathbf{P}_1 + \mathbf{B}_1\right),\ \partial s_1/\partial t_2 = 0$$

$$\partial s_2/\partial t_1 = \mathbf{K}_2\phi_2(\tau_2)\left(\mathbf{A}_1\mathbf{P}_1 + \mathbf{B}_1 - \mathbf{A}_2\mathbf{P}_1 - \mathbf{B}_2\right)$$

$$\partial s_2/\partial t_2 = \mathbf{K}_2\left(\mathbf{A}_2(\mathbf{P}_2 \circ \mathbf{P}_1)+\mathbf{B}_2\right)$$

$$\partial s_1/\partial \mathbf{x}_n = \mathbf{K}_1\phi_1(\tau_1),\ \partial s_2/\partial \mathbf{x}_n = \mathbf{K}_2\phi_2(\tau_2)\phi_1(\tau_1)$$

where $\mathbf{P}_2 \circ \mathbf{P}_1 = \phi_2(\tau_2)\mathbf{P}_1+\psi_2(\tau_2)\mathbf{B}_2$.

For the switching state sequence $Z_2 = (1, 4)$, the elements of the Jacobi matrix can be written as

$$\partial f_2/\partial t_1 = \phi_4(\tau_4)\left(\mathbf{A}_1\mathbf{P}_1+\mathbf{B}_1 - \mathbf{A}_4\mathbf{P}_1 - \mathbf{B}_4\right),$$

$$\partial s_1/\partial t_1 = \mathbf{K}_3\left(\mathbf{A}_1\mathbf{P}_1+\mathbf{B}_1\right),\ \partial s_1/\partial \mathbf{x}_n = \mathbf{K}_3\phi_1(\tau_1).$$

For the switching state sequence $Z_3 = (1, 3, 4)$, the elements of the Jacobi matrix can be written as

$$\partial f_3/\partial t_1 = \phi_4(\tau_4)\phi_3(\tau_3)\left(\mathbf{A}_1\mathbf{P}_1+\mathbf{B}_1 - \mathbf{A}_3\mathbf{P}_1 - \mathbf{B}_3\right)$$

$$\partial f_3/\partial t_2 = \phi_4(\tau_4)\left(\mathbf{A}_3(\mathbf{P}_3 \circ \mathbf{P}_1)+\mathbf{B}_3 - \mathbf{A}_4(\mathbf{P}_3 \circ \mathbf{P}_1) - \mathbf{B}_4\right)$$

$$\partial s_1/\partial t_1 = \mathbf{K}_3\left(\mathbf{A}_1\mathbf{P}_1+\mathbf{B}_1\right),\ \partial s_1/\partial t_2 = 0$$

$$\partial s_2/\partial t_1 = \mathbf{K}_1\phi_3(\tau_3)\left(\mathbf{A}_1\mathbf{P}_1+\mathbf{B}_1 - \mathbf{A}_3\mathbf{P}_1 - \mathbf{B}_3\right)$$

$$\partial s_2/\partial t_2 = \mathbf{K}_1\left(\mathbf{A}_3(\mathbf{P}_3 \circ \mathbf{P}_1)+\mathbf{B}_3\right)$$

$$\partial s_1/\partial \mathbf{x}_n = \mathbf{K}_3\phi_1(\tau_1),\ \partial s_2/\partial \mathbf{x}_n = \mathbf{K}_1\phi_3(\tau_3)\phi_1(\tau_1)$$

where $\mathbf{P}_3 \circ \mathbf{P}_1 = \phi_3(\tau_3)\mathbf{P}_1+\psi_3(\tau_3)\mathbf{B}_3$.

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