Soft-Switched Integrated AC–DC Bidirectional Converter With Natural Grid Harmonic Elimination

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***Abstract*—Two-stage ac–dc converters have hard-switched ac–dc stage followed by soft-switched dc–dc stage. Since devices in the ac–dc stage are switched at low frequency (typically 10–20 kHz), bandwidth of current control loop of this stage is limited (typically less than 2 kHz). This low bandwidth current loop fails to reject current harmonic disturbances arising due to distorted grid voltages, thus necessitating multiple harmonic compensation loops or complex control algorithms for meeting IEEE Std 519-2014. Lack of soft-switching prohibits devices of the ac–dc stage from being switched at a frequency above 100 kHz and thereby attain a bandwidth of around 10 kHz for natural rejection of grid current harmonics. This article proposes an integrated three-phase bidirectional isolated ac–dc converter, where soft-switching operation is extended to devices in ac–dc stage as well. Thus, high bandwidth current loop can be achieved without reduction in efficiency. The proposed modulation scheme decouples ac–dc and dc–dc operations using XOR logic. An iterative procedure for design of resonant tank is provided. The integration also leads to 25% fewer devices. Experiments carried out on a 5-kW prototype demonstrate that a low current total harmonic distortion, complying with IEEE standard, can be achieved with good efficiency, even under distorted grid voltages.**

***Index Terms*—Bandwidth, bidirectional converter, current control, disturbance rejection, hard switching, harmonic distortion, resonant converter, soft switching.**

I. Introduction

With the advancements in wide bandgap semiconductor technology, power converters with silicon carbide (SiC) devices are employed in emerging applications such as the integration of energy storage to the grid [1]. There are stringent requirements imposed by IEEE standards for renewable energy and energy storage integration to grid [2]. Even with a specified total harmonic distortion (THD) in grid voltages, the grid currents drawn or injected by the power electronic converter have to meet individual harmonic limits as well as overall THD limit, as specified by these standards [3]. The harmonics present in the grid voltages worsen the quality of the grid currents, which otherwise have low THD [4].

Most of the existing converters follow a two-stage design approach [5], [6], [7]. Here, the first stage is a hard-switched ac–dc stage, which is switched at low frequency to avoid excessive switching losses. This is followed by a high frequency (HF) soft-switched dc–dc stage. Several methods [3], [8], [9], [10], [11], [12], [13] are proposed in the literature for improving the current control algorithm to reduce grid current THD in the presence of distorted grid voltages [3]. A popular technique is to separate the individual harmonic currents and attenuate each of them to zero through PI or resonant controllers [8], [9], [10]. But this method considerably increases the computational load, execution time, and memory usage of the processor, as the algorithm requires separate control loops for each harmonic current to be eliminated [3]. The state feedback approach proposed in [12] achieves reasonable attenuation of current harmonics. However, the complexity and computational burden is increased with the use of Kalman filter [3]. The state space approach detailed in [13] requires additional harmonic compensators for obtaining better THD. The control algorithm proposed in [3] employs an additional plant model and controller in the current control structure for better rejection of current harmonic disturbances. However, the attenuation thus obtained is not adequate to effectively eliminate eleventh and higher order grid harmonic currents.

In order to naturally reject the current harmonics due to distorted grid voltages, the bandwidth of the current loop of the ac–dc stage must be at least ten times the frequency of the highest harmonic current to be attenuated [4]. The current controller bandwidth is also chosen to be at most one-tenth of the switching frequency [4], [14]. This necessitates a switching frequency greater than 100 kHz for the ac–dc stage. It is shown experimentally in [15] and [16] that the efficiency of the ac–dc stage drops to below 95% with SiC MOSFETs hard-switched at 130 kHz. Assuming the efficiency of the bidirectional isolated soft-switched dc–dc stage to be 98%, the overall efficiency falls to around 93%.

There are various single-stage topologies available in the literature. In the existing single-stage ac–dc converters reported in literature [17], [18], there exists coupling between the ac–dc and dc–dc operations, i.e., the variation in duty cycle for the continuous conduction mode ac–dc operation affects the duty cycle of the dc–dc operation also. To prevent the variation in the duty cycle of dc–dc stage, most single-stage ac–dc converters have discontinuous conduction mode (DCM) ac–dc operation.

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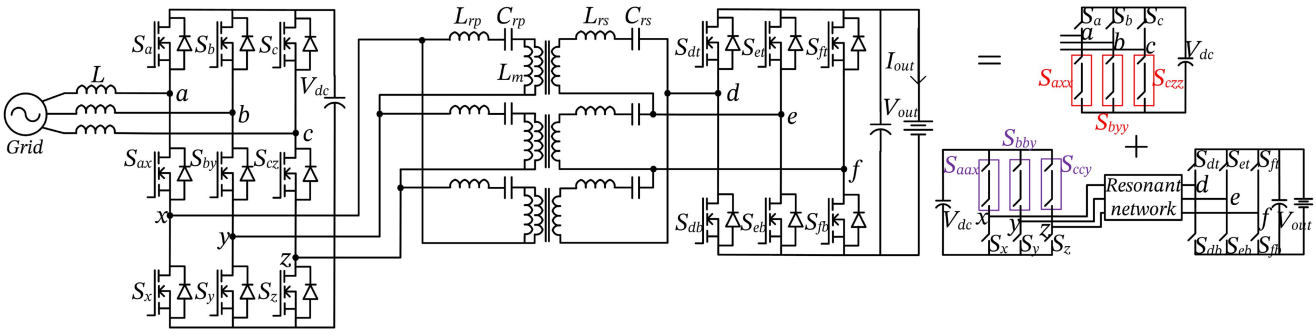


Fig. 1. Block diagram of the proposed soft-switched integrated ac–dc bidirectional converter and its decomposition into three-phase boost rectifier and three-phase full bridge dc–dc bidirectional resonant converter.

This prevents these converters from operating above a couple of kWs to avoid the disadvantages of high peak current arising from DCM operation. These converters suffer from increased device turn-OFFcurrent, design challenges, and EMI issues. Matrix converter based topologies proposed in [19], [20], and [21] require complex auxiliary stages to achieve a limited range of soft-switching. They also require large input filter, leading to poor power density.

The nine-switch topology proposed in [22], [23], [24], and [25] integrates the ac–dc and dc–dc stages, thereby facilitating soft-switched operation of the devices in the ac–dc stage as well. Therefore, the switching frequency of the ac–dc stage can be increased without resulting in high switching losses. However, the topology operates exactly at the resonant frequency and allows only unidirectional power flow. Since the intended applications are network servers and telecom devices [22], methods for realization of bidirectional power flow and soft-switching operation under nonunity power factors were not investigated.

The aforementioned issues are addressed in the proposed bidirectional converter, which operates above the series resonant frequency. Here, the ac–dc and dc–dc stages are integrated, which in turn facilitates soft-switched operation of devices in the ac–dc stage in addition to those of the dc–dc stage. Hence, the devices in the ac–dc stage can also be switched at higher frequency without a notable loss of efficiency. High bandwidth current and voltage control loops are thus feasible. With the proposed converter, the current harmonics due to distorted grid voltages are well attenuated by the high bandwidth current loop without any additional control techniques. Bidirectional power flow is enabled by a fully controlled three-phase bridge on the secondary side. Modulation and power transfer schemes for the converter are also proposed. The contributions of the article are summarized as follows.

1) A single-stage ac–dc bidirectional resonant converter is proposed along with the modulation scheme and control. The modulation scheme effectively decouples the ac–dc and dc–dc operations. The closed loop control and mechanism for bidirectional power transfer are also illustrated.
2) An iterative design procedure for the resonant tank considering nonunity power factor operation is presented.
3) The proposed modulation scheme generates bipolar HF voltages on the primary and secondary sides of the resonant tank. Thus, multiharmonic power transfer is performed, which in turn leads to higher efficiency.
4) All the devices in the proposed converter are soft-switched at 130 kHz. The bandwidths of the current and voltage control loops can be as high as 13 and 1.3 kHz, respectively. This high bandwidth current control loop can reject all current harmonic disturbances arising due to distorted grid voltages, without the need for any additional control techniques or hardware filters.

II. Proposed Soft-Switched Integrated AC–DC Bidirectional Converter

The topology, control, modulation, and power transfer schemes of the proposed bidirectional converter are described in this section.

A. Topology and Control

A block diagram of the proposed bidirectional converter is given in Fig. 1. The front-end comprises three legs with three devices in each of the legs. In addition to converting the ac grid voltages into dc voltage (V_{dc}), the converter also generates HF ac voltages at the drain terminals (x,y,z) of its bottom switches. These HF ac voltages are fed to the primary sides of three resonant networks, which are isolated from the output dc side (V_{out}) with HF transformers. The secondary side voltages are connected to a three-phase full bridge converter, which feeds power to a dc source (V_{out}). Thus, the ac (grid) to dc (V_{dc}) and dc (V_{dc}) to dc (V_{out}) stages are integrated, facilitating soft-switched operation of all the devices, unlike in existing two-stage converter. Hence, all devices can be switched at an HF of about 100 kHz, without incurring high switching losses, and also facilitating higher current control bandwidth. The device count is also reduced by 25%, as a result of the integration, compared to a two-stage converter.

The proposed converter facilitates bidirectional power transfer power from the ac grid to the dc output (V_{out}) and vice versa. While transferring power, the intermediate dc link voltage (V_{dc}) is maintained at the commanded value with dc-link voltage control algorithm [22] consisting of inner current control loops

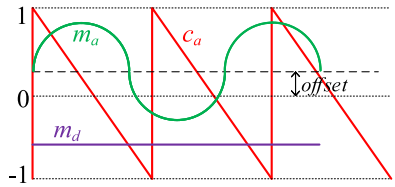
and an outer voltage loop. Since all the devices in the proposed converter are switched at an HF, high current controller bandwidth is achieved, which in turn results in the natural rejection of current harmonic disturbances, while operating with distorted grid voltages. In a two-stage ac–dc converter with SiC MOSFETs, switching the devices of the ac–dc stage leads to excessive switching losses, as these devices are not soft-switched. This is experimentally verified in [15] and [16], where it is shown that with increase in switching frequency of the hard-switched SiC MOSFETs from 20 to 130 kHz and above, the efficiency drops from 98% to below 95%. If an efficiency of 98% is assumed for the soft-switched dc–dc stage, the overall efficiency is 93% for the two-stage converter with all devices switched at 130 kHz. However, the proposed converter achieves an overall efficiency of 95.3% with all devices soft-switched at 130 kHz.

Three-phase modulating signals (m_a, m_b, m_c) are generated from the dc-link voltage control algorithm. These modulating signals are used for the generation of pulsewidth modulation (PWM) pulses for the top and middle switches of the three legs on the primary side of the converter, as will be explained in the following subsection. The commanded voltage is then developed across the dc-link. The specified power can now be transferred to the output dc voltage (V_{out}). For this, both the primary and secondary sides of the resonant tank are excited. The primary side is excited by switching the lower devices (S_x, S_y, S_z) at a constant duty cycle. This is achieved using a constant modulating signal m_d. Similarly, the bottom devices of the secondary side (S_{db}, S_{eb}, S_{fb}) are also switched at the same duty cycle. The top devices of the secondary side (S_{dt}, S_{et}, S_{ft}) are switched in a complementary fashion. In order to transfer power, a phase shift is introduced between the corresponding line-to-line voltages at the primary and secondary sides of the resonant stages, namely, v_{xy} and v_{de}; v_{yz} and v_{ef}; and v_{zx} and v_{fd}. A method to introduce phase-shift is explained in Section II-C.

B. Modulation Scheme and Decoupling of AC–DC and DC–DC Operations

As mentioned in Section I, in most of the existing single-stage ac–dc converters, the ac–dc and dc–dc operations are coupled, which enforces discontinuous conduction mode for ac–dc operation, restricting their power handling capability. This is overcome by the proposed nine-switch based converter, where the gating pulses for middle switches are generated using XOR logic to effectively decouple the ac–dc and dc–dc operations. The modulating signals generated from the dc-link voltage control algorithm are compared with a sawtooth carrier to generate gating pulses for the top switches (g_a, g_b, g_c). When m_a is greater than the carrier, S_a is turned ON. This switch is turned OFFwhen m_a is lower than the carrier. To generate gating pulses for the bottom devices (g_x, g_y, g_z), a constant modulating signal m_d is compared with the carrier. The switch S_x is turned ON when m_d is lower than the carrier and it is turned OFFwhen m_d is greater than the carrier.

The gating signals for the middle switches (g_{ax}, g_{by}, g_{cz}) are generated using XOR logic. All switches in a leg should not be off simultaneously. This can be avoided by ensuring that



g_a	g_x	g_a XOR g_x	g_{ax}
0	0	0	X
0	1	1	1
1	0	1	1
1	1	0	0

(b)

Fig. 2. (a) Proposed modulation scheme (frequency of carrier is reduced for illustration). (b) XOR logic for PWM pulse generation for middle switch (X-avoided state).

g_a	g_{ax} AND g_x
0	1
1	0

(a)

g_a AND g_{ax}	g_x
0	1
1	0

(b)

Fig. 3. Decoupled operation. (a) Gating signal of S_a and that of effective single switch (S_{axx}–S_{ax} and S_x) for ac–dc operation. (b) Gating signal of effective single switch (S_{aax}–S_a and S_{ax}) and that of S_x for dc–dc operation.

m_a, m_b, and m_c are always greater than m_d. Fig. 2(a) shows the two modulating signals, m_a and m_d, with m_a offset from m_d. It may be noted that the addition of an equal offset to the three-phase modulating signals does not cause any change in the phase voltages. All combinations of gating signals for the devices in the a-phase leg are shown in Fig. 2(b), where "x" represents the avoided state. Also, all switches in a leg should not be turned ON at the same instant. It can be seen from Fig. 2(b) that when S_a and S_x are ON, S_{ax} is OFF.

For better understanding, Fig. 1 also shows the decomposition of the proposed converter into a three-phase rectifier and a three-phase dc–dc bidirectional resonant converter. It can be inferred from Fig. 3(a) and (b) that XOR logic decouples ac–dc and dc–dc operations. For ac–dc operation, whenever S_a is OFF, both S_{ax} and S_x are ON [see Fig. 2(b)]. When S_a is ON, either S_{ax} or S_x is OFF[see Fig. 2(b)]. S_{ax} and S_x can be thought of as a single switch (S_{axx} in Fig. 1) with switch state given by AND operation of g_{ax} and g_x, as shown in Fig. 3(a). Similarly, Fig. 3(b) shows the switching state of S_x and that of the effective single switch (S_{aax} in Fig. 1), obtained by AND operation of g_a and g_{ax}, for dc–dc operation.

C. Power Transfer

Fig. 4(a) shows the PWM pulses for the switches in the a-phase leg, where the pulses for the top and bottom devices are generated by comparing modulating signals (m_a, m_b, m_c) and m_d with the carrier, and those for the middle switches are obtained using XOR logic. The desired phase shift ϕ is introduced between the line-to-line voltages of the primary and secondary sides of the resonant stages for a specified power transfer. This is realized by shifting the secondary side carrier $c_{a\phi}$ from the primary side carrier c_a by the same phase angle ϕ. Fig. 4(b) shows the phase angle ϕ to be lagging for ac–dc power flow. A reverse power flow is achieved with a leading phase angle. The switching logic for the top devices of the secondary side

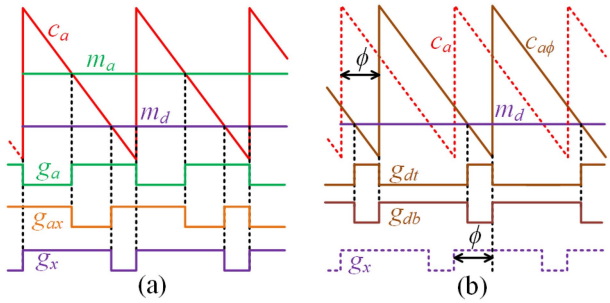


Fig. 4. PWM generation for (a) primary-side devices (b) and secondary-side devices; carrier of the secondary side $c_{a\phi}$ lagging carrier of primary side c_a by ϕ for power flow from ac to dc side.

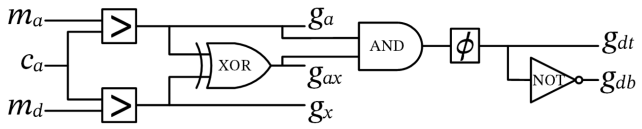


Fig. 5. Illustration of generation of PWM pulses for devices in the a-phase leg on the primary and secondary sides of the proposed converter using logic gates.

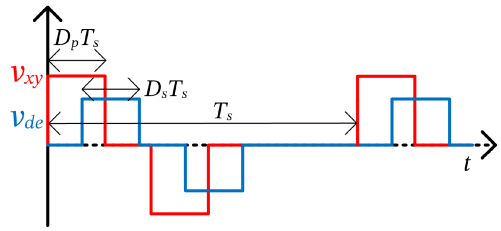


Fig. 6. Primary and secondary side voltages, v_{xy} and v_{de}, applied across the resonant network.

(S_{dt}, S_{et}, S_{ft}) is the inverse of that followed for the bottom devices of the primary side (S_x, S_y, S_z) [see Fig. 4(a)]. The PWM signals for the a-phase top and bottom switches of the secondary side, g_{dt} and g_{db}, are given in Fig. 4(b). It can be seen that the secondary side PWM signal g_{db} lags that of the primary side g_x by ϕ. An illustration of generation of PWM pulses for devices in the a-phase leg on the primary and secondary sides of the proposed converter using logic gates is presented in Fig. 5.

III. Design of Resonant Network

Design of the resonant tank and nonunity power factor operation are discussed in this section.

A. Iterative Design Procedure

The primary and secondary side voltages, v_{xy} and v_{de}, obtained following the modulation scheme explained in Section II-B are given in Fig. 6. Similar phase shifted voltages are applied to the resonant network in b- and c-phases as well. A simplified circuit diagram for the design of resonant elements is shown in Fig. 7. All the resonant elements are defined in Table I. X_p is the net impedance of the inductance and capacitance on the primary side. Similarly, the net impedance of those on the

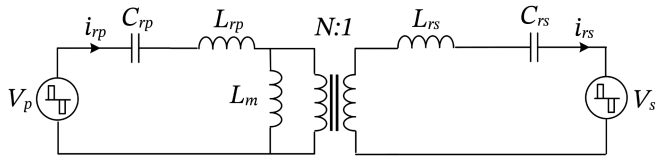


Fig. 7. Circuit for design of components of resonant network.

TABLE I
Specifications of the Proposed Converter

Parameters	Specifications
Power rating	5 kW
Switching frequency, f_{sw}	130 kHz
Input ac voltage (V_{ac}, L-L)	208 V, 60 Hz
DC-link voltage (V_{dc})	500 V
Output dc voltage (V_{out})	300–400 V
HF transformer turns ratio ($N = N_p : N_s$)	38:28
Input ac PFC inductances (L_a, L_b, L_c)	800 μH
HF transformer magnetizing inductance (L_m)	170 μH
DC-Link capacitance (C_{dc})	300 μF
Primary side resonant inductance (L_{rp})	50 μH
Secondary side resonant inductance (L_{rs})	21 μH
Primary side resonant capacitance (C_{rp})	47 nF
Secondary side resonant capacitance (C_{rs})	110 nF
Output dc capacitances (C_o)	150 μF

secondary side is referred to the primary side and is represented as X_s. X_m is the magnetizing impedance. The harmonics of the bridge voltages, V_p and V_s, on the primary and secondary sides of the resonant circuit are given below, where D_p and D_s are the respective duty cycles, and h is the order of the switching frequency harmonics present in the HF bipolar voltages and currents in the resonant tank ($h = 1, 2, 3, \ldots$). Fourier analysis of V_p yields the individual harmonic components as given by the following equation:

$$V_{\text{ph}} = V_{\text{dc}}\Big[j\sin(2\pi hD_p) - \sin\{2\pi h(D_p + \frac{1}{3})\} + \sin\frac{2\pi h}{3} + 1 - \cos(2\pi hD_p) + \cos\{2\pi h(D_p + \frac{1}{3})\} - \cos\frac{2\pi h}{3}\Big] / \sqrt{2}\pi h. \quad (1)$$

Similarly, harmonic components of V_s without phase shift can be calculated as shown in the following equation:

$$V_{\text{sh}}{}' = V_{\text{out}}\Big[j\sin(2\pi hD_s) - \sin\{2\pi h(D_s + \frac{1}{3})\} + \sin\frac{2\pi h}{3} + 1 - \cos(2\pi hD_s) + \cos\{2\pi h(D_s + \frac{1}{3})\} - \cos\frac{2\pi h}{3}\Big] / \sqrt{2}\pi h. \quad (2)$$

Since V_s is phase shifted from V_p by ϕ, the individual harmonic components can be calculated as given in the following equation:

$$V_{sh} = V_{sh}{}'e^{h\gamma}, \qquad \gamma = \lambda + \phi, \qquad \lambda = \angle V_{p1} - \angle V_{s1}{}'. \quad (3)$$

Using KCL for the circuit in Fig. 7, the node voltage V_{xh} can be obtained as shown in the following equation:

$$V_{xh} = \left[\frac{V_{ph}}{X_{ph}} + \frac{V_{sh}}{X_{sh}}\right]\left[\frac{X_{mh}X_{ph}X_{sh}}{X_{mh}X_{ph} + X_{mh}X_{sh} + X_{ph}X_{sh}}\right]. \tag{4}$$

The primary and secondary side resonant harmonic currents can be calculated as given by the following equation:

$$I_{rph} = \frac{V_{ph} - V_{xh}}{jX_{ph}}, \qquad I_{rsh} = \frac{V_{xh} - V_{sh}}{jX_{sh}}. \tag{5}$$

The currents at the turn-ON and turn-OFF instants, I_{on} and I_{off}, are calculated using grid currents and primary and secondary side resonant currents. Zero voltage turn-ON occurs when the body diode conducts before the MOSFET turns ON. Hence, for zero voltage turn-ON of devices, I_{on} should be less than zero. Also, for negligible turn-OFFloss, I_{off} should be less than I_{zvs} [26], given as follows:

$$I_{\text{zvs}} = \frac{V_o}{2L_s}(-R_g C_{\text{gd}} + \sqrt{(R_g C_{\text{gd}}^2) - 8(V_g - V_{\text{th}})\frac{L_s(C_{\text{gd}} + C_{\text{ds}})}{Vo}}). \tag{6}$$

Here, R_g, L_s, C_{gd}, and C_{ds} are the gate resistance, source inductance, gate–drain capacitance, and drain–source capacitance, respectively. The voltage V_o is equal to V_{dc} for primary side devices and V_{out} for secondary side devices; V_g is the gate drive voltage during turn-OFFand V_{th} is the MOSFET threshold voltage. Thus, the two conditions specified in (7) have to be satisfied for design of the resonant components

$$I_{\text{on}} < 0, \qquad I_{\text{off}} < I_{\text{zvs}}. \tag{7}$$

A switching frequency of 130 kHz is selected from the bode magnitude plots in Fig. 13. With this choice, the current controller bandwidth can be theoretically as high as 13 kHz, which in turn provides good disturbance rejection while operating with distorted grid voltages. Also, since this switching frequency is greater than the resonant frequency, soft-switching operation can be achieved. The series resonant frequency, turns ratio, primary and secondary side duty cycles, dc-link voltage, and output voltage are tabulated in Table I. An iterative solution of (1)–(7) introduced in this section along with the zero voltage switching (ZVS) condition imposed on resonant tank current when operated at the extremes of the leading and lagging power factor and peak volt-ampere (VA) of the converter (explained in the next subsection) is performed to find the resonant tank parameters. Initial values of L_m and L_{rp} are assumed to be 10 and 1 μH, respectively. These values are incremented in steps of 0.5 and 0.1 μH, respectively. The value of C_{rp} is calculated using the series resonant frequency and L_{rp}. At each iteration, I_{on} and I_{off} are calculated. If all the ZVS conditions are satisfied, the values of the resonant parameters are chosen.

B. Operation Under Nonunity Power Factor

In soft-switched converters with ZVS, the losses in semiconductors are mostly from conduction and hence dependent on their root mean square (rms) currents. The semiconductor losses should remain fairly uniform while operated at the rated VAs with varying power factor to facilitate a uniform thermal design for all operation conditions. This implies that, as the power factor degrades, the magnitude of active power decreases and reactive power increases, keeping the rms current in the devices for ac–dc operation fairly unchanged and hence their thermal stress. The rms current through a device is dependent on the input ac current and resonant current, corresponding to that leg of the converter.

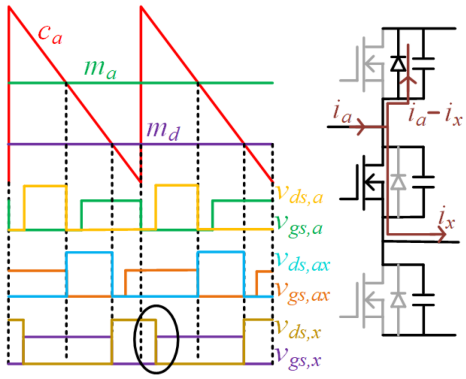


Fig. 8. Hard turn-ON of S_x as $i_{a,pk} > i_{x,pk}$.

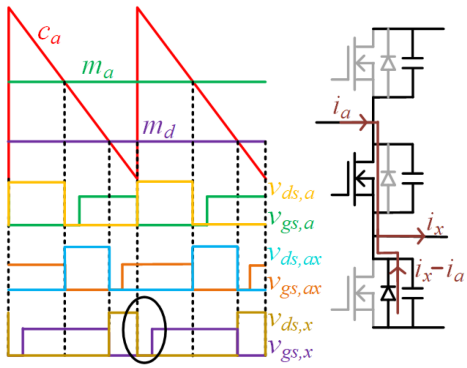


Fig. 9. Zero voltage turn-ON of S_x as $i_{a,pk} < i_{x,pk}$.

The top switch achieves ZVS only for positive half cycle of line current, as in a three-phase boost rectifier. The condition to be satisfied for the middle and bottom switches to achieve ZVS turn-ON over the entire line cycle are explained using Figs. 8 and 9, which show the gate–source voltage v_{gs} and drain–source voltage v_{ds} of devices in the a-phase leg, for two switching cycles. The adjacent circuit show the path of current flow. Fig. 8 shows that when the peak of phase current $i_{a,pk}$ is greater than that of the resonant tank current $i_{x,pk}$, the difference current $i_a - i_x$ flows through the body diode of the top switch. Thus, the output capacitance of the bottom switch is charged to V_{dc}, causing a hard turn-ON of the bottom switch. However, if $i_{a,pk} < i_{x,pk}$, then current $i_x - i_a$ flows through the body diode of the bottom switch itself, after discharging its output capacitance. The bottom switch, thus, achieves ZVS turn-ON as shown in Fig. 9. It can be shown in a similar way that the same condition, given by (8), has to be satisfied for achieving ZVS turn-ON over the entire line cycle, for the middle switch as well

$$i_{a,pk} < i_{x,pk}. \tag{8}$$

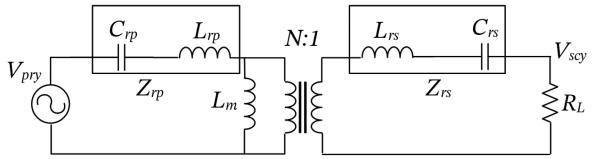


Fig. 10. Equivalent circuit for plotting voltage gain versus frequency curves for different loads.

The resonant tank current, i_{rp} (or i_x), can be calculated using I_{rph} [see (5)], as shown in the following equation:

$$i_{rp} = \sum_{h=1}^{n} \sqrt{2}\left[\mathrm{Re}(I_{rph})\sin(h\theta) + \mathrm{Im}(I_{rph})\cos(h\theta)\right]. \quad (9)$$

The resonant tank currents during transition should comply with the above-discussed ZVS condition when the converter is operated at rated VA and least magnitude of power factor. This is because the resonant tank current at the de-rated real power at those extremes of input power factor should still be able to meet the ZVS condition by overcoming the boost inductor current as mentioned above.

The apparent power S_h is given by the following equation:

$$S_h = V_{ph} I^*_{rph}. \quad (10)$$

Substituting expression for I_{rph} in (10) and equating the real part on both sides yield active power P_h as given in the following equation:

$$P_h = \frac{V_{ph} V_{sh} \sin\phi_h}{(X_{ph} + X_{sh} + \frac{X_{ph} X_{sh}}{X_m h})}. \quad (11)$$

The total output power P_T is given by the following equation:

$$P_T = \sum P_h. \quad (12)$$

Similarly, the reactive power can be derived by equating the imaginary parts on both sides of (10).

C. Voltage Gain

The voltage gain versus frequency curves for different loads are plotted using the equivalent circuit shown in Fig. 10. Here, Z_{rp} and Z_{rs} are the combined impedances of the inductance and capacitance on the primary and secondary sides, respectively. The effective load seen at the secondary output is denoted as R_L. The applied primary voltage is V_{pry} and the voltage developed across R_L is V_{scy}, as shown in Fig. 10. Both V_{pry} and V_{scy} are sinusoidal voltages at switching frequency. The voltage gain equation derived using phasor analysis is shown in the following equation:

$$\frac{V_{\text{scy}}}{V_{\text{pry}}} = \frac{[Z_m||(Z'_{rs} + R'_L)]R'_L}{(Z_{rp} + [Z_m||(Z'_{rs} + R'_L)])(Z'_{rs} + R'_L)N}. \quad (13)$$

The designed values of the resonant tank elements of the proposed converter are tabulated in Table I. The plot of the voltage gain versus frequency for different loads (R_L) is presented in Fig. 11. At the series resonant frequency (104 kHz), the gain is equal to the inverse of the turns ratio of the transformer. The operating switching frequency is 130 kHz, which is above the series resonant frequency.

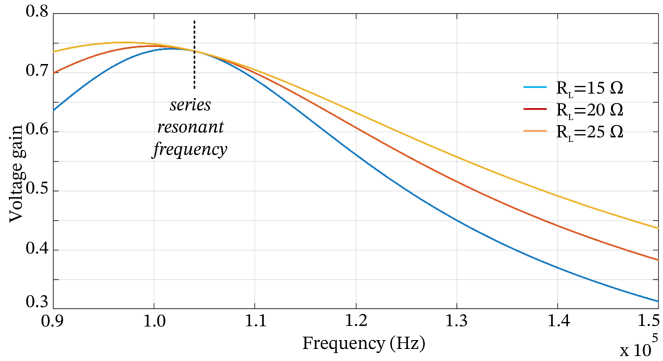


Fig. 11. Voltage gain versus frequency curves for different loads.

IV. Disturbance Rejection of Current Loop

The overall control algorithm is shown in Fig. 12(a). This involves dc-link voltage control [22] for maintaining the commanded dc-link voltage and generation of required phase angle for the desired power flow. The dc-link voltage control algorithm for the proposed converter has an outer voltage loop and inner d- and q-axes current control loops [22]. Here, ω_g and θ_{pll} are the frequency and angle of the grid voltage vector, obtained using phase locked loop (PLL). The dc-link voltage control algorithm generates the three-phase modulating signals (m_a, m_b, m_c). The constant modulating signal m_d is an user input, which is chosen such that the ZVS turn-ON of the bottom devices of the nine-switch bridge can be achieved [24]. Design of the voltage and current controllers is explained in detail in [27]. The phase angle ϕ is generated at the output of a controller, as also presented in Fig. 12(a). The reference output dc current $I_{\text{out}}{}^*$ can be calculated from the desired power command and output voltage V_{out}. The actual output current I_{out} is sensed and fed back. The error between the reference and actual output currents is fed to the controller. The controller generates the required phase angle for the desired power flow.

A block diagram of d-axis current control loop is given in Fig. 12(b), where i_{dh} is the current harmonic disturbance. The plant of current loop $G_i(s)$ and PI controller $G_{ci}(s)$ are given in (14), where R and L are the resistance and inductance of the inductor

$$G_i(s) = \frac{1/R}{1 + sL/R}, \quad G_{ci}(s) = k_{ci}\frac{1 + s/z_{ci}}{s}. \quad (14)$$

For a simplified design, the controller zero z_{ci} can be chosen to cancel the plant pole (R/L), resulting in a phase margin of 90°. The controller gain k_{ci} can be calculated for the desired bandwidth ω_{gci}. The current controller parameters are given by the following equation:

$$z_{ci} = R/L, \quad k_{ci} = R\omega_{gci}. \quad (15)$$

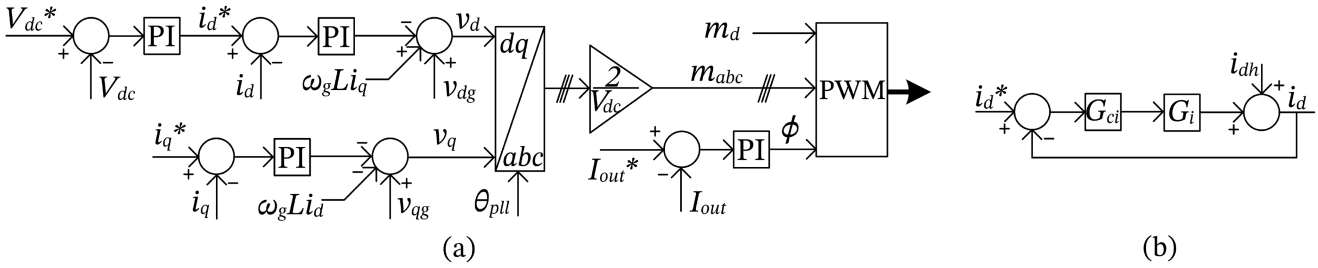


Fig. 12. (a) Overall control algorithm: dc-link voltage control with an outer voltage control and inner current control ($m_{abc} = \{m_a, m_b, m_c\}$), along with phase angle generation for the desired power flow. (b) Block diagram of current loop with disturbance i_{dh}.

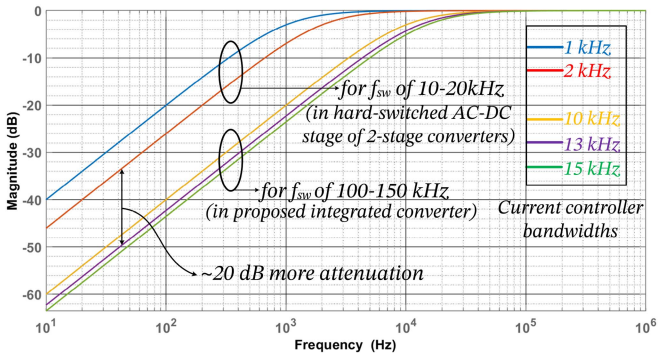


Fig. 13. Bode magnitude plots of disturbance rejection transfer function $D_i(s)$ of current control loop with different bandwidths (f_{sw} is switching frequency).

Using (15), the disturbance rejection transfer function $D_i(s)$ [14] can be derived as shown in the following equation:

$$D_i(s) = \frac{i_d}{i_{dh}} = \frac{s}{s + \omega_{gci}}. \tag{16}$$

The bode magnitude plots of $D_i(s)$ for different current controller bandwidths are shown in Fig 13. The bandwidth ω_{gci} is chosen to be one-tenth of switching frequency [4]. The devices in the hard-switched ac–dc stage of two-stage converters are typically switched at 10–20 kHz to avoid high switching losses, with corresponding bandwidths of 1–2 kHz. However, in the proposed converter, the ac–dc and dc–dc stages are integrated, facilitating soft-switching operation of all devices. Thus, higher switching frequencies (≥100 kHz), and higher bandwidths, are feasible, without leading to excessive switching losses. It can be seen from Fig. 13 that the rejection offered by these higher bandwidth (10–15 kHz) current loops are higher (≈ 20 dB) compared to those offered by the lower bandwidth loops (1–2 kHz). The utility of higher current control bandwidth in improving the current THD, without any additional hardware filter or control techniques, is demonstrated in Section V-C.

V. Experimental Results

This section first describes the 5-kW laboratory prototype of the proposed converter. The performance of the converter is then validated. The attenuation of harmonic currents with high bandwidth current control loop is also demonstrated by operating the converter with the distorted grid, which contains lower order harmonics.

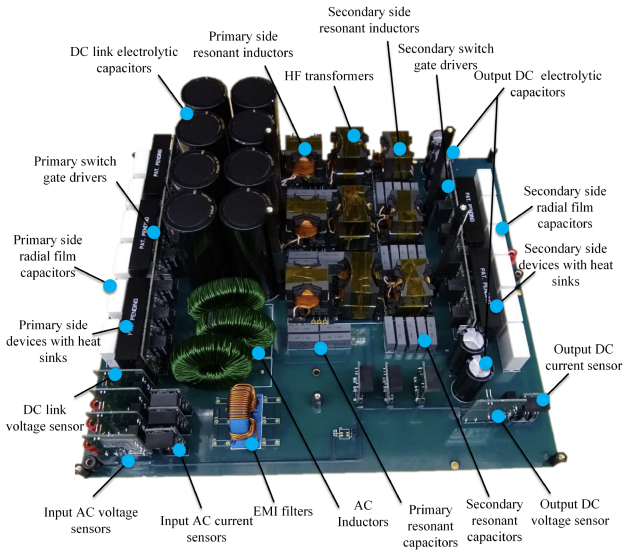


Fig. 14. Photograph of a 5-kW prototype of the proposed converter.

A. Hardware Description

A photograph of a 5-kW prototype of the proposed converter is given in Fig. 14. The dc-link voltage (V_{dc}) is 500 V. SiC devices (C3M0280090D) are used for primary and secondary sides of the converter. All these devices are switched at 130 kHz. The converter is used for a battery charging application. The output voltage is marked as V_{out} in Fig. 1. The specifications of the converter and designed parameter values are provided in Table I. The designed values of inductances in the power factor correction (PFC) stage, turns ratio of HF transformer and its magnetizing inductance, dc-link capacitance, resonant inductances and capacitances, and output dc capacitance are tabulated. The control algorithm is implemented in a TMS320F28379D DSP. The algorithm requires sensing of three-phase grid voltages and currents and dc-link voltage. The bandwidths of the current loops and voltage loop are 8 kHz and 500 Hz, respectively. These values for the current and voltage controller bandwidths were found to be good enough for rejection of harmonic current disturbances and load disturbance, respectively.

B. Start-up Process

The start-up process is explained in this subsection. Initially, the bottom switches on the primary (S_x, S_y, and S_z) and those on

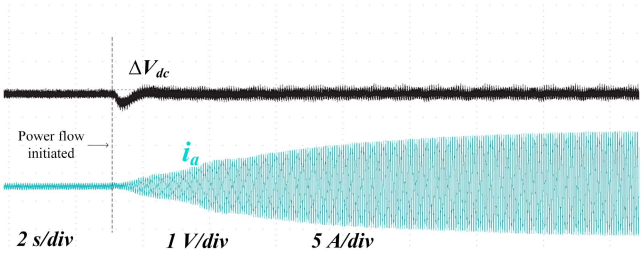


Fig. 15. Start-up process: negligible droop in dc-link voltage with power flow initiated to secondary side.

TABLE II
INDIVIDUAL HARMONIC COMPONENTS AND THD OF (a) a-phase GRID VOLTAGE V_a AND THOSE OF a-phase GRID CURRENT I_a WITH CURRENT CONTROLLER BANDWIDTHS OF (b) 3 kHz AND (c) 8 kHz

v_1	117.4 V
v_5	3.02 %
v_7	0.92 %
v_{11}	2.42 %
v_{13}	2.19 %
THD	6.45 %

(a)

i_1	3.98 A
i_5	1.59 %
i_7	0.96 %
i_{11}	3.33 %
i_{13}	2.79 %
THD	6.82 %

(b)

i_1	3.96 A
i_5	0.27 %
i_7	0.17 %
i_{11}	0.57 %
i_{13}	0.49 %
THD	2.46 %

(c)

the secondary (S_{db}, S_{eb}, and S_{fb}) are switched ON. All the other devices are kept OFF. Three-phase grid voltages are then applied. The converter acts like a three-phase diode bridge rectifier and the corresponding voltage is developed on the dc-link capacitor. The PLL algorithm is then executed. Once the angle of the grid voltage vector is obtained, dc-link voltage control is enabled. The dc-link voltage is ramped to the commanded value of 500 V at a rate of 40 V/s. Now, the desired power command (in the form of I^*_{out}) is given. The required phase angle is generated at the output of the controller. This phase angle is introduced between the primary and secondary side carriers for the specified power flow. The duty cycle of the bottom devices on the primary and secondary sides is changed from 100% to 75% with a time constant of 1 s. Simultaneously, the duty cycle of the top devices in the secondary side is changed from 0% to 25%. Fig. 15 shows that the grid current rises with the same time constant, causing negligible dip in the dc-link voltage.

C. Performance of the Proposed Converter With Distorted Grid

The three-phase voltages, namely, v_a, v_b, and v_c, obtained from the distorted grid are shown in Fig. 16. The dominant lower order harmonics present in the grid voltages are 5th, 7th, 11th, and 13th harmonics. The rms value of the fundamental component of a-phase voltage v_a is given in Table II(a). Magnitudes of the harmonic components as percentage of its fundamental component are also enlisted in Table II(a) along with the voltage THD.

The proposed converter is operated with current controller bandwidths of 3 and 8 kHz. The resulting grid currents are shown in Fig. 16(a) and (b), respectively. Magnitudes of the harmonic components of i_a, along with its THD, for 3- and 8-kHz current controller bandwidths are provided in Tables II(b) and (c), respectively. The maximum allowable harmonic current distortion as percentage of fundamental frequency component is specified in Table III. It can be seen that with a 3-kHz bandwidth, the 5th and 7th harmonic components are less than the specified limit. However, the 11th and 13th harmonic components and the overall THD exceed the stipulated limits. Table II(c) shows that, with a 8-kHz bandwidth, all individual harmonic components are significantly reduced and are less than 1%, leading to an overall THD of 2.46%. This complies with the IEEE standards for individual harmonic limits as well as overall THD.

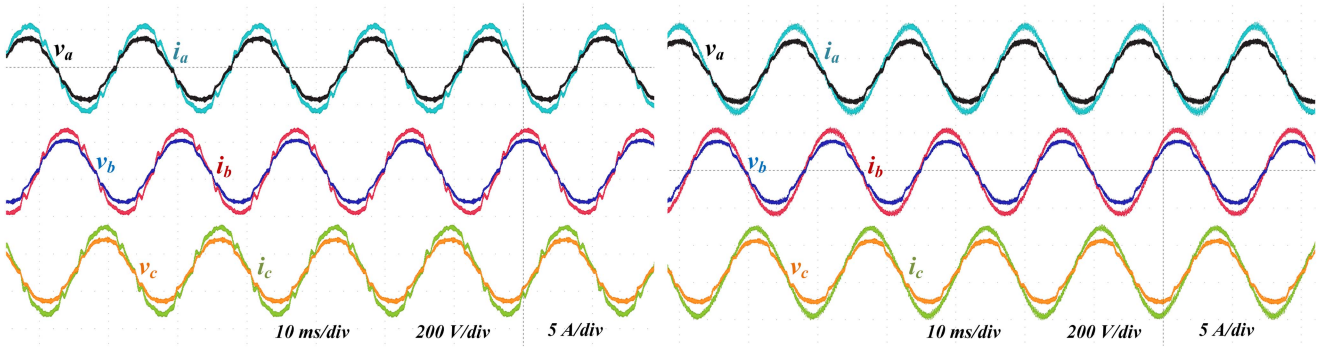
TABLE III
MAXIMUM ALLOWABLE HARMONIC CURRENT DISTORTION IN % OF FUNDAMENTAL FREQUENCY COMPONENT (h IS HARMONIC ORDER) [2]

$3\leq h<11$	$11\leq h<17$	$17\leq h<23$	$23\leq h<35$	TDD
4 %	2 %	1.5 %	0.6 %	5 %

Fig. 17 shows the experimental waveforms for ac–dc operation of the converter. It can be seen from Fig. 17 that the primary side line–line voltage v_{xy} leads the secondary side line–line voltage v_{de}. The dc-link voltage V_{dc} primary and secondary side resonant currents i_{xr} and i_{dr} are also shown in the figure. The dc-link voltage V_{dc} and output dc voltage on the secondary side V_{out} are 500 and 350 V, respectively. The grid currents for unity power factor operation are given in Fig. 17(b). Similar experimental results for dc–ac operation are shown in Fig. 18, where v_{xy} lags v_{de}.

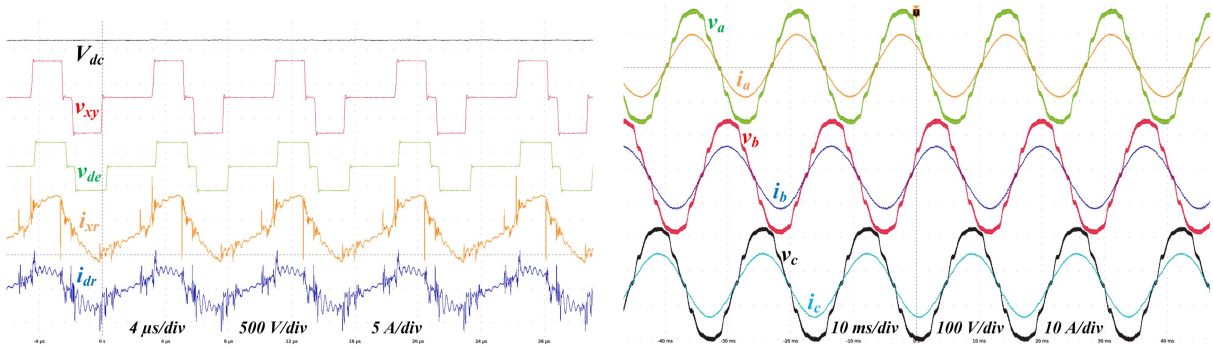
D. Soft-Switched Operation

The soft switched operation of devices are briefly described in this subsection. The conduction of the body diode of the MOSFET before it turns ON causes it to undergo a zero-voltage turn ON. The top devices of the primary side undergo ZVS turn-ON for positive half cycle of line current under various loading conditions. As discussed in Section III-B, resonant tank parameters are designed with the peak of the resonant current greater than that of the phase current, thereby achieving ZVS turn-ON of the middle and bottom devices over the entire line cycle. It is demonstrated in [24] that with duty cycle less than 30%, ZVS turn-ON of the bottom devices can be achieved for the entire cycle. In the proposed converter, a duty cycle of 25% is used to achieve ZVS for the bottom device. It can be observed from Fig. 20 that during turn-ON of the bottom switch, the gate–source voltage v_{GS} begins to rise after the drain–source voltage v_{DS} has fallen to zero. Similar experimental waveforms validating the ZVS turn-ON for other devices in the primary and secondary sides can also be shown. Out of the nine switches on the primary side, six are completely soft switched and the remaining three (S_a, S_b, and S_c) are semisoft switched (i.e., for positive half cycle of line current). The grid voltage and current during nonunity power factors of 0.8 lead and 0.8 lag are presented in Fig. 19(a) and (b), respectively. The ZVS turn-ON of the devices in the a-phase leg for power factor of 0.8 leading are shown in Fig. 20.



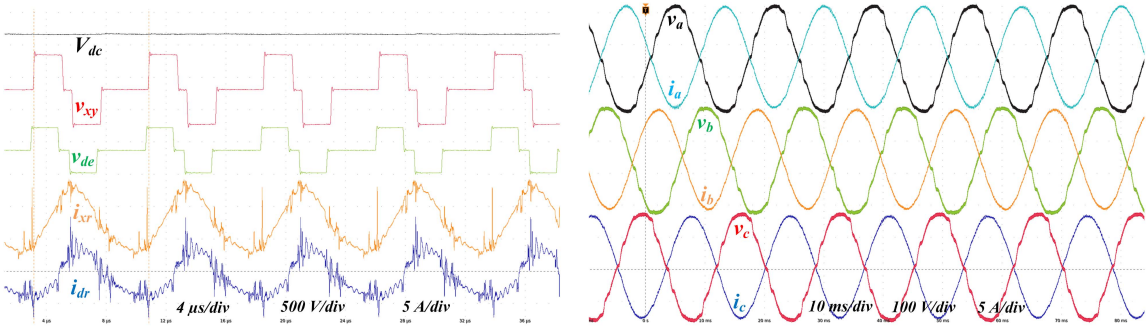
(a) (b)

Fig. 16. Attenuation of harmonic current disturbances with the proposed converter with current control bandwidths of (a) 3 kHz, (b) 8 kHz; v_a, v_b, and v_c are grid voltages; i_a, i_b, and i_c are grid currents.



(a) (b)

Fig. 17. AC–DC operation. (a) DC-link voltage $V_{\rm dc}$, secondary side line–line voltage v_{de}, lagging primary side line–line voltage v_{xy}, and primary and secondary side resonant currents i_{xr} and i_{dr}. (b) Grid voltages and currents.



(a) (b)

Fig. 18. DC–AC operation. (a) DC-link voltage $V_{\rm dc}$, secondary side line–line voltage v_{de}, leading primary side line–line voltage v_{xy}, and primary and secondary side resonant currents i_{xr} and i_{dr}. (b) Grid voltages and currents.

E. Efficiency

The losses in various components of the converter for the specifications listed in Table I with an output dc voltage of 350 V are shown in Fig. 21. The losses are calculated by following a similar approach as described in [22] and [28]. The plots of efficiency versus output power for output dc voltages of 300, 350, and 400 V are given in Fig. 22. The peak efficiency at these operating points are 94.51%, 95.01%, and 95.31%, respectively. The corresponding total losses are 152.7, 137.7, and 128.7 W. The experimentally calculated efficiency versus switching frequency plot in [15] shows that the efficiency of the ac–dc stage drops to 95% with SiC MOSFETs hard-switched at 130 kHz. Assuming the efficiency of the soft-switched dc–dc stage to be 98%, the overall efficiency falls to 93%.

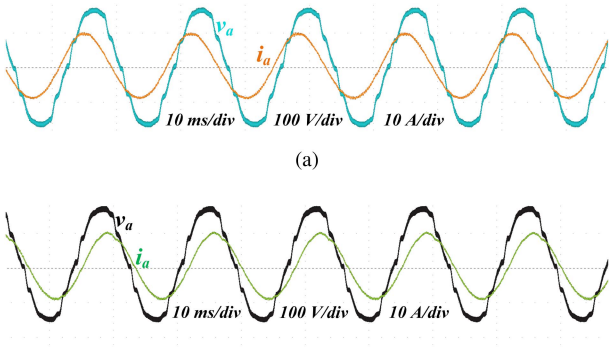


Fig. 19. Nonunity power factor operation: (a) 0.8 lead; (b) 0.8 lag.

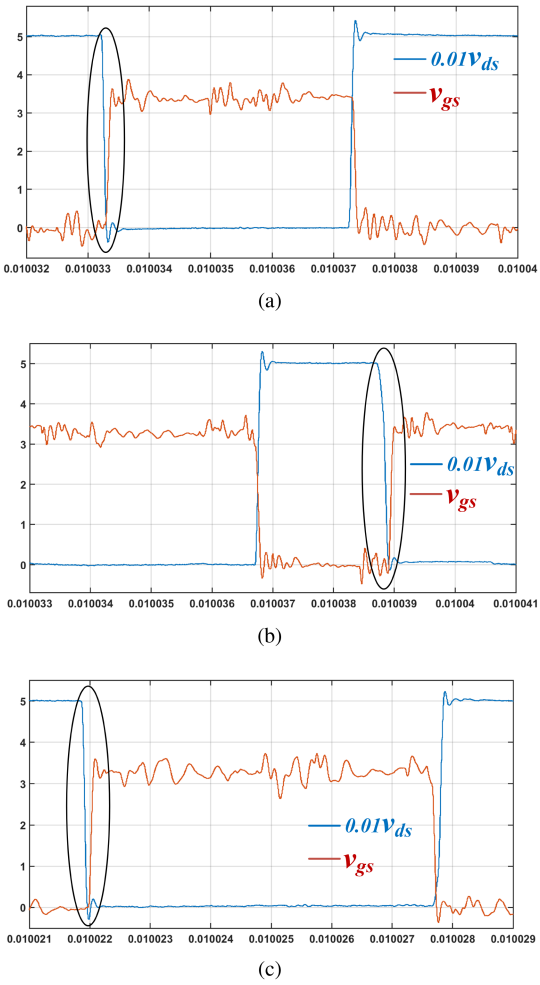


Fig. 20. ZVS operation for 0.8 power factor (lead): ZVS turn-ON of devices in a-phase leg on the primary side (a) top device, (b) middle device, and (c) bottom device; scale—v_{ds}: 100 V/div; v_{gs}: 1 V/div.

VI. Comparison With Existing Topologies

A comparative study of the proposed topology with existing nine-switch topologies, and other single-stage and two-stage bidirectional ac–dc converters is presented in this section.

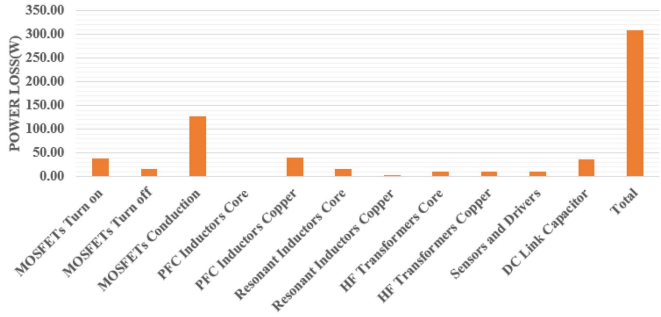


Fig. 21. Distribution of losses in various converter components, when operating under conditions specified in Table I for an output dc voltage of 350 V.

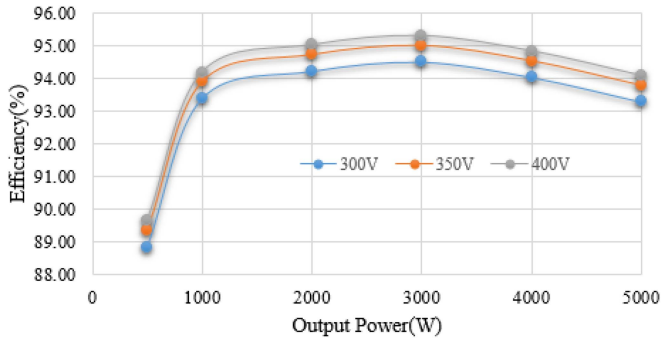


Fig. 22. Plot of efficiency versus output power for different output dc voltages.

A. Comparison With Existing Nine-Switch Topologies

Conventionally, the nine-switch converter is employed for ac–ac power conversion [32], [33]. Here, two sets of three-phase modulating signals are used for ac–dc and dc–ac operations, respectively [32]. These converters use IGBT devices which are hard-switched at around 5–10 kHz. The use of nine-switch topology as a dc–ac converter is presented in [34] and [35] for an integrated motor drive and battery charger system for electric vehicles. The current proposed converter based on nine-switch topology is inspired by the advent of SiC MOSFETs, which are capable of switching at HF. This facilitated the integration of three-phase resonant isolated dc–dc converter with three-phase ac–dc boost rectifier, thus enabling the soft-switching of devices for ac–dc operation as well. The proposed modulation scheme employs three-phase modulating signals and a constant dc signal for ac–dc and dc–dc operations, respectively. The decoupling of the ac–dc and dc–dc operations is achieved by XOR logic based switching of the middle devices of the nine-switch bridge as explained in Section II-B.

B. Comparison With Other Existing Topologies

Table IV shows a comparison of the proposed bidirectional ac–dc converter with existing single-stage and two-stage bidirectional ac–dc converters. The converter proposed in [29] has an unfolder circuit based on a neutral point clamped topology. Even though this converter can be switched at 100 kHz, the device count is higher and the efficiency is lower compared to the proposed converter. The work [7] proposes a converter

TABLE IV
COMPARISON WITH EXISTING TOPOLOGIES

Converter	Rated power (P_o)	Input voltage (V_{rms})	Output voltage (V_{out})	Switching frequency (f_{sw})	Peak efficiency (η)	Current THD (full-load)	Device count
Chen [29]	2 kW	208–380 V	500 V	100 kHz	93%	2.5%	20
Sayed [7]	1 kW	200 V	230 V	20 kHz	96.01%	11.1%	16
Almeida [30]	5 kW	380 V	380 V	50 kHz	92.5%	3.2%	24
Ling Gu [31]	3 kW	380 V	380 V	20 kHz	94.3%	1.91%	18
Two stage	5 kW	400 V	380 V	130 kHz	93.8%	2.58%	18
This work	5 kW	208 V	300-400 V	130 kHz	95.3%	2.46%	15

with an efficiency of 96%. But this converter is switched at a frequency of 20 kHz only. Also, the THD achieved is 11.1%, which does not satisfy IEEE Std 519-2014. The proposed converter in [30] is switched at 50 kHz and achieves a THD of 3.2%. However, the device count is high, namely 24. A 20-kHz switching converter is presented in [31], which achieves an efficiency of 94.3% and a THD of 1.91%, with a device count of 18. The conventional back-to-back two-stage converter with a similar device count has a calculated efficiency of 93.8% and a THD of 2.58%. The converter proposed in this work achieves an efficiency of 95.3% and a THD of 2.46%, even with distorted grid voltages. It can be seen from Table IV that the proposed converter has the lowest device count of 15 compared to other topologies.

VII. CONCLUSION

This article proposes a three-phase integrated bidirectional isolated ac–dc converter with soft-switching operation extended to all devices, unlike in an existing two-stage converter, where only the devices in the dc–dc stage are soft-switched. This, in turn, facilitated a high switching frequency of 130 kHz for all the devices, without resulting in much switching losses. Thus, a current control loop with a bandwidth of 8 kHz could be realized, which resulted in the rejection of current harmonic disturbances, arising due to distorted grid voltages. The decoupling of the ac–dc and dc–dc operations with the proposed modulation scheme involving XOR logic is illustrated. The values of the elements of the resonant network are found using an iterative design procedure detailed in the article. A comparison of the proposed topology with existing topologies is provided. It is experimentally demonstrated on a 5-kW laboratory prototype that the proposed converter achieves good efficiency with a low current THD, complying with IEEE Std 519-2014, when operated under distorted grid voltages. The soft-switching operation of devices is also validated experimentally.

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