

# Small-Signal Stability Analysis With Approximated PV Model for Solar Array Simulator

Thusitha Randima Wellawatta , *Member, IEEE*, and Sung-Jin Choi , *Member, IEEE*

**Abstract**—Solar array simulators (SAS) equipment is used to mimic the characteristics curve for photovoltaic (PV) generators. However, an in-depth stability analysis of the SAS with respect to its reference signal is yet to be investigated. This is due to implicit and nonlinear mapping equations used to describe the  $I$ - $V$  curve, which complicates the loop analysis. Our study proposes a super-elliptical method to approximate the  $I$ - $V$  characteristic curve and provide an explicit PV equation that is straightforward to manipulate. Furthermore, this approximate model is then used for the dynamic performance assessment for the typical control architecture. Based on the comparative study using the approximate mode either in the theoretical analysis and the experimental verification, the resistance-sensing control scheme tends to reduce the effect of loop interactions in the SAS, thereby showing more consistent dynamic performance than the other control structure.

**Index Terms**—Photovoltaic (PV) modeling, small-signal model, solar array simulators (SAS).

## I. INTRODUCTION

SOLAR Array Simulators (SAS) are used to imitate the behavior of photovoltaic (PV) panels under varying irradiation and temperatures. SAS consists of a dc–dc converter, a reference generator, and a controller, as indicated in Fig. 1. A PV equation or look-up table is always embedded into the reference generator to ensure that the SAS output and  $I$ - $V$  characteristics curve correspond [1].

The hardware control structures of SAS can be categorized based on its control and sensing method. The control method can either be the voltage reference control (VRC) or the current reference control (CRC), as shown in Fig. 2. Whereas the CRC utilizes the current reference signal generated from a sensed voltage, the reference signal in VRC is produced from a sensed current. Depending on its operating points, the dc–dc converter

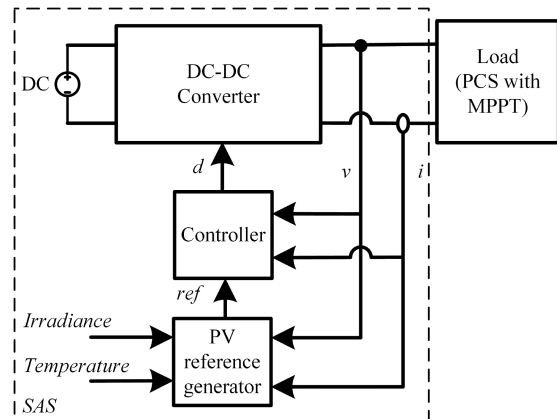


Fig. 1. Typical SAS system.

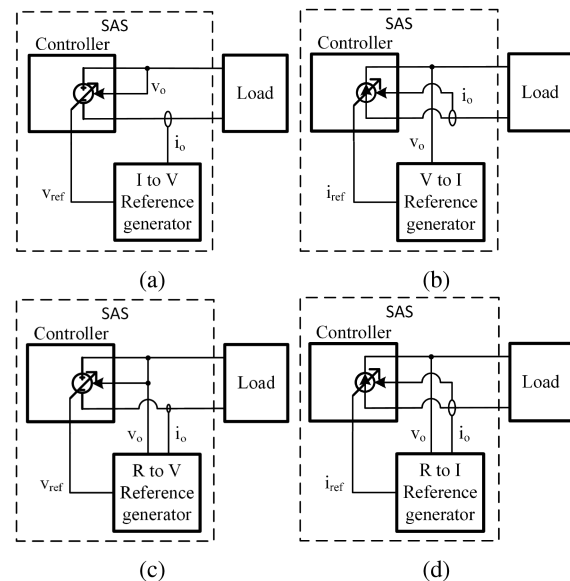


Fig. 2. Block diagrams of SAS configuration. (a) CS-VRC. (b) VS-CRC. (c) RS-VRC. (d) RS-CRC.

Manuscript received 19 March 2022; revised 13 June 2022; accepted 30 June 2022. Date of publication 18 July 2022; date of current version 10 October 2022. This work was supported by the National Research Foundation of Korea (NRF) with a grant funded by the Korea government (MSIT) (NRF-2020R1A2C2009303). Recommended for publication by Associate Editor D. M. Xu. (*Corresponding author: Sung-Jin Choi.*)

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Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TPEL.2022.3191672>.

Digital Object Identifier 10.1109/TPEL.2022.3191672

should operate as either a current or voltage source, where the dynamic response can be intensely dependent on the control structure in the current source segment (CSS) and voltage source segment (VSS), as shown in Fig. 3. Most commercially available SAS seek stable and accurate points for their operation in the  $I$ - $V$  curve. A detailed classification of the various hardware typologies currently in use is shown in Table I.

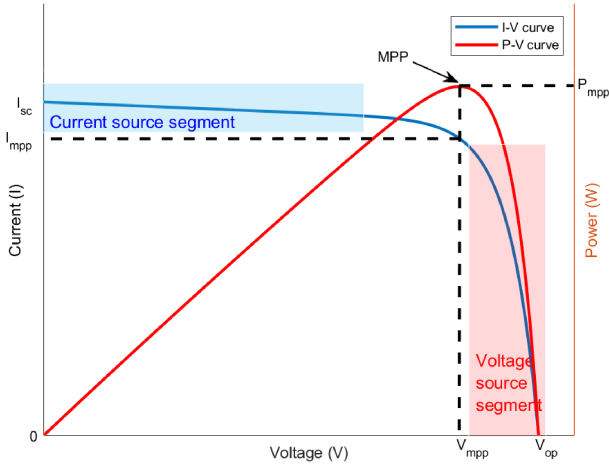


Fig. 3. Typical characteristic of the PV curve.

TABLE I  
PREVIOUS STUDIES ON SAS ARCHITECTURE

Ref.	Structure	Reference generator	Controller
[1]	VS-CRC	PV equation	FS-MPC
[2]	VS-CRC	PV equation	PI
[3]	VS-CRC	Reference PV cell	PI
[4]	VS-CRC	Lookup table	PID
[5]	VS-CRC	Lookup table	PID
[6]	VS-CRC	Lookup table	Current mode PI
[7]	VS-CRC	Lookup table	PI
[8]	VS-CRC	PV equation	Peak voltage controlled PI
[9]	VS-CRC	PV equation	PI
[10]	VS-CRC	PV equation	FOPI
[11]	RS-CRC	PV equation	Current mode PI
[12]	RS-VRC	Lookup table	Boundary control law
[13]	RS-VRC	PV equation	Backstepping
[14]	RS-VRC	PV equation	PI or FLC
[15]	CS-VRC	Lookup table	FLC
[16]	CS-VRC	Lookup table	Current mode PI
[17]	CS-VRC	PV equation	Type III
[18]	CS-VRC	PV equation	PI
[19]	Hybrid (VS, RS-CRC)	Lookup table	PID
[20]	Hybrid (VS-CRC, CS-VRC)	Lookup table	PID
[21]	Hybrid (VS-CRC, CS-VRC, RS-VRC)	PV equation	PI

The SAS sensing method can either be a voltage sensing (VS) [1]–[10], current sensing (CS) [15]–[18], or a resistance sensing (RS) [11]–[14]. Regardless of the sensing method used, the reference generator induces the reference signal according to the look-up table or approximate  $I$ – $V$  characteristic equation embedded into the circuit. Some recent studies proposed a more advanced sensing method that combines VS, CS, and RS sensing methods to form a hybrid sensing method [19]–[21].

Although the reference generator of most commercial SAS is primarily based on predefined values stored in a look-up table,

the resilience of the  $I$ – $V$  characteristics curve is significantly reduced. The equation-based SAS offers more flexibility than a look-up table. However, it requires iterations to solve the implicit  $I$ – $V$  relation. The Lambert-W function [10], [22], [23], which also requires long and complex iterations. Especially in [10], Lambert-W function PV reference generator and fractional-order PI (FOPI) controller are used and got comparatively better  $I$ – $V$  curve but still has a deviation in CCS.

Due to this complexity, various studies have focused significantly on understanding the steady-state accuracy and inner loop interactions of the SAS under a constant load condition [21], [24]. Hence, for either a VRC or CRC hardware structure, only the voltage and current controllers were studied, respectively. However, the reference signal being a time-varying quantity reflects changes in its output into the SAS, disturbing overall system dynamics. Even though various studies have raised this opinion, not enough comprehensive and detailed explanation has been given. Specifically, the stability analysis and performance comparison of the different SAS hardware structures have a lack of research focus [19]–[21].

In this study, the various hardware structures of SAS are evaluated and compared with respect to multiloop stability. Section II proposes the super-elliptical method as an approximation method for solving the implicitness of the PV characteristic equation; Section III discusses the small-signal model of the various hardware structures describing it as a multiloop system. Section IV examines the multiloop analysis based on these models. In addition, theoretical analysis confirming simulation results is indicated. Finally, Section VI concludes this article.

## II. MODELING OF PV REFERENCE GENERATOR

### A. Elliptical Approximation for $I$ – $V$ Characteristics of PV Panels

The reference signal of an equation-based SAS is generated from a sensed variable based on the PV characteristics equation. The PV panel is modeled by an equivalent circuit consisting of a current source, two resistors, and a PN junction diode. The mathematical equation describing the characteristic curve of a PV panel becomes complex and implicit due to the exponential function. As a result, the iterative solutions for the module output voltage and current often require complicated and long expressions. The basic implicit equation for a PV generator is given as

$$i_{pv} = I_{ph} - I_s \left[ e^{\left( \frac{v_{pv} + i_{pv} R_s}{ANV_t} \right)} - 1 \right] - \frac{v_{pv} + i_{pv} R_s}{R_{sh}} \quad (1)$$

where  $i_{pv}$  represents the module output current (A),  $I_{ph}$  represents the PV current (A),  $I_s$  represents the saturation current of the diode (A),  $v_{pv}$  represents the module output voltage (V),  $V_t$  represents the thermal voltage (V),  $A$  represents the ideality factor,  $R_s$  represents the series resistance ( $\Omega$ ),  $R_{sh}$  represents the parallel resistance ( $\Omega$ ) [6], and  $N$  represents the number of series cells in the module.

$V_t$  can be further demonstrated as

$$V_t = \frac{NkT}{q_e} \quad (2)$$

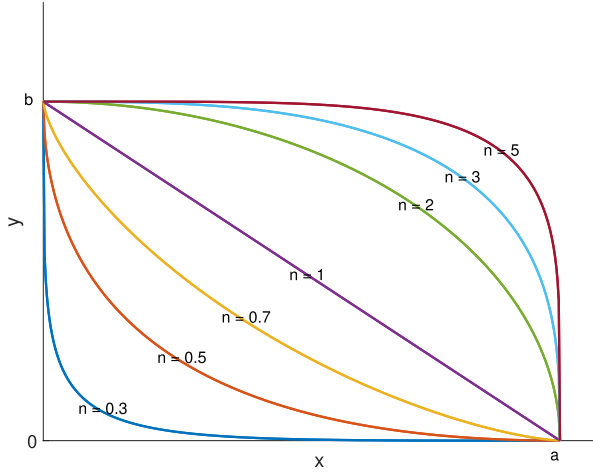


Fig. 4. Typical super-elliptical curves with different  $n$ .

where  $N$  represents the number of cells in a series string,  $k$  represents the Boltzmann constant,  $T$  represents the absolute temperature of PV string in Kelvin, and  $q_e$  represents the electron charge ( $1.602 \times 10^{-19} C$ ).

The PV current  $I_{ph}$  is dependent on both the light intensity and temperature levels of each solar cell. This current can be calculated using

$$I_{ph} = \frac{G}{G_n} (I_{scn} + K_I(T - T_n)) \quad (3)$$

where  $I_{scn}$  represents the short-circuit current at standard test condition (STC:  $T_n = 298.15 K$  ( $25^\circ C$ ) in temperature,  $G_n = 1000 W/m^2$  in insolation condition),  $T$  represents the module temperature in Kelvin, and  $G$  represents the module insolation, and  $K_I$  represents the temperature coefficient of  $I_{sc}$ .

Another key component of the characteristic equation of the PV panel is the saturation current  $I_s$ .  $I_s$  can be expressed as

$$I_s = \frac{I_{scn} + K_I(T - T_n)}{e^{\frac{V_{ocn} + K_V(T - T_n)}{AV_t}} - 1} \quad (4)$$

where  $V_{ocn}$  represents the open-circuit voltage at STC and  $K_V$  represents the temperature coefficient of  $V_{oc}$ .

Section I states that the reference signal generated in an SAS depends on the sensed variables. There is a need to find a mathematical equation that approximates the characteristic equation to reduce the cumbersome iterations required due to the implicitness of this signal.

In this regard, the super-elliptical method gives a simple and fast approximation of the  $I$ - $V$  characteristic equation. A super-ellipse (or Lamé curve) has a similar curve as an  $I$ - $V$  curve. In its first quadrant, both a super-ellipse and an  $I$ - $V$  curve have a similar curve, as shown in Fig. 3. As a result, the tangents of this slope at two separate points ( $V_{oc}, 0$ ) and ( $0, I_{sc}$ ) can then be approximated as zero and an infinite value, respectively.

This basic assumption makes the characteristic equation become a simple mathematical equation. Therefore, applying the Cartesian coordinate system to the curve shown in Fig. 4, the

Lamé curve must satisfy the equation

$$\left| \frac{x}{a} \right|^n + \left| \frac{y}{b} \right|^n = 1. \quad (5)$$

Using (5), an approximated mathematical expression for the PV characteristic equation can then be written as

$$\left[ \frac{v}{V_{oc}} \right]^n + \left[ \frac{i}{I_{sc}} \right]^n = 1, (v \geq 0, i \geq 0). \quad (6)$$

In this study, the super-elliptical curve is chosen to go through ( $V_{oc}, 0$ ), ( $0, I_{sc}$ ), and ( $V_{mpp}, I_{mpp}$ ). Thus, the value of  $n$  can be solved by using the formula

$$\left[ \frac{V_{mpp}}{V_{oc}} \right]^n + \left[ \frac{I_{mpp}}{I_{sc}} \right]^n = 1. \quad (7)$$

To solve (7), by substituting

$$\left[ \frac{V_{mpp}}{V_{oc}} \right] = A, \left[ \frac{I_{mpp}}{I_{sc}} \right] = B. \quad (8)$$

Hence, the value of  $n$  can be obtained by iteration

$$n_{i+1} = \frac{-B^{n_i}}{\log\left(\frac{A}{B}\right)} \quad (9)$$

where  $i$  represents the iteration index.

Thus, for the super-elliptical curve, the current reference in VS architecture is given as

$$i_{ref} = I_{sc} \sqrt[n]{1 - \left(\frac{v}{V_{oc}}\right)^n} \quad (10)$$

where  $v$  is the measured output voltage of SAS. Similarly, in the case of CS structure, the voltage reference can be expressed as

$$v_{ref} = V_{oc} \sqrt[n]{1 - \left(\frac{i}{I_{sc}}\right)^n} \quad (11)$$

where  $i_{ref}$  represents the reference current signal obtained in the VS structure and  $v_{ref}$  represents the voltage signal obtained using the CS structure. In addition,  $i$  and  $v$  are the sensed current and voltage at every instant.

### B. Small-Signal Modeling of a Voltage- or Current-Sensing (VS or CS) Reference Generator

The reference signal is differentiated with respect to the sensed signal to obtain the small-signal gain of the reference generator. Therefore, the small-signal gain is obtained by differentiating (11) with respect to the sensed current at any given point ( $V_{op}, I_{op}$ ) in a CS-VRC hardware structure. This small-signal gain is called trans-resistance gain

$$k_{v_{ref}, i} = \frac{\hat{v}_{ref}}{\hat{i}} \Big|_{(V_{op}, I_{op})} = -\frac{V_{oc} I_{op}^{(n-1)}}{I_{sc}^n} \left[ 1 - \left(\frac{I_{op}}{I_{sc}}\right)^n \right]^{\left(\frac{1}{n}-1\right)}. \quad (12)$$

Similarly, a trans-conductance small-signal gain at point ( $V_{op}, I_{op}$ ) is obtained by differentiating (10) with respect to the

sensed voltage

$$k_{\hat{i}_{\text{ref}},v} = \left. \frac{\hat{i}_{\text{ref}}}{\hat{v}} \right|_{(V_{\text{op}}, I_{\text{op}})} = -\frac{I_{\text{sc}} V_{\text{op}}^{(n-1)}}{V_{\text{oc}}^n} \left[ 1 - \left( \frac{V_{\text{op}}}{V_{\text{oc}}} \right)^n \right]^{\left( \frac{1}{n} - 1 \right)}. \quad (13)$$

### C. Small-Signal Modeling of an RS Reference Generator

Two stages are involved when an RS reference generator is involved. First, the instantaneous resistance is obtained by dividing the sensed voltage by the sensed current

$$r = \frac{v}{i}. \quad (14)$$

Second, (14) is substituted into (11) and (10), respectively, to obtain the reference signal. Therefore, the reference for RS-VRC and RS-CRC is given, respectively

$$v_{\text{ref,RS}} = \frac{1}{\sqrt[n]{\left( \frac{1}{r I_{\text{sc}}} \right)^n + \left( \frac{1}{V_{\text{oc}}} \right)^n}} \quad (15)$$

$$\hat{i}_{\text{ref,RS}} = \frac{1}{\sqrt[n]{\left( \frac{r}{V_{\text{oc}}} \right)^n + \left( \frac{1}{I_{\text{sc}}} \right)^n}}. \quad (16)$$

The small-signal gain describing the first step of instantaneous resistance (14) can be written as

$$\hat{r} = k_{\text{rv}} \hat{v} + k_{\text{ri}} \hat{i}. \quad (17)$$

As a result, these two small-signal gains can, therefore, be represented by differential equations at any operating point

$$k_{\text{rv}} = \left. \frac{\hat{r}}{\hat{v}} \right|_{(V_{\text{op}}, I_{\text{op}})} = \frac{1}{I_{\text{op}}}, \quad k_{\text{ri}} = \left. \frac{\hat{r}}{\hat{i}} \right|_{(V_{\text{op}}, I_{\text{op}})} = -\frac{V_{\text{op}}}{I_{\text{op}}^2}. \quad (18)$$

Two different cases are to be considered to describe the small-signal model of the actual reference signal. If the reference signal is given as  $v_{\text{ref}} = f(r)$  as in (15), then the small-signal gain at the operating point  $(V_{\text{op}}, I_{\text{op}})$  is determined to be

$$k_{v_{\text{ref}},r} = \left. \frac{\hat{v}_{\text{ref}}}{\hat{r}} \right|_{(V_{\text{op}}, I_{\text{op}})} = \frac{1}{r^{1+n} I_{\text{sc}}^n \left( \left( \frac{1}{r I_{\text{sc}}} \right)^n + \left( \frac{1}{V_{\text{oc}}} \right)^n \right)^{\frac{1}{n} + 1}}. \quad (19)$$

In addition, if the reference signal is of the form  $i_{\text{ref}} = g(r)$  as represented in (16), then the gain is given to as

$$k_{i_{\text{ref}},r} = \left. \frac{\hat{i}_{\text{ref}}}{\hat{r}} \right|_{(V_{\text{op}}, I_{\text{op}})} = -\frac{r^{n+1}}{V_{\text{oc}}^n \left( \left( \frac{r}{V_{\text{oc}}} \right)^n + \left( \frac{1}{I_{\text{sc}}} \right)^n \right)^{\frac{1}{n} + 1}}. \quad (20)$$

From theory, the reference signal in the outer loop must not be faster than the signal generated by the control loop. An intentional time-delay function  $L(s)$  is introduced in this model to account for any time-delay effect in the reference signal at any time. In its simplified form,  $L(s)$  is given by the first series expansion of the Padé approximation as

$$L(s) = e^{-st_d} \approx \frac{1 - \alpha s}{1 + \alpha s}; \quad \alpha = t_d/2 \quad (21)$$

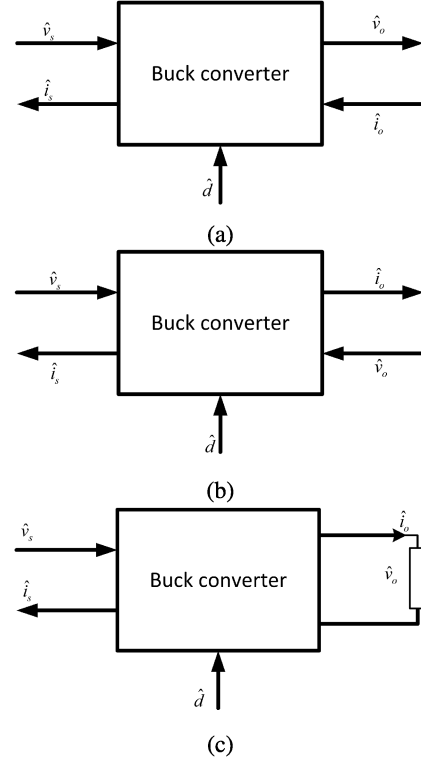


Fig. 5. Block diagrams of converter model. (a) Current-terminated model. (b) Voltage-terminated model. (c) Resistive load-terminated model.

where the  $t_d$  accounts for such a time delay effect in the reference generation.

## III. MODELING AND ANALYSIS OF SAS SYSTEMS

To have a clear picture of the dynamics of an SAS, the dc-dc converter model behavior as determined by the connected load, can be represented to be an unterminated converter model having three inputs ( $\hat{v}_s$ ,  $\hat{i}_o$ , and  $\hat{d}$ ) and two outputs ( $\hat{v}_o$ ,  $\hat{i}_s$ ), as shown in Fig. 5. This study assumes a buck converter for the dc-dc power stage; therefore, different small-signal models are obtained under different load configurations.

### A. Current-Terminated Buck Converter Model

When SAS is connected to the current-sink type of load such as fractional short-circuit current MPPT tracker, the SAS should be modeled as a current-terminated converter. The small-signal model is changed by replacing the load with a current source, as shown in Fig. 5(a). Hence, the differential output voltage is defined to be

$$\hat{v}_o = dv_o(\hat{v}_s, \hat{i}_o, \hat{d}). \quad (22)$$

Thus,

$$\hat{v}_o \cong \left. \frac{\hat{v}_o}{\hat{v}_s} \right|_{(\hat{i}_o, \hat{d})=0} \hat{v}_s - \left. \frac{\hat{v}_o}{\hat{i}_s} \right|_{(\hat{v}_s, \hat{d})=0} \hat{i}_s + \left. \frac{\hat{v}_o}{\hat{d}} \right|_{(\hat{i}_o, \hat{v}_s)=0} \hat{d} \quad (23)$$

If a well-regulated power supply provides an input voltage to the buck converter,  $\hat{v}_s$  can be determined to be zero. The resulting transfer function for the unterminated voltage source converter



However, the overall loop gain is not uniquely defined in the multiloop system, but defined by either the signal injection point or the breaking point [25], [31]. Therefore, special consideration is needed. If the overall loop is intercepted at a point A as shown in Fig. 7, then the outer loop gain is obtained as

$$T_A(s) = \frac{T_{iv}(s)}{1 + T_v(s)}. \quad (35)$$

Similarly, if the loop is interrupted at point B, then the overall loop gain is derived to be

$$T_B(s) = T_v(s) + T_{iv}(s). \quad (36)$$

This study focuses on the overall loop gain  $T_B(s)$  to analyze the loop interactions within the multiloop systems. By substituting (34) and (33) into (36), we obtain

$$T_B(s) = F_m C(s) G_{vd}(s) K_1(s) \quad (37)$$

where  $K_1(s)$  represents the degree of interference from the outer loop and is defined as

$$K_1(s) = (1 - k_1 L(s)); k_1 = \frac{k_{v_{ref},i}}{R_L}. \quad (38)$$

If the value of  $K_1(s)$  is unity, then no interactions exist between the inner and outer loops. Hence, this system is seen as a single loop. Practically, the determinant factors for calculating the value of  $K_1(s)$  are the resistance ratio  $k_1$  and the time delay function  $L(s)$ .

$k_1$  is the ratio of incremental resistance of the PV curve to the load resistance at every instant by definition. This value is always negative and exhibits the following trends:

$$(V_{op}, I_{op}) \rightarrow (V_{OC}, 0) : k_1 \rightarrow 0 (< 0)$$

$$(V_{op}, I_{op}) \rightarrow (V_{mpp}, I_{mpp}) : k_1 \rightarrow -1$$

$$(V_{op}, I_{op}) \rightarrow (0, I_{SC}) : k_1 \rightarrow -\infty.$$

From this trend, it can be concluded that the value of  $k_1$  becomes a very small negative value when it operates either near the open circuit condition or in the VSS. While  $k_1$  becomes a very large number (approaching negative infinity) when either operating under short-circuit conditions or in the CSS.

$L(s)$  is the intentional time-delay effect introduced into the reference signal of an SAS as introduced in Section II-C. To effectively examine the effect of the loop interactions, the mathematical expression for  $K_1$  is rearranged using the Padé approximant in (21) as

$$K_I(s) = (1 - k_1) \frac{1 + \frac{\alpha(1+k_1)s}{(1-k_1)}}{1 + \alpha s}. \quad (39)$$

Fig. 8 shows the simulation results describing the effect of varying  $k_1$  and  $L(s)$  on the overall loop gain in the frequency domain. First, by taking a constant time-delay  $t_d = 10 \mu s$  and varying the values of  $k_1$ , the result of this variation is shown in Fig. 8(a). A small loop interaction was observed in the system due to the presence of a left-half plane zero and small phase angle delay when  $-1 < k_1 < 0$ . As the SAS operates under MPP, this left-half plane zeros diminish when  $k = -1$ . Nevertheless, the SAS operates in the CSS when  $k_1 < -1$ , hence, a right-half

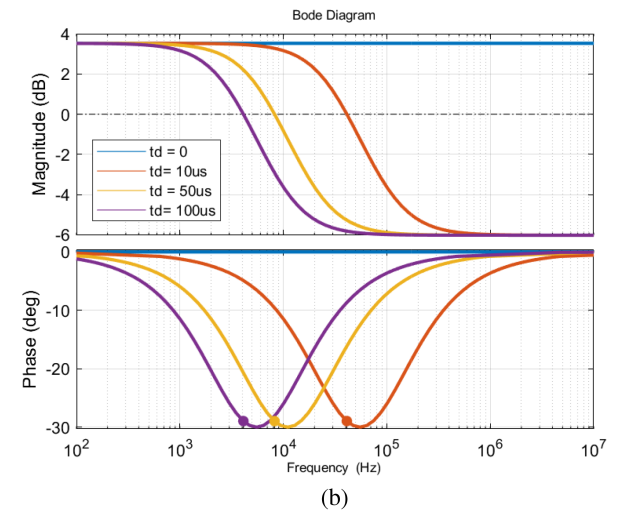
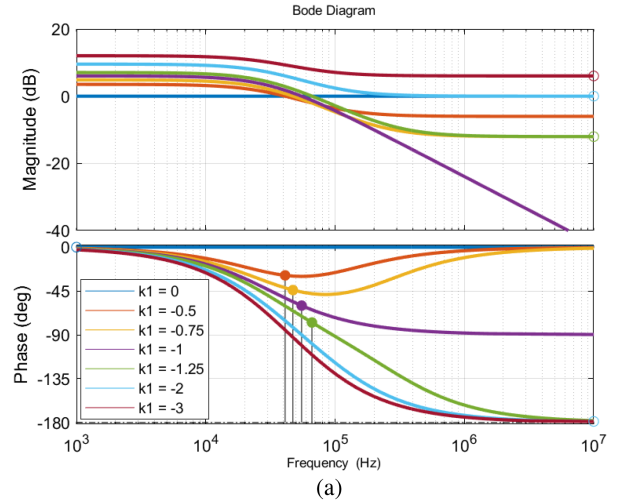


Fig. 8. Loop interaction function  $K_1(s)$ . (a) according to  $k_1$  when  $t_d = 10 \mu s$ . (b) according to  $t_d$  when  $k = -0.5$ .

plane zero is observed, resulting in a remarkable phase angle delay in the system. This increased phase delay reduces the overall system stability of the SAS.

Another possibility is to maintain the value of  $k_1 = -0.5$  constant while varying  $t_d$  shown in Fig. 8(b). The overall stability of the SAS deteriorates if an inappropriate time delay is added to the system, even at a fixed operating point.

### E. Small-Signal Analysis of Voltage-Sensing Current Reference Control (VS-CRC)

In the VS-CRC hardware structure, the main control loop is the current loop since the sensed voltage is used to generate the reference current. The loop gain at breaking point B as shown in Fig. 9 can be expressed as

$$T_B(s) = T_i(s) + T_{vi}(s) \quad (40)$$

where the individual loop gains are derived as

$$T_i(s) = F_m C(s) G_{iod}(s) \quad (41)$$

$$T_{vi}(s) \equiv F_m C(s) G_{iod}(s) R_L k_{i_{ref},v} L(s). \quad (42)$$

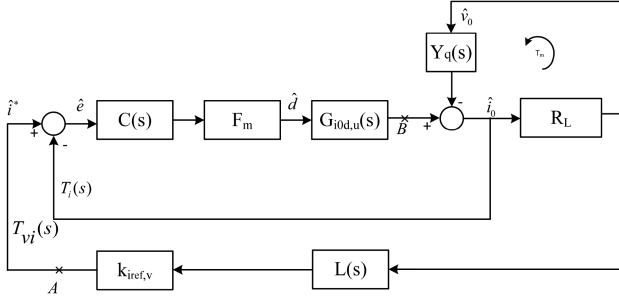


Fig. 9. Small-signal block diagram of the VS-CRC system.

Hence, the small-signal model equation for the overall loop gain is given as

$$T_B(s) = F_m C(s) G_{iod}(s) K_2(s) \quad (43)$$

where  $K_2(s)$  defines the degree of interference between the inner loop and the reference signal

$$K_2(s) = 1 - k_2 L(s); k_2 = k_{i_{ref},v} R_L. \quad (44)$$

Unlike the CS-VRC hardware structure, the resistance ratio ( $k_2$ ) in (44) is only proportional to the load resistance ( $R_L$ ) and has the following trends:

$$\begin{aligned} (V_{op}, I_{op}) \rightarrow (V_{OC}, 0) : k_2 &\rightarrow -\infty \\ (V_{op}, I_{op}) \rightarrow (V_{mpp}, I_{mpp}) : k_2 &\rightarrow -1 \\ (V_{op}, I_{op}) \rightarrow (0, I_{SC}) : k_2 &\rightarrow 0 (< 0). \end{aligned}$$

These operating point characteristics of  $K_2$  are the exact opposite of  $K_1$ . Similarly,  $K_2$  can also be approximated by using the Padé approximation as

$$K_2(s) = (1 - k_2) \frac{1 + \frac{\alpha(1+k_2)s}{(1-k_2)}}{1 + \alpha s}. \quad (45)$$

As a result, it can be concluded that the VS-CRC system suffers from loop interactions in VSS due to the low phase margin near the open-circuit point.

#### F. Small-Signal Analysis of Resistance-Sensing Voltage Reference Control (RS-VRC)

Fig. 10 shows the small-signal block diagram for the hardware structure for a RS-VRC, where the current and reference loop gains can be written as

$$T_v(s) = F_m C(s) G_{vd}(s) \quad (46)$$

$$T_{rv}(s) = -F_m C(s) G_{vd}(s) k_{v_{ref},r} \left( k_{rv} + \frac{k_{ri}}{R_L} \right) L(s). \quad (47)$$

Hence, the overall

$$T_B(s) = F_m C(s) G_{vd}(s) K_3(s) \quad (48)$$

where

$$K_3(s) = 1 - k_{v_{ref},r} \left( k_{rv} + \frac{k_{ri}}{R_L} \right) L(s) \quad (49)$$

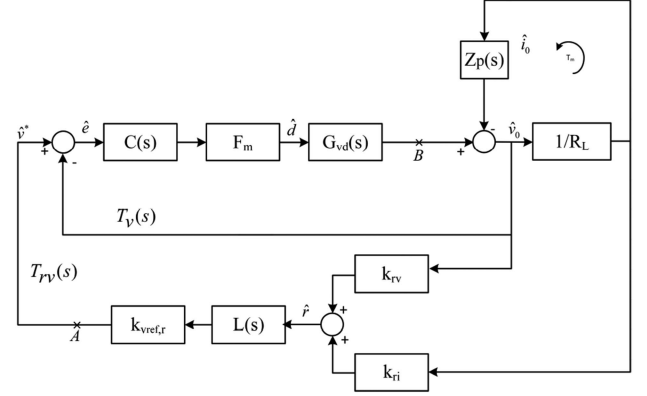


Fig. 10. Small-signal block diagram of the RS-VRC system.

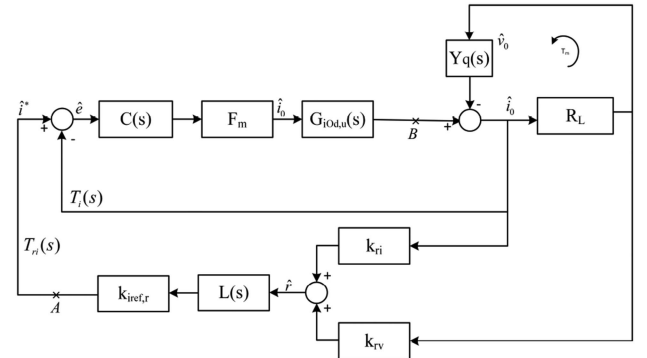


Fig. 11. Small-signal block diagram of the RS-CRC system.

and  $k_{v_{ref},r}$  is the small-signal gain in (19) according to the slope of the solar panel curve.

Since the following equality must hold true:

$$k_{rv} + \frac{k_{ri}}{R_L} = \frac{1}{I_{op}} - \frac{V_{op}/I_{op}^2}{V_{op}/I_{op}} = 0 \quad (50)$$

we can get that  $K_3(s) \equiv 1$ . RS reference generation nullifies the effect of loop interactions within a multiloop system regardless of variations in either the operating point or time-delay effects in reference signals. This is considered a salient advantage based on the overall system stability.

#### G. Small-Signal Analysis of Resistance-Based Current Reference Control (RS-CRC)

The RS-CRC hardware is dual to the RS-VRC, as shown in Fig. 11. The gain of the current and reference loops can, therefore, be written as

$$T_i(s) = F_m C(s) G_{iod}(s) \quad (51)$$

$$T_{ri}(s) \equiv F_m C(s) G_{iod}(s) L(s) k_{i_{ref},r} (k_{ri} + k_{rv} R_L). \quad (52)$$

Consequently, the overall loop gain becomes

$$T_B(s) = F_m C(s) G_{iod}(s) K_4(s) \quad (53)$$

where

$$K_4(s) = 1 - k_{i_{ref},r} (k_{ri} + k_{rv} R_L) L(s). \quad (54)$$

TABLE II  
CONVERTER COMPONENTS AND TYPE III CONTROLLER PARAMETERS

Parameter	Value	Unit	Parameter	Value	Unit
$V_S$	60	V	$\omega_{z1}$	4.4	krad/s
$L$	210	$\mu\text{H}$	$\omega_{z2}$	8.8	krad/s
$R_l$	2	$\Omega$	$\omega_{p1}$	314	krad/s
$C$	47	$\mu\text{F}$	$\omega_{p2}$	6.89	Mrad/s
$r_c$	3.1	$m\Omega$	$\omega_s$	628.3	krad/s
$k_u(\text{VRC})$	50	rad/s	$f_s$	100	kHz
$k_u(\text{CRC})$	550	rad/s			

TABLE III  
PV MODULE PARAMETERS (MSX120) [32]

Parameter	Value	Unit
$P_{\text{Max}}$	120	W
$V_{\text{oc}}$	42.1	V
$I_{\text{sc}}$	3.87	A
$V_{\text{mpp}}$	33.7	V
$I_{\text{mpp}}$	3.56	A

Also, the value for  $K_4(s)$  becomes unity since

$$k_{ri} + k_{rv}R_L = -V_{\text{op}}/I_{\text{op}}^2 + \frac{1}{I_{\text{op}}} \frac{V_{\text{op}}}{I_{\text{op}}} = 0. \quad (55)$$

In addition, this result also confirms the ability of the RS reference generator to nullify the effect of variations in operating points in an SAS.

#### IV. PERFORMANCE ANALYSIS

This section evaluates the four SAS hardware structures discussed in Section III under varying operating point conditions. In addition, both the frequency- and time-domain analysis is carried out, thereby justifying the theoretical results observed in the small-signal models.

##### A. Frequency-Domain Analysis

Each SAS structure is arranged as shown in Figs. 7 and 9–11 to evaluate the SAS in the frequency domain. In addition, Tables II and III show the design parameters for the buck converter and PV panel specifications, respectively. The approximate  $I$ – $V$  curve using the proposed super-elliptical method in Section II is shown in Fig. 12 indicating both  $V_{\text{oc}}$  and  $I_{\text{sc}}$  based on the PV specifications for MSK120.

Three different load resistances, 7  $\Omega$ , 11  $\Omega$ , and 20  $\Omega$ , are chosen to evaluate the stability of the system in the CSS, MPP, and VSS, respectively. Under each condition, the inner loop gains  $T_v(s)$ ,  $T_i(s)$  and the overall loop gain  $T_B(s)$

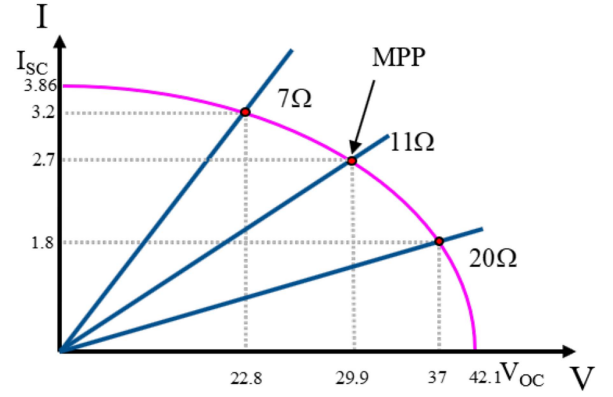


Fig. 12. Operating point and load resistance set-up for verification on the approximate PV curve for MSX120.

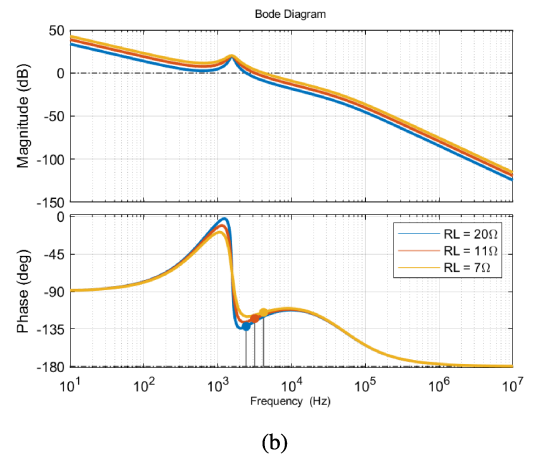
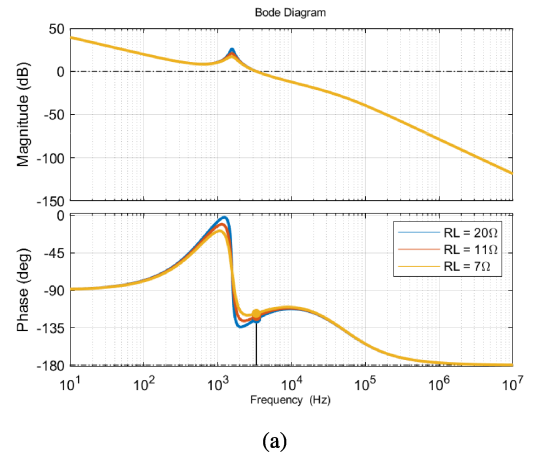


Fig. 13. Bode diagrams of the inner loop gain. (a)  $T_v(s)$  in VRC. (b)  $T_i(s)$  in CRC.

are evaluated, and the simulation results are shown in both Figs. 13 and 14.

In the CS-VRC structure, the operating point shifts toward the CSS with a decrease in the load resistance, resulting in the increase in both the loop gain and gain cross-over frequency. Therefore, a significant loss in the phase margin is observed, as shown in Fig. 14(a). Comparatively to this, under the RS-VRC hardware structure shown in Fig. 14(c), the loop gain change is quite insignificant for the three load resistances.

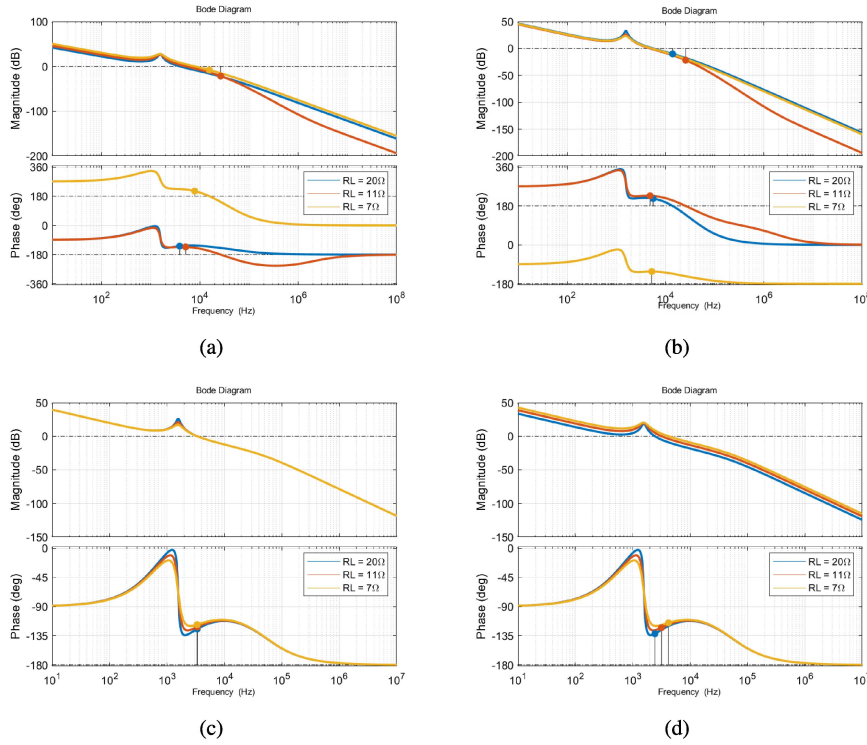


Fig. 14. Bode diagrams of the overall loop gain  $T_B(s)$ . (a) CS-VRC. (b) VS-CRC. (c) RS-VRC. (d) RS-CRC.

TABLE IV  
SIMULATION RESULTS

Operating point	Current segment		MPP		Voltage segment	
	Overshoot (V)	Settling time (ms)	Overshoot (V)	Settling time (ms)	Overshoot (V)	Settling time (ms)
CSVRC	1.9*	2.2	1.3*	0.7	0.2*	0.4
RSVRC	0*	0.9	0*	1.0	0*	0.4
VSCRC	0.8	0.3	1.5	0.8	10	9.3
RSCRC	0.5	0.3	0.3	0.9	0.8	1.8

\* = Undershoot

The loop characteristics of CRC are more load-dependent than VRC based on simulation results in Fig. 14(b) and (d). However, RS-CRC is far less sensitive when compared with VS-CRC, thus making the overall loop gain behave in a similar fashion described in Fig. 13(b).

**B. Time-Domain Analysis**

The time-domain analysis of these SAS configurations is carried out on PSIM by using the average buck converter models shown in Fig. 15. Two load resistances are connected in parallel to give the desired load disturbance to simulate results accurately. Furthermore, the load resistances are adjusted by approximately 40% in both directions at each operating point. The overall step-response waveform is illustrated in Fig. 16.

Different load tests are carried out since CRC, and VRC hardware structures become load-dependent at VSS and CSS.

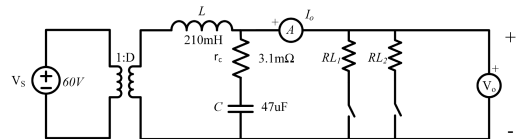


Fig. 15. Average buck converter model.

The step-down load test is performed in VRC, while the step-up load test is carried out in CRC. The simulated results under step-load changes are shown and marked in Fig. 16. In addition, a summarized result of the dynamic performance of the SAS system under varying operating points is shown in Fig. 17 and Table IV.

According to the small-signal analysis in Section III, the VRC system is expected to have a small phase margin at a low resistive

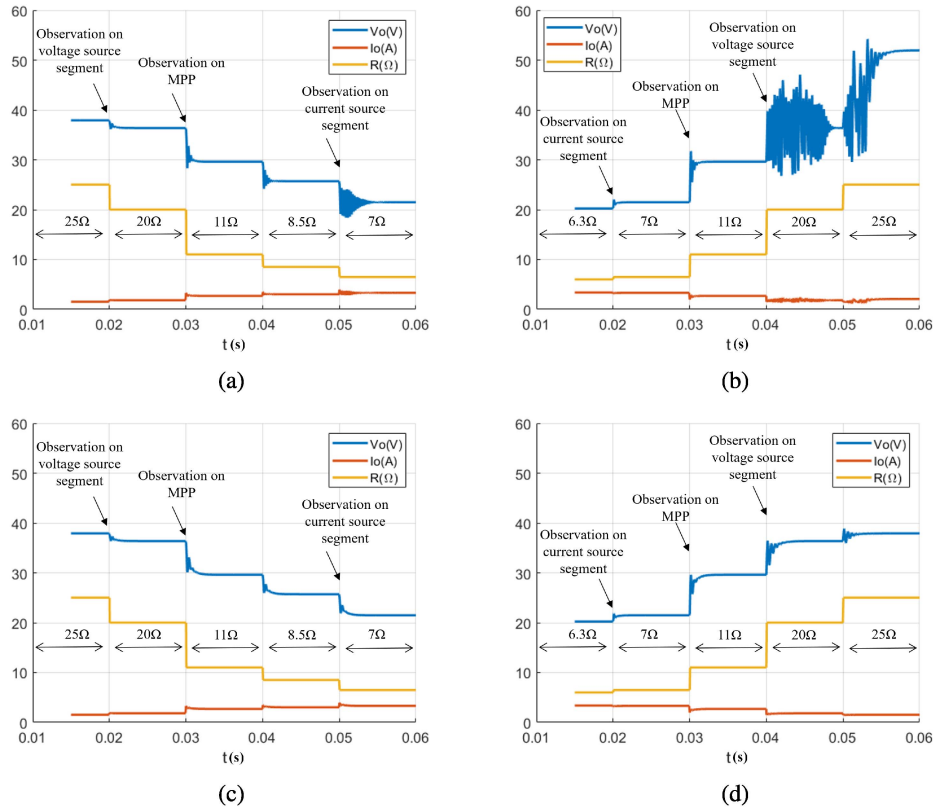


Fig. 16. Step load response for the different configurations used. (a) CS-VRC. (b) VS-CRC. (c) RS-VRC. (d) RS-CRC.

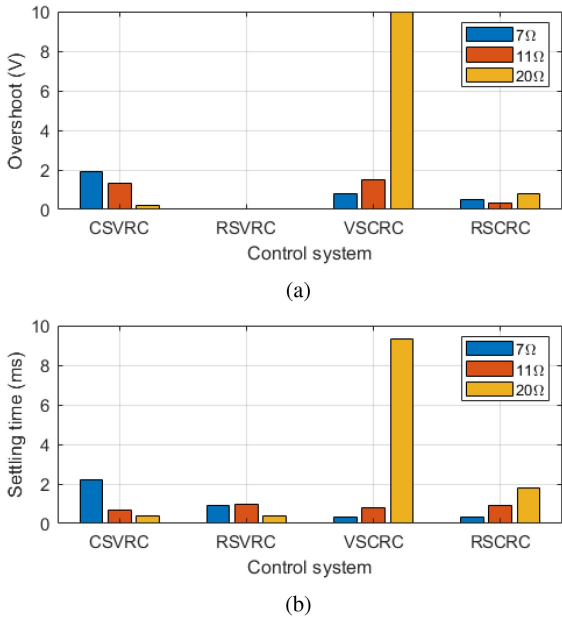


Fig. 17. Simulation results. (a) Overshoot. (b) Settling time.

load. In accordance with this prediction, in the CS-VRC system shown in Fig. 15(a), as the load decreases from  $20\ \Omega$  to  $7\ \Omega$ , the settling time is increased from 0.27 to 2.1 ms, and the phase margin is reduced, resulting in an undershoot in the output. The system shows underdamped oscillations in the condition of low resistance since the phase margin is not sufficient.

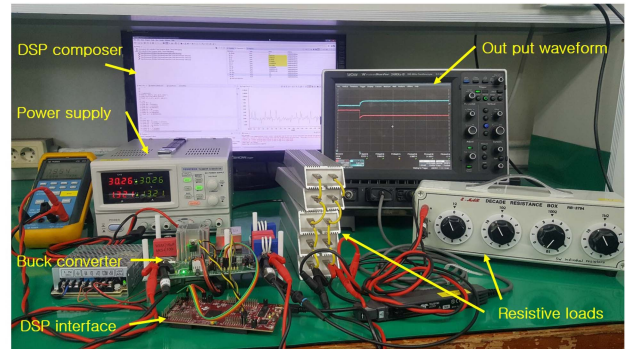


Fig. 18. Hardware setup of SAS.

Whereas, the response of the RS-VRC system illustrated in Fig. 15(c) shows that regardless of different operating points, the settling time changes only slightly from 0.3 to 0.9 ms without severe oscillations. This tendency matches well with the expected results indicating the operating point insensitivity of the RS-VRC configuration mentioned in Section III-D.

Similarly, VS-CRC and RS-CRC systems are compared to demonstrate theoretical predictions established in the small-signal modeling. In this case, the load resistance is tested in ascending order from  $7\ \Omega$  to  $20\ \Omega$ , considering a more stable operation in VSS. In addition, Fig. 15(b) and (d) shows that the output response is the same under the VRC hardware structure. According to the duality between RS-CRC and VS-CRC configurations, the system stability deteriorates at high load resistance,

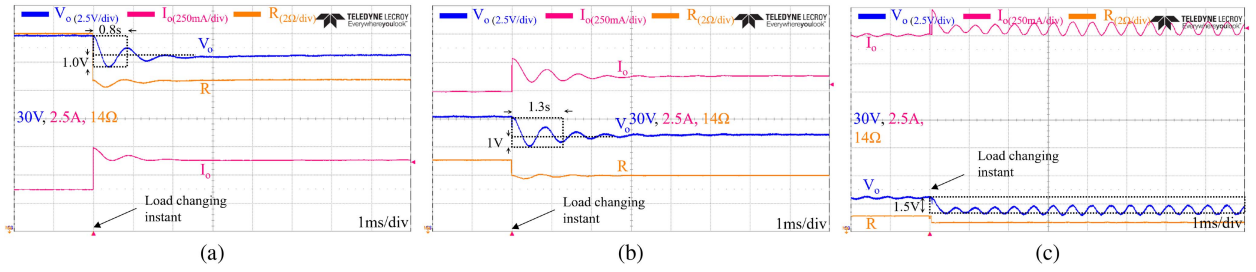


Fig. 19. Step response of the CS-VRC hardware prototype. (a)  $20\ \Omega \rightarrow 15\ \Omega$ . (b)  $11\ \Omega \rightarrow 10\ \Omega$ . (c)  $7\ \Omega \rightarrow 6.3\ \Omega$ .

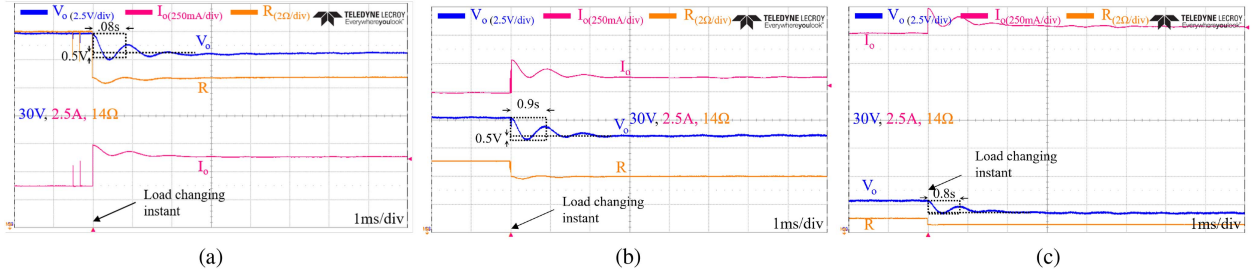


Fig. 20. Step response of the RS-VRC hardware prototype. (a)  $20\ \Omega \rightarrow 15\ \Omega$ . (b)  $11\ \Omega \rightarrow 10\ \Omega$ . (c)  $7\ \Omega \rightarrow 6.3\ \Omega$ .

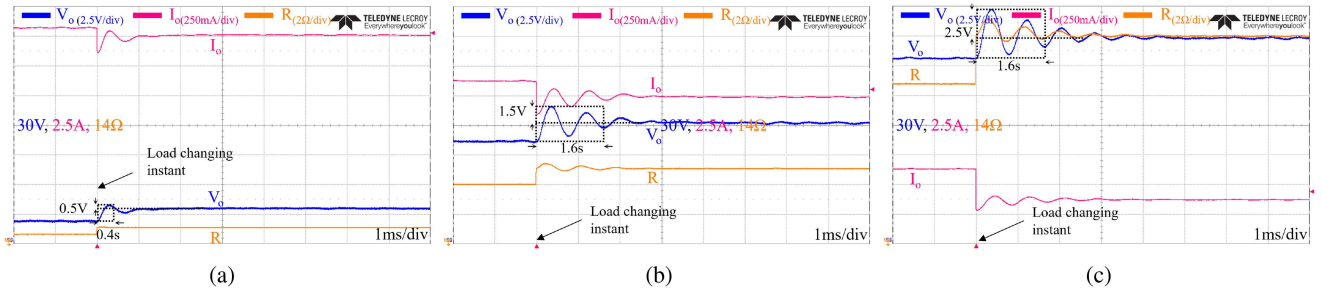


Fig. 21. Step response of the VS-CRC hardware prototype. (a)  $6.3\ \Omega \rightarrow 7\ \Omega$ . (b)  $10\ \Omega \rightarrow 11\ \Omega$ . (c)  $15\ \Omega \rightarrow 20\ \Omega$ .

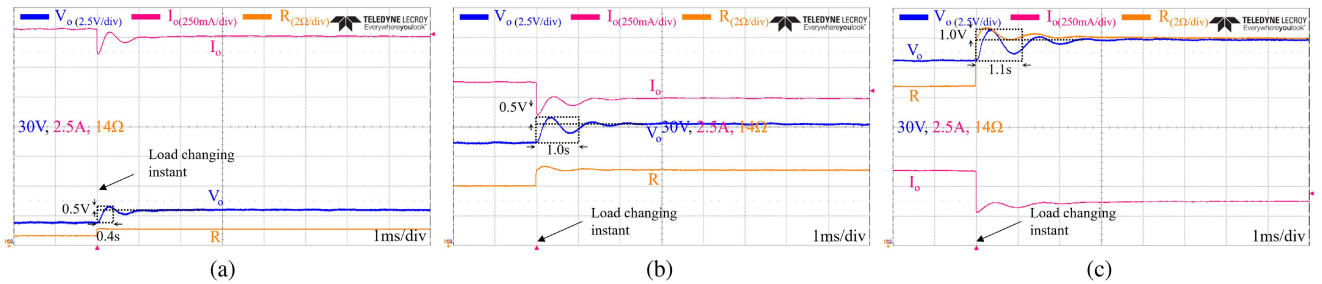


Fig. 22. Step response of the RS-CRC hardware prototype. (a)  $6.3\ \Omega \rightarrow 7\ \Omega$ . (b)  $10\ \Omega \rightarrow 11\ \Omega$ . (c)  $15\ \Omega \rightarrow 20\ \Omega$ .

and RS-CRC is less sensitive to changes in the operating point than VS-CRC.

Despite RS-CRC showing similar trends to RS-VRC, its dynamic response is relatively sensitive to the operating point variations because the power stage transfer function has load-dependent dc-gain characteristics. Therefore, RS-VRC appears to be the best configuration in terms of load-independent dynamic characteristics. This confirms the validity of the comparison based on the small-signal analysis presented in this study.

## V. EXPERIMENTAL VERIFICATION

Fig. 18 shows the setup for the hardware verification of the SAS control structures. The SAS is made up of a buck converter incorporated with a TMS320F28379D DSP controller. Variable load resistances are also connected in parallel with the SAS system for step load change to verify the same scenarios. Figs. 19–22 and Table V show the experimental results obtained.

The settling time in the CS-VRC hardware structure fluctuates as the undershoot becomes more prominent due to small

TABLE V  
HARDWARE RESULTS

Operating point System	Current segment		MPP		Voltage segment	
	Overshoot (V)	Settling time (ms)	Overshoot (V)	Settling time (ms)	Overshoot (V)	Settling time (ms)
CSVRC	1.5*	oscillatory	1*	1.3	1.0*	0.8
RSVRC	0*	0.8	0.5*	0.9	0.5*	0.8
VSCRC	0.5	0.4	1.5	1.6	2.5	1.6
RSCRC	0.5	0.4	0.5	1.0	1.0	1.1

\*\* = Undershoot

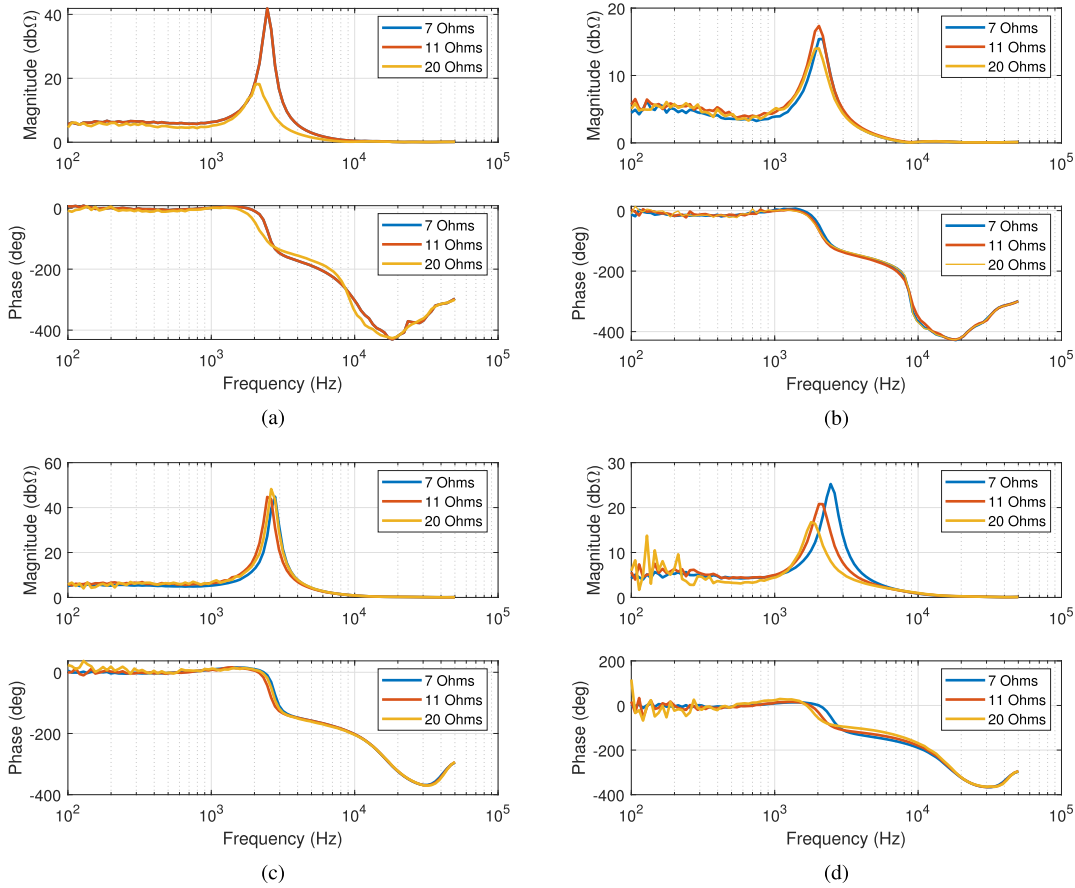


Fig. 23. Measured output impedance of the hardware prototypes. (a) CS-VRC. (b) VS-CRC. (c) RS-VRC. (d) RS-CRC.

load resistance. This underdamped oscillation becomes very pronounced for the  $7\ \Omega$ , as shown in Fig. 19. In addition, the RS-VRC hardware system has a minimal undershoot with an almost constant settling time, as shown in Fig. 20. Thus proving that CSS is the worst-case scenario for a CS-VRC, while the stability of CS-VRC structures is load-dependent, the RS-VRC shows an almost constant dynamic response under varying load conditions.

Furthermore, the CRC hardware structures shown in Figs. 21 and 22 also show similar behavior as discussed in Section IV-B. The experiment starts from a low resistance load ( $7\ \Omega$ ) to a very

high-resistance load ( $20\ \Omega$ ). Low overshoot and settling time were observed at low resistance, while very high overshoot and settling time was observed at high resistance.

Therefore, this confirms that RS-CRC structures can suppress the effect of performance degradation caused by a change in operating point. However, RS-CRC is slightly sensitive to operating point change when compared with RS-VRC hardware structures. Hence, both the simulation and experimental verification confirm the small-signal analysis results.

Fig. 23 shows the output impedance characteristics of the SAS measured by the network analyzer (Ridley Engineering,

TABLE VI  
COMPARISON OF MODEL ACCURACY

PV module	PV model	$P_{mpp}$ (W)	Error %	$I_{mpp}$ (A)	Error %	$V_{mpp}$ (V)	Error %
MSX 120	Datasheet	120		3.56		33.7	
	Single-diode model	121.45	1.21	3.45	3.19	35.2	-4.26
	Super elliptical model ( $n = 4.9$ )	122.78	2.32	3.35	6.27	36.6	-7.92
KC 65GT	Datasheet	65		3.75		17.4	
	Single-diode model	65.95	1.46	3.6	4.17	18.3	-4.92
	Super elliptical model ( $n = 5.6$ )	67.6	4	3.52	6.53	19.2	-9.37
KC 200GT	Datasheet	200		7.61		26.3	
	Single-diode model	203	1.5	7.33	3.82	27.7	-5.05
	Super elliptical model ( $n = 5.1$ )	205.81	2.90	7.15	6.43	28.8	-8.68
SQ 160-PC	Datasheet	160		4.58		35	
	Single-diode model	162.01	1.26	4.43	3.39	36.6	-4.37
	Super elliptical model ( $n = 5.4$ )	164.89	3.06	4.31	6.26	38.3	-8.62

AP300). It is observed that the phase of the output impedance is not always within  $\pm 90^\circ$ , which is different from a real PV generator always exhibiting passive behavior [33]. However, every impedance shows a purely resistive in its low-frequency region like a real PV generator, which indicates that with an appropriate input filter design with damping, system interconnection issue can be avoided considering minor loop gain analysis suggested by [34]. It should be noted that the system interaction issue is yet to be discussed in this paper and thus will be our future work.

## VI. CONCLUSION

In this study, the small-signal modeling and stability analysis of SAS was examined using the multiloop analysis technique. The super-elliptical method was proposed as a fast and straightforward method for approximating the  $I-V$  curve to simplify the  $I-V$  characteristic equation. It was also shown that SAS is a multiloop system consisting of an inner control loop and reference generator loop and the overall loop gain is heavily dependent on the operating point due to the interactions between these two loops. For a use case of the approximate analysis, four SAS hardware structures are examined and compared to investigate the effect of the operating point variation on the dynamic performance, which shows the RS-VRC hardware structure more robust and insensitive to load fluctuations. In conclusion, the proposed approach is expected to be very helpful in improving the control and performance of SAS systems.

### APPENDIX A

#### ACCURACY OF SUPER-ELLIPTICAL APPROXIMATION FOR PV CURVE

Fig. 24 illustrates the  $I-V$  and  $P-V$  curves to validate the feasibility of the super-elliptical model. The results confirm that

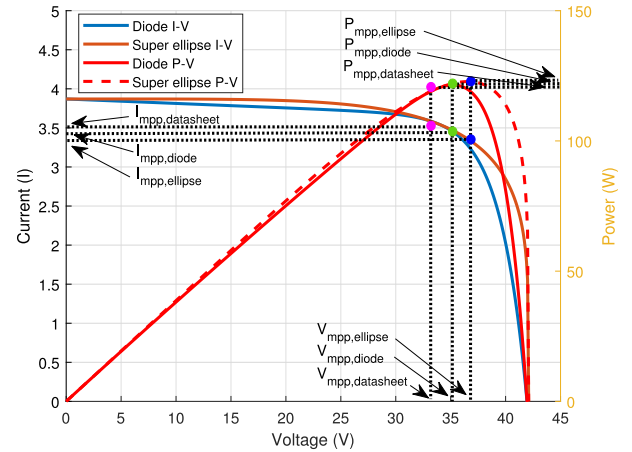


Fig. 24. PV characteristic curves under different PV models.

super-elliptical approximation is almost as accurate as of the single-diode model.

To prove the PV model accuracy quantitatively, Table VI summarizes the accuracy of two different PV models for four commercial PV panels, compared with datasheet values in terms of PV curve parameters. Even though the super-elliptical model has a slightly higher error of 4%, than the diode model, it is quite acceptable for the analysis of SAS.

## REFERENCES

- [1] S. E. I. Remache, A. Y. Cherif, and K. Barra, "Optimal cascaded predictive control for photovoltaic systems: Application based on predictive emulator," *IET Renewable Power Gener.*, vol. 13, no. 15, pp. 2740–2751, 2019.
- [2] L. P. Sampaio and S. A. O. da Silva, "Graphic computational platform integrated with an electronic emulator dedicated to photovoltaic systems teaching," *IET Power Electron.*, vol. 10, no. 14, pp. 1982–1992, 2017.

- [3] A. Koran, T. LaBella, and J.-S. Lai, "High efficiency photovoltaic source simulator with fast response time for solar power conditioning systems evaluation," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1285–1297, Mar. 2014.
- [4] S. Jin, D. Zhang, Z. Bao, and X. Liu, "High dynamic performance solar array simulator based on a SiC MOSFET linear power stage," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1682–1695, Feb. 2018.
- [5] S. Jin, D. Zhang, C. Wang, and Y. Gu, "Optimized design of space solar array simulator with novel three-port linear power composite transistor based on multiple cascaded SiC-JFETs," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 4691–4701, Jun. 2018.
- [6] W. Zhang and J. W. Kimball, "DC–DC converter based photovoltaic simulator with a double current mode controller," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5860–5868, Jul. 2018.
- [7] A. F. Cupertino, H. A. Pereira, and V. F. Mendes, "Modeling, design and control of a solar array simulator based on two-stage converters," *J. Control, Autom. Elect. Syst.*, vol. 28, no. 5, pp. 585–596, 2017.
- [8] A. N. Ali, K. Premkumar, M. Vishnupriya, B. Manikandan, and T. Thamizhselvan, "Design and development of realistic PV emulator adaptable to the maximum power point tracking algorithm and battery charging controller," *Sol. Energy*, vol. 220, pp. 473–490, 2021.
- [9] M. Chaker et al., "Development of a PV emulator using SMPS converter and a model selection mechanism for characteristic generation," *Sol. Energy*, vol. 239, pp. 117–128, 2022.
- [10] S. Esfandiari, M. A. L. Khaniki, S. H. Montazeri, and J. Milimonfared, "Performance improvement of photovoltaic emulator using lambert W model and fractional order PI controller," in *Proc. 12th Power Electron. Drive Syst. Technol. Conf.*, 2021, pp. 1–5.
- [11] R. Job and C. W. Tan, "Rapid prototyping of photovoltaic emulator using buck converter based on fast convergence resistance feedback method," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8715–8723, Sep. 2019.
- [12] I. D. G. Jayawardana, C. N. M. Ho, M. Pokharel, and G. E. Valderrama, "A fast-dynamic control scheme for a power-electronics-based PV emulator," *IEEE J. Photovolt.*, vol. 11, no. 2, pp. 485–495, Mar. 2021.
- [13] M. Alaoui, H. Maker, and A. Mouhsen, "An accurate photovoltaic source emulator with high-bandwidth using a backstepping controller," in *Proc. 4th World Conf. Complex Syst.*, 2019, pp. 1–6.
- [14] A. Boucharef, A. Tahri, F. Tahri, S. Silvestre, and M. Bourahla, "Solar module emulator based on a low-cost microcontroller," *Measurement*, vol. 187, 2022, Art. no. 110275.
- [15] D. Subhi and R. Thabit, "A new low cost solar array emulator based on fuzzy and 32-bit microcontroller," *Int. J. Sci. Eng. Investigations*, vol. 9, no. 101, pp. 63–69, 2020.
- [16] S. Gadelovits, M. Sitbon, and A. Kuperman, "Rapid prototyping of a low-cost solar array simulator using an off-the-shelf DC power supply," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5278–5284, Oct. 2014.
- [17] M. Farahani, M. A. Shamsi-nejad, and H. R. Najafi, "Design and construction of a digital solar array simulator with fast dynamics and high performance," *Sol. Energy*, vol. 196, pp. 319–326, 2020.
- [18] S. Jenkal, M. Kourchi, A. Rachdy, O. Oussalem, M. Ajaamoum, and M. Oubella, "Modeling a photovoltaic emulator using four methods and buck-boost converter," *Eng. Lett.*, vol. 29, no. 2, pp. 1–8, 2021.
- [19] S. Jin, D. Zhang, and C. Wang, "UI-RI hybrid lookup table method with high linearity and high-speed convergence performance for FPGA-based space solar array simulator," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 7178–7192, Aug. 2018.
- [20] U. K. Shinde, S. G. Kadwane, R. K. Keshri, and S. Gawande, "Dual mode controller-based solar photovoltaic simulator for true PV characteristics," *Can. J. Elect. Comput. Eng.*, vol. 40, no. 3, pp. 237–245, 2017.
- [21] Y. Li, T. Lee, F. Z. Peng, and D. Liu, "A hybrid control strategy for photovoltaic simulator," in *Proc. 24th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2009, pp. 899–903.
- [22] "Lambert w-function based exact representation for double diode model of solar cells: Comparison on fitness and parameter extraction," *Energy Convers. Manage.*, vol. 127, pp. 443–460, 2016.
- [23] E. I. Batzelis, I. A. Routsolias, and S. A. Papathanassiou, "An explicit PV string model based on the lambert  $w$  function and simplified MPP expressions for operation under partial shading," *IEEE Trans. Sustain. Energy*, vol. 5, no. 1, pp. 301–312, Jan. 2014.
- [24] B. H. Cho, J. R. Lee, and F. C. Lee, "Large-signal stability analysis of spacecraft power processing systems," *IEEE Trans. Power Electron.*, vol. 5, no. 1, pp. 110–116, Jan. 1990.
- [25] B. Choi, *Pulsewidth Modulated DC-to-DC Power Conversion: Circuits, Dynamics, and Control Designs*. Hoboken, NJ, USA: Wiley, 2013.
- [26] J. Lee, H. Bae, and B.-H. Cho, "Resistive control for a photovoltaic battery charging system using a microcontroller," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2767–2775, Jul. 2008.
- [27] H. Bae, J. Lee, S. Park, and B. H. Cho, "Large-signal stability analysis of solar array power system," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 44, no. 2, pp. 538–547, Apr. 2008.
- [28] J. Lee, H. Bae, S. Park, and B. H. Cho, "Constant resistance control of solar array regulator using average current mode control," in *Proc. 21st Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2006, pp. 1544–1548.
- [29] H. Bae, S. Park, J. Lee, B. H. Cho, and S. Jang, "Digital control of the parallel interleaved solar array regulator using the digital signal processor," in *Proc. 37th IEEE Power Electron. Specialists Conf.*, 2006, pp. 1–5.
- [30] B. Cho and F. Lee, "Modeling and analysis of spacecraft power systems," *IEEE Trans. Power Electron.*, vol. 3, no. 1, pp. 44–54, Jan. 1988.
- [31] B. Cho and F. C. Lee, "Measurement of loop gain with the digital modulator," *IEEE Trans. Power Electron.*, vol. PE-1, no. 1, pp. 55–62, Jan. 1986.
- [32] W. Hayder, A. Abid, M. Ben Hamed, E. Ogliari, and L. Sbita, "Comparison of MPPT methods FLC & PSO for PV system under variable irradiance and temperature," in *Proc. 18th Int. Multi-Conf. Syst. Signals Devices*, 2021, pp. 1247–1251.
- [33] L. Nousiainen et al., "Photovoltaic generator as an input source for power electronic converters," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 3028–3038, Jun. 2013.
- [34] R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, 1976, pp. 366–382.



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