Sampled-Data Modeling and Stability Analysis of Digitally Controlled Buck Converter With Trailing-Edge and Leading-Edge Modulations

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***Abstract*—For a digitally controlled dc–dc converter with leading-edge modulation or trailing-edge modulation, due to the delay and different sampled points, its nonlinear behavior and the magnitude-phase response in high frequency and low frequency cannot be accurately depicted by the averaged modeling method, but can be predicted by the sampled-data modeling method. However, the conventional sampled-data model is usually more complicated and less intuitive, which is not conducive to the presentation of physical meaning and the design of the controller for the converter. Based on the reasonable approximation of the sampled-data model, this article proposes a second-order global equivalent circuit for the buck converter with different modulations. Meanwhile, the small-signal model in the z-domain based on the equivalent circuit is derived. Using the proposed equivalent circuit, the detailed operating waveform of the switching circuit of dynamic and stable state can be predicted without considering the ripple ratio of the state variables and the stability boundaries of various parameters of the system can be accurately analyzed, including the parasitic parameters. Furthermore, based on the stability analysis of the controller parameters, a proportional-integral-derivative controller is designed to verify the stability difference between the two modulation modes when the load steps. Finally, a prototype of the buck converter was constructed to verify the effectiveness of the model and theoretical analysis.**

***Index Terms*—Digitally controlled buck converter, equivalent circuit, leading-edge modulation (LEM), sampled-data model, small-signal model, stability, trailing-edge modulation (TEM), z-domain.**

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I. Introduction

PULSEWIDTH modulation (PWM) has been widely used in dc–dc converters [1]. It generates the duty ratio to control the power transmission of the converter by comparing the control signal with the triangular carrier in each cycle. According to the triangle carrier shown in Fig. 1, PWM can be set to leading-edge modulation (LEM) or trailing-edge modulation (TEM) [2], which are widely used in dc–dc converters. In fact, the modulation mode of analog peak current control is essentially the TEM. In addition, the minimum phase response of the analog controlled boost and flyback converters can be realized by using the LEM [3]. In cascaded converters, the LEM and TEM are usually used together to reduce the inductor current ripple and improve the efficiency [4], [5]. Therefore, it is very important to study the influence of different PWM on the converter.

With the continuous development and maturity of digital signal processing (DSP) technology, its superiority has become increasingly prominent. Compared with the traditional analog control, the signal in digital control will not be distorted by the change of component performance and environment, and the anti-interference ability of the digital system is much stronger. In addition, more complex nonlinear control strategies can be achieved by flexibly programming in the digital system, which can lead to making the power converters tend to be more robust, intelligent and versatile [6], meanwhile, the circuits of the control part could be simplified and low cost. But due to the influence of the quantization processing link and the sample-and-hold link as well as the delay characteristics of the software [7], [8], the digital control system will show a different nonlinear dynamic behavior from the analog control system. In general, due to the influence of the total loop delay, the parameter stability range of the digital control system is smaller than that of the analog control for the same power stage circuit [9], [10]. If the system is instable, the output voltage and current may oscillate and cause disorder and failure of the circuit operation [11], [12]. Therefore, it is necessary to establish an accurate mathematical model of the digital control system and conduct research on its stability.

The averaged model is currently the most widely used modeling method for power converters [13], [14]. It focuses on the impact of low-frequency perturbation on the dynamic performance of the system [15], [16]. Therefore, the averaged modeling

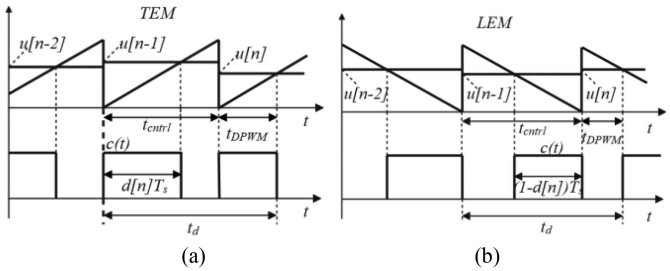


Fig. 1. Timing diagram of different modulations based on digital control. (a) TEM. (b) LEM.

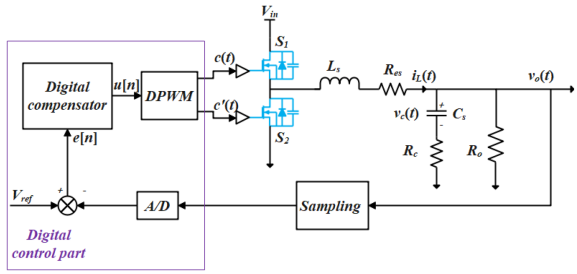


Fig. 2. Digitally controlled voltage-mode synchronous buck converter.

method can be used to build the averaged equivalent circuit of the system by averaging the high-frequency switching components, which is intuitive and easy to analyze. However, the accuracy of the averaged modeling approach depends on the suppression degree of the nonfundamental components in the duty cycle. Besides, it also cannot effectively reflect the loop delay. Then, the averaged model considering the delay link is proposed to model the digital control system. However, the characteristics of the model still deviate from the actual system in amplitude and phase response at high frequency [17]. The literature [18] uses the z-domain model converted by an averaged model to analyze and verify the stability range of the digitally controlled buck converter, but it neither proposes a large signal model with physical meaning nor analyzes the frequency characteristic of the small-signal model.

The sampled-data model has gradually become the main modeling method of digitally controlled systems because its modeling method is suitable for describing digitally controlled characteristics [6], [17]–[21], therefore, the corresponding model is more realistic and accurate. By using the sampled-data modeling approach, the state variables are not averaged, so precise state transition characteristics can be obtained at the sampling point [22], [23]. The literature [24]–[26] uses the sampled-data model to study the stability and bifurcation behavior of dc–dc converters. The literature [24] uses the sampled-data model to analyze the stability of the single-inductor dual-output buck converter. The literature [25] describes the period-doubling bifurcation phenomenon of the buck converter through the sampled-data model. The literature [26] analyzes the bifurcation and chaos characteristics of analog controlled buck converter by using the discrete-time model. The literature [27]–[29] pays more attention to the influence of different modulations on dc–dc converters. The literature [27] uses the sampled-data model to find the minimum phase condition for digitally controlled boost and flyback converters. The literature [28] uses the discrete-time model to analyze the dynamic characteristics of the V^2-controlled buck converter with LEM and TEM. The literature [29] derives the z-domain transfer functions in different modulations based on the sampled-data model and makes a first-order approximation to obtain the corresponding analytic models. However, the derivation process of the conventional sampled-data model (CSDM) is very complicated and the analysis of the model usually relies on numerical calculation instead of an equivalent circuit so that the physical meaning is not clear.

So far, intuitive and accurate large-signal equivalent circuit models are rarely reported in the research of digital-pulsewidth-modulated (DPWM) dc–dc converters. In this article, a second-order global equivalent circuits (SOGECs) of digital controlled synchronous buck converter operating in continuous-current mode (CCM) for different modulation methods are established. By improving the conventional sampled-data modeling method proposed in the literature [26], both the mathematical model and equivalent circuit are built by merging the two switching states of each cycle into one state in the detailed switching circuit, which can overcome the contradiction between the accuracy and intuitiveness of the existing model. The proposed modeling method effectively reflects the influence of the LEM and the TEM on the system and provides an accurate representation of the output voltage and inductor current at the sampling point. Thereafter, considering the control delay t_{cntrl} and the modulation delay t_{DPWM}, the small-signal model of control-output in z-domain is derived. Furthermore, the magnitude and phase responses, respectively, obtained by the small-signal model from the proposed method and the experiment are compared to verify the accuracy of the model. In addition, the method for analyzing the stability of the system by using the equivalent circuit is given, and the theoretical range of parameters of proportional-integral-derivative (PID) control that can stabilize the digitally controlled buck converter is further derived. On this basis, the case that the stability boundary varies with the duty cycle under two different modulations is studied, and the nature of the effect of the modulation on the system is revealed. Then, the influence of certain circuit parameters on system stability is explored, including the input voltage, the load, the output capacitor, the inductor, and the parasitic parameters. Comparing the stability boundaries of these parameters under different models, the simplicity and accuracy of the global equivalent circuit proposed in this article are proved. Furthermore, the controller is designed based on an open-loop transfer function, whose effectiveness is verified by comparing the settling time and overshoot voltage of the two different modulations when load steps. Finally, the correctness and effectiveness of the theoretical analysis are verified by a simulating and an experimental platform respectively.

The rest of this article is organized as follows. In Section II, the SOGEC of the buck converter for both LEM and TEM are derived based on the improved modeling approach. The delay characteristics of the digitally controlled buck converter are explored, and the z-domain transfer function based on the

SOGEC is given in Section III. In Section IV, the stability range of the control parameters is discussed and the influence of loop parameters and different modulations on system stability is analyzed. In Section V, the PI controller is designed based on the critical stable boundary theory discussed in Section IV. Finally, a series of experiments are used to verify the accuracy of the model and the validity of the theoretical analysis. Finally, Section VII concludes this article.

II. SOGEC Based on Improved Sampled-Data Approach of Synchronous Buck Converter

A. Operating Principle of Synchronous Buck Converter

The voltage-mode DPWM synchronous buck converter is shown in Fig. 2, which is composed of the main power stage and the digital control loop. The main power stage comprises the input voltage V_{in}, the main switch S_1 and the rectifier switch S_2, the inductor L_s, the output load resistor R_o, and the capacitor C_s. $i_L(t)$ is the current flowing through the inductor L_s, the output voltage and the voltage across the capacitor C_s are $v_o(t)$ and $v_c(t)$, respectively. d is the duty cycle. The digital control loop includes the analog to digital conversion (A/D) conversion module, digital compensation module and DPWM module. The A/D conversion module will sample $v_o(t)$ at the sampling rate of switching frequency f_s. The discrete error signal $e[n]$ is obtained by the difference between the sampled output voltage $v_o[n]$ and the reference voltage V_{ref}. $e[n]$ is processed by a discrete-time compensator which outputs the control signal $u[n]$. Thereafter, $u[n]$ generates the pulse signal $c(t)$ via the DPWM to control S_1 and S_2.

It is assumed that the synchronous buck converter operating in continuous-conduction mode (CCM). The converter of two switching states in each switching period can be described by the following linear, time-invariant state-space equation:

$$\begin{cases} \frac{dx(t)}{dt} = \mathbf{A}_j\, x(t) + \mathbf{B}_j V_{\text{in}} \\ y\,(t) \;\; = \mathbf{C}_j\, x(t) \end{cases} \tag{1}$$

where $x(t)$ represents the state variables (i.e., $x\ (t) = (\,i_L(t)\ v_c(t)\,)^T$), $y(t)$ is the output voltage $v_o(t)$. $\mathbf{A}_j$, $\mathbf{B}_j$, and $\mathbf{C}_j$ are the system state matrix, input matrix, and output matrix, respectively. The subscript j represents the jth switching state. The equivalent resistance R_c in series with the capacitor and the equivalent resistance R_{es} in series with the inductor are also considered in the model. Therefore, the state matrix ($\mathbf{A}_1$, $\mathbf{A}_2$), input matrix ($\mathbf{B}_1$, $\mathbf{B}_2$), and output matrix ($\mathbf{C}_1$, $\mathbf{C}_2$) of the two switching states of the buck converter are obtained as follows, respectively:

$$\begin{cases} \mathbf{A}_1 = \mathbf{A}_2 \;= \begin{pmatrix} \frac{-R_{\text{es}} - \frac{R_c R_o}{R_c+R_o}}{L_s} & \frac{-R_o}{(R_o+R_c)L_s} \\ \frac{R_o}{(R_o+R_c)C_s} & \frac{-1}{(R_o+R_c)C_s} \end{pmatrix} \\ \mathbf{B}_1 = \begin{pmatrix} \frac{1}{L_s} \\ 0 \end{pmatrix},\ \mathbf{B}_2 = \begin{pmatrix} 0 \\ 0 \end{pmatrix} \\ \mathbf{C}_1 = \mathbf{C}_2 \;= \begin{pmatrix} \frac{R_c R_o}{R_c+R_o} & \frac{R_o}{R_c+R_o} \end{pmatrix} \end{cases}. \tag{2}$$

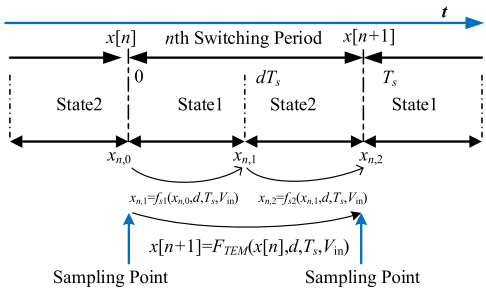


Fig. 3. Iterative relationship of the state variable with TEM for the sampled-data modeling method.

B. CSDM of Buck Converter

The differential equations corresponding to each substate in (1) are solved in a cycle, and the following equation is obtained:

$$\begin{cases} x(t_0+dt) \;\; = e^{\boldsymbol{A}_1 dt}\, x\,(t_0) + \int_{t_0}^{t_0+dt} e^{\boldsymbol{A}_1 \tau} d\tau \mathbf{B}_1 V_{\text{in}} \\ x\,(t+t_0) \;\; = e^{\boldsymbol{A}_2 (1-d)t}\, x\,(t_0+dt) + \int_{t_0+dt}^{t+t_0} e^{\boldsymbol{A}_2 \tau} d\tau \mathbf{B}_2 V_{\text{in}} \end{cases} \tag{3}$$

where t_0 is the initial time of a cycle. The relationship of the state variable from t_0 to $t+t_0$ can be obtained by iterating the two substates of (3), as follows:

$$\begin{aligned} x\ (t+t_0) = {} & e^{\boldsymbol{A}_2 (1-d)t}\, e^{\boldsymbol{A}_1 dt} x\,(t_0) \\ & + e^{\boldsymbol{A}_2 (1-d)t} \int_{t_0}^{t_0+dt} e^{\boldsymbol{A}_1 \tau} d\tau \mathbf{B}_1 V_{\text{in}} \\ & + \int_{t_0+dt}^{t+t_0} e^{\boldsymbol{A}_2 \tau} d\tau \mathbf{B}_2 V_{\text{in}}. \end{aligned} \tag{4}$$

The iterative relationship of the state variable of a buck converter with TEM is illustrated, as shown in Fig. 3. t represents anytime from the beginning to the end of the cycle. In Fig. 3, $x_{n,0}$ represents the sample of the state variable in the nth switching cycle, which can be recorded as $x[n]$; $x_{n,2}$ represents the sample of the state variable in the $(n+1)$th switching cycle, which can be denoted as $x[n+1]$; $x_{n,1}$ represents the sample of the state variable when the control signal $u[n]$ intersects with the carrier waveform. According to the equal-period sampling characteristics of digital control, the continuous time from t_0 to time $t+t_0$ can be discretized into the time interval of equal period, which means t_0 and $t + t_0$ in (4) is denoted as nT_{s} and $(n+1)T_{\text{s}}$, respectively. Therefore, the state transition function $F(x[n]\ d,\ V_{\text{in}},\ T_s)$ for two consecutive sampling points can be obtained

$$\begin{aligned} x\ [n+1] &= F_{\text{TEM}}\ (x\,[n]\,,\ d,\ V_{\text{in}},\ T_s) \\ &= \mathbf{G}_{\text{TEM}}\, x\,[n] + \mathbf{H}_{\text{TEM}} V_{\text{in}} \end{aligned} \tag{5}$$

where

$$\begin{cases} \mathbf{G}_{\text{TEM}} = e^{\mathbf{A}_2 (1-d)T_s}\, e^{\mathbf{A}_1 dT_s} \\ \mathbf{H}_{\text{TEM}} = e^{\mathbf{A}_2 (1-d)T_s} \int_0^{dT_s} e^{\mathbf{A}_1 t} dt \mathbf{B}_1 + \int_0^{(1-d)T_s} e^{\mathbf{A}_2 t} dt \mathbf{B}_2 \end{cases}.$$

So, a set of differential equations describing the change of state variables in a cycle can be obtained

$$\begin{cases} x\ [n+1] = \mathbf{G}_{\text{TEM}}\, x\,[n] + \mathbf{H}_{\text{TEM}} V_{\text{in}} \\ y\ [n+1] = \mathbf{C}_2\, x\,[n] \end{cases} \tag{6}$$

where the output matrix for TEM is defined as $\mathbf{C}_2$. The switching order for trailing edge and LEMs of the dc–dc converter are opposite in one cycle. The output matrix for LEM is defined as $\mathbf{C}_1$. Therefore, a set of differential equations in a cycle for LEM can be obtained

$$\begin{cases} x\ [n+1] = \mathbf{G}_{\text{LEM}}\, x\,[n] + \mathbf{H}_{\text{LEM}} V_{\text{in}} \\ y\ [n+1] = \mathbf{C}_1\, x\,[n] \end{cases} \tag{7}$$

where

$$\begin{cases} \mathbf{G}_{\text{LEM}} = e^{\mathbf{A}_1(1-d)T_s}\ e^{\mathbf{A}_2 dT_s} \\ \mathbf{H}_{\text{LEM}} = e^{\mathbf{A}_1(1-d)T_s}\ \int_0^{dT_s} e^{\mathbf{A}_2 t} dt \mathbf{B}_2 + \int_0^{(1-d)T_s} e^{\mathbf{A}_1 t} dt \mathbf{B}_1 \end{cases}.$$

Since the output voltage of the buck converter is continuous, the output matrix should be equal in both trailing edge and LEMs

$$\mathbf{C}_1 = \mathbf{C}_2. \tag{8}$$

But for the boost converter, the output voltage is discontinuous. In the switching state that the capacitor is charged by the inductor current, the output voltage sampled by A/D is not only the output capacitor voltage but also a voltage step generated by the ac component of the inductor current through R_c. In another switching state, the inductor current no longer charges the capacitor, so the output voltage sampled by A/D can be approximated as the capacitor voltage. Therefore, it is not accurate to directly average the output matrix in the averaging model. The output matrix of the converter in which the output voltage is discontinuous should be calculated according to the position of the sampling point. Hence, the discrete-time model can describe the characteristics of the system more accurately.

C. Equivalent Circuit Based on Sampled-Data Modeling Method With TEM

The CSDM can accurately reflect the characteristic of the detailed switching circuit when the perturbation frequency of duty cycle d is lower than the Nyquist frequency since the Shannon's sampling theorem should be satisfied at this time [27]. However, the CSDM has some limitations. First, there are a large number of exponential matrix calculations in the model that cannot be avoided. Second, it does not have an intuitive equivalent circuit and the transfer function cannot be effectively deduced, consequently, the controller cannot be directly designed.

In order to obtain an intuitive equivalent circuit, while ensuring the accuracy of the model, this article uses an improved approximate method of the CSDM proposed in the literature [26] to derive the equivalent circuit of the buck converter. The state-space description is expressed as the following form for the equivalent circuit:

$$\begin{cases} \frac{dx(t)}{dt} = \mathbf{A}_{\text{eq,TEM}}\, x\,(t) + \mathbf{B}_{\text{eq,TEM}} V_{\text{in}} \\ y\,(t) = \mathbf{C}_{\text{eq,TEM}}\, x\,(t) \end{cases}. \tag{9}$$

Among them, $\mathbf{A}_{\text{eq,TEM}}$, $\mathbf{B}_{\text{eq,TEM}}$, and $\mathbf{C}_{\text{eq,TEM}}$ are the state matrix, input matrix, and output matrix of the equivalent circuit with TEM, respectively. Therefore, the state-space description of the equivalent circuit in the discrete domain can be simplified as shown in Fig. 4.

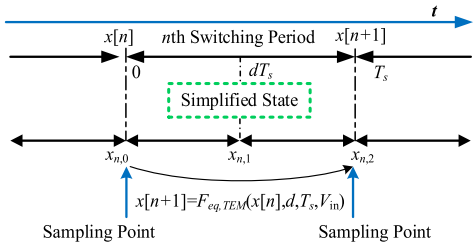


Fig. 4. Simplified iterative relationship of the state variable with TEM for the sampled-data modeling method.

The state transition function $F_{\text{eq,TEM}}(x[n]\, d,\, V_{\text{in}},\, T_s)$ within a switching period no longer needs to iterate over the two states. It only needs to directly discretize the state equation in (9). Then, the corresponding state transition function can be described as

$$\begin{aligned} x\ [n+1] &= F_{\text{eq,TEM}}\left(x\,[n]\,,\ d,\ V_{\text{in}},\ T_s\right). \\ &= \mathbf{G}_{\text{eq,TEM}}\, x\,[n] + \mathbf{H}_{\text{eq,TEM}} V_{\text{in}} \end{aligned} \tag{10}$$

Wherein, the state matrix $\mathbf{G}_{\text{eq,TEM}}$ and input matrix $\mathbf{H}_{\text{eq,TEM}}$ of the equivalent circuit in the discrete domain are

$$\begin{cases} \mathbf{G}_{\text{eq,TEM}} = e^{\mathbf{A}_{\text{eq}} T_s} \\ \mathbf{H}_{\text{eq,TEM}} = \int_0^{T_s} e^{\mathbf{A}_{\text{eq}} t} dt \mathbf{B}_{\text{eq,TEM}} \end{cases}.$$

In order to use the equivalent circuit to accurately predict the dynamic and steady-state system characteristics of the detailed switching circuit, it is necessary to make $F_{\text{eq,TEM}}$ accurately approach F_{TEM}. Therefore, model (10) should be equivalent to model (6), correspondingly the following approximation should be made:

$$\begin{cases} \mathbf{G}_{\text{eq,TEM}} \approx \mathbf{G}_{\text{TEM}} \\ \mathbf{H}_{\text{eq,TEM}} \approx \mathbf{H}_{\text{TEM}} \end{cases}. \tag{11}$$

Calculating (11), $\mathbf{A}_{\text{eq,TEM}}$ and $\mathbf{B}_{\text{eq,TEM}}$ can be obtained

$$\begin{cases} \mathbf{A}_{\text{eq,TEM}} = \mathbf{A}_{\text{I}} \\ \mathbf{B}_{\text{eq,TEM}} = \left[\int_0^{T_s} e^{\mathrm{A}_{\text{eq,TEM}} t}\, dt\right]^{-1} e^{\mathrm{A}_2(1-d)T_s} \int_0^{dT_s} e^{\mathrm{A}_1 t} dt \mathbf{B}_1 V_{\text{in}} \end{cases}. \tag{12}$$

Expanding with the period T_s as the series for $\mathbf{B}_{\text{eq,TEM}}$, the higher order components are so small that can be omitted, and the lowest order term is retained. $\mathbf{B}_{\text{eq,TEM}}$ can be approximated as follows:

$$\mathbf{B}_{\text{eq,TEM}} \approx \begin{pmatrix} \frac{d}{L_s} \\ \frac{d(1-d)R_o}{2L_s f_s C_s (R_c + R_o)} \end{pmatrix}. \tag{13}$$

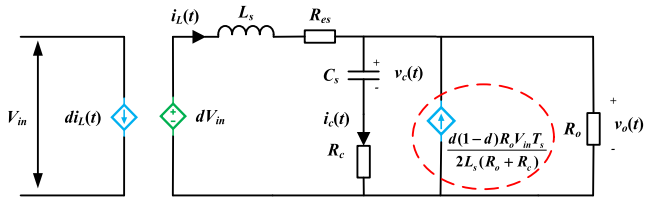


Fig. 5. SOGEC of the buck converter with TEM.

Therefore, the specific forms of the state-space description in the continuous domain can be obtained

$$\begin{cases} \begin{pmatrix} \frac{di_L(t)}{dt} \\ \frac{dv_c(t)}{dt} \end{pmatrix} = \begin{pmatrix} \frac{-R_{es}-\frac{R_cR_o}{R_c+R_o}}{L_s} & \frac{-R_o}{(R_o+R_c)L_s} \\ \frac{R_o}{(R_o+R_c)C_s} & \frac{-1}{(R_o+R_c)C_s} \end{pmatrix} \begin{pmatrix} i_L(t) \\ v_c(t) \end{pmatrix} \\ + \begin{pmatrix} \frac{d}{L_s} \\ \frac{d(1-d)R_o}{2L_sf_sC_s(R_c+R_o)} \end{pmatrix} V_{\text{in}} \\ v_o(t) = \begin{pmatrix} \frac{R_cR_o}{R_c+R_o} & \frac{R_o}{R_c+R_o} \end{pmatrix} \begin{pmatrix} i_L(t) \\ v_c(t) \end{pmatrix} \end{cases} . \tag{14}$$

This set of equations can be realized as an SOGEC with an ideal controlled current source of buck converter, as shown in Fig. 5.

Compared with the equivalent circuit constructed by the averaged model, the SOGEC has an additional controlled current source on the output side. In order to explain the physical meaning of the SOGEC more clearly, R_c and R_{es} will be ignored. From Fig. 5, the current $i_c(t)$ flowing through the capacitor can be obtained as

$$i_c(t) = i_L(t) - \frac{v_o(t)}{R_o} + \frac{d(1-d)}{2L_sf_s}V_{\text{in}}. \tag{15}$$

The ripple Δi_L of the inductor current can be obtained as

$$\Delta i_L = \frac{1}{2} \cdot \frac{v_o(t)}{L_s} \cdot (1-d)\, T_s = \frac{d(1-d)}{2L_sf_s}\, V_{\text{in}}. \tag{16}$$

For the equivalent circuit, the inductor current $i_L(t)$ is corrected to

$$i_L(t) = i_c(t) + \frac{v_o(t)}{R_o} - \Delta i_L. \tag{17}$$

Based on the abovementioned analysis, the SOGEC is equivalent to adding an additional power loop from the input to the output. This power loop contains the inductor current ripple information that is ignored in the averaged model. Therefore, the SOGEC although ignores the information of the state variable $x_{n,1}$ at the intersecting point of $u[n]$ and the carrier waveform, but accurately retains the information of the state variable at the sampling point. Fig. 6 shows the comparison of $i_L(t)$ between the SOGEC and the detailed switching circuit with TEM. $i_L(t)$ of SOGEC is not the sliding average value of the inductor current of the detailed switching circuit, and the trajectories of the two accurately coincide at the sampling point, i.e., the valley point of the inductor current. For the trailing-edge modulated buck converter, it is verified that the waveform of $i_L(t)$ for the SOGEC is the lower envelope for the detailed switching circuit.

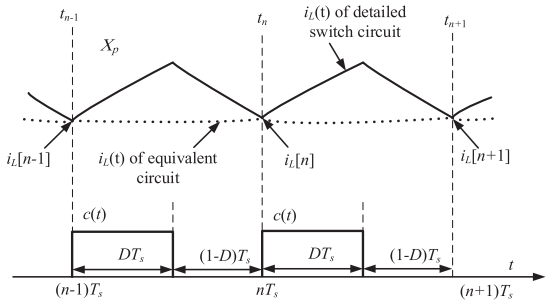


Fig. 6. Comparison of the waveform of $i_L(t)$ for SOGEC and detailed switching circuit with TEM.

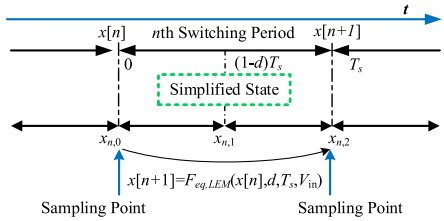


Fig. 7. Simplified iterative relationship of the state variable with LEM for the sampled-data modeling method.

D. Equivalent Circuit Based on the Sampled-Data Modeling Method With LEM

Compared with the derivation process of the trailing-edge modulated equivalent circuit, the equivalent circuit derivation with LEM is similar. The only thing that needs to be noted is that the sequence of switching ON and OFF of the buck converter in LEM in one cycle is opposite to that in TEM. As shown in Fig. 7, the simplified state variable transition relationship with LEM is given. Let F_{LEM} and $F_{\text{eq,LEM}}$ be sufficiently approximate, so $\mathbf{A}_{\text{eq,LEM}}$ and $\mathbf{B}_{\text{eq,LEM}}$ can be solved

$$\begin{cases} \mathbf{A}_{\text{eq,LEM}} = \mathbf{A}_{\text{I}} \\ \mathbf{B}_{\text{eq,LEM}} = \left[\int_0^{T_s} e^{\mathbf{A}_{\text{eq,LEM}}t}\, dt\right]^{-1} \int_0^{dT_s} e^{\mathbf{A}_{\text{I}}t} dt \mathbf{B}_{\text{I}} \end{cases} . \tag{18}$$

Expanding with the period T_s as the series for $\mathbf{B}_{\text{eq,LEM}}$, the higher order components are so small that can be omitted, and the lowest order term is retained

$$\mathbf{B}_{\text{eq,LEM}} \approx \begin{pmatrix} \frac{d}{L_s} \\ \frac{-d(1-d)R_o}{2L_sf_sC_s(R_c+R_o)} \end{pmatrix} . \tag{19}$$

Therefore, the specific forms of the leading-edge modulated state-space description in the continuous domain is

$$\begin{cases} \begin{pmatrix} \frac{di_L(t)}{dt} \\ \frac{dv_c(t)}{dt} \end{pmatrix} = \begin{pmatrix} \frac{-R_{es}-\frac{R_cR_o}{R_c+R_o}}{L_s} & \frac{-R_o}{(R_o+R_c)L_s} \\ \frac{R_o}{(R_o+R_c)C_s} & \frac{-1}{(R_o+R_c)C_s} \end{pmatrix} \begin{pmatrix} i_L(t) \\ v_c(t) \end{pmatrix} \\ + \begin{pmatrix} \frac{d}{L_s} \\ \frac{-d(1-d)R_o}{2L_sf_sC_s(R_c+R_o)} \end{pmatrix} V_{\text{in}} \\ v_o(t) = \begin{pmatrix} \frac{R_cR_o}{R_c+R_o} & \frac{R_o}{R_c+R_o} \end{pmatrix} \begin{pmatrix} i_L(t) \\ v_c(t) \end{pmatrix} \end{cases} . \tag{20}$$

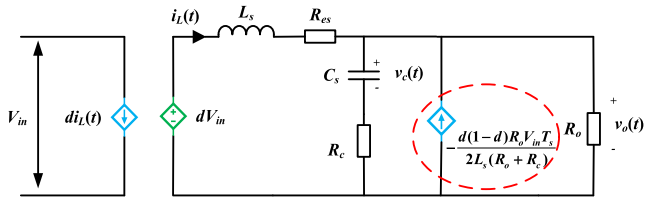


Fig. 8. SOGEC of the buck converter with LEM.

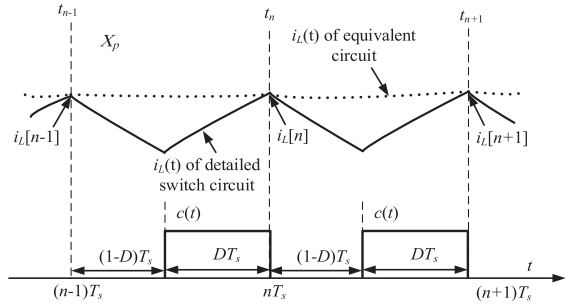


Fig. 9. Comparison of the waveform of $i_L(t)$ for SOGEC and detailed switching circuit with LEM.

This set of equations can be realized as the leading-edge DPWM SOGEC with an ideal controlled source of buck converter, as shown in Fig. 8.

It can be seen from the equivalent circuit with TEM and LEM that the controlled current source on the output side is opposite. In fact, the controlled current source is a function of modulation delay in the z-domain, and the main difference between TEM and LEM is also reflected in the controlled current source, which will be further discussed as follows. Fig. 9 shows the comparison of the waveform of $i_L(t)$ between the SOGEC and the detailed switching circuit with LEM. For the buck converter with LEM, the sampling point is the peak of $i_L(t)$ in each cycle, so the waveform of $i_L(t)$ for the SOGEC is the upper envelope of that for the detailed switching circuit.

III. Small-Signal Model of Z-Domain Based on SOGEC

A. S-Domain Small-Signal Transfer Function

In engineering applications, it is necessary to obtain the amplitude and phase characteristics of the system in the frequency domain to facilitate the design of the control loop. Therefore, the linearization of (14) and (20) around the converter steady-state operating point $Q = (I_L,V_o,D,V_c)$ is required. As usual, all the relevant quantities can be expressed in terms of steady-state component and small-signal ac component

$$\begin{aligned} i_L(t) &= I_L + \hat{i}_L(t) \\ v_O(t) &= V_O + \hat{v}_O(t) \\ v_C(t) &= V_C + \hat{v}_C(t) \\ d(t) &= D + \hat{d}(t). \end{aligned} \tag{21}$$

The transfer functions of control-output voltage and control-inductance current in s-domain can be derived. For TEM

$$\begin{aligned} G_{\mathrm{eq,TEM,vd}}(s) &= \frac{\hat{v}_o(s)}{\hat{d}(s)} \\ &= \frac{V_{\mathrm{in}}R_o}{C_sL_s(R_o+R_c)} \frac{\left[R_o\frac{(1-2D)}{2f_s(R_o+R_c)}+C_sR_c\right]s+R_oR_{\mathrm{es}}\frac{(1-2D)}{2f_sL_s(R_o+R_c)}+1}{s^2+\frac{L_s+C_SR_cR_o+C_sR_{es}(R_o+R_c)}{C_sL_s(R_o+R_c)}s+\frac{R_{\mathrm{es}}+R_o}{C_sL_s(R_o+R_c)}} \end{aligned} \tag{22}$$

$$\begin{aligned} G_{\mathrm{eq,TEM,id}}(s) &= \frac{\hat{i}_L(s)}{\hat{d}(s)} \\ &= \frac{V_{\mathrm{in}}}{C_sL_s(R_o+R_c)} \frac{C_s(R_o+R_c)s+\left(1+R_o^2\frac{(2D-1)}{2f_sL_s(R_o+R_c)}\right)}{s^2+\frac{L_s+C_SR_cR_o+C_sR_{\mathrm{es}}(R_o+R_c)}{C_sL_s(R_o+R_c)}s+\frac{R_{\mathrm{es}}+R_o}{C_sL_s(R_o+R_c)}}. \end{aligned} \tag{23}$$

For LEM

$$\begin{aligned} G_{\mathrm{eq,LEM,vd}}(s) &= \frac{\hat{v}_o(s)}{\hat{d}(s)} \\ &= \frac{V_{\mathrm{in}}R_o}{C_sL_s(R_o+R_c)} \frac{\left[R_o\frac{(2D-1)}{2f_s(R_o+R_c)}+C_sR_c\right]s+R_oR_{\mathrm{es}}\frac{(2D-1)}{2f_sL_s(R_o+R_c)}+1}{s^2+\frac{L_s+C_SR_cR_o+C_sR_{es}(R_o+R_c)}{C_sL_s(R_o+R_c)}s+\frac{R_{\mathrm{es}}+R_o}{C_sL_s(R_o+R_c)}} \end{aligned} \tag{24}$$

$$\begin{aligned} G_{\mathrm{eq,LEM,id}}(s) &= \frac{\hat{i}_L(s)}{\hat{d}(s)} \\ &= \frac{V_{\mathrm{in}}}{C_sL_s(R_o+R_c)} \frac{C_s(R_o+R_c)s+\left(1+R_o^2\frac{(1-2D)}{2f_sL_s(R_o+R_c)}\right)}{s^2+\frac{L_s+C_SR_cR_o+C_sR_{\mathrm{es}}(R_o+R_c)}{C_sL_s(R_o+R_c)}s+\frac{R_{\mathrm{es}}+R_o}{C_sL_s(R_o+R_c)}}. \end{aligned} \tag{25}$$

B. Small-Signal Transfer Function in Z-Domain Considering Loop Delay

Since the time delay caused by the sampling and holding process has a great impact on system characteristics, the total loop delay t_d must be taken into account. In fact, DSP operates with the shadow register mode, the control command $u[n]$ has the delay time of one cycle to be updated, which is called the control delay t_{cntrl}. Assuming the amplitude of the saw-tooth modulating wave is 1, then the duty cycle $d[n]$ of the nth cycle is

$$d[n] = u[n-1]. \tag{26}$$

Thereafter $u[n]$ needs to be modulated by DPWM. The time between the update of $u[n]$ and the intersection point of $u[n]$ and the carrier waveform can be named the modulation delay t_{DPWM}. t_{DPWM} of trailing-edge and leading-edge modulated converter are $d[n]T_s$ and (1- $d[n]$)T_s, respectively. Therefore, the total delay of the digital control system is

$$t_d = t_{\mathrm{DPWM}} + t_{\mathrm{cntrl}}. \tag{27}$$

However, the s-domain small-signal model does not include a sampling and holding process. For the case of sampling with constant time intervals, the s-domain small-signal model can be directly discretized into the z-domain to reflect the sampling and delay characteristics in the digitally controlled buck converter. Fig. 10 shows the control block diagram of the digitally controlled buck converter. Wherein, the sensing gain of $H(s)$ is generally assumed to be 1. The digital controlled loop can be equivalent to the series of compensator $G_c(s)$, modulator $G_{\mathrm{DPWM}}(s)$, and a delay z^{-1} Finally, the digital controlled signal is converted into an analog signal through DPWM and D/A modules to control the power loop, which makes the entire circuit

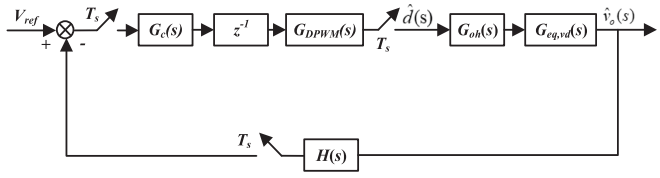


Fig. 10. Block diagram of the digitally controlled closed-loop buck converter.

has a zero-order holder effect. Therefore, the D/A module can be equivalent to the series connection of a sampling switch and a zero-order holder link $G_{\mathrm{oh}}(s)$, and then the control pulse acts on $G_{\mathrm{oh}}(s)G_{\mathrm{eq,vd}}(s)$.

The open-loop z-domain transfer function of the converter does not require complex transformations with delay links, which is a key superiority compared with the models in [19], [23], [27], and [28]. Since the SOGEC is derived by the sampled-data modeling method, it already contains the time span information from the sampling point to the intersecting point, that is, the item that contains the duty cycle is built in the model. When the sampling switch operates with a period of T_s, only the open-loop transfer function $G_{\mathrm{oh}}(s)G_{\mathrm{eq,vd}}(s)$ needs to be transferred into z-domain, and then the z-domain transfer function $G_{\mathrm{eq}}(z)$ from the control to the output can be obtained

$$
\begin{aligned}
&G_{\mathrm{eq}}\ (z) = z^{-1}\ \mathcal{Z}\left[G_{\mathrm{oh}}\,(s)\,G_{\mathrm{eq,vd}}\,(s)\right] \\
&= z^{-1}\ \left(1-z^{-1}\right)\mathcal{Z}\left[\frac{G_{\mathrm{eq,vd}}(s)}{s}\right] \\
&= z^{-1}\ \left(1-z^{-1}\right)\mathcal{Z}\left[\frac{Ms+N}{s(s+a)(s+b)}\right] \\
&= \left(z^{-1}-z^{-2}\right)\ \mathcal{Z}\left[\frac{Aa}{s(s+a)a}+\frac{Bb}{s(s+b)b}\right] \\
&= \frac{A}{a}\frac{1-e^{-aT_s}}{z^2-e^{-aT_s}z}+\frac{B}{b}\frac{1-e^{-bT_s}}{z^2-e^{-bT_s}z} \\
&= \frac{\left[\frac{A}{a}\left(1-e^{-aT_s}\right)+\frac{B}{b}\left(1-e^{-bT_s}\right)\right]z-\frac{A}{a}\left(1-e^{-aT_s}\right)e^{-bT_s}-\frac{B}{b}\left(1-e^{-bT_s}\right)e^{-aT_s}}{z^3-\left(e^{-aT_s}+e^{-bT_s}\right)z^2+e^{-(a+b)T_s}z}
\end{aligned}
$$

Denote $G_{\mathrm{eq}}(z)$ as

$$
G_{\mathrm{eq}}\ (z) = \frac{P_1 z + P_0}{z^3 + Y_1 z^2 + Y_0 z} \tag{28}
$$

where

$$
\begin{aligned}
A &= -\frac{N-Ma}{a-b} \\
B &= \frac{N-Mb}{a-b} \\
P_1 &= \frac{A}{a}\left(1-e^{-aT_s}\right)+\frac{B}{b}\left(1-e^{-bT_s}\right) \\
P_0 &= -\frac{A}{a}\left(1-e^{-aT_s}\right)e^{-bT_s}-\frac{B}{b}\left(1-e^{-bT_s}\right)e^{-aT_s} \\
Y_1 &= -\left(e^{-aT_s}+e^{-bT_s}\right) \\
Y_0 &= e^{-(a+b)T_s}.
\end{aligned}
$$

In order to verify the accuracy of $G_{\mathrm{eq}}(z)$, MATLAB is used to get the magnitude and phase responses for $G_{\mathrm{ex}}(z)$, $G_{\mathrm{ave}}(s)$, and $G_{\mathrm{eq}}(z)$. The simulation parameters are given in Table I. Bode diagrams of control-output voltage and control-inductance

TABLE I
CIRCUIT PARAMETERS OF BUCK CONVERTER

Items	Descriptions	Specifications
V_{in}	Input voltage	48 V
V_{ref}	Reference voltage	12 V
D	Open-loop duty cycle	0.25
L_s	Inductance	220 μH
C_s	capacitance	160 µF
R_o	Load resistance	1.1 Ω
f_s	switching frequency	20 kHz
T_S	period	50e−6 s
R_{es}	Inductance equivalent series resistance	40 mΩ
R_c	Capacitor equivalent series resistance	4 mΩ

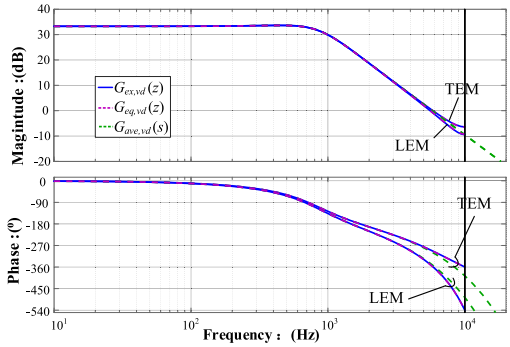
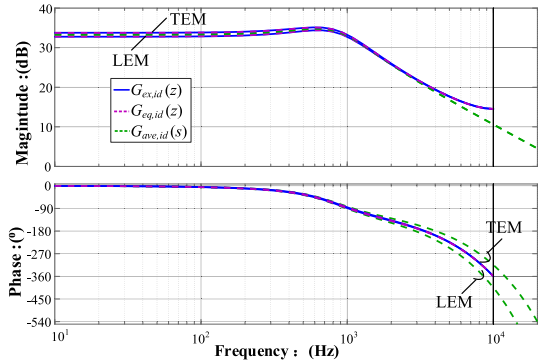
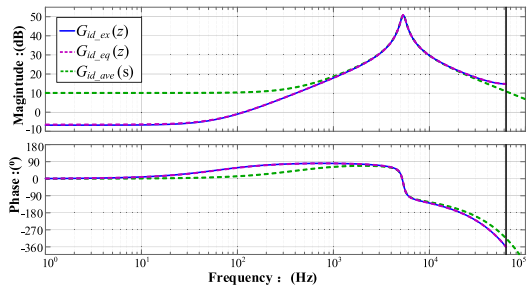


Fig. 11. Magnitude and phase responses of the control-output voltage transfer function obtained by different modeling methods.



(a)



(b)

Fig. 12. Magnitude and phase responses of the control-inductor current transfer function obtained by different modeling methods. (a) $R_{\mathrm{o}} = 1.1\ \Omega$. (b) $R_{\mathrm{o}} = 20\ \Omega$.

current transfer functions are shown in Figs. 11 and 12, respectively. $G_{\mathrm{ex}}(z)$ is derived by the CSDM, which is proposed by the literature [17], [28]; $G_{\mathrm{ave}}(s)$ is obtained from the averaged model modified by adding a delay link. For the three models, $G_{\mathrm{ex}}(z)$ can be used as a reference when the perturbation frequency is less than the Nyquist frequency.

Compared with Figs. 11 and 12, the following conclusions are drawn.

1) According to Fig. 11, the phase with LEM lags more when the steady-state duty cycle D is 0.25. This is because when the duty cycle is less than 0.5, the system with LEM has a large modulation delay.
2) From Fig. 11, it can be seen that due to the existence of signal aliasing effect, $G_{\mathrm{ave,vd}}(s)$ cannot accurately describe the high-frequency characteristics of the control-output voltage transfer function. The cutoff frequency and phase margin are different from $G_{\mathrm{ex,vd}}(z)$. However, the comparison of $G_{\mathrm{ex,and}}(z)$ and $G_{\mathrm{eq,vd}}(z)$ confirms the two approaches yield the same result.
3) From Fig. 12(a), due to the aliasing effects of sampling, it can be seen the high-frequency response cannot be reflected well by $G_{\mathrm{ave,\ id}}(s)$. And when the load resistance is increased to 20 Ω with other parameters unchanged in Table I, the low-frequency response of $G_{\mathrm{ave,\ id}}(s)$ shown in Fig. 12(b) loses accuracy as well. So, the average model cannot meet the accuracy requirement of modeling. Therefore, the consistency of $G_{\mathrm{ex,\ id}}(z)$ and $G_{\mathrm{eq,\ id}}(z)$ verifies the accuracy and necessity of constructing the second-order equivalent model.

It should also be noted that the modeling method proposed in this article is generally applicable to other PWM type dc–dc converters with CCM operation. The proposed modeling method can effectively reflect the influence of sampling point position and delay on system characteristics.

IV. System Stability Analysis

In this section, a digitally voltage-controlled buck converter system with proportional controller k_p will be used to study the system stability, and k_p is used as the standard to measure the stability of the system. First, the stability analyzing methods for the Jacobian matrixes and the z-domain characteristic equations for the buck converter are introduced, respectively, and then the influence of key circuit parameters on the system stability is studied.

A. Global System Stability Analysis

Fig. 13 shows the block diagram of the single-voltage closed-loop buck converter with a P controller. The control method of the system is proportional control, and a cycle delay caused by the shadow register is considered. In Fig. 13, $e[n+1]$ represents the error sampling value in the $n+1$ cycle, $v_o[n+1]$ represents the output voltage sampling value in the $n+1$ cycle, and $d[n]$ represents the duty cycle calculated at the beginning of the n cycle.

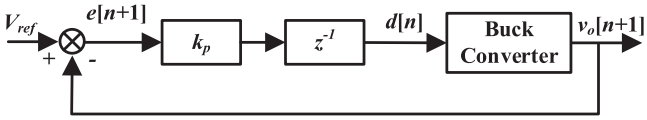


Fig. 13. System block diagram of a closed-loop buck converter with P controller.

Combined with Fig. 13 and the equivalent state transition function, a set of differential equations describing the closed-loop system can be written:

$$\begin{cases} i_L\ [n+1] = g_{\mathrm{eq},1,1}\ i_L\ [n] + g_{\mathrm{eq},1,2} v_C\ [n] + h_{\mathrm{eq},1}\ (d\,[n])\ V_{\mathrm{in}} \\ v_C\ [n+1] = g_{\mathrm{eq},2,1}\ i_L\ [n] + g_{\mathrm{eq},2,2} v_C\ [n] + h_{\mathrm{eq},2}\ (d\,[n])\ V_{\mathrm{in}} \\ d\ [n+1] = k_p\ \left(V_{\mathrm{ref}} - (i_L\ [n]\ R_c + v_c\ [n])\left(\frac{R_o}{R_o+R_c}\right)\right) \end{cases}. \tag{29}$$

Among them, the state matrix is defined as $\mathbf{G}_{\mathrm{eq}} = [g_{\mathrm{eq},i,j}]_{2\times 2}$, and the input matrix is defined as $\mathbf{H}_{\mathrm{eq}} = [h_{\mathrm{eq},i}]_{2\times 1}$. The first two equations of (29) are differential equations of the power loop, and the last equation is the controller differential equation. The stability of the system can be analyzed by solving the Jacobi matrix of the formula (29) at the steady-state operating point. This point can be solved by the Newton–Raphson iteration method. The Jacobian matrix J_D and characteristic equation $f(\lambda)$ of the system are given by

$$J_D = \begin{pmatrix} g_{\mathrm{eq},1,1} & g_{\mathrm{eq},1,2} & \left(\frac{\partial h_{\mathrm{eq},1}(d[n])}{\partial d[n]}\right) V_{\mathrm{in}} \\ g_{\mathrm{eq},2,1} & g_{\mathrm{eq},2,2} & \left(\frac{\partial h_{\mathrm{eq},2}(d[n])}{\partial d[n]}\right) V_{\mathrm{in}} \\ -k_p \frac{R_c R_o}{R_c+R_o} & -k_p \frac{R_o}{R_c+R_o} & 0 \end{pmatrix} \tag{30}$$

$$\begin{aligned} f(\lambda) = {} & \lambda^3 - (g_{\mathrm{eq},1,1} + g_{\mathrm{eq},2,2})\,\lambda^2 \\ & + (g_{\mathrm{eq},1,1} g_{\mathrm{eq},2,2} + k_p r_a h_1 v_{\mathrm{in}} - g_{\mathrm{eq},1,2} g_{\mathrm{eq},2,1} + k_p r_b h_2 V_{\mathrm{in}})\,\lambda \\ & - k_p r_a h_1 g_{\mathrm{eq},2,2} V_{\mathrm{in}} - k_p r_b h_2 g_{\mathrm{eq},1,1} V_{\mathrm{in}} + k_p r_a\ h_2 g_{\mathrm{eq},1,2} V_{\mathrm{in}} \\ & + k_p r_b h_1\ g_{\mathrm{eq},2,1} V_{\mathrm{in}} = 0 \end{aligned} \tag{31}$$

where $h_i = \frac{\partial \mathrm{H}_i(d[n])}{\partial d[n]}$ $r_a = \frac{R_c R_o}{R_c+R_o}$ $r_b = \frac{R_o}{R_c+R_o}$.

As the optimal linear approximation of the nonlinear system, the convergence and divergence characteristics of the Jacobian matrix are consistent with the original system. When the spectral radius of the Jacobian matrix is greater than 1, the system is unstable; when the spectral radius is equal to 1, the system is critically stable and at this time the maximum gain $k_{p,\ \max}$ of the proportional controller that can stabilize the system is obtained.

B. System Stability Analysis Based on Z-Domain Small-Signal Model

The z-domain block diagram of the closed-loop system is shown in Fig. 14, so the closed-loop transfer function of the system can be expressed as follows:

$$\begin{aligned} \Phi_{\mathrm{eq}}(z) &= \frac{z^{-1} k_p G_{\mathrm{DPWM}}(z)\, G_{\mathrm{oh}} G_{\mathrm{eq,vd}}(z)}{1 + z^{-1} k_p G_{\mathrm{DPWM}}(z)\, G_{\mathrm{oh}} G_{\mathrm{eq,vd}}(z)} \\ &= \frac{k P_1 z + k P_0}{z^3 + Y_1 z^2 + (Y_0 + k P_1) z + k P_0}. \end{aligned} \tag{32}$$

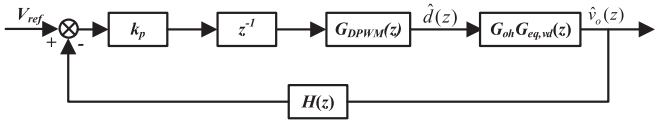


Fig. 14. *Z*-domain block diagram of P controller of the closed-loop buck converter.

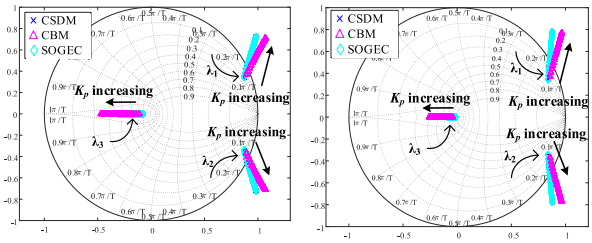


Fig. 15. Root loci of eigenvalues of the closed-loop system with increasing k_p. (a) LEM. (b) TEM.

So, the characteristic equation $D(z)$ is given by

$$D\ (z) = z^3\ + Y_1 z^2 + (Y_0 + k_p P_1) z + k_p\ P_0 = \ 0. \quad (33)$$

If and only if all the characteristic roots z_i ($i = 12{,}3$) of the $D(z)$ are uniformly distributed in the unit circle on the z-plane, that is $\max_{1\le i\le 3} |z_i| < 1$, the system is stable. When the largest modulus of the characteristic root is equal to 1, that is $\max_{1\le i\le 3}\ |z_i| = \ 1$, the system is critically stable, and $k_{p,\max}$ can be obtained.

C. *Influence of Control Parameter* $\mathrm{K_p}$ *on System Stability*

First, the influence of k_p on the stability of the system is analyzed. Fig. 15 shows the eigenvalues of the Jacobian matrix of the closed-loop system with k_p varying from 0.02 to 0.22, considering the parameters given in Table I. In Fig. 15, three models are compared to verify the accuracy of the global equivalent circuit model in analyzing system stability. The CSDM without any simplification can be used as a standard for comparison of model accuracy. However, the CSDM is generally transformed into the bilinear model through first-order approximation because of its simplicity. From Fig. 15, the root loci predicted by the proposed equivalent circuit model is well consistent with the result of the CSDM. However, the predicted result of the conventional bilinear model (CBM) has a large error with the accurate result.

The Jacobian matrix in (30) is three order, and its three characteristic roots are composed of a real root λ_3 and a pair of conjugate complex roots λ_1 and λ_2. When k_p increases, the root loci of a pair of conjugate complex roots λ_1 and λ_2 change greatly, while the real root λ_3 does not change significantly. As k_p increases to $k_{p,\max}$, λ_1 and λ_2 will pass through the unit circle in two opposite directions and the system will undergo low-frequency oscillation. $k_{p,\max}$ calculated by the model proposed in this article and CSDM are the same, which are 0.061 and 0.087, respectively, for TEM and LEM. The same $k_{p,\max}$ can also be obtained by using the characteristic equation $D(z)$ in (33), which means the z-domain model can accurately predict the stable boundary of the system.

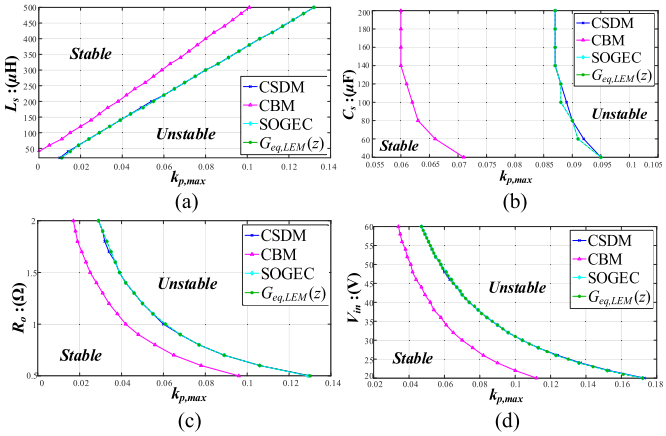


Fig. 16. For LEM, comparison of stability boundaries predicted by different models. (a) $k_{p,\max}$ versus L_s. (b) $k_{p,\max}$ versus C_s. (c) $k_{p,\max}$ versus R_o. (d) $k_{p,\max}$ versus V_{in}.

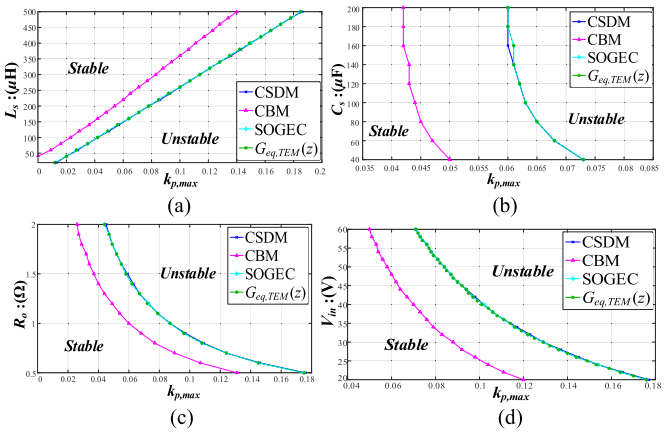


Fig. 17. For TEM comparison of stability boundaries predicted by different models. (a) $k_{p,\max}$ versus L_s. (b) $k_{p,\max}$ versus C_s. (c) $k_{p,\max}$ versus R_o. (d) $k_{p,\max}$ versus V_{in}.

D. *Influence of Power Loop Parameters on System Stability*

The equivalent circuit model is a good tool for analyzing the stability of the system. It can be used to not only guide the component selection, but also to guide the design of the controller when the loop parameters change. Figs. 16 and 17 show the comparison of stability boundaries predicted by the CSDM, the SOGEC, the $D(z)$, and the CBM, respectively, in LEM and TEM. $k_{p,\max}$ is used to measure the range of the stability boundaries of the power loop parameters.

By comparing Figs. 16 and 17, and analyzing $D(z)$, the following conclusions are drawn.

1) First, the trend of system stability varying with parameters is obtained. From $D(z)$ in (33) and Cardan's formula, it can be obtained that the characteristic roots of $D(z)$ satisfy the following equation:

$$z_1 \times z_2 \times\ z_3 = \ -k_p P_0. \quad (34)$$

From (34), it can be obtained that $z_3<0$ and z_3 changes little as k_p increases. Therefore, (34) can approximately reflect the relationship between the square of the module of the conjugate characteristic roots (i.e., $z_1 \times z_2 = |z_1|^2 = |z_2|^2$) and the loop parameters. In (34), k_p and V_{in} appear in the form of product. So, the increase of V_{in} is equivalent to the increase of k_p, leading to reduction of the stability margin of the system. So, the closed-loop controller design should be based on the maximum input voltage that may occur for the buck converter.

The trend of stability boundary changing with R_o, L_s, and C_s can be analyzed by deriving (34)

$$\frac{\partial(-k_p P_0)}{\partial R_o} < 0 \tag{35}$$

$$\frac{\partial(-k_p P_0)}{\partial C_s} < 0 \tag{36}$$

$$\frac{\partial(-k_p P_0)}{\partial L_s} > 0. \tag{37}$$

According to the result of (35), the increasing of R_o will increase the modulus of characteristic roots that means the stability margin will be smaller under the lighter load. Therefore, the critical control parameters should be obtained at light load to ensure the stability of the converter for the whole load ranges.

For the system filtering parameters C_s and L_s, the increasement of them will reduce the output ripple of the system. However, according to the formula (36), the increasing of C_s will cause the system stability boundary to be reduced. This is caused by the delay of output filter. The phase difference between the inductor current and the output voltage is

$$\varphi_{\text{iv}} = -\arctan\left(R_o C_s \omega_p\right) \tag{38}$$

where ω_p represents the frequency of duty cycle perturbation. When C_s increases, the phase lag of the output voltage relative to the inductor current increases, leading to reduction of the robustness of the system.

2) Comparing the stability boundary predicted by different models, it can be obtained that SOGEC and $G_{\text{eq}}(z)$ can accurately predict the relationship between parameters and $k_{p,\max}$. However, the CBM has a large error in predicting system stability. This shows that the proposed model can effectively reflect the stability of the system. However, the CSDM cannot accurately reflect the stability of the system through first-order approximation.
3) By comparing the critical curves in LEM and TEM shown in Figs. 16 and 17, it can be known that although the stability of leading-edge and trailing-edge modulated converters has the same trend with the change of power circuit parameters, the stability range of LEM is smaller than that of TEM.

E. Influence of Parasitic Parameters on System Stability

In an actual circuit, the characteristics of the components are not ideal, so it is necessary to consider the influence of parasitic parameters when modeling. Therefore, as shown in Fig. 18, the three-dimensional stable boundaries of k_p, R_c, and R_{es} are drawn in different modulations by calculating the SOGEC. To clearly

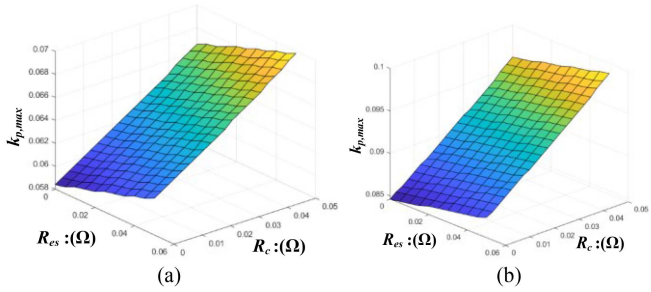


Fig. 18. Stability boundary of the system when R_c and R_{es} change. (a) LEM. (b) TEM.

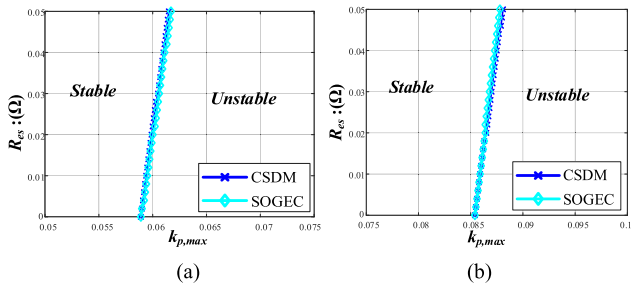


Fig. 19. Critical curves for $k_{p,\max}$ versus R_{es}. (a) LEM. (b) TEM.

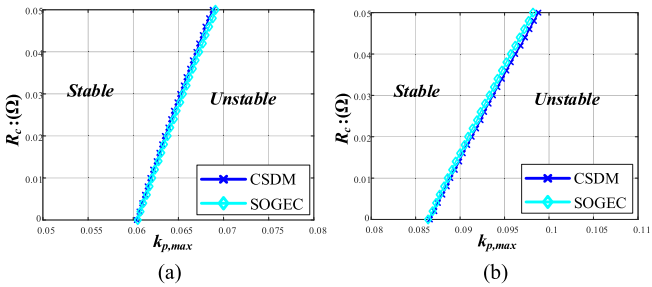


Fig. 20. Critical curves for $k_{p,\max}$ versus R_c. (a) LEM. (b) TEM.

analyze the influence of R_c and R_{es} on the system stability, Figs. 19 and 20, respectively, show the curve of R_c versus $k_{p,\max}$ with $R_{\text{es}} = 0.04$ and the curve of R_{es} vesus $k_{p,\max}$ with $R_c = 0.004$. It can be found that the stability boundary predicted by the SOGEC still accurately coincides with the CSDM, which means SOGEC is also suitable for analyzing the impact of parasitic parameters on system stability.

From Figs. 19 and 20, it can be shown that larger R_c and R_{es} can expand the stability boundary of the system, but neither can be too large. Because larger R_c will greatly increase the output voltage ripple and larger R_{es} will increase the loss of circuit resulting in efficiency decrease.

F. Influence of Different Modulations on System Stability

The influence of TEM and LEM on system stability is the focus of this article. According to SOGEC, the main difference between the two modulations is reflected in the controlled current source on the output side with the same value and opposite

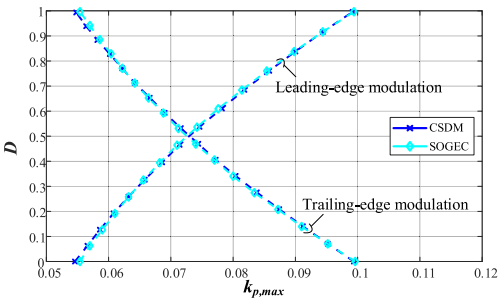


Fig. 21. Stability boundary of the system when D changes in different modulations.

direction. The value of the controlled current source is a function of the duty cycle, which is the mapping of the modulation delay t_{DPWM} on the model. Therefore, the derivative of (34) with respect to the duty ratio D with different modulations is given. For LEM

$$\frac{\partial\left(-k_pP_0\right)}{\partial D}>0. \tag{39}$$

For TEM

$$\frac{\partial\left(-k_pP_0\right)}{\partial D}<0. \tag{40}$$

The stability boundary of D with respect to $k_{p,\,\max}$ in different modulations is shown in Fig. 21. It can be known from (39), (40) and Fig. 21 that $k_{p,\,\max}$ decreases as the duty cycle D increases with TEM. For LEM, the opposite situation appears. In summary, the stability of the system decreases as the modulation delay t_{DPWM} increases. When the duty cycle D is 50%, SOGEC is the same for two different modulations, which means the stability of the system is the same as well. Therefore, when the duty cycle D is less than 50%, TEM should be selected. At this time, the system delay with TEM is smaller and the stability is better than that with LEM. If the duty cycle D is greater than 50%, the situation is just the opposite.

In order to verify the abovementioned analysis results, the detailed switching circuit and the equivalent circuit were built on the PLECS platform. The basic parameters of the simulation circuit are shown in Table I. It should be noted that because of the characteristics of digital control, it is necessary to add a first-order delay and a zero-order holder in the simulation. The transient characteristics of the system when the reference voltage steps from 6 V to 12 V is investigated. The reference voltage step decreases the duty cycle D. As shown in Fig. 22(a), after the reference voltage is stepped, the system with TEM changes from a stable operating state to an oscillating state. As shown in Fig. 22(b), the system with LEM from an unstable oscillation state gradually converges to a stable operating state. The simulation phenomenon is consistent with the calculation results shown in Fig. 21. When the system enters instability from stability, the closed-loop system loses its steady-state operating point. Under this condition, the waveform of the detailed switching circuit can still be tracked and represented by that of the SOGEC, which further proves the accuracy of the proposed model.

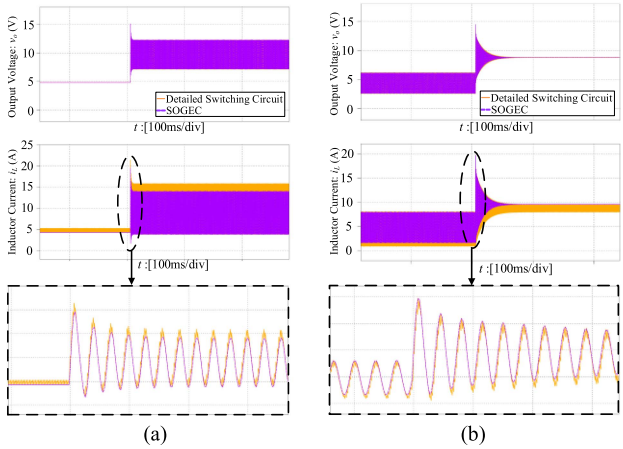


Fig. 22. Comparison of operating waveforms when V_{ref} changes from 6 to 12 V by simulation software. (a) LEM with $k_p=0.063$. (b) TEM with $k_p=0.085$.

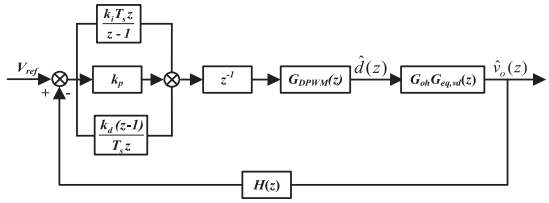


Fig. 23. Z-domain block diagram of PID controller of the closed-loop buck converter.

It should be pointed out that the proposed model can be used to build the large-signal equivalent circuit for the converter with a large ripple of state variable working in CCM mode.

V. Controller Design

A. Stability Range of Controller Parameters

In this section, the z-domain model will be used to design the controller. In engineering applications, the requirements of rapidity, stability and zero steady-state error for the system need to be realized through the closed-loop circuit. So, the PI or PID controller is generally chosen. But before the controller is selected, it is necessary to analyze the stability boundary of the controller gain to ensure that the controller parameters do not exceed the stability range of the system. The digital PID equations $G_c(z)$ in the z-domain is commonly written as

$$G_c\left(z\right)=k_p+\frac{k_iT_sz}{z-1}+\frac{k_d\left(z-1\right)}{T_sz}. \tag{41}$$

Fig. 23 shows the z-domain structure of the closed-loop buck converter with the PID controller, the feedback gain $H(s)$ is 1. The loop gain of the voltage controlled buck converter is

$$T_{\mathrm{vd}}\left(z\right)=z^{-1}G_c\left(z\right)G_{\mathrm{oh}}G_{\mathrm{eq,vd}}\left(z\right). \tag{42}$$

From (42), the closed-loop transfer function of buck converter can be derived, Eq. (43) shown at the bottom of the next page.

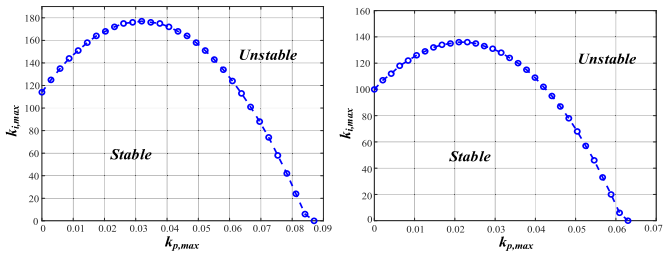


Fig. 24. Critical curves for $k_{p,\max}$ versus $k_{i,\max}$. (a) LEM. (b) TEM.

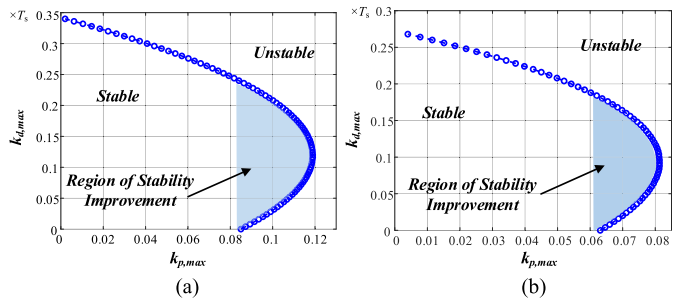


Fig. 25. Critical curves for $k_{p,\max}$ versus $k_{d,\max}$. (a) LEM. (b) TEM.

So, the characteristic equation $D(z)$ of the closed-loop transfer function is

$$\begin{aligned} D(z) &= T_s z^5 + (T_s Y_1 - T_s) z^4 \\ &+ \left(k_d P_1 + k_p P_1 T_s + k_i P_1 T_s^2 + T_s Y_0 - T_s Y_1\right) z^3 \\ &+ \left(k_d P_0 - 2k_d P_1 + k_p P_0 T_s\right) z^2 \\ &+ \left(-k_p P_1 T_s + k_i P_0 T_s^2 - T_s Y_0\right) z^2 \\ &+ \left(-2k_d P_0 + k_d P_1 - k_p P_0 T_s\right) z + k_d P_0 = 0. \end{aligned} \tag{44}$$

Since k_p can be used to reflect the stability of the system with k_d being 0, the characteristic equation $D(z)$ is used to get the corresponding relationship between $k_{p,\max}$ and $k_{i,\max}$. Fig. 24 shows the analytically obtained critical curves in the (k_p, k_i) plane for the parameter in Table I. The following conclusions can be drawn by observing Fig. 24.

1) In Fig. 24, the stability region is located in the area under the critical curve. If the controller parameters k_p and k_i are above the critical curve, the system will have unstable oscillation. The curve of k_i changing with k_p shows a parabolic shape, indicating that there is a k_p value that enables $k_{i,\max}$ to reach the maximum.
2) The stability region in TEM is larger than that in LEM illustrated in Fig. 24(a) and (b), which means that the system has a more flexible parameter design method in TEM.
3) It also can be seen from Fig. 24 that when k_i increases from 0, the range of $k_{\mathrm{p,max}}$ will decrease, which shows that although the integral control can raise the order of the system and reduce the steady-state error to 0, it will also reduce the stability of the system.

Thereafter, the corresponding relationship between $k_{\mathrm{p,max}}$ and $k_{\mathrm{d,max}}$ can be obtained through the characteristic (44) with k_i being 0 as well. Fig. 25 shows the analytically obtained critical curves in (k_p, k_d) plane for the parameter in Table I. The following conclusions can be drawn by observing Fig. 25.

1) In Fig. 25, the stable area is located on the left side of the critical curve. As shown in the figure, the light blue area, i.e., named as the region of improvement stability, shows the selection of k_d that helps us to improve the stability of buck converter. If k_d in the light blue area is selected, the stable region of buck converter with PID controller is much larger than that with PI controller. As k_d increases, $k_{p,\max}$ will start to increase from the value of $k_d = 0$ and then gradually decrease to 0. This means that if k_d chooses appropriately (in the light blue area), the PID controller can increase the damping of the system, which is equivalent to the increasement of stability. The selection of k_d should make the zero introduced by the differentiation controller as close as possible to the cut-off frequency to help improve the phase margin.
2) The stable area in TEM is greater than the stable areas in the LEM from Fig. 25(a) and (b), which means that the system has a more flexible parameter design method in TEM.

B. Controller Design

The PI and PID controllers will be further compared through simulation both in the frequency-domain and time domain to explain the different effects of the integral and derivative controller parameters on the stability and rapidity of the system. At the same time, the stability and transient characteristics of TEM and LEM will be illustrated as well.

For the PI controller, the parameter $k_p = 0.03$, and $k_i = 5$ is selected to ensure the sufficient phase margin and bandwidth. It can also be seen from Fig. 24 that this set of controllers is located in the stability region. So, the equation of PI controller

$$\begin{aligned} \Phi_{\mathrm{eq}}(z) &= \frac{T_{\mathrm{vd}}(z)}{1+T_{\mathrm{vd}}(z)} \\ &= \frac{\begin{array}{l} k_d P_0 + \left(-2k_d P_0 + k_d P_1 - k_p P_0 T_s\right) z \\ + \left(k_d P_0 - 2k_d P_1 + k_p P_0 T_s - k_p P_1 T_s + k_i P_0 T_s^2\right) z^2 \\ + \left(k_d P_1 + k_p P_1 T_s + k_i P_1 T_s^2\right) z^3 \end{array}}{\begin{array}{l} T_s z^5 + (T_s Y_1 - T_s) z^4 + \left(k_d P_1 + k_p P_1 T_s + k_i P_1 T_s^2 + T_s Y_0 - T_s Y_1\right) z^3 \\ + \left(k_d P_0 - 2k_d P_1 + k_p P_0 T_s - k_p P_1 T_s + k_i P_0 T_s^2 - T_s Y_0\right) z^2 \\ + \left(-2k_d P_0 + k_d P_1 - k_p P_0 T_s\right) z + k_d P_0 \end{array}}. \end{aligned} \tag{43}$$

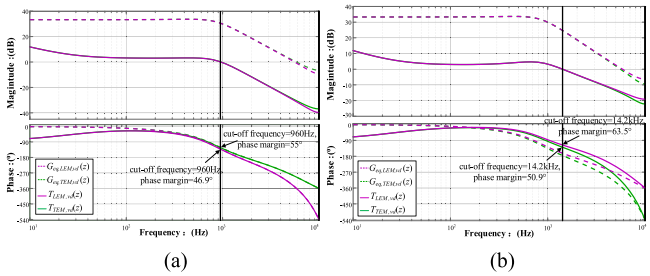


Fig. 26. Magnitude and phase responses of the $T_{vd}(z)$. (a) With PI controller. (b) With PID controller.

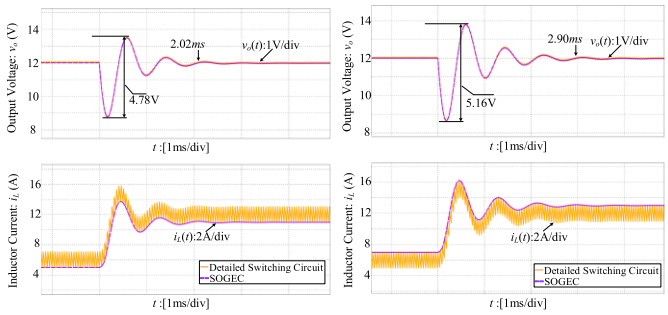


Fig. 27. Comparison of operating waveforms when R_o steps with PI controller by simulation software (a) TEM. (b) LEM.

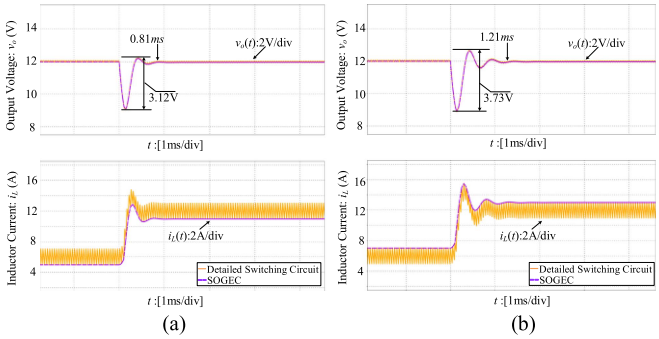


Fig. 28. Comparison of operating waveforms when R_o steps with PID controller by simulation software. (a) TEM. (b) LEM.

in z-domain is

$$G_{c,\mathrm{PI}}(z) = 0.03 + \frac{5 \times 5e^{-5} z}{z-1}. \tag{45}$$

The magnitude-phase characteristic of $T_{\mathrm{vd}}(z)$ compensated by $G_{c,\mathrm{PI}}(z)$ with different modulation is compared, as shown in Fig. 26(a). The phase margin of the loop is greater than 45° and the bandwidth is 960 Hz, which is about 1/20 of the switching frequency in both modulations through compensation.

For the PID controller, the parameter $k_d = 0.1T_s$ of the derivative element is added to the (45). This value of parameter k_d is located in the improvement stability region in Fig. 25. So, the equation of PID controller in z-domain is

$$G_{c,\mathrm{PID}}(z) = 0.03 + \frac{5 \times 5e^{-5} z}{z-1} + \frac{0.1(z-1)}{z}. \tag{46}$$

The magnitude-phase characteristic of different $T_{vd}(z)$ compensated by $G_{c,\mathrm{PID}}(z)$ is compared, as shown in Fig. 26(b). Compared with the PI controller, the phase margin and bandwidth with PID controller conditions have been greatly improved, which will certainly increase the stability and rapidity of the system. So, it is undoubtedly necessary to calculate and select the appropriate range of k_d.

Meanwhile, for both PI and PID compensation, the cut-off frequencies of the two modulations are almost the same, but the phase margin of $T_{\mathrm{vd,TEM}}(z)$ is higher than that of $T_{\mathrm{vd,LEM}}(z)$. This shows that the stability of the system in TEM is better than that in LEM. In the high frequency range, due to the delay effect in digital control, the phase margin of the system in LEM decreases faster than that in TEM.

In order to prove the correctness of the theoretical analysis, the operating condition of the load step is simulated in the time domain through PLECS software. Figs. 27 and 28 illustrate the simulation waveform when the load steps from 2 Ω to 1 Ω with PI and PID controllers, respectively. The parameters of the PI and PID controller are selected by (45) and (46), respectively. The relevant data in Figs. 27 and 28 is given in Table II. From Figs. 27 and 28 and Table II, the following conclusions can be drawn.

1) Due to the higher bandwidth and phase margin under PID control, the transient response time and overshoot voltage of PID control are less than the PI control when the load steps.

TABLE II
SIMULATION DATA COMPARISON

		PI	PID
Overshoot Voltage (V)	TEM	4.78	3.12
	LEM	5.16	3.73
Response Time(ms)	TEM	2.02	0.81
	LEM	2.90	1.21

2) With LEM, the converter has a longer transient response time compared with TEM. Moreover, the drop voltage and overshoot voltage when the load steps in the LEM system are smaller than that in the TEM system, indicating that the stability of the converter in the TEM is better, which is well consistent with the theoretical analysis.
3) From Figs. 27 and 28, it can be seen that the predicted waveform of the global equivalent circuit matches well with the operating waveform of the detailed switching circuit during the transient load stepping, indicating the accuracy of the model.

TABLE III
CIRCUIT PARAMETERS OF PROTOTYPE

Items	Descriptions	Specifications
V_{in}	Input voltage	48 V
V_{ref}	Reference voltage	12 V
L_s	Inductance	230 μH
C_s	capacitance	158.8 μF
R_o	Load resistance	1 Ω
f_s	switching frequency	20 kHz
T_S	period	50e−6 s
R_{es}	Inductance equivalent series resistance	40 mΩ
R_c	Capacitor equivalent series resistance	4 mΩ

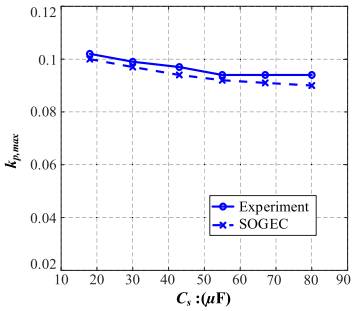


Fig. 29. Comparison of system stability boundary when C_s increases.

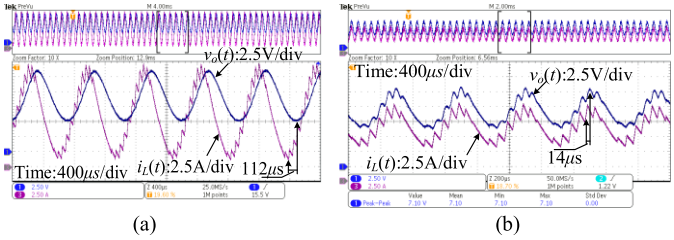


Fig. 30. Experimental waveform corresponding to different C_s. (a) C_s = 158.8 μF. (b) C_s = 19.8 μF.

VI. EXPERIMENT VERIFICATION

A. Prototype Design

In this section, a prototype of buck converter is built to verify the theoretical results of the proposed model. The controlling and sampling processes are achieved by the digital processor TMS320F28379D of TI. The parameters of the prototype are shown in Table III.

The design of the output capacitor is very important, which is related to the system stability and the voltage ripple. As shown in Fig. 29, both the calculation results and the experimental results show that the stability boundary of the system will gradually decrease as the capacitance increases. In Fig. 30, when C_s is 158.8 μF and 19.8 μF, the delay time of capacitance voltage to inductance current is 112 μs and 14 μs, respectively, under low-frequency oscillation. However, the output voltage has a larger ripple (about 0.75 V) when C_s is selected to be 19.8 μF, which may not meet the circuit design requirements. Therefore, under the premise of ensuring the voltage ripple meets the design

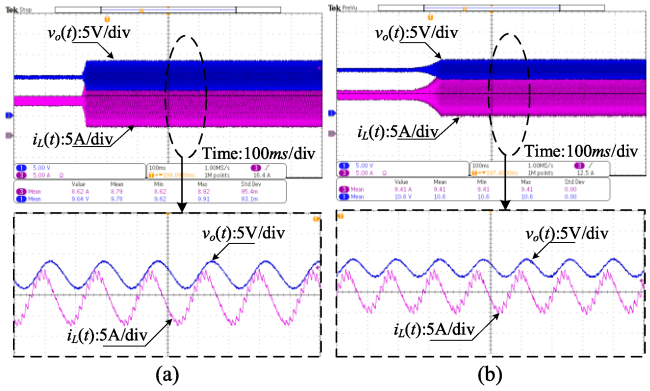


Fig. 31. Experimental waveforms of closed-loop buck converter. (a) LEM at $k_p = 0.058$. (b) TEM at $k_p = 0.091$.

index, C_s should be reduced as much as possible to increase the system stability. In this experiment, C_s is constructed by paralleling multiple ceramic capacitors and one electrolytic capacitor. It is important to reduce R_c by paralleling multiple ceramic capacitors because excessive R_c is the main source of output voltage ripples. But the capacitance of ceramic capacitors decreases with the increase of dc bias voltage [31], [32], [34], so a large electrolytic capacitor is added to stabilize the capacitance. The C_s of the prototype is 158.8 μF at 20 kHz and atmosphere temperature.

B. Experimental Results

To verify the influence of k_p and k_i on system stability, the experiment of controller gain step of closed-loop buck converter is carried out. Considering k_i is fixed to 0, the experimental waveform of the leading-edge and trailing-edge modulated converter are shown in Fig. 31 when k_p is stepped. The $k_{p,\max}$ of the leading-edge modulated converter prototype is tested to be 0.058, so the system changes from a stable state to a low-frequency oscillation state as k_p steps from 0.055 to 0.06 according to Fig. 31(a). Similarly, according to Fig. 31(b), when k_p steps from 0.087 to 0.092, the trailing-edge modulated closed-loop circuit operating from stability to instability, $k_{p,\max}$ in TEM is tested to be 0.091. The theoretical $k_{p,\max}$ calculated by SOGEC in leading-edge and TEM are 0.061 and 0.087, respectively. It can be found that the experimental results are consistent with the calculation results, indicating the accuracy of the model calculation. Meanwhile, the small deviation of the two results is mainly due to the influence of bandwidth of the sampling circuit, the delay of the driving circuit and the influence of the line parasitic parameters.

k_p is considered as a constant value, the experimental waveform of the leading-edge and trailing-edge modulated converter are shown in Fig. 32 when k_i is stepped. Fig. 32(a) illustrates that when k_i steps from 35 to 45, the system gradually transforms from stability to instability. At this time, k_p is fixed to be 0.55, and the integral critical gain of the system is measured to be 40. Similarly, when k_p is 0.075, $k_{i,\max}$ is measured to be 45, so the system changes from stability to instability as k_i

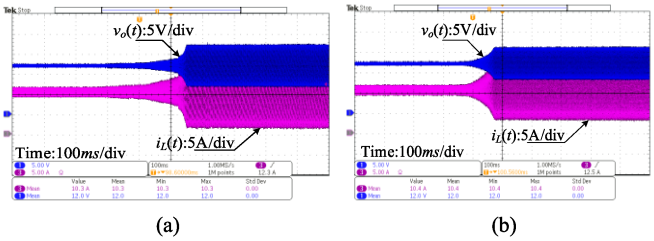


Fig. 32. Experimental waveforms of closed-loop buck converter. (a) LEM at $k_p = 0.055$, $k_i = 40$. (b) TEM at $k_p = 0.075$, $k_i = 45$.

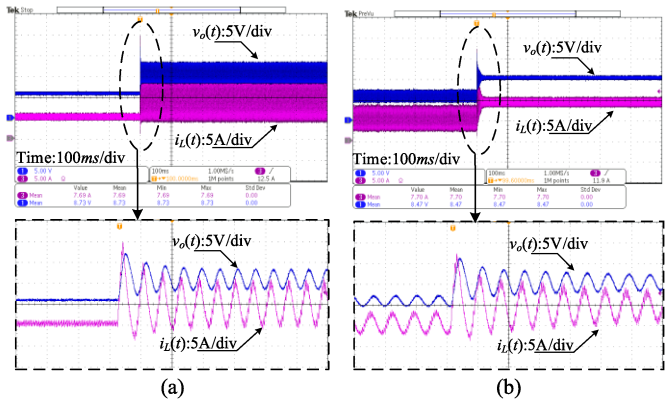


Fig. 33. Experimental waveforms of closed-loop buck converter when V_{ref} steps from 6 to 12 V. (a) $k_p = 0.059$ at LEM. (b) $k_p = 0.089$ at TEM.

steps from 40 to 50 as illustrated in Fig. 32(b). According to the proposed model, the calculated theoretical $k_{i,\max}$ at these conditions in leading-edge and trailing-edge modulated systems are 47 and 60, respectively. The experimental results are matched well with the calculation results, verifying the accuracy of the equivalent model for the stability boundary prediction of the integral controller gain.

The influence of different modulations on system stability has been analyzed in Section IV-F. To verify the correctness of the theoretical analysis and the accuracy of the model, the system transient response with reference voltage stepping from 6 to 12 V is tested in the converter prototype, as shown in Fig. 33. With the leading-edge modulated converter operating in $k_p = 0.059$, the reference voltage step will make the originally oscillating waveform converge, leading the system back to a stable state, as shown in Fig. 33(a). And when the converter modulated by TEM operates with $k_p = 0.089$, the reference voltage step leads to an unstable state according to Fig. 33(b). Compared with Fig. 22, the simulation waveform and experimental waveform are relatively close at the reference voltage step point. It shows that the theoretical analysis exactly explains how different modulations affect the system stability.

In order to verify the system stable boundary of input and output parameters predicted by SOGEC in Section IV-D, the critical curve of system stability with input and output parameters changing are obtained based on the converter prototype. Fig. 34 shows the comparison of stable boundaries as the value of output and input parameters increase. With the increase of

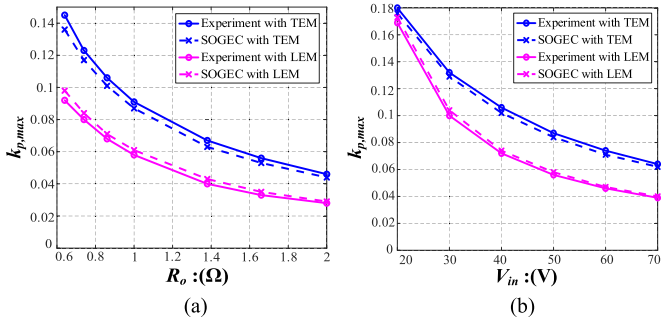


Fig. 34. Comparison of stability boundaries for different parameters. (a) $k_{p,\max}$ versus R_o. (b) $k_{p,\max}$ versus V_{in}.

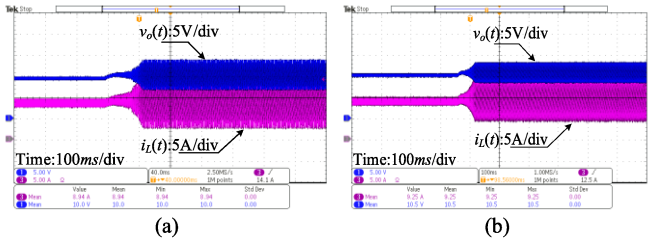


Fig. 35. Experimental waveforms of closed-loop buck converter when input voltage steps from 36 to 48 V. (a) $k_p = 0.065$ with LEM. (b) $k_p = 0.094$ with TEM.

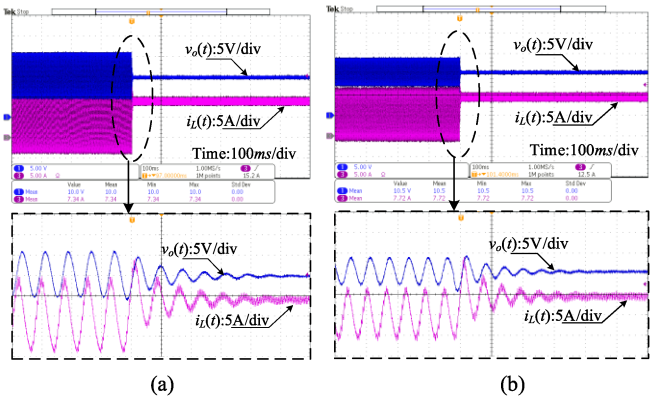


Fig. 36. Experimental waveforms of closed-loop buck converter when load steps from 50% to 100%. (a) $k_p = 0.045$ with LEM. (b) $k_p = 0.078$ with TEM.

load resistance and input voltage, $k_{p,\max}$ obtained by model calculation and experiment shows the same decreasing trend. Moreover, the accuracy of the model is shown by the two well consistent results. In order to further illustrate this result, a set of experiments are used to verify the change of system stability when the step perturbation of input voltage and the load resistance occurs with two different modulations. Fig. 35 shows input voltage steps from 36 to 48 V, at this time, the system tends to oscillate from a stable state. While Fig. 36 shows load steps from 50% to 100%, at this time, the system converges to stable from the oscillation state. The results further illustrate the correctness of the model analysis.

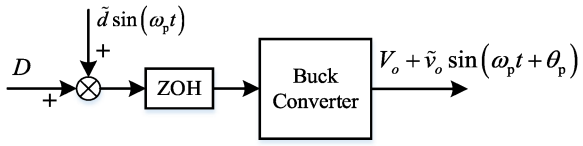


Fig. 37. Control-output frequency response measurement principle.

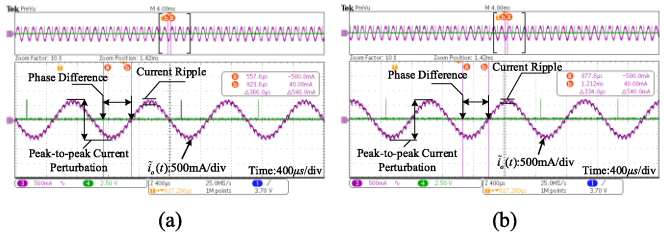


Fig. 38. Control-output frequency response measurement waveforms of buck converter when the small-signal perturbation frequency is 1 kHz. (a) LEM. (b) TEM.

In order to verify the accuracy of the equivalent open-loop control-output transfer function $G_{\rm eq}(z)$ and prepare for controller design, a buck converter prototype is built to test the frequency response. Its parameters are given in Table III. The measurement principle of the small-signal transfer function is shown in Fig. 37. A steady-state operating point D is selected and a sinusoidal small-signal perturbation is superimposed on it [35]. In this way, the output voltage v_o can be expressed as the sum of a steady-state output voltage V_o and a sinusoidal small-signal perturbation voltage. Therefore, the control variable of the converter is

$$d \;=\; D+\tilde{d}\sin\left(w_p t\right). \tag{47}$$

And the output voltage of the converter is

$$v_o = V_o \;+\tilde{v}_o\sin\left(w_p t+\theta_p\right). \tag{48}$$

Among them, $\tilde{d}$ is the amplitude of the sinusoidal signal, and ω_p is the angle frequency of the sinusoidal signal. $\tilde{v}_o$ is the amplitude of the ac component of the output voltage, and θ_p is the phase difference from control to output. $\tilde{d}$ is set to 0.02 in the experiment, and the range of ω_p is 50–5 kHz. The frequency response of control-output can be obtained by measuring the corresponding $\tilde{v}_o$ and θ_p. As shown in Fig. 38, the control-output frequency response is measured at 1 kHz for different modulations. $\tilde{v}_o$ is obtained by measuring the amplitude of ac component of the output current $\tilde{i}_o$ multiplied by the load resistance. θ_p is obtained by marking the moment of $\omega_p t = 2k\pi$ (which is the zero-crossing moment of the perturbation source), which is represented by a green pulse in Fig. 38, and the phase difference between this moment and the corresponding zero-crossing moment of the ac component of the output current waveform is measured. The amplitude of the ac component of the output current is the peak value of the current waveform minus the current ripple, as shown in Fig. 38.

For the buck converter prototype, the duty cycle of stable operation is selected as $D = 0.25$. The control-output frequency

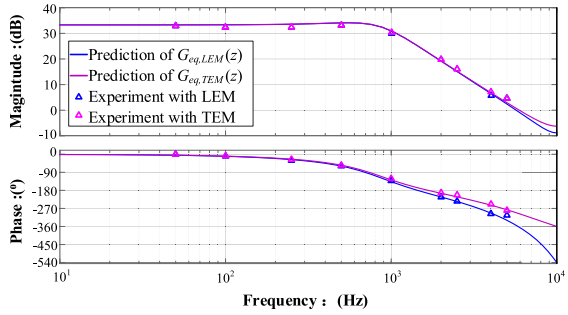


Fig. 39. Control-output frequency characteristic comparison of the buck converter.

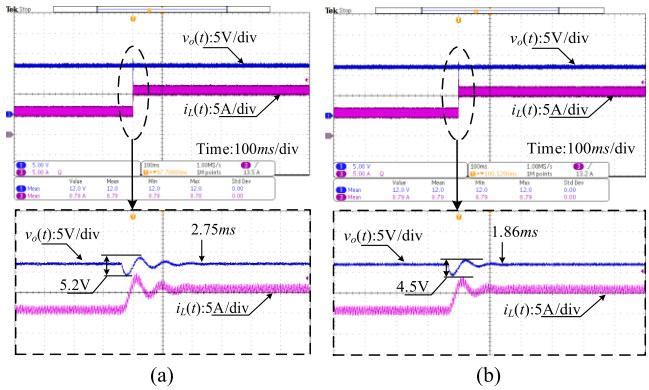


Fig. 40. Experimental waveforms of closed-loop buck converter when load steps from 50% to 100%. (a) LEM at $k_p = 0.03$, $k_i = 5$. (b) TEM at $k_p = 0.03$, $k_i = 5$.

response shown in Fig. 39 shows the experimental measurement results of control-output frequency characteristics ($\tilde{d} \sim \tilde{v}_o$) and the calculation results of $G_{\rm eq}(z)$. The comparison illustrates that for the two different modulations, the amplitude and phase characteristics of the theoretical results and the experimental results are in good consistency. The abovementioned comparative analysis also verifies the correctness of the model.

After the abovementioned verification, the controller of the closed-loop prototype can be accurately designed using the process shown in Section V-B. And the z-domain controller (45) needs to be written in the form of difference in the actual controller

$$\begin{aligned} D_{\rm pi}\;[n+1] &= D_{\rm pi}\;[n] + 5\times 50e^{-6}\times(12-v_o\,[n]) \\ D\;[n+1] &= D_{\rm pi}\;[n+1] + 0.03\times(12-v_o\,[n]) \end{aligned} \tag{49}$$

where $D_{\rm pi}[n+1]$ is the state variable corresponding to the integral link in the $n+1$th cycle, and $D[n+1]$ is the duty cycle in the $n+1$th cycle. The transient response of the prototype with stepping load is tested to verify the effectiveness of controller parameter design and the dynamic characteristics of the different modulated converters. Fig. 40 shows the operating waveform as the load stepping from 50% to 100%. For LEM, the valley value of the drop voltage to the peak value of the overshoot voltage is 5.2 V, and the settling time is 2.75 ms. For the TEM, the peak–peak voltage is 4.5 V, and the settling time is 1.86

m*s*, which indicates that the stability of the trailing-edge modulated converter is better. Meanwhile, the experimental waveform shown in Fig. 40 is consistent with the simulation waveform shown in Fig. 22, verifying the correctness of the theoretical analysis and model.

VII. Conclusion

The CSDM can accurately describe the characteristics of a digitally controlled buck converter, but the model is highly complex and not intuitive enough. By applying the approximate method of the CSDM, this article establishes the SOGEC of the buck converter for the LEM and TEM. Since SOGEC can accurately retain the information of the sampling points of the state variables, the operating waveform of the equivalent circuit can have an accurate prediction of the operating waveform of the detailed switching circuit even at an unstable operating point, without taking into account the ripple ratio of the state variable. On this basis, the delay characteristics of digital control are analyzed and the z-domain small-signal model based on the characteristics of digital control is derived. The frequency response from control to output shows that when the duty cycle is lower than 50%, the phase margin is larger with TEM. In addition, the roots of the characteristic equations are studied to analyze the stability of the buck converter. Then, the effects of the controller parameters k_p, k_i, and k_d, input voltage, load, energy storage element parameters, and parasitic parameters on the stability of the system are explained in detail. At the same time, how the different modulations affect the stability of the system is explained in detail. The TEM and the LEM have an opposite changing trend of stability boundaries with the change of duty cycle. The reason is the influence of modulation delay. When the steady-state duty cycle is 50%, the system stability is the same with different modulations. Therefore, when the duty cycle is less than 50%, the TEM should be selected to reduce the system delay to improve the system stability. Finally, the controller is designed according to the theoretical analysis, and the correctness and effectiveness of theoretical results are verified through the PLECS simulation and experiment platform of the circuit.

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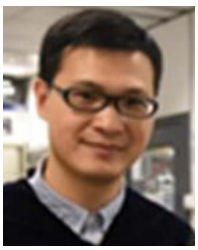

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