Piecewise-Approximated Time Domain Analysis of *LLC* Resonant Converter Considering Parasitic Capacitors and Deadtime

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***Abstract*—*LLC* resonant converters are widely used in high power density and high efficiency applications. Practically, the parasitic capacitors of MOSFETs and diodes, the stray capacitor of the high frequency transformer, and the dead time will have a great impact not only on the steady state resonant waveforms but also on the zero voltage switching-ON (ZVS-ON) of the MOSFETs. This article presents a piecewise-approximated time domain analysis of *LLC* both considering the parasitic/stray capacitors and the dead time. On this basis, not only the accurate steady state resonant waveforms, but also the ZVS-ON boundary can be obtained, which will guide the parameter design, and switching frequency/dead time configuration instead of slow and cumbersome simulations. The major applications of the presented analysis, including the resonant/switching waveform illustration, the critical dead time calculation, and the optimal converter design are verified by a 500 W asymmetric half bridge *LLC* experimental prototype.**

***Index Terms*—*LLC* resonant converter, parasitic capacitor, zero voltage switching-ON.**

I. Introduction

THE *LLC* resonant converters are widely applied in server power supplies [1], [2], data centers [3], [4], [5], LED drivers [6], [7], [8], onboard battery chargers [9], [10], [11], etc. due to the advantage of wide voltage gain, high power density, ZVS-ON for MOSFETs, and smooth waveforms.

The analysis methods of *LLC* can be divided into three approaches: the frequency domain analysis; the frequency domain analysis with time domain correction; and the time domain analysis. In frequency domain analysis, fundamental harmonic approximation (FHA) [12], [13] is widely used due to its simple concept. FHA assumes all the resonant waveforms are sinusoidal and shows good accuracy when the switching frequency f_s is close to the series resonant frequency f_r. However, the accuracy of FHA degrades when f_s moves away from f_r. As for the frequency domain analysis with time domain correction, Oeder et al. [14], Liu et al. [15] consider the phase lag, Ivensky et al. [16] adjusts the load factor to compensate for the error. However, the derivation procedure is complicated and the accuracy improvement is not obvious. In time domain analysis, according to different resonant conditions in one switching cycle, *LLC* can be divided into several stages and the operation of *LLC* can be summarized as different operation stage trajectories (OSTs). Compared to the frequency domain methods, the accuracy is improved at the cost of calculation complexity.

Most of the previous articles have focused on the analysis and design of the *LLC* with pulse frequency modulation, including the circuit parameter design [2], [3], the soft-start process [17], [18], the burst mode [19], and light load efficiency improvement [20]. However, the above analyses are usually based on the ideal *LLC* ignoring the parasitic capacitors and dead time. Practically, these two factors play a critical role in the performance of the *LLC*. Ren et al. [21] points out that the experimental prototype of a 1 MHz *LLC* failed ZVS-ON even though it satisfies the previous ZVS-ON constraints. The impact of secondary parasitic capacitors on ZVS-ON transition is analyzed in [22], [23], and [24], but the classification is not comprehensive. In the above articles, only the parasitic capacitors of MOSFETs C_{oss} or diodes C_d are taken into consideration while the stray capacitor C_s of the HFT is omitted. Blanken [25], Prieto et al. [26], and Saket et al. [27] give the derivation, calculation, and optimization of the stray capacitors based on the physical models considering different winding dispositions. Wang et al. [28] considers the stray capacitor of the HFT to enhance the efficiency of the *LLC*. Shafiei et al. [29] analyze the resonant converter based on a high-order transformer model. Considering the nonlinear parasitic capacitor of the MOSFETs, the current-based and energy-based ZVS-ON criteria are proposed in [30], [31], [32], [33], [34], and [35]. During these processes, numerical integration is inevitable, which significantly increases the complexity.

In summary, the FHA method is not accurate to analyze the effect of the parasitic capacitors and dead time. All the parasitic capacitors are not fully considered in the exiting time domain methods. Some articles only discussed special cases, which are

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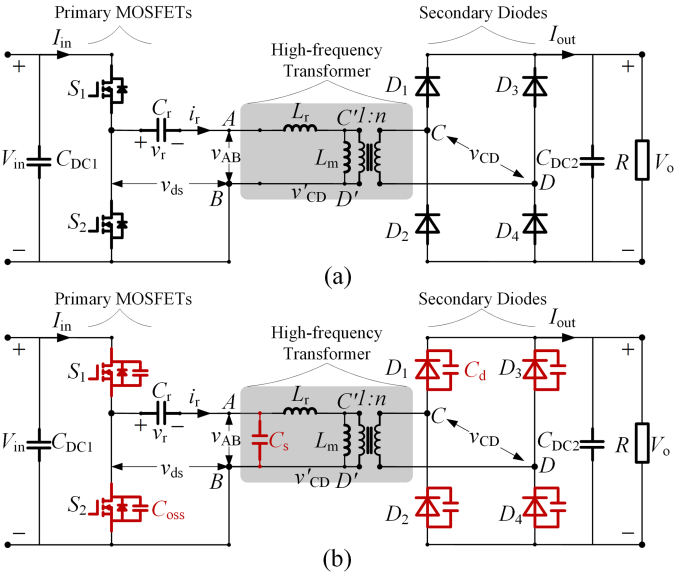

Fig. 1. Topology of the AHB-*LLC*. (a) Ignoring the parasitic capacitors. (b) Considering the parasitic capacitors.

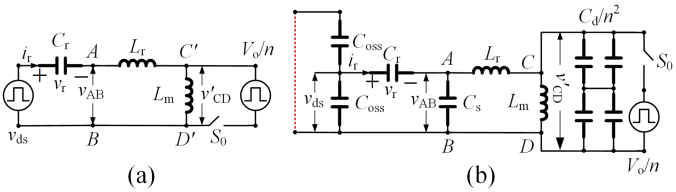

Fig. 2. Simplified equivalent circuit of the AHB-*LLC* resonant tank. (a) Ignoring the parasitic capacitors. (b) Considering the parasitic capacitors.

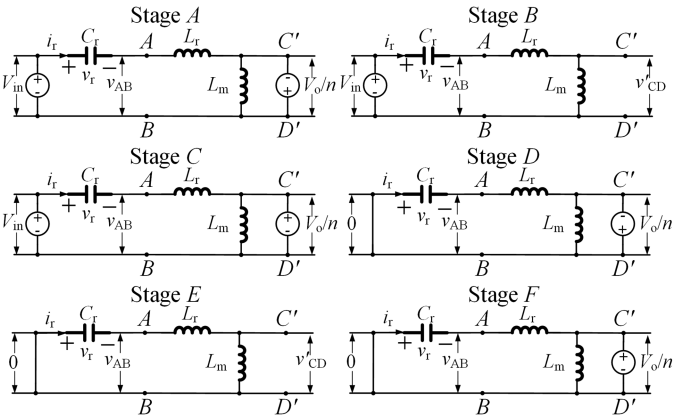

Fig. 3. Stages of the ideal AHB-*LLC* in one switching cycle.

not comprehensive. Only numerical solutions can be obtained for the articles based on the integration-based analysis.

The major contributions of this article can be summarized as follows.

1) A piecewise-approximated time domain analysis of *LLC* considering all the parasitic capacitors and dead time is proposed based on the major resonant process.
2) The method to illustrate the operation/switching waveforms of *LLC*, both at the steady state and during the dead time. The optimal dead time calculation is also presented.
3) Optimal design flowchart of the *LLC* without iterations to speed up the design process.

The proposed method made a compromise between accuracy and calculation complexity. The calculation complexity is only slightly increased but the accuracy is sufficient.

The rest of this article is organized as follows. Operation stages and OSTs of the ideal *LLC* are presented in Section II as the basis for further analysis and derivation. The time domain analysis of *LLC* considering the parasitic capacitors and dead time is presented in Section III. The resonant waveform calculation and optimal design process are discussed in Section IV, which are verified by the experimental results in Section V. Finally, Section VI concludes the article.

II. Time Domain Analysis of Ideal LLC

This section is based on the time domain analysis of the ideal *LLC* [33] to be improved in the following sections, establishes important terms and notation, and provides the basic derivation.

A. *Operation Stages of* LLC

The topology of the simplest asymmetric half bridge *LLC* (AHB-*LLC*) is depicted in Fig. 1. The AHB-*LLC* consists of two dc capacitors $C_{\rm DC1}$, $C_{\rm DC2}$, two MOSFETs S_1-S_2, four diodes D_1-D_4, a resonant tank, and an HFT with 1:n turn ratio. The switching period is $T_s = 1/f_s$, and the dead time is t_d. The resonant tank is formed by the resonant capacitor C_r, the resonant inductor L_r, and the excitation inductor L_m. In some applications, the leakage inductor of the HFT is adopted as the resonant inductor to increase the power density (depicted as the gray area in Fig. 1). The topology of AHB-*LLC* considering the parasitic capacitors is depicted in Fig. 1(b). The lumped stray capacitor C_s is considered to the left-hand side of L_r. In some articles, C_s is presented paralleled to L_m. These two equivalent circuits of the HFTs are equivalent by arranging the values of the inductances/ capacitances.

The input and output voltages of the HFT are denoted as v_{AB} and v_{CD}, respectively. The reflected value of v_{CD} from secondary to primary is denoted as v'_{CD}. The input voltage and output voltage of the AHB-*LLC* are denoted as $V_{\rm in}$, and $V_{\rm out}$, respectively.

The simplified equivalent circuit of the resonant tank ignoring/considering the parasitic capacitors and t_d are depicted in Fig. 2. The input voltage of the resonant tank is also the square wave drain-source voltage $v_{\rm ds}$ of S_2. The output voltage of the resonant tank is a square wave voltage source $V_{\rm o}/n$. S_0 is the equivalent switch for secondary diodes. When $S_0 = 1$, $v'_{CD} = V_{\rm o}/n$, D_1 and D_4 conduct; When $S_0 = 1$, and $v'_{CD} = -V_{\rm o}/n$, D_2 and D_3 conduct; When $S_0 = 0$, four diodes turn OFF. According to the value of v_{AB}, v'_{CD}, and S_0, the operation of the ideal AHB-*LLC* can be classified into six stages named from stage A to stage F in one switching cycle, and the equivalent circuits are depicted in Fig. 3. In every stage, the resonant current $i_r(t)$, the

excitation current $i_m(t)$, and the resonant voltage $v_r(t)$ are used to describe the resonant process.

In stage A, L_r and C_r are in resonance. Denote the resonant frequency, resonant period, and characteristic impedance as ω_r, T_r, and Z_r where

$$\omega_r = \sqrt{\frac{1}{L_r C_r}}, T_r = 2\pi\sqrt{L_r C_r}, Z_r = \sqrt{\frac{L_r}{C_r}}. \tag{1}$$

The expressions of resonant current and voltage are given as

$$i_{rA}(t) = \left(\frac{V_{\text{in}} - v_{rA}(0)}{Z_r} + \frac{V_{\text{o}}}{nZ_r}\right)\sin(\omega_r t) + i_{rA}(0)\cos(\omega_r t) \tag{2}$$

$$v_{rA}(t) = V_{\text{in}} + \frac{V_{\text{o}}}{n} - \left(V_{\text{in}} - v_{rA}(0) + \frac{V_{\text{o}}}{n}\right)\cos(\omega_r t) + i_{rA}(0) Z_r \sin(\omega_r t). \tag{3}$$

Here, L_m is negatively clamped by $v'_{CD} = -V_{\text{o}}/n$, and $i_m(t)$ decreases linearly from the initial value. Hence, the expressions of excitation voltage and current are given as

$$v_{mA}(t) = -\frac{V_{\text{o}}}{n} \tag{4}$$

$$i_{mA}(t) = i_{mA}(0) - \frac{V_{\text{o}}\omega_r t}{nL_m}. \tag{5}$$

Stage B is different from stage A as L_m joins the resonant process. Denote the resonant frequency, resonant period, and characteristic impedance as ω_m, T_m, and Z_m where

$$\omega_m = \sqrt{\frac{1}{(L_m + L_r)\, C_r}}, T_m = 2\pi\sqrt{(L_m + L_r)\, C_r},$$
$$Z_m = \sqrt{\frac{L_m + L_r}{C_r}}. \tag{6}$$

The expressions of $i_r(t)$, $i_m(t)$, and $v_r(t)$ in stage B are given as

$$i_{rB}(t) = i_{mB}(t) = \left(\frac{V_{\text{in}} - v_{rB}(0)}{Z_{\text{m}}}\right)\sin(\omega_m t) + i_{rB}(0)\cos(\omega_m t) \tag{7}$$

$$v_{rB}(t) = V_{\text{in}} - (V_{\text{in}} - v_{rB}(0))\cos(\omega_m t) + i_{rB}(0) Z_m \sin(\omega_m t). \tag{8}$$

The excitation voltage $v_{mB}(t)$ is given as

$$v_{mB}(t) = \frac{L_m}{L_m + L_r}\left((V_{\text{in}} - v_{rB}(0))\cos(\omega_m t) - i_{rB}(0) Z_m \sin(\omega_m t)\right). \tag{9}$$

Denote the duration of stage B as t_B, $v_{mB}(t)$ should not exceed the output voltage to prevent the conduction of output diodes, and the inequality constraint is expressed as

$$v_{mB}(t) \le \frac{V_{\text{o}}}{n} \forall 0 < t < t_B. \tag{10}$$

Stages C, D, and F are similar to stage A because they are with identical resonant frequency and characteristic impedance. The expressions of $i_r(t)$, $i_m(t)$, and $v_r(t)$ from stages C to stage F can be found in [6].

B. Operation Stages Trajectories of AHB-LLC

Different combinations of stages form the operation stage trajectory (OST). For instance, OST AC-DF indicates the AHB-*LLC* enters stages A, C, D, and F sequentially. A hyphen is used to denote the gate signal transition of S_2.

The boundary equations consist of the continuity equations and the symmetric equations. If we use *X*, *Y* to denote two different adjacent stages, the continuity equations are given as

$$i_{rX}(t_X) = i_{rY}(0), i_{mX}(t_X) = i_{mY}(0), v_{rX}(t_X) = v_{rY}(0). \tag{11}$$

If *Y* is the last stage in while *X* is the first stage, the symmetric equations are given as

$$i_{rX}(0) = i_{rY}(t_Y), i_{mX}(0) = i_{mY}(t_Y), v_{rX}(0) = v_{rY}(t_Y). \tag{12}$$

The duration balance equation is given as

$$t_A + t_B + t_C = DT_s, t_D + t_E + t_F = (1 - D)\, T_s \tag{13}$$

where *D* is the duty ratio.

The average input power p_{in} and output power p_{out} are given as

$$p_{\text{in}} = V_{\text{in}} f_s \left(\int_0^{t_{\text{A}}} i_{rA}(t)dt + \int_0^{t_{\text{B}}} i_{rB}(t)dt + \int_0^{t_{\text{C}}} i_{rC}(t)dt\right)$$

$$p_{\text{out}} = \frac{V_{\text{o}} f_s}{n}\left(\int_0^{t_{\text{C}}} (i_{rC}(t) - i_{mC}(t))\, dt + \int_0^{t_{\text{F}}} (i_{rF}(t) - i_{mF}(t))\, dt\right) - \frac{V_{\text{o}} f_s}{n}\left(\int_0^{t_{\text{A}}} (i_{rA}(t) - i_{mA}(t))\, dt + \int_0^{t_D} (i_{\text{rD}}(t) - i_{mD}(t))\, dt\right)$$

$$p = p_{\text{in}} = p_{\text{out}}. \tag{14}$$

According to the stage equations and OST equations, the resonant process of the AHB-*LLC* is equivalent to solving an equation set of (f_s, *D*, V_o, *p*). Given three of the four unknowns and one can solve the fourth unknown. For instance, numerical solving the equation sets (1)–(14), and it outputs t_C, t_B, t_A, $i_{rC}(0), i_{rB}(0), i_{rA}(0), v_{rC}(0), v_{rB}(0), v_{rA}(0), i_{mC}(0), i_{mB}(0)$, and $i_{mA}(0)$. With these initial values, the ideal resonant waveforms can also be illustrated.

III. Time Domain Analysis of LLC Considering Parasitic Capacitors and Dead Time

From the above analysis, there are three resonant elements in the resonant tank, and the ideal *LLC* model is third order at most. When C_s is taken into consideration, the above resonant process is increased by one order. During t_d, C_{oss} and C_d join the resonant process and the model is increased to sixth order.

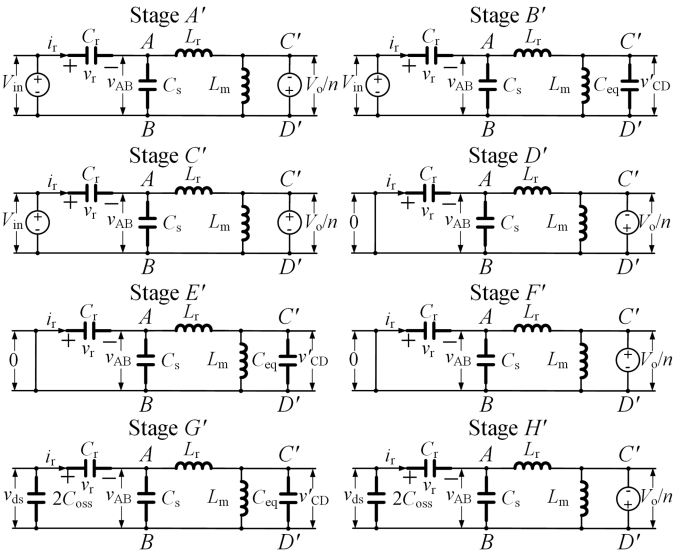

Fig. 4. Stages of the AHB-*LLC* in one switching cycle considering parasitic capacitors and t_d.

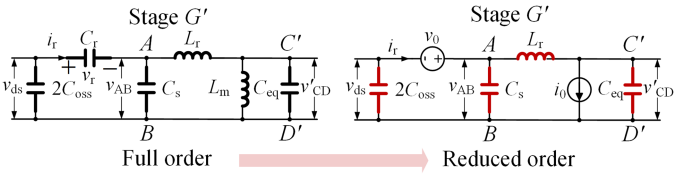

Fig. 5. Full order and reduced order ac equivalent circuits in stage G'.

When considering t_d, there are eight stages in total. These eight stages are named from A' to H', and the equivalent circuits are depicted in Fig. 4. In stages A', C', D', and F' when both the input and output of the resonant tank are clamped, C_s and C_r join the resonance. The effect brought by C_s is inconspicuous since $C_s << C_r$. Hence, it is reasonable to ignore the effect of C_s, and the equations in stages A', C', D', and F' will be equivalent to the equations in stages A, C, D, and F.

During t_d, the resonant process can be divided into stage G' and stage H' depending on whether the diodes are clamped by the output (i.e., the conduction condition of S_0). To simplify the analysis, the following assumptions are made in this article.

1) The nonlinear parasitic capacitances $C_{\rm oss}$ and C_d are replaced with their equivalent linear values.
2) The drain to source resistance $r_{\rm ds\text{-}on}$ of MOSFETs, winding resistance of the HFT, and the voltage drop of diodes are assumed to be zero.
3) $C_{\rm DC1}$ and $C_{\rm DC2}$ are ideal large enough, and the equivalent series resistances are zero.

A. Approximated Analysis on Stage G'

The full and reduced order ac equivalent circuits in stage G' are depicted in Fig. 5. In stage G', both the two MOSFETs turn OFF and $i_r(t)$ needs to charge/ discharge the two parasitic capacitors $2C_{\rm oss}$. At the same time, C_d joins the resonant process. The equivalent parasitic capacitance $C_{\rm eq}$ is given as

$$C_{\rm eq} = \frac{C_d}{n^2}. \tag{15}$$

Because there are six resonant elements L_r, L_m, C_r, C_s, $2C_{\rm oss}$, and $C_{\rm eq}$, the resonant circuit is a sixth order circuit. If we focus on the major resonant process, the following two approximations can be made.

1) C_r is approximated to a voltage source $v_0 = v_{rG}(0) - V_{\rm in}/2$ since C_s, $2C_{\rm oss}$, and $C_{\rm eq}$ are much smaller than C_r.
2) L_m is approximated to a current source $i_0 = i_{mG}(0)$ since L_m is much greater than L_r.

These two assumptions are reasonable because $t_{\rm d}$ is much shorter than T_s. During t_d, $i_r(t)$, as well as $v_r(t)$, can be regarded as a constant. With these two approximations, the resonant components are colored in red in the reduced order equivalent circuit (the equivalent circuit in stage G' is a third order circuit because $2C_{\rm oss}$ and C_s are in parallel).

Denote the resonant frequency, resonant period, and characteristic impedance as ω_{d1}, T_{d1}, and Z_{d1} where

$$\begin{aligned}
\omega_{d1} &= \sqrt{\frac{(2C_{\rm oss}+C_s)+C_{\rm eq}}{(2C_{\rm oss}+C_s)\,C_{\rm eq}L_r}},\\
T_{d1} &= 2\pi\sqrt{\frac{(2C_{\rm oss}+C_s)\,C_{\rm eq}L_r}{(2C_{\rm oss}+C_s)+C_{\rm eq}}}\\
Z_{d1} &= \sqrt{\frac{L_{\rm r}\,(2C_{\rm oss}+C_s+C_{\rm eq})}{(2C_{\rm oss}+C_s)\,C_{\rm eq}}}.
\end{aligned} \tag{16}$$

The expressions of $i_{\rm r}(t)$, $v_{\rm ds}(t)$ and $v'_{\rm CD}(t)$ are given as

$$\begin{aligned}
i_r(t) = {} & \frac{2C_{\rm oss}+C_s}{2C_{\rm oss}+C_s+C_{\rm eq}}i_0 + \frac{C_{\rm eq}i_0}{2C_{\rm oss}+C_s+C_{\rm eq}}\\
& \times\cos(\omega_{d1}t) - \frac{v_0}{L_r\omega_m}\sin(\omega_{d1}t)
\end{aligned} \tag{17}$$

$$\begin{aligned}
v_{\rm ds}(t) = {} & V_{\rm in} - \frac{i_0 t}{2C_{\rm oss}+C_s+C_{\rm eq}} - \frac{C_{\rm eq}v_0}{2C_{\rm oss}+C_s+C_{\rm eq}}\\
& \times\cos(\omega_{d1}t)\\
& - \frac{C_{\rm eq}i_0}{(2C_{\rm oss}+C_s)\,(2C_{\rm oss}+C_s+C_{\rm eq})\,\omega_{\rm m}}\sin(\omega_{d1}t)\\
& + \frac{C_{\rm eq}v_0}{2C_{\rm oss}+C_s+C_{\rm eq}}
\end{aligned} \tag{18}$$

$$\begin{aligned}
v'_{CD}(t) = {} & -\frac{V_{\rm o}}{n} + \frac{i_0 t}{2C_{\rm oss}+C_s+C_{\rm eq}}\\
& - \frac{i_0}{2C_{\rm oss}+C_s+C_{\rm eq}}\sin(\omega_{d1}t)\\
& + \frac{(2C_{\rm oss}+C_s)\,v_0}{2C_{\rm oss}+C_s+C_{\rm eq}}\cos(\omega_{d1}t)\\
& + \frac{(2C_{\rm oss}+C_s)\,v_0}{2C_{\rm oss}+C_s+C_{\rm eq}}.
\end{aligned} \tag{19}$$

TABLE I
ELECTRIC PARAMETERS OF THE AHB-LLC

Item	Parameters
Input voltage V_{in}	300 V
Load R_L	120 Ω
Resonant capacitor C_r	621 nF
Resonant inductor L_r	2.86 μH
Excitation inductor L_m	500 μH
HFT turn ratio n	1: 2
MOSFET parasitic capacitor C_{oss}	180 pF
Diode parasitic capacitor C_d	290 pF
HFT parasitic capacitor C_s	350 pF

From (18) and (19), $v_{ds}(t)$ and $v'_{CD}(t)$ are decomposed into the dc part, the linear part, and the resonant part. The dc parts of $v_{ds}(t)$ and $v'_{CD}(t)$ are V_{in} and V_o/n. The linear parts of $v_{ds}(t)$ and $v'_{CD}(t)$ are given as

$$v_{ds-linear}(t) = -v'_{CD-linear}(t) = -\frac{i_0 t}{2C_{oss} + C_s + C_{eq}}. \tag{20}$$

Denote the duration of stage G' as t_{d1}, if t_d is sufficient, at the end of stage G', there is

$$v'_{CD}(t_{d1}) = \frac{V_o}{n} \tag{21}$$

t_{d1} can be obtained by numerical solving the transcendental (21). At the same time, one can also calculate the zero crossing time t_{d2} of $v_{ds}(t)$ by solving $v_{ds}(t_{d2}) = 0$. An AHB-*LLC* example is used to exam how the parasitic components affect the resonant waveform under different f_s and t_d. The electric parameters of the AHB-*LLC* (also equivalent to the experimental prototype) are given in Table I.

There are four possibilities in stage G' according to the relation of t_{d1} and t_{d2}. The calculated waveforms of $v_{ds}(t)$ and $v'_{CD}(t)$ are depicted in Fig. 6 where the solid red and blue lines denote $v_{ds}(t)$ and $v'_{CD}(t)$. The dashed lines denote the linear parts in $v_{ds}(t)$ and $v'_{CD}(t)$. The x-axis is chosen as the normalized value of t_d (in the four cases, the base values of t_d are 500 ns, 1 μs, 800 ns, and 744 ns, respectively) for a clear illustration.

1) *Case 1:* $t_{d1} > t_d$ and $t_{d2} > t_d$. This case usually occurs in short t_d condition. In this case, $v_{ds}(t_d)$ and $v'_{CD}(t_d)$ are still positive. An example of $f_s = 100$ kHz, $t_d = 500$ ns is depicted in Fig. 6(a). Because there is $v_{ds}(t_d) = 84.2$ V, $v'_{CD}(t_d) = 87.9$ V, the MOSFETs suffer from hard switching and the diodes suffer from extreme reverse recovery loss.
2) *Case 2:* $t_d > t_{d2} > t_{d1}$. This case usually occurs in long t_d condition. Typical waveforms of $v_{ds}(t)$ and $v'_{CD}(t)$ when $f_s = 100$ kHz, $t_d = 1$ μs are depicted in Fig. 5(b). In this case, there is $t_{d1} = 708$ ns, $t_{d2} = 771$ ns. Because $v_{ds}(t_{d1})$ is still positive, the AHB-*LLC* will enter stage H'.
3) *Case 3:* $t_d > t_{d1} > t_{d2}$. This case usually occurs in long T_s and short t_d condition. Typical waveforms of $v_{ds}(t)$ and $v'_{CD}(t)$ when $f_s = 90$ kHz, $t_d = 800$ ns are depicted in Fig. 6(c). In this case, there is $t_{d1} = 647$ ns, $t_{d2} = 617$ ns. $v'_{CD}(t_{d2}) = 137.4$ V < 150 V. Since stage G' is not ended, the $2C_{oss}$ will be charged in reverse direction.

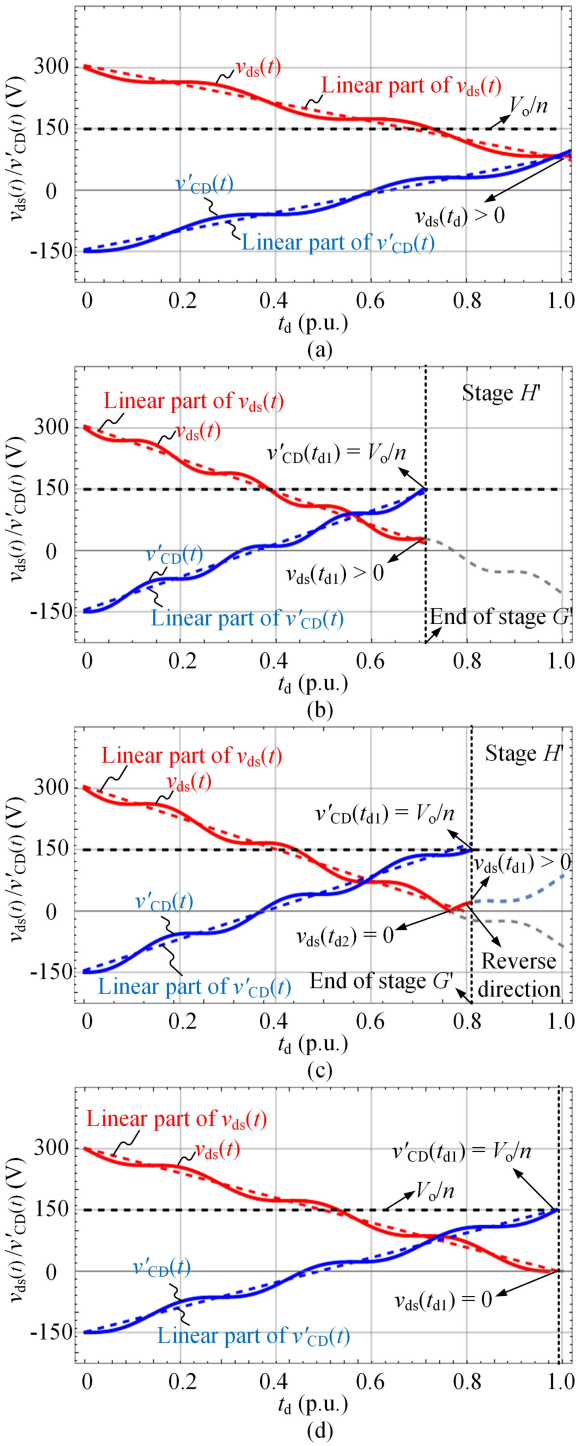

Fig. 6. Four possibilities in stage G'. (a) $t_{d1} > t_d$ and $t_{d2} > t_d$. (b) $t_d > t_{d2} > t_{d1}$. (c) $t_d > t_{d1} > t_{d2}$. (d) $t_d = t_{d2} = t_{d1}$.

4) *Case 4:* $t_d = t_{d2} = t_{d1}$. This case occurs in a specified t_d condition. In this case, t_d needs to be carefully tuned to meet $t_d = t_{d2} = t_{d1}$. When $f_s = 100$ kHz, the results are given as $t_d = 744$ ns, and $v_0 = 2.5$ V. The resonant waveforms are depicted in Fig. 6(d).

There are multiple factors related to t_{d1} and t_{d2}. These factors can be classified into two groups, the circuit parameter (C_{oss},

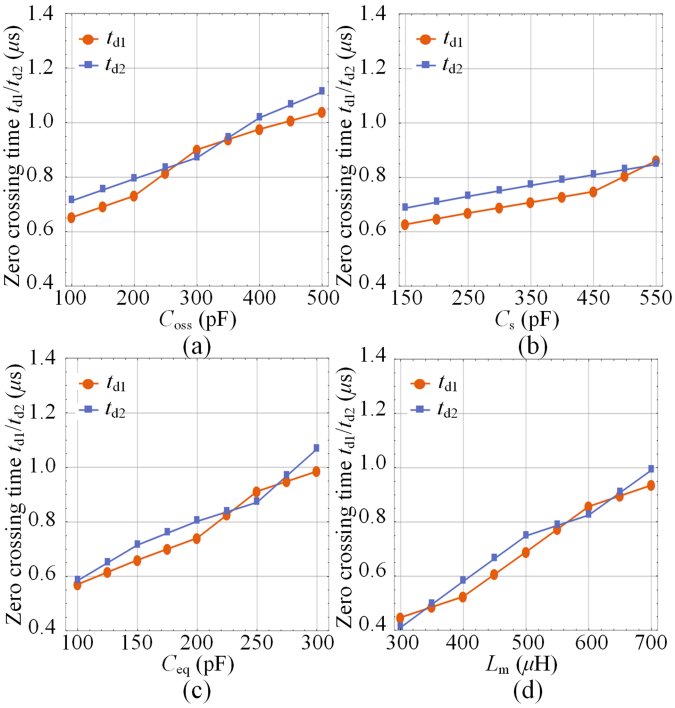

Fig. 7. The relation of zero crossing time t_{d1}, t_{d2} against different circuit parameters. (a) C_{oss}. (b) C_{eq}. (c) C_s. (d) L_m.

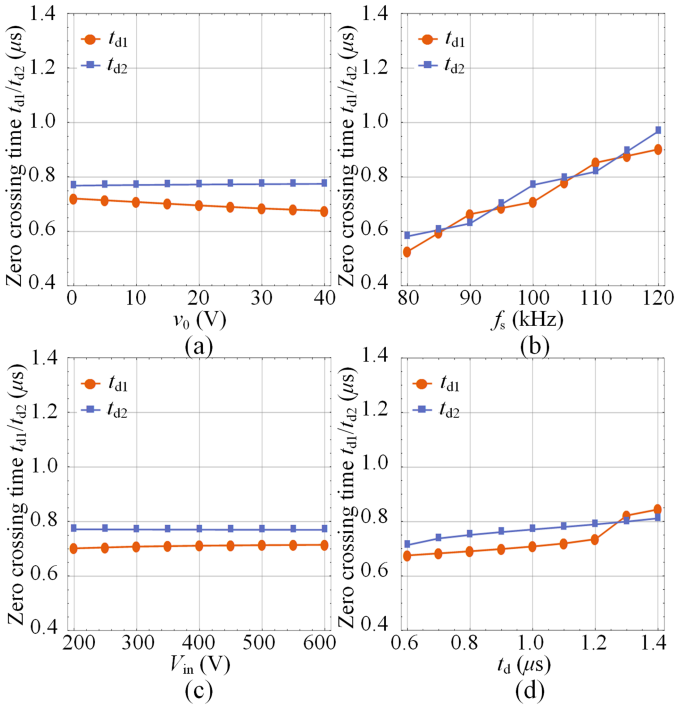

Fig. 8. Relation of zero crossing time t_{d1}, t_{d2} against different control parameters. (a) v_0. (b) f_s. (c) V_{in}. (d) t_d (assuming C_{oss} and C_d are constant when V_{in} varies).

C_{eq}, C_s, and L_m), and the control parameter (v_0, f_s, V_{in}, and t_d). These relations are depicted in Figs. 7 and 8.

When C_{oss} and C_{eq} increases, a longer time is required to fully charge/ discharge these parasitic capacitors, leading to a longer t_{d1} and t_{d2}. Compared to C_{oss} and C_{eq}, the impact of C_s is much smaller since C_s do not have to be charged in this process. L_m also has a significant impact on t_{d1} and t_{d2}. Because L_m is almost inversely proportional to i_0, a larger L_m corresponds to a lower i_0, which requires a longer t_{d1} and $t_{d2}$to fully charge/discharge the parasitic capacitors. In Fig. 8, the curves of v_0 and V_{in} versus t_{d1} and $t_{d2}$are very flat, which indicate that both the input voltage and load condition are with weak impact on t_{d1} and t_{d2}. f_s and t_d are with a relatively strong impact on t_{d1} and t_{d2}because i_0 decreases with the increase of f_s and i.

B. Approximated Analysis on Stage H'

Generally, $t_d > t_{d2} > t_{d1}$ is satisfied in most conditions. At the end of stage G', $v_{ds}(t_{d1})$ is still positive and it will enter stage H'. The equivalent circuits of stage H' are depicted in Fig. 9.

In this stage, C_{eq} and L_m are clamped by the output. With a similar approximation approach, the reduced order circuit is depicted in the right part in Fig. 9. In the reduced order circuit, $2C_{oss}$ and C_s are in parallel.

Denote the resonant frequency, resonant period, and characteristic impedance as ω_{d3}, T_{d3}, and Z_{d3} where

$$\omega_{d3} = \sqrt{\frac{1}{(2C_{oss}+C_s)L_r}}, T_{d3} = 2\pi\sqrt{(2C_{oss}+C_s)L_r} \\ Z_{d3} = \sqrt{\frac{L_r}{2C_{oss}+C_s}}. \tag{22}$$

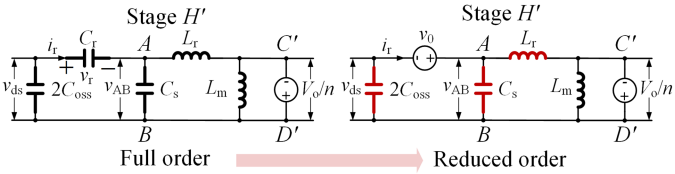

Fig. 9. Full order and reduced order ac equivalent circuits in stage H'.

The expression of $v_{ds}(t)$ is given as

$$v_{ds}(t) = v_0 + (v_{ds}(0) - v_0)\cos(\omega_{d3}t) - i_r(0)Z_{d3}\sin(\omega_{d3}t). \tag{23}$$

This process will continue until t_d ends. During this process, $v_{ds}(t)$ will cross zero a couple of times. The zero crossing time is crucial as it determines whether the ZVS-ON can be achieved.

When t_d is chosen as 1250 and 1150 ns, the key waveforms are depicted in Fig. 10. In Fig. 10(a), $v_{ds}(t_d)$ almost reaches the peak value, and ZVS-ON is failed. In Fig. 10(b), $v_{ds}(t_d)$ is still zero, and ZVS-ON is achieved.

C. Approximated Analysis on Stage B' and Stage E'

The equivalent circuits of stage B' and stage E' are depicted in Fig. 11.

When m is greater than 50, the resonant frequency of L_r, L_m, C_r (i.e., ω_m) is low, and the resonant waveforms change slowly during this process. Hence, C_r can also be regarded as a voltage source v_1, where $v_1 = v_{rB}(0)$. $i_m(t)$ can be approximated to a

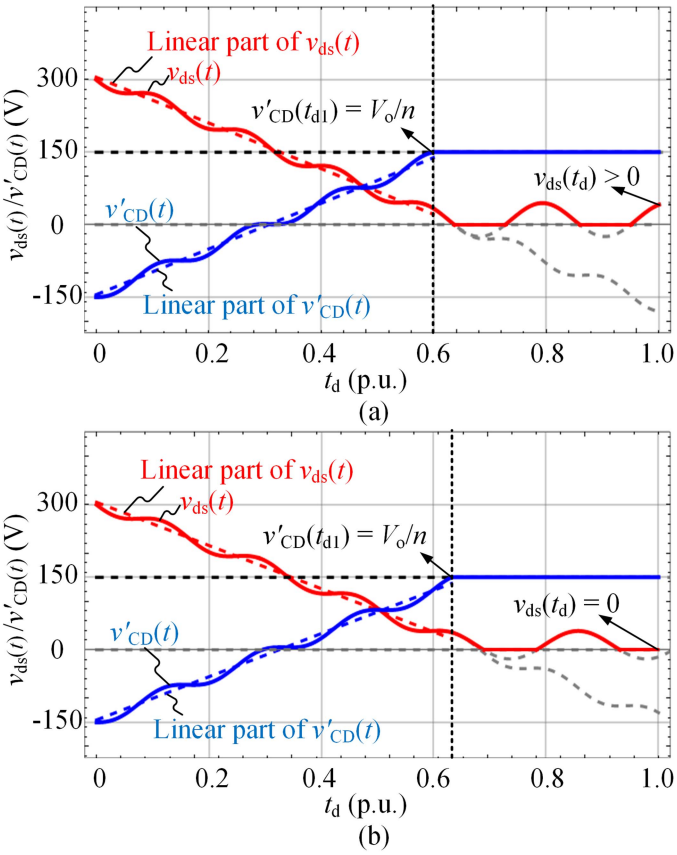

Fig. 10. Key waveforms in stage H'. (a) $t_d = 1250$ ns. (b) $t_d = 1150$ ns.

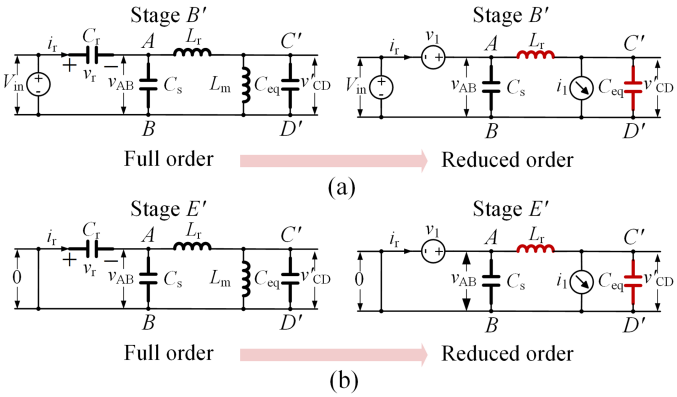

Fig. 11. Full order and reduced order ac equivalent circuits in (a) Stage B'. (b) Stage E'.

$r_{\rm amp}$ current source $i_1(t)$ where

$$i_1(t) = i_1(0) - \frac{V_o \omega_r t}{n L_m}. \tag{24}$$

In this resonant process, there is $v_{AB} = V_{\rm in} + v_1$ in stage B' and $v_{AB} = v_1$ in stage E'. The resonant elements are L_r and $C_{\rm eq}$.

In stage B', the resonant frequency, resonant period, and characteristic impedance are denoted as ω_b, T_b, and Z_b where

$$\omega_b = \sqrt{\frac{1}{C_{\rm eq} L_r}}, T_b = 2\pi\sqrt{C_{\rm eq} L_r}, Z_b = \sqrt{\frac{L_r}{C_{\rm eq}}}. \tag{25}$$

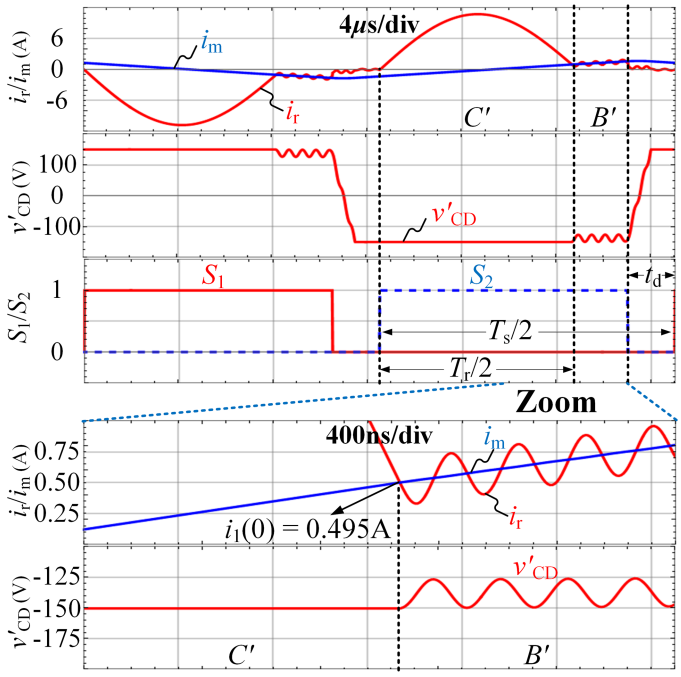

Fig. 12. Typical waveforms of OSTs including stages C' and B'.

The expressions of $v'_{CD}(t)$ and $i_r(t)$ are given as

$$v'_{CD}(t) = v_1 \cos(\omega_b t) - \frac{V_o}{n} - v_1. \tag{26}$$

$$i_r(t) = -\frac{v_1}{Z_b} \sin(\omega_b t) + i_r(0) + \frac{V_{\rm in} t}{L_m}. \tag{27}$$

The initial resonant current $i_1(0)$ can be approximately calculated as

$$i_1(0) \approx \frac{V_{\rm in}(T_s - t_d) f_s}{8 L_m f_r}. \tag{28}$$

The equations in stage E' can be obtained in a similar way and it is not repeated here.

Typical waveforms of OSTs including stages C' and B' are depicted in Fig. 12 where the control parameter is given as $f_s = 80$ kHz, and $t_d = 1.2$ μs. Under this control parameter, $t_{C'}$ and $t_{B'}$ are given as $t_{C'} = T_r/2 = 4.1$ μs, $t_{B'} = (T_s/2 - T_r/2 - t_d) = 1.05$ μs. $i_1(0)$ can be calculated by (28), which is 0.495 A. v_1 reveals the ripple of $v'_{cd}(t)$, which is 13V in this case. According to the relation of T_b and $t_{B'}$ ($t_{B'}/T_b \approx 4$), there are around four resonant switching cycles in stage B' (see the zoomed waveforms in the bottom of Fig. 12).

IV. Resonant Waveform Calculation and Optimal Converter Design

According to the proposed piecewise-approximation method, the critical dead time can also be derived. On this basis, an optimal converter design is introduced in this Section.

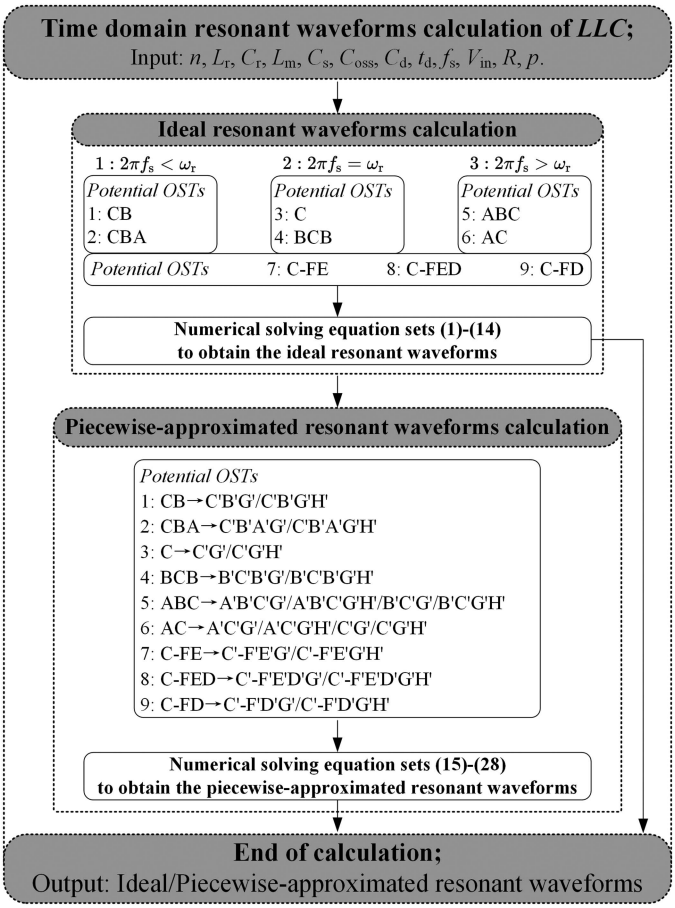

Fig. 13. Algorithm chart of the time domain resonant waveforms calculation of *LLC*.

A. Accurate Resonant Waveform Calculation

The piecewise-approximated method is proposed to solve the equation sets in different stages, and the algorithm flowchart is depicted in Fig. 13.

There are two steps in the algorithm flowchart.

1) Ignore all the parasitic capacitors ($C_{\rm oss}$, C_d, and C_s) and set t_d to zero to calculate the ideal resonant waveforms. There are nine potential OSTs for the ideal *LLC*. The ideal resonant waveforms can be solved via (1)–(14).
2) Considering the parasitic capacitors and t_d, and calculate the piecewise-approximated resonant based on the calculated results of the ideal waveforms. If one OST contains stages B or E, recalculate the resonant waveforms via (24)–(28), and replace the two stages with stages B' or E'. Take $t_{\rm d}$ into consideration and calculate the resonant waveforms in stages G' and H' via (15)–(23). When t_d is considered, the potential OSTs are changed (i.e., from CB to C'B'G' or C'B'G'H'). Generally speaking, one can assume stage H' exists. If the calculated results show that the constraints are not met (e.g., the duration of stage H' is negative, or the calculation results do not converge within the predefined maximum iteration), C'B'G'H' is not valid.

To achieve ZVS-ON, t_d is recommended for the MOSFET when $v_{\rm ds}(t)$ cross zero for the first time. The critical dead time, $t_{d\text{-}cr}$, can be solved via $v_{\rm ds}(t_{d\text{-}cr})=0$. Hence, we will obtain the value of $t_{d\text{-}cr}$ related to the resonant parameters (L_r, C_r, L_m), control parameters (f_s, t_d), $V_{\rm in}$, parasitic capacitors ($C_{\rm oss}$, C_d, C_s), and load condition, etc.

B. Optimal LLC Resonant Converter Design Method

As for a well-designed *LLC* resonant converter, the impact of $t_{\rm d}$ on the voltage gain is tiny. The actual voltage gain is higher than 0.99 when the t_d/T_s is smaller than 5%. Consequently, t_d can be ignored during the design process. As pointed out in [10] and [36], the maximum voltage gain $M_{\max}$ should be high enough in the heaviest load condition while the minimum voltage gain $M_{\min}$ should be low enough in the lightest load condition. To meet the two critical operation conditions, the *LLC* can be designed based on the peak gain method. In [10] and [36], $M_{\rm Peak}$ is searched via solving the differential equation sets iteratively. Because the iteration process is the most time-consuming step during this process, we can fit the relations between power transmission P, switching frequency F, and inductor ratio $m=L_m/(L_m+L_r)$ to eliminate the iteration process. To simplify the analysis, we used the normalization qualities. The frequency base $f_{\rm Base}$, voltage base $V_{\rm Base}$, impedance base $Z_{\rm Base}$, current base $I_{\rm Base}$, power base $P_{\rm Base}$, and voltage gain M are given as

$$f_{\rm Base}=\frac{1}{2\pi\sqrt{L_rC_r}}, V_{\rm Base}=\frac{V_{\rm out}}{n}, Z_{\rm Base}=\sqrt{\frac{L_r}{C_r}}$$
$$I_{\rm Base}=\frac{nZ_r}{V_{\rm out}}, P_{\rm Base}=\frac{V_{\rm out}^2}{n^2Z_r}, M=\frac{V_{\rm out}}{nV_{\rm in}}. \quad (29)$$

The variables after normalization are represented by the corresponding capital letters. When $m=4$, the operation region of the ideal *LLC* is depicted in Fig. 14, where the red dashed line denotes the zero load voltage gain while the black dashed line denotes $M_{\rm Peak}$ and the corresponding power, $P_{\rm Peak}$. When m changes, the operation region of the ideal *LLC* also changes. To obtain the relation of $M_{\rm Peak}$–m and $P_{\rm Peak}$–m, we assume the functions of $M_{\rm Peak}(m, F)$ and $P_{\rm Peak}(m, F)$ as

$$P_{\rm Peak}=f_1(m,F), M_{\rm Peak}=f_2(m,F). \quad (30)$$

According to the precision and complexity of the fitting, we apply the quartic function fitting, where

$$\begin{cases} P_{\rm Peak}=f_1(m,F)=a_1(m)F^4+a_2(m)F^3+a_3(m)F^2 \\ \qquad +a_4(m)F+a_5(m), \\ M_{\rm Peak}=f_2(m,F)=b_1(m)F^4+b_2(m)F^3+b_3(m)F^2 \\ \qquad +b_4(m)F+b_5(m). \end{cases} \quad (31)$$

By observing the changing trends of $a_1(m)\sim a_5(m)$ and $b_1(m)\sim b_5(m)$, the coefficients in $a_1(m)\sim a_5(m)$ and

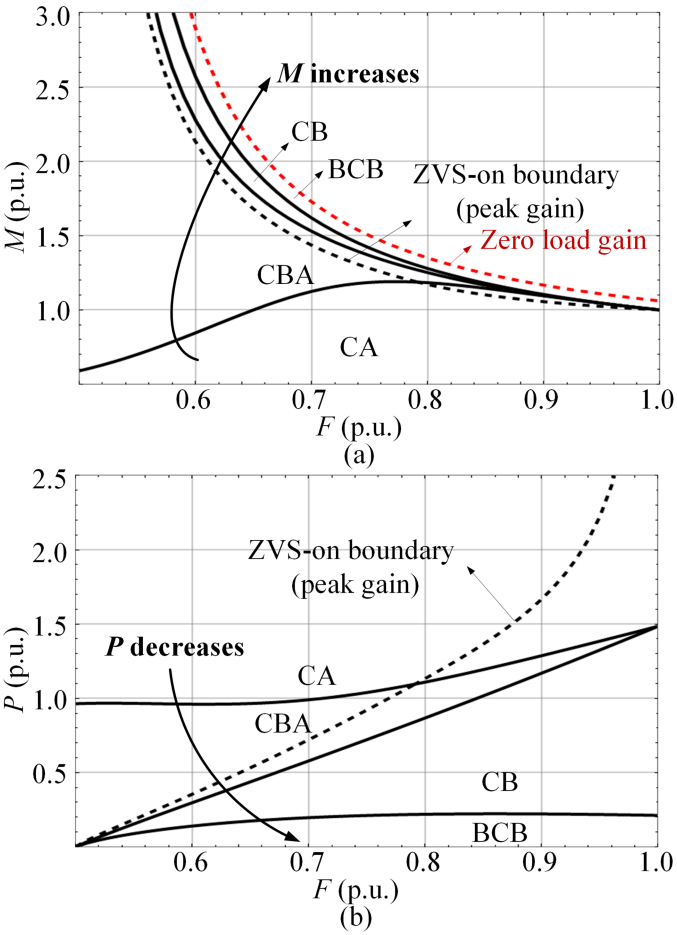

Fig. 14. Operation region of the ideal *LLC* when $m = 4$. (a) Frequency versus voltage gain relation. (b) Frequency versus power transformation relation.

$b_1(m)\sim b_5(m)$ can be determined as

$$\begin{cases} a_1(m) = 4.56m^2 - 94.5m + 744.4 \\ a_2(m) = -12.8m^2 + 265.1m - 2091 \\ a_3(m) = 13.27m^2 - 276m + 2178 \\ a_4(m) = -6.02m^2 + 125.4m - 990 \\ a_5(m) = 0.991m^2 - 20.72m + 164.7 \end{cases} \tag{32}$$

$$\begin{cases} b_1(m) = 15.26 + \frac{234.7}{1+(m/5.46)^{13.2}} \\ b_2(m) = -50 - \frac{787.8}{1+(m/5.38)^{12.5}} \\ b_3(m) = 62.4 + \frac{992.7}{1+(m/5.33)^{11.8}} \\ b_4(m) = -35.6 - \frac{558.2}{1+(m/5.27)^{11.1}} \\ b_5(m) = 8.95 + \frac{118.7}{1+(m/5.20)^{10.3}} \end{cases}. \tag{33}$$

The fitted functions, $P_{\text{Peak}}(m, F)$, $M_{\text{Peak}}(m, F)$, and the original data points are shown in Fig. 15. The conduction loss and output voltage regulation range are a pair of contradictions. To reduce the conduction loss while satisfying the required output voltage regulation range, m should be maximized. To take full advantage of the voltage boost capability of the *LLC*, the $M_{\min}$ point at light load can be designed at f_r and the $M_{\max}$ point at heavy load can be designed at the peak gain. When the switching

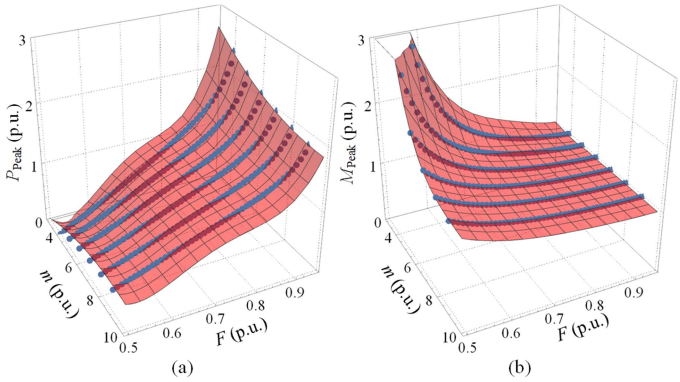

Fig. 15. Fitted surfaces and the original data points of the ideal *LLC* when $m = 4$. (a) $P_{\text{Peak}}(m, F)$. (b) $M_{\text{Peak}}(m, F)$.

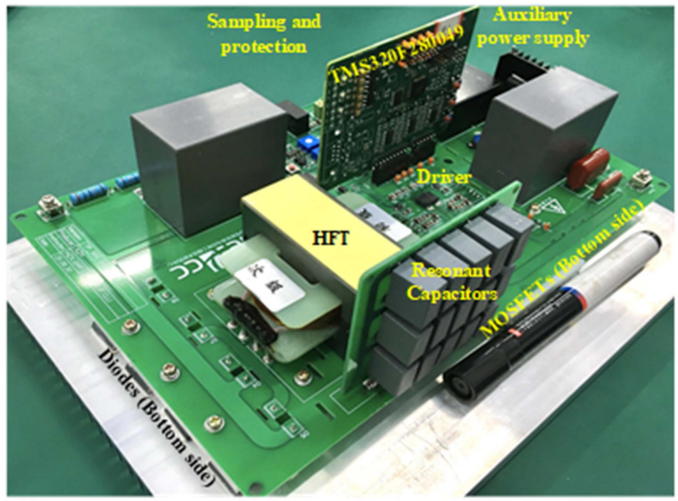

Fig. 16. Experimental prototype of the AHB-*LLC*.

frequency range ($f_{\min}$, $f_{\max}$), the input voltage range ($V_{\text{in-min}}$, $V_{\text{in-max}}$), the output voltage range ($V_{o\text{-min}}$, $V_{\text{o-max}}$), and the power transmission range ($p_{\min}$, $p_{\max}$) are given, the HFT turn ratio n, the resonant parameters (L_r, C_r, L_m) can be obtained via solving (34). The essence of this method is equivalent to the peak gain method in [10] and [36]. However, the time-consuming iteration process is eliminated. During the experiment, both the measured M_{Peak} and P_{Peak} are consistent with the modeled values within the margin of error (smaller than 5% relative error)

$$\begin{cases} \frac{V_{o-\min}}{V_{\text{in}-\max}} = n \wedge \frac{V_{\text{in}-\max} V_{o-\max}}{V_{\text{in}-\min} V_{o-\min}} = M_{\text{Peak}} \\ \frac{p_{\max}}{p_{\text{Base}}} = P_{\text{Peak}} \wedge F_{\max} = 1 \wedge F_{\min} = \frac{f_{s-\min}}{f_{s-\max}} \end{cases}. \tag{34}$$

V. Experimental Verifications

The experimental prototype is depicted in Fig. 16 and the circuit specifications are given in Table II. The parasitic capacitors of SiC MOSFET C2M0080170P C_{oss} and SiC diode C5D25170H C_{d} are approximated with their linear capacitors extracted from the datasheet. The specifications of the

TABLE II
SPECIFICATION OF THE EXPERIMENTAL PROTOTYPE

Component	Part number	Parameters
MOSFETs	C2M0080170P × 2	1.7 kV, 40 A, 80 mΩ
Diodes	C5D25170H × 4	1.7 kV, 34 A
MCU	TMS320F28062	Digital signal processer C2000 32-bit 90-MHz
DC capacitors	C4AQSBW5220A3NJ × 2	22 μF, 1.5 kV,
Drivers	4 A/6 A, 5 kV isolation dual-channel gate driver; 20 V/-4 V 3.5 kV isolation driver source.	
Resonant capacitors	C823A473J61C322 × 9 C823A333J60C320× 6	47 nF, 1 kV, 33 nF, 1 kV 47 × 9 + 33 × 6 = 621 nF
HFTs	500 V/1000 V, 14/28 turns in primary/secondary side 1:2 turn ratio, PC95/EEP70B, 3.5 kV isolation	$L_{lk} \approx 2.86\ \mu$H, $L_m \approx 500\ \mu$H, $C_s \approx 350$ pF

HFT are calculated via the measurement of the open/short circuit impedance under PSM3750 NumetriQ frequency analyzer. When V_{in} and V_o are both 300 V, the linear values of C_{oss} and C_d are given as $C_{oss}(300\text{ V}) = 180$ pF, and $C_d(300\text{ V}/2) = 290$ pF. v_{CD} is twice of v'_{CD} since the turn ratio of the HFT is 1:2.

A. Accurate Steady-State Waveforms of LLC

Three cases are given to demonstrate the instruction of the application of accurate steady-state waveform description. The control parameters in these three cases are given as $f_s = 100$ kHz ($T_s = 10\ \mu$s), $t_d = 1\ \mu$s; $f_s = 80$ kHz ($T_s = 12.5\ \mu$s), $t_d = 600$ ns; and $f_s = 150$ kHz ($T_s = 6.7\ \mu$s), $t_d = 600$ ns. The calculated ideal/ piecewise-approximated resonant waveforms and the experimental waveforms are depicted in Fig. 17.

1) Case One: Run the ideal resonant waveform calculation, and it outputs $t_C = 4.2\ \mu$s, $t_B = 0.8\ \mu$s. Because t_C is beyond the conduction time of S_2 ($T_s/2 - t_d = 4\ \mu$s), stage C' will take up all the resonant processes. i_0 and v_0 in stage G' are calculated as 0.57 A and 9.2 V. From (16), the resonant period in stage G' is 220 ns. From (21), there is $t_{d1} = 770\text{ ns} < t_d$. As a result, the *LLC* will enter stage H' and there is $t_{d3} = t_d - t_{d1} = 230$ ns. According to (22), $v_{ds}(0)$ and $i_r(0)$ in stage H' are given as 27.6 V, 0.05 A.

During this resonant process, the resonant period is 279 ns. According to (23) and solving the equation of $v_{ds}(t) = 0$, $v_{ds}(t)$ will cross zero for many times and the first four zero crossing times of $v_{ds}(t)$ are given as [84 ns, 179 ns], and [363 ns, 458 ns].

Since $t_{H'}$ is out of the above two zero crossing regions, $v_{ds}(t_{d3})$ is calculated as 20.9 V, and the ZVS-ON is almost achieved.

The calculated and measured values of T_{d1}, t_{d1}, and t_{d3} are given as (199, 770, and 230 ns) and (170, 750, and 250 ns).

2) Case Two: In this case, there is $t_C = 4.32\ \mu$s, $t_B = 1.33\ \mu$s. Because t_C is shorter than the conduction time of S_2 ($T_s/2 - t_d = 5.65\ \mu$s), $v_{ds}(t)$ is regarded as a trapezoid, and $t_{C'}$ can be roughly calculated as $t_{C'} = t_C - t_d/2 = 4.02\ \mu$s. Hence, $t_{B'}$ is given as $t_{B'} = T_s/2 - t_d - t_{C'} = 1.63\ \mu$s. According to (25), the resonant period in stage B' is given as 285 ns, and there will be around 5.7 resonant cycles. According to (16) and (21), the duration of stage G' is given as $t_{d1} = 504\text{ ns} < t_d$, and the *LLC* will enter stage H'. The initial values of $v_{ds}(0)$ and $i_r(0)$ in stage H' are 25.37 V, 0.012 A. The zero crossing time of $v_{ds}(t)$ in stage H' is given as [93 and 181 ns], and [372 and 460 ns] when considering the first four points. Because the duration of stage H' $t_{d3} = t_d - t_{d1} = 96$ ns belongs to the first zero crossing region, ZVS-ON is completely achieved.

The calculated and measured values of T_b, t_{d1}, and t_{d3} are given as (285, 504, and 96 ns) and (300, 500, and 100 ns).

3) Case Three: As for the ideal resonant waveform of OST ac, there is $t_A = 29$ ns, $t_C = 3.3\ \mu$s. When we assume the piecewise- approximated OST to be A'C'G'H', A'C'G', and C'G'H', the results will not converge after 100 iterations in the numerical calculation process, which indicate that the above OSTs are not valid, and the OST has to be C'G'. In this case, stage C' takes up all the conduction time of S_2. If we assume $v'_{CD}(t)$ can be clamped by the output at the end of t_d, the minimum t_d can be calculated by (21), which is given as 1075 ns $>$ 600 ns. Hence, there is only stage G' and $v_{ds}(t_d) = 133.7$ V. This result agrees with the numerical calculation process. Hence, the MOSFETs suffer from hard-switching with high voltage spikes.

It has to be mentioned that when ZVS-ON is not achieved, the experimental waveforms are with relatively large errors due to the high *dv/dt* and *di/dt* affects not only the power switches but also the driver circuit.

When $f_s = 100$ kHz, $t_d = 1\ \mu$s, two cases when $R_L = 240\ \Omega$ and $R_L = 480\ \Omega$ are depicted in Fig. 18. It can be observed that when the load increases, the duration of stage G' tends to increase slightly. Both the theoretical analysis [cf. Fig. 8(a)] and the experimental waveforms verify that the load condition impact on the operation waveforms in the dead time is tiny.

B. Accurate ZVS Boundary of LLC

It can be inferred from Fig. 8 that when the circuit parameters are determined, the load condition and V_{in} have weak relation (assuming C_{oss}, C_d are constant) to $t_{d\text{-}cr}$ while the control parameters (f_s, t_d) are with strong relationships.

When $f_s = 100$ kHz, 1 μs dead time is surplus. In this case, $t_{d\text{-}cr}$ is calculated as 744 ns. Two cases when $t_d = 750$ ns and $t_d = 550$ ns are depicted in Fig. 19. As can be observed, the measured $v_{ds}(t_d)$ crosses zero exactly at the end of t_d when $t_d = 750$ ns. When t_d is reduced to 550 ns, there is $v_{ds}(t_d) = 51.2$ V and hard switching causes $v_{ds}(t)$ and $i_r(t)$ ringing.

The calculated $t_{d\text{-}cr}$ of the proposed method, the conventional method, and the experimental results with 300 and 200 V input voltages and 120 Ω load are depicted as the red, orange, and blue lines in Fig. 20. In Fig. 20, the orange line is exactly straight because $t_{d\text{-}cr}$ in the conventional method is proportional to f_s. The same solution of $t_{d\text{-}cr}$ in the conventional method can also be obtained if one uses the linear part of $v_{ds}(t)$ in (20). In the proposed method, the relation between $t_{d\text{-}cr}$ and f_s is close to proportional but there are some deviation points like 90 kHz in Fig. 20(a) and 120 kHz in Fig. 20(b). This is caused by the resonant part of $v_{ds}(t)$. Within the tolerance of error, the experimental result is in agreement with the proposed method.

C. Calculation Time Comparisons

The calculation time of different methods are obtained via the "*Timing*" function, and the equation sets are solved via

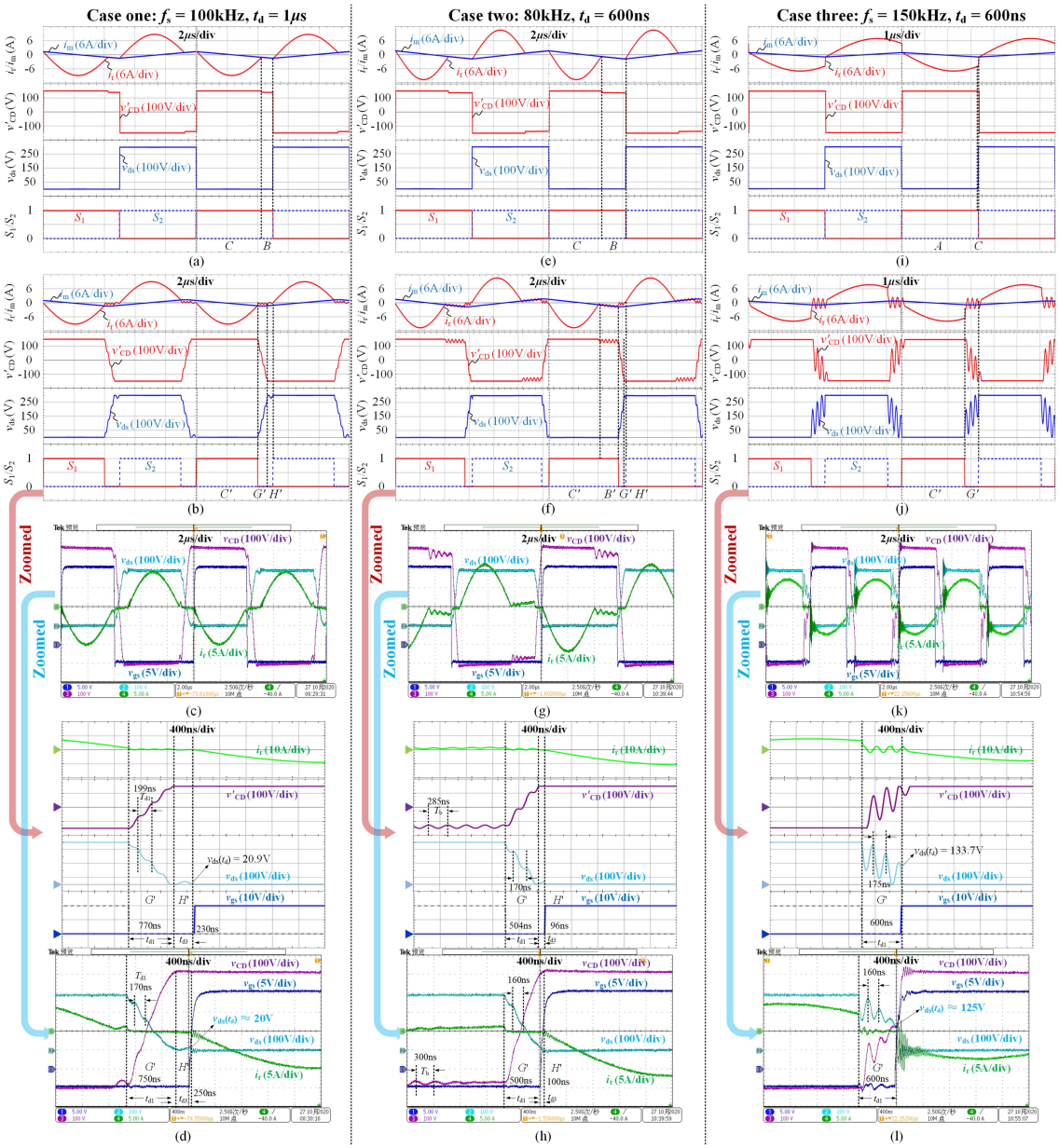

Fig. 17. Key waveforms of the three cases (the control parameters in the three cases are given as case one: $f_s = 100$ kHz, $t_d = 1$ μs, case two: 80 kHz, $t_d = 600$ ns, case three: $f_s = 150$ kHz, and $t_d = 600$ ns). (a) Calculated ideal resonant waveforms in case one. (b) Calculated piecewise-approximated resonant waveforms in case one. (c) Experimental resonant waveforms in case one. (d) Calculated piecewise-approximated and experimental turning on waveforms in case one. (e) Calculated ideal resonant waveforms in case two. (f) Calculated piecewise-approximated resonant waveforms in case two. (g) Experimental waveforms in case two. (h) Calculated piecewise-approximated and experimental turning on waveforms in case two. (i) calculated ideal resonant waveforms in case three. (j) Calculated piecewise-approximated resonant Waveforms in case three. (k) Experimental waveforms in case three. (l) Calculated piecewise-approximated and experimental turning on waveforms in case three (Ch1: the gate driver $v_{\rm gs}$ of the MOSFET, 5 V/div; Ch2: the drain-source voltage of the MOSFET $v_{\rm ds}$, 100 V/div; Ch3: the output voltage of the HFT v_D, 100 V/div; Ch4: the resonant current i_r, 5 A/div).

the "*FindRoot*" function in Mathematica software based on an Intel Core i5-8600 3.1GHz processor with 16 GB RAM. The comparison results are given in Table III.

There are nine OSTs tested in the ideal model, and 20 OSTs tested in the full/reduced order models. In each OST, ten different operation conditions are applied.

Although the initial values can be tuned beforehand to save the calculation time, the comparative fairness might be lost. Consequently, the initial value of M is set as 1, and the initial values of $t_C/t_{C'}$ are set as $T_r/2$. The initial values of the other variables are all set to 0.01(the initial values are not set as zero to avoid the singularity of the Jacobian matrix). The selection of the above initial values is reasonable because the resonant waveforms of the *LLC* is sinusoidal on the whole. The maximum iteration step is set as 100, and the precision is set as 0.001.

After obtaining the calculated results, the stage constraints, as well as the positive stage durations, are checked to see whether these results are valid.

In Table III, the ideal model is the fastest since the other two methods are based on the ideal model. Although the numbers

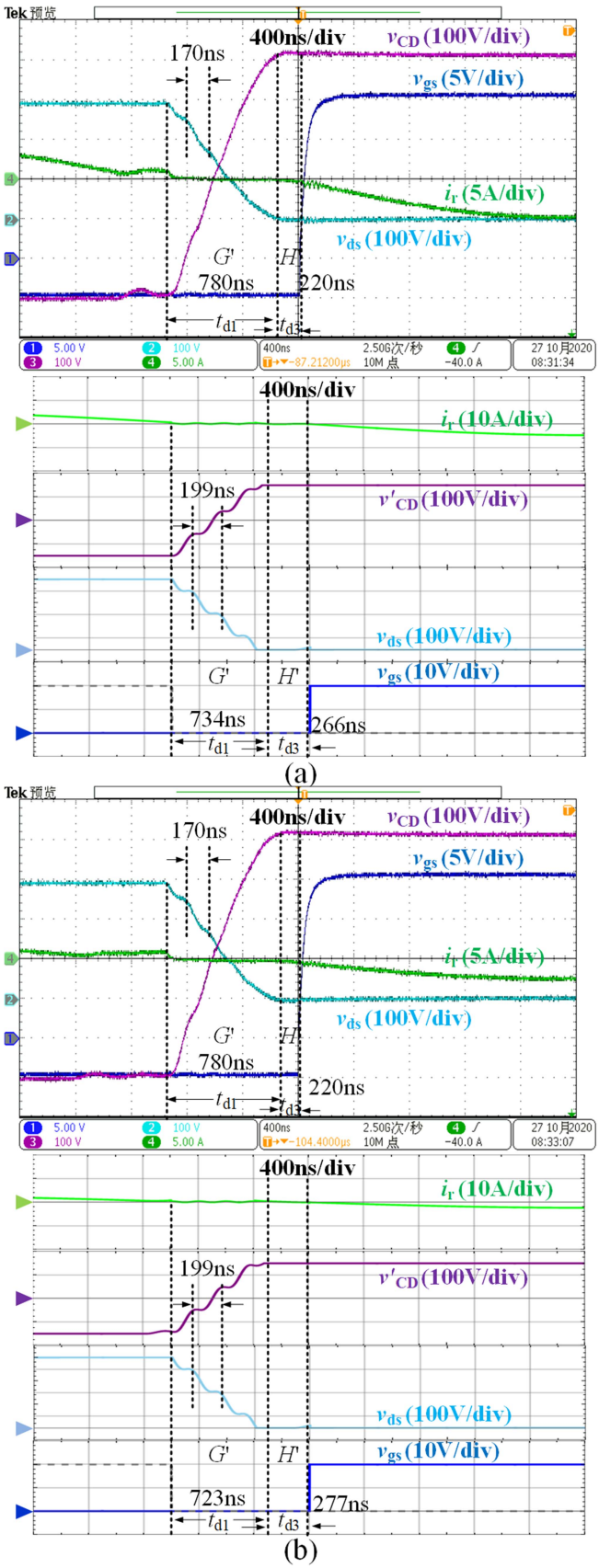

Fig. 18. Calculated piecewise-approximated and experimental turning on waveforms when $f_s = 100$ kHz, $t_d = 1$ μs. (a) $R_L = 240$ Ω. (b) $R_L = 480$ Ω.

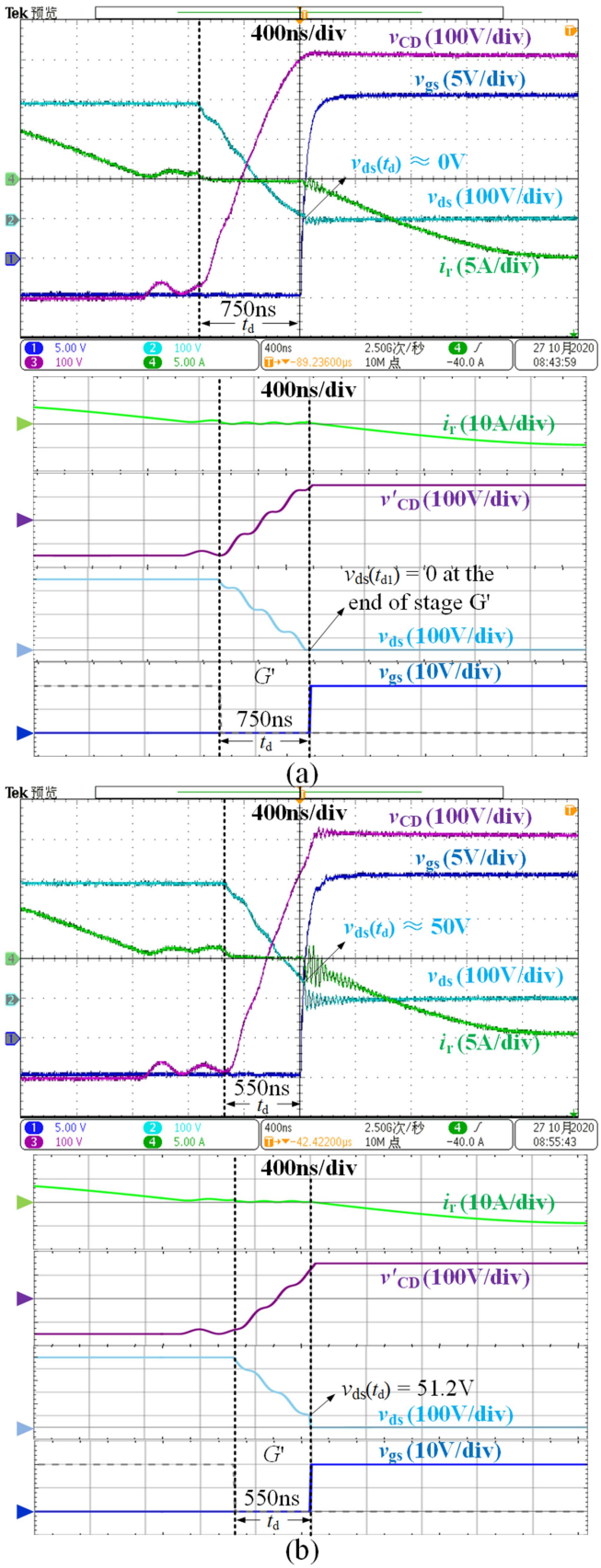

Fig. 19. Calculated piecewise-approximated and experimental turning on waveforms when $f_s = 100$ kHz. (a) $t_d = 750$ ns. (b) $t_d = 550$ ns.

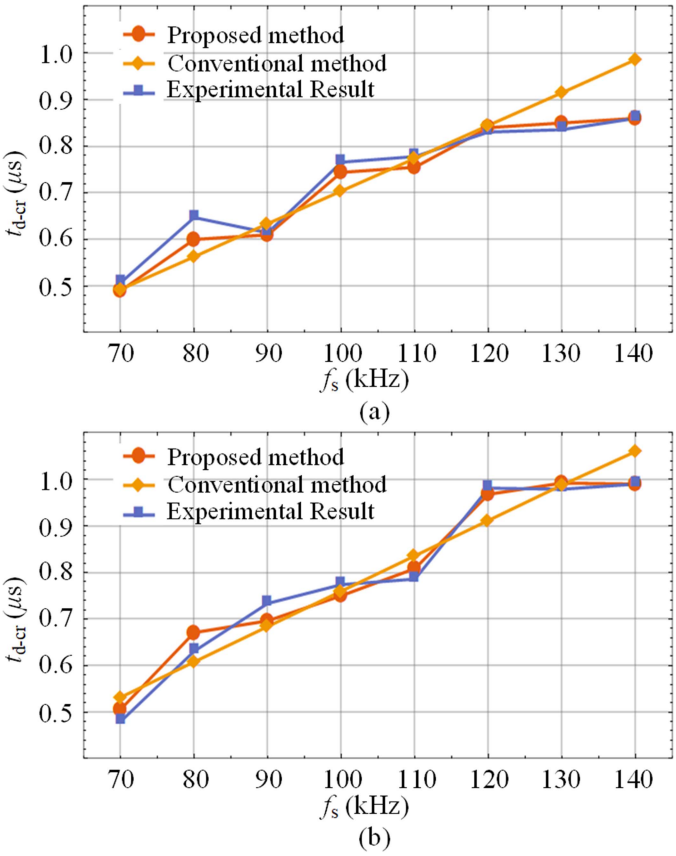

Fig. 20. Calculated and experimental $t_{d\text{-}cr}$ under different conditions. (a) Input voltage $V_{\text{in}} = 300$ V. (b) Input voltage $V_{\text{in}} = 200$ V.

TABLE III
COMPARISON RESULTS BETWEEN DIFFERENT METHODS

	Ideal	Full-order	**Reduced-order**
Maximum calculation time (ms)	225	2401	**784**
Minimum calculation time (ms)	36	441	**144**
Average calculation time (ms)	122	1318	**430**
Average stages in the OST	2.6	4.1	**4.1**
Average calculation time of one stage (ms)	11.48	34.59	**19.76**
Average unknowns in one OST	10.67	38.11	**21.78**

of average stages in the full/reduced order model are identical, the average unknowns are reduced in the reduced order model. As a result, the average calculation time in the reduced order model is reduced by 67%, and the average calculation time of one stage in the reduced order model is reduced by 43%. We also used commercial circuit simulators piecewise linear electrical circuit simulation (PLECS) and power simulation (PSIM) for run time comparison. To illustrate the switching characteristic during t_d, the step size is chosen as 1E-9 (fixed-step), and the total simulation duration is 10 ms. As for each circuit simulator, we tested 16 different operation conditions. f_s and t_d in these

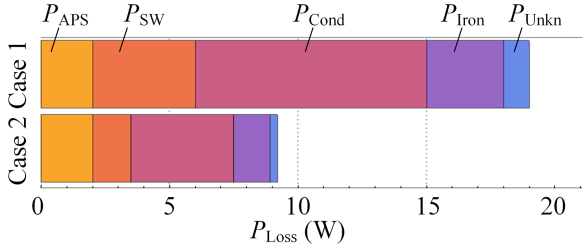

Fig. 21. Power loss breakdown diagrams of the *LLC* prototype in two cases.

16 different operation conditions are 80/100/120/150 kHz, and 400/600/800/1000 ns. It is found that the average run time of PLECS and PSIM are 77 and 49 s, respectively. Compared to the discrete-time simulators, the proposed approach is continuous-time, and analytical. Besides, the calculation time is much saved.

D. Loss Breakdown and Experimental Curves

The total power loss of the converter, P_{Loss}, can be divided into the conduction loss P_{Cond} of all the power switches and the HFT, the switching loss P_{SW}, the iron loss P_{Iron}, and the power consumption of the control board, P_{APS}, etc. The iron loss P_{Iron} can be further divided into the iron loss of the resonant inductor, $P_{\text{Iron-}L}$ and the iron loss of the HFT, $P_{\text{Iron-}T}$.

The iron loss P_{Iron} can be roughly estimated by the original Steinmetz equation

$$\begin{cases} P_{\text{Iron}-L} = k_L f_s^{\alpha_L} B_{Lm}^{\beta_L} \\ P_{\text{Iron}-T} = k_T f_s^{\alpha_T} B_{Tm}^{\beta_T} \end{cases} \tag{35}$$

where B_{Lm}, and B_{Tm} are the magnetic flux density amplitudes of the resonant inductor and the excitation inductor, k_L, α_L, β_L, and k_T, α_T, β_T are the Steinmetz parameters.

The major part of the switching loss P_{SW} in the *LLC* is caused by the MOSFETs with peak turn-OFF current, I_{Peak}. Under reasonable assumptions, P_{SW} can be roughly calculated as [41]

$$P_{\text{SW}} \approx \frac{I_{\text{Peak}}^2}{48 C_{\text{oss}} f_s}. \tag{36}$$

Consequently, P_{Loss} can be expressed as

$$P_{\text{Loss}} = P_{\text{APS}} + P_{\text{SW}} + P_{\text{Iron}-L} + P_{\text{Iron}-T} + P_{\text{Cond}} + P_{\text{Unkn}} \tag{37}$$

where the unknown loss P_{Unkn} is calculated via the difference between the calculated and measured power losses.

The measured power consumption of the control board (including the digital signal processor, the gate driver circuits, the sampling circuits, etc.) is around 2 W. The power loss breakdown diagrams of the *LLC* prototype at 350 V/500 W (case 1), and 300 V/350 W (case 2) are depicted in Fig. 21.

The efficiency curves of the *LLC* prototype when the output voltage ranged from 250 to 350 V are depicted in Fig. 22(a). The peak efficiency is achieved as 97.5%. When the output is reduced to 250 V, f_s is increased to 170 kHz. In this condition, ZVS-ON is not achieved and the efficiency dropped to 94.2%. The relation of switching frequency versus the maximum output power is depicted in Fig. 22(b). When the switching frequency

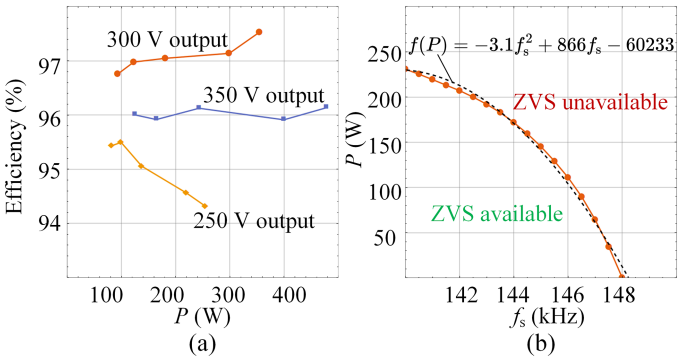

Fig. 22. (a) Efficiency curves of the *LLC* prototype in different output voltage conditions. (b) ZVS-ON regions of the *LLC* prototype.

TABLE IV
COMPARISON OF CONVERTERS WITH AROUND 500 W OUTPUT POWER

Ref	Power	Efficiency	Frequency	Output Voltage
[9]	1000 W	95.4%	172–208 kHz	320–420 V
[37]	500 W	96%	90–200 kHz	48 V
[38]	480 W	96.7%	116–251 kHz	12 V
[39]	350 W	96.4%	60–117 kHz	56 V
[40]	500 W	95%	100 kHz	24 V
This article	500 W	**97.5%**	70–170 kHz	250–350 V

is above 148 kHz, ZVS-ON is impossible because there is no reasonable solution for $t_{d\text{-}cr}$.

To illustrate the ZVS-ON regions, we also fit the relation to the quadratic function $f(P)$ as

$$f(P) = -3.1f_s^2 + 886f_s - 60233. \tag{38}$$

Above the lines in Fig. 22(b), ZVS-ON is unavailable. The efficiency comparisons of the prototype against similar articles are given in Table IV. With around 500 W power rating, the efficiency of the *LLC* prototype is advantageous compared to some similar articles.

VI. CONCLUSION

This article presents a piecewise-approximated time domain analysis of *LLC* considering the parasitic capacitors and dead time. The piecewise-approximated time domain analysis provides a highly accurate description of resonant waveforms and guides the design of *LLC* resonant components as well as the dead time configuration at the cost of only slightly increased calculation complexity. The major applications of the presented analysis, including the resonant/switching waveform illustration, the critical dead time calculation, and the optimal converter design, are verified by a 500 W AHB-*LLC* prototype.

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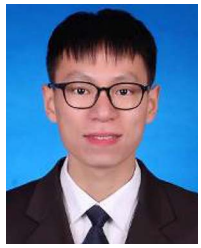

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