Novel Soft-Switched Three-Phase Inverter With Output Current Ripple Cancellation

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***Abstract*—A novel three-phase dc–ac full-bridge soft-switched inverter topology is proposed in this article that provides an ultralow ripple output current. The proposed circuit utilizes a passive filter that comprises a transformer, an inductor, and a capacitor for achieving soft switching and output current ripple cancellation. Zero-voltage switching (ZVS) is achieved at turn ON time instant for all the switches in the proposed circuit. The magnitude of ZVS current is optimized throughout the line cycle by the application of the variable frequency modulation technique. In addition to soft switching, an ultralow ripple output current is achieved due to the current ripple cancellation property of the proposed circuit. The output current ripple cancellation is achieved by combining the inverter current with an additional high-frequency ripple current generated by the passive filter. The soft-switched inverter operation and inherent current ripple cancellation achieved by the proposed circuit, result in a high power conversion efficiency. Theoretical analysis and the improvements in inverter performance presented in this article are validated through the experimental verification of the proposed converter topology using a 600-W lab prototype.**

***Index Terms*—Current ripple cancellation, dc–ac inverter, soft-switched inverter.**

I. Introduction

PHOTOVOLTAIC (PV) microinverters are widely used for harnessing solar energy through PV panels in residential and commercial installations. The microinverters track peak power of each panel independently, so they are able to solve the problems due to partial shading of PV panels. Furthermore, they improve system safety by eliminating high dc voltage wiring and increase system resiliency to single point failures. Traditionally, the microinverter-based residential and commercial PV power generation systems are small in size ($\sim$ 6–10 kW) and connect with a single-phase utility grid. However, the benefits of a PV microinverter and the availability of high-power PV panels (300–650 W) [1], [2], [3] have increased their popularity in large size PV installations ($\sim$ 10 kW or higher). The large size PV rooftop installations are typically required to be connected to a three-phase power grid. In such a scenario, typically three single-phase microinverters are used to connect with the three-phase grid. Such an architecture of a three-phase PV power generation system requires external phase-disconnect switches and protection devices. These external devices are required to isolate the system from the grid, in case a significant unbalance in phase voltages appears. Therefore, native three-phase PV microinverters are required for connecting large size PV power generation systems with the three-phase power grid.

Traditionally, a two-stage power architecture is employed for a native three-phase microinverter, which consists of a full-bridge dc–ac inverter interfacing the utility grid [4], [5], [6], [7], [8], [9], [10], [11], [12]. A conventional hard-switched dc–ac inverter is used in microinverters, since the benefits and effectiveness of the existing soft-switching topologies do not justify their additional cost and complexity in this application [9], [12], [13], [14], [15], [16], [17], [18]. However, the switching losses form a dominant portion of the losses in three-phase microinverters. Therefore, significant improvement in power conversion efficiency can be obtained by introducing soft-switching techniques for the inverter. Numerous soft-switching techniques have been proposed in the literature for a full-bridge dc–ac inverter [19], [20], [21], [22], [23], [24], [25], [26], [27], [28]. Soft-switched inverter topologies, such as active clamp resonant dc-link inverter [19], [20] and parallel resonant dc-link inverter [21], [22], [23], utilize an auxiliary circuit on dc-link for achieving soft switching. A major drawback of these topologies is that the voltage across the inverter switches is significantly higher than that of the source dc voltage. Topologies, such as notch commutated inverter [24], [25] and the circuit topologies presented in [26], [27], [28], solved the problem of higher dc-link voltage while providing soft switching. However, special modulation techniques are required for driving the inverter with these auxiliary circuits to achieve soft-switching conditions. The other drawbacks of this type of topologies include the use of floating gate drive circuitry and high current rating of the auxiliary switches. The need for a dedicated active auxiliary circuit and use of specialized modulation methods increase the cost and complexity of the inverter, making them unsuitable for the low-power three-phase microinverter.

The auxiliary circuits have also been introduced on the ac side of the inverter for achieving zero-voltage switching (ZVS) conditions [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39]. These soft-switching methods rely on the bidirectional nature of the ripple current generated by the auxiliary circuit to

Manuscript received 11 May 2022; revised 21 July 2022; accepted 19 August 2022. Date of publication 31 August 2022; date of current version 10 October 2022. Recommended for publication by Associate Editor Y. Yang. *(Corresponding author: Snehal Bagawade.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3203055.

Digital Object Identifier 10.1109/TPEL.2022.3203055

achieve ZVS at the turn ON time instant. Near zero-voltage conditions are also achieved for turn OFF transition by the addition of external snubber capacitors in parallel with the switches [24], [25]. The large magnitude of current ripple is typically filtered from the output current using a large capacitive filter. One of the main benefits of introducing the auxiliary circuit on the ac side for soft switching is that the peak voltage stress of the switching devices remains the same as the input dc voltage. Moreover, the inverters utilizing these methods can be operated using state-of-the-art pulse width modulation (PWM) techniques and control algorithms that result in high-quality output sinusoidal voltages and currents [20]. High-quality sinusoidal currents are required to comply with the stringent regulatory standards for grid-connected inverters, such as IEEE1547 [40], UL1741 [41], etc.

An inverter topology, using auxiliary circuit on ac side, was presented in [19] and [20], where a resonant pole was created between the capacitors in parallel with the inverter switches and the filter inductor. However, the introduction of resonant capacitors increase the magnitude of ZVS current required to achieving soft switching. In addition, the high-frequency current flowing through the filter inductors increases the circuit losses. The problems pertaining to increased losses were solved by the topology presented in [37] that utilizes an active auxiliary circuit to achieve ZVS. Soft switching is achieved in this inverter through ZVS at turn ON and zero current switching at turn OFF by the operation of auxiliary switches for a short duration close to the switching instant of the main switches. However, it requires auxiliary floating switches and their precise control to realize the benefits of soft switching. Another active auxiliary circuit introduced in [34] utilizes auxiliary inductors and an active voltage source for generating the ZVS current, which only flows through the auxiliary network. Although soft switching is achieved by introduction of active auxiliary circuits, they increase the circuit cost and operational complexity, which makes them unsuitable for use in microinverter applications.

Soft-switched inverter topologies and control techniques have been developed in the past, which are aimed at microinverter applications, such as those presented in [35], [38], and [42]. These soft-switching techniques use the current ripple through the switching node for achieving ZVS conditions and are suitable for low-current applications, such as three-phase microinverters. In [35] and [39], a coupled inductor (CI)-based passive circuit was used for achieving soft switching using conventional PWM techniques. In addition, the current ripple in the output was significantly attenuated by magnetic flux cancellation in the CI. In [35], [43], and [44], CI-based soft-switching techniques were further investigated. However, a low coupling coefficient is typically used in the CI for this application. Such CIs tend to become large in volume and have a complex geometric shape that increases the core losses (especially, at light loads). The peak-to-peak values of current ripple in these inverters have been optimized by employing variable frequency techniques for limiting the magnetic losses. The variable frequency PWM techniques were also presented in [38], [42], and [45] for controlling the magnitude of current ripple through the inductors of the *LCL* filters to achieve ZVS. A hybrid ZVS technique was presented in [46], [47], and [48] that utilizes the boundary conduction mode (BCM) operation of each phase leg using variable switching frequency to control the magnitude of current ripple required for achieving soft switching. A major drawback of this technique is that a large capacitor is used to filter the high-frequency ripple from the output current, which is undesirable for microinverters.

In this article, a novel soft-switched dc–ac inverter topology is proposed that utilizes a passive filter circuit comprising a transformer, an inductor, and a capacitor for generating an ultralow ripple output current. Soft switching is achieved through ZVS at the turn ON instant because of the bidirectional nature of the inverter current. The magnitude of required ZVS current is optimized throughout the line cycle by implementing the variable frequency modulation technique. The proposed inverter is operated using the conventional sinusoidal PWM (SPWM) implemented on a digital processor. The digital control system continuously monitors the phase angle of the ac line cycle and load conditions for adjusting the operation of the inverter so that optimal ZVS is achieved. Furthermore, the novel current ripple cancellation property of the proposed circuit significantly attenuates the ripple from the output current. The proposed method of soft switching while providing current ripple cancellation significantly improves the performance of the three-phase inverter for low-power applications.

II. Proposed Circuit and Its Analysis

The proposed three-phase full-bridge soft-switched inverter circuit is shown in Fig. 1. The proposed filter at the output of the inverter legs is shown enclosed in dotted lines, which consists of a transformer, an inductor, and a capacitor. Only two extra passive components are required to realize this circuit as compared to the conventional full-bridge circuit with inductive output filter. The primary winding of the transformer T with the magnetizing inductance L_m is connected between the switching node and the output ac voltage. Therefore, the high-frequency voltage is applied across the primary winding of the transformer. Consequently, a high-frequency current is developed in this circuit. The magnetizing inductance is designed, so that the high-frequency current is able to provide the ZVS conditions in every switching cycle. The high-frequency voltage across the primary winding of the transformer is reflected to the secondary side, according to the transformation ratio ($N:1$). The secondary-side circuit is designed to provide a ripple current that has opposite slope, but same magnitude, as that in the primary-side circuit. Since the voltage reflected in the secondary side is much smaller than the primary circuit, only a small inductance L_2 is required to generate a current ripple with same magnitude as the primary side. Therefore, a small value of external inductance L_{ext} is sufficient in the secondary-side circuit for achieving the required inductance value in the secondary-side circuit. The currents in the primary and secondary sides circuits are added at the output common ac voltage point to cancel the ripple and achieve an ultralow ripple output ac current.

A single-phase equivalent circuit of the proposed topology is shown in Fig. 2 for the circuit analysis. The output ac current in the single-phase equivalent circuit is injected into a voltage

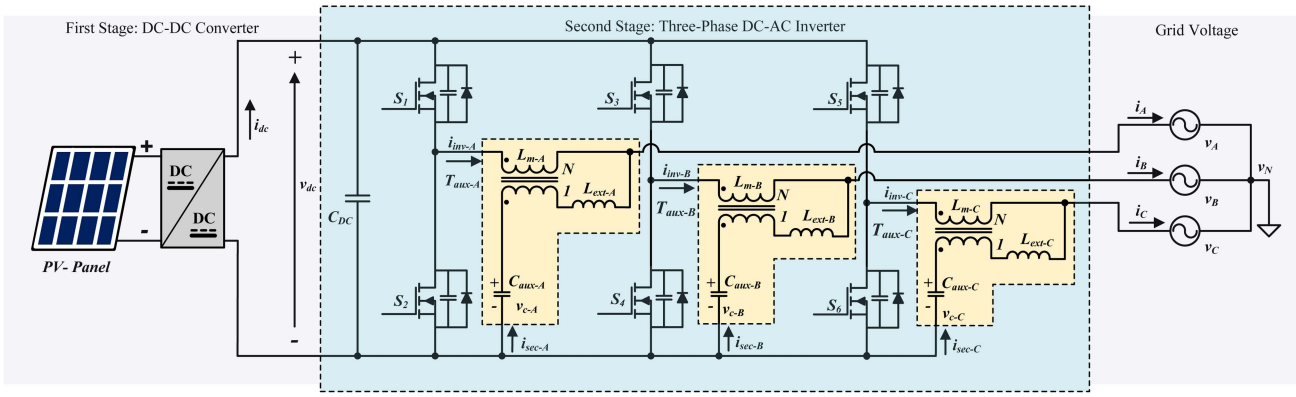

Fig. 1. Circuit diagram of the proposed three-phase soft-switched full-bridge inverter with current ripple cancellation circuit.

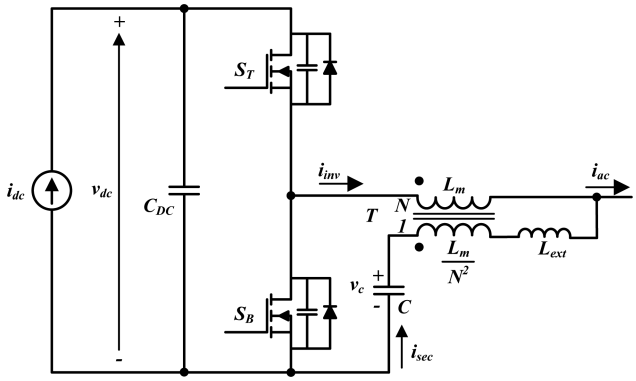

Fig. 2. Single-phase equivalent circuit diagram of the proposed soft-switched full-bridge inverter employing transformer for canceling current ripple in ac current.

source $v_{\rm ac}$, which is referenced to the neutral point voltage v_N. The neutral point voltage v_N is referenced to the negative terminal of the dc bus. Therefore, the output ac voltage source has a value $v_{\rm AC}$, which is given by

$$v_{\rm AC} = v_{\rm ac} + v_N. \tag{1}$$

The circuit analysis is performed with the help of equivalent circuits shown in Fig. 3. The equivalent circuits are shown in Fig. 3(a) and (b) for the two different time intervals during a switching cycle: 1) $0 \le t < d.T_s$; and 2) $d.T_s \le t < T_s$. The corresponding waveforms of key circuit parameters are shown in Fig. 4. The circuit analysis in this section assumes ideal circuit components and the voltages at the input and output of the circuit are slow varying, such that they are assumed constant over a switching cycle. Circuit analysis equations for the two equivalent circuits are written using the Kirchoff's current and voltage laws. The voltage drop through the transformer primary-side circuit consisting of inductance L_1 is given by

$$\begin{aligned} L_1\frac{{\rm d}i_{\rm inv}}{{\rm d}t} + \frac{L_m}{N}\frac{{\rm d}i_{\rm sec}}{{\rm d}t} &= V_{\rm dc} - v_{\rm AC}, \qquad 0 \le t < d.T_s \\ L_1\frac{{\rm d}i_{\rm inv}}{{\rm d}t} + \frac{L_m}{N}\frac{{\rm d}i_{\rm sec}}{{\rm d}t} &= -v_{\rm AC}, \qquad d.T_s \le t < T_s. \end{aligned} \tag{2}$$

For a stable steady-state operation of the inverter using SPWM, average voltage is across the inductor L_1 must be zero over a switching cycle. Therefore, on applying the volt–sec balance law on the primary-side circuit, using (2) and averaging the voltage on inductance L_1, the following relation is achieved:

$$d.V_{\rm dc} = v_{\rm AC}. \tag{3}$$

The duty cycle of inverter switches is modulated in synchronism with the sinusoidal ac voltage $v_{\rm ac}$. On the secondary-side circuit of the transformer consisting of inductor L_2 and capacitor C, the voltage drop in the loop is given by

$$\begin{aligned} L_2\frac{{\rm d}i_{\rm sec}}{{\rm d}t} + \frac{L_m}{N}\frac{{\rm d}i_{\rm inv}}{{\rm d}t} &= v_c - v_{\rm AC} \\ C\frac{{\rm d}v_c}{{\rm d}t} &= -i_{\rm sec}. \end{aligned} \tag{4}$$

The systems (2) and (4) are averaged over a switching cycle and rearranged to determine the dynamics of inverter current, secondary current, capacitor voltage, and output current as follows:

$$\begin{aligned} L_\gamma\frac{{\rm d}i_{\rm inv}}{{\rm d}t} &= L_2(d.V_{\rm dc} - v_{\rm AC}) - \frac{L_m}{N}(v_c - v_{\rm AC}) \\ L_\gamma\frac{{\rm d}i_{\rm sec}}{{\rm d}t} &= L_1(v_c - v_{\rm AC}) - \frac{L_m}{N}(d.V_{\rm dc} - v_{\rm AC}) \\ C\frac{{\rm d}v_c}{{\rm d}t} &= -i_{\rm sec}, \quad \frac{{\rm d}i_{\rm ac}}{{\rm d}t} = \frac{{\rm d}i_{\rm inv}}{{\rm d}t} + \frac{{\rm d}i_{\rm sec}}{{\rm d}t} \end{aligned} \tag{5}$$

where

$$L_\gamma = \left(L_1L_2 - \frac{L_m^2}{N^2}\right). \tag{6}$$

The average value of capacitor voltage at steady-state can be determined by applying the charge balance law. According to this law, a net zero-current passes through the capacitor over a switching cycle at steady-state. Hence, from (5), the change in $i_{\rm sec}$ over a switching cycle is zero, i.e.,

$$L_1(v_c - v_{\rm AC}) - \frac{L_m}{N}(d.V_{\rm dc} - v_{\rm AC}) = 0. \tag{7}$$

From the inverter steady-state operation given by (3), substituting the value of duty cycle in (7). Hence, the capacitor voltage

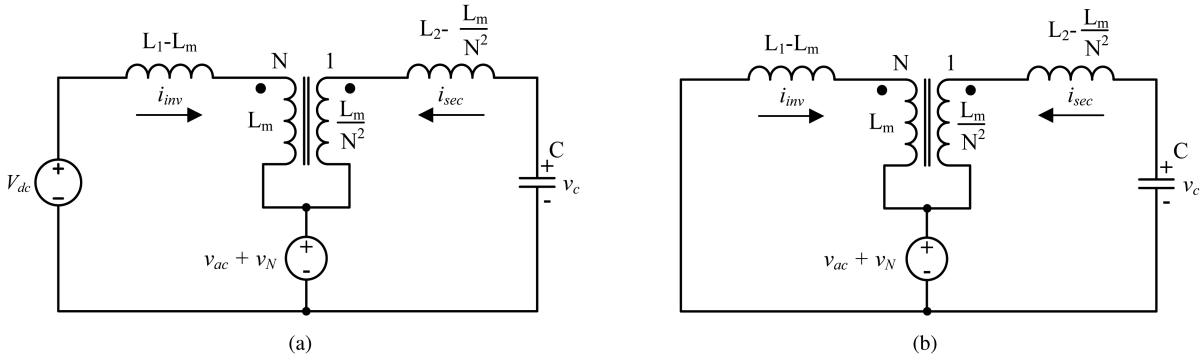

Fig. 3. Equivalent circuits for current injection-based current ripple cancellation circuit. (a) $0 \leq t < d.T_s$. Equivalent circuit of the inverter with top switch ON. (b) $d.T_s \leq t < T_s$. Equivalent circuit of the inverter with bottom switch ON.

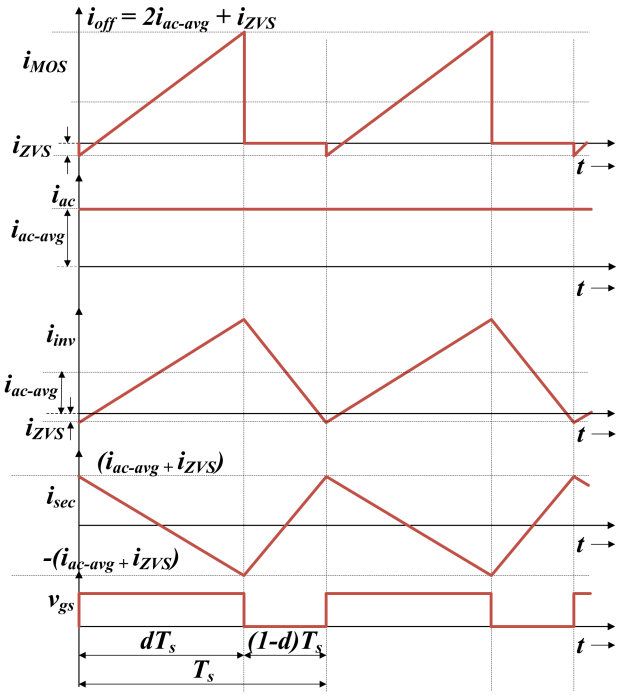

Fig. 4. Key waveforms of a soft-switched full-bridge inverter utilizing current cancellation for reducing switching ripple in the ac current.

v_c is given by

$$v_c = v_{\text{AC}}. \tag{8}$$

1) Analysis of Ripple Cancellation in AC Current: One of the primary objectives of the proposed circuit is to achieve current ripple cancellation in the output current. An ultralow ripple ac current can be achieved if i_{inv} and i_{sec} have identical magnitude of ripple with opposite slopes in each time interval, such that the ripple current at the output in each time interval is zero, i.e.,

$$\frac{\text{d}i_{\text{inv}}}{\text{d}t} + \frac{\text{d}i_{\text{sec}}}{\text{d}t} = 0 \qquad 0 \leq t < d.T_s \tag{9}$$

and

$$\frac{\text{d}i_{\text{inv}}}{\text{d}t} + \frac{\text{d}i_{\text{sec}}}{\text{d}t} = 0 \qquad d.T_s \leq t < T_s. \tag{10}$$

From (2) and (4), the equations for change in inverter current and transformer secondary current can be obtained during the time interval $0 \leq t < d.T_s$ as follows:

$$\begin{aligned} L_\gamma \frac{\text{d}i_{\text{inv}}}{\text{d}t} &= L_2(V_{\text{dc}} - v_{\text{AC}}) - \frac{L_m}{N}(v_c - v_{\text{AC}}) \\ L_\gamma \frac{\text{d}i_{\text{sec}}}{\text{d}t} &= L_1(v_c - v_{\text{AC}}) - \frac{L_m}{N}(V_{\text{dc}} - v_{\text{AC}}). \end{aligned} \tag{11}$$

From (9) and (11), the change in current ripple in first time interval is

$$\left(L_2 - \frac{L_m}{N}\right)(V_{\text{dc}} - v_{\text{AC}}) + \left(L_1 - \frac{L_m}{N}\right)(v_c - v_{\text{AC}}) = 0. \tag{12}$$

Since the voltage across the capacitor is equal to the ac voltage [as shown in (8)] and the term $(V_{\text{dc}} - v_{\text{AC}})$ is always a positive value, the following condition must be satisfied in order to obtain ripple cancellation in ac current:

$$L_2 = \frac{L_m}{N}. \tag{13}$$

It can be verified that the same condition also satisfies (10). Furthermore, the total required inductance in (13) is larger than the magnetizing inductance of the transformer secondary winding, i.e., $\frac{L_m}{N^2}$. Therefore, in the proposed circuit, a discrete inductor L_{ext} is connected in series with the secondary winding of the transformer to achieve the required inductance. The value of L_{ext} is determined by subtracting the transformer magnetizing inductance on the secondary winding from the total required secondary-side inductance, i.e.,

$$L_{\text{ext}} = \frac{(N-1)}{N^2} L_m. \tag{14}$$

The value of inductance required in the secondary circuit is significantly smaller than the value of primary-side magnetizing inductance of the transformer, and hence can physically be a smaller component. However, on the primary side, an external inductance in the primary circuit does not provide significant benefit. Therefore, only transformer magnetizing inductance is utilized in that branch. Hence, the value of filter inductor L_1 is chosen same as the transformer magnetizing inductance L_m, i.e., $L_1 = L_m$.

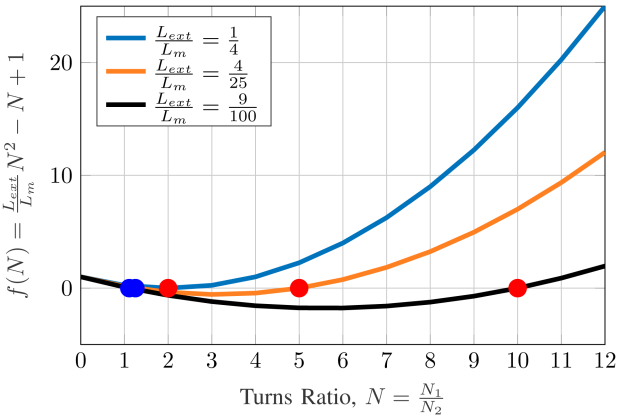

Fig. 5. Curves for determining the limits of transformation ratio, with the inductance ratio $\frac{L_{\text{ext}}}{L_m}$ as a parameter.

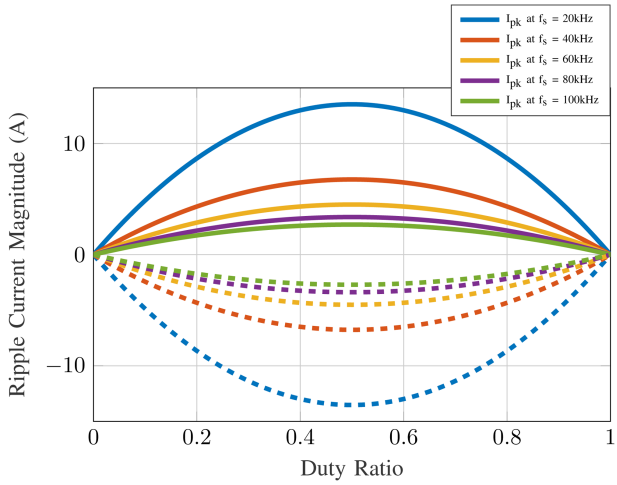

Fig. 6. Current ripple magnitude as a function of duty cycles with switching frequency as a parameter. (Solid lines show the positive peak and dotted lines show the negative peak for the same operating frequency).

Substituting the value of L_1 and L_2 in (5), the averaged inverter current and secondary current dynamics are given by

$$(N-1)\frac{L_m}{N}\frac{\mathrm{d}i_{\text{inv}}}{\mathrm{d}t} = d.V_{\text{dc}} - v_c$$
$$(N-1)\frac{L_m}{N}\frac{\mathrm{d}i_{\text{sec}}}{\mathrm{d}t} = Nv_c - d.V_{\text{dc}} - (N-1)v_{\text{AC}}$$
$$C\frac{\mathrm{d}v_c}{\mathrm{d}t} = -i_{\text{sec}}. \tag{15}$$

Consequently, the output ac current dynamics are given by the following differential equation:

$$\frac{L_m}{N}\frac{\mathrm{d}i_{\text{ac}}}{\mathrm{d}t} = v_c - v_{\text{AC}}. \tag{16}$$

Equation (16) shows that the equivalent inductance for ac current dynamics is reduced by a factor of $\frac{1}{N}$, as compared to the conventional inductive filter current dynamics. As the turns ratio of the transformer increases, i.e., $\frac{1}{N} \to 0$ as $N \to \infty$, the dynamics of current will become more prone to noise and disturbances. However, from (15), the inverter current dynamics in the proposed circuit are seen to converge to that of inductive filter as the turns ratio increases, i.e., $\frac{N-1}{N} \to 1$ as $N \to \infty$, since the effective inductance is reduced by $\frac{N-1}{N}$.

The transformer turns ratio N for achieving the current cancellation is further analyzed by rearranging (14) to the following form:

$$N^2\frac{L_{\text{ext}}}{L_m} - N + 1 = 0. \tag{17}$$

Curves for the left-hand side of (17) are shown in Fig. 5. Equation (17) is a quadratic equation in N, and its solutions are determined to be

$$N = \frac{L_m}{2L_{\text{ext}}}\left(1 \pm \sqrt{1 - 4\frac{L_{\text{ext}}}{L_m}}\right). \tag{18}$$

Positive real roots can be achieved if

$$\frac{L_m}{L_{\text{ext}}} \geq 4. \tag{19}$$

From (18) and (19), the transformation ratio N can have two possible solutions for a given ratio of $\frac{L_m}{L_{\text{ext}}}$. The solution corresponding to positive sign yields a value greater than 2 (shown by red dots in Fig. 5), i.e., $N \geq 2$, and that corresponding to negative sign remains between 1 and 2 (shown by blue dots in Fig. 5), i.e., $1 \leq N \leq 2$. The converter dynamics given by (15) shows that the proposed filter becomes more sensitive as the value of N increases. However, the same situation appears for values of N lower than 2. The values of $1 \leq N \leq 2$ can be seen to make the converter dynamics more sensitive to the value of N as it tends toward 1, i.e., $N \to 1$.

2) Analysis of Output Current Ripple and Capacitor Voltage Ripple: The proposed filter circuit is able to significantly attenuate the switching frequency current ripple from the output current. However, the high-frequency current in the secondary side of the transformer passes through the filter capacitor that generates a finite magnitude of voltage ripple across it. The voltage ripple across the capacitor generates a residual high-frequency component in the output current. The capacitor voltage ripple depends on the value of capacitance and can be determined from (5) and (11). The circuit dynamics in the time duration $0 \leq t < d.T_s$ is represented by

$$\frac{(N-1)}{N}L_m\frac{\mathrm{d}i_{\text{inv}}}{\mathrm{d}t} = V_{\text{dc}} - v_c$$
$$\frac{(N-1)}{N}L_m\frac{\mathrm{d}i_{\text{sec}}}{\mathrm{d}t} = Nv_c - V_{\text{dc}} - (N-1)v_{\text{AC}}$$
$$C\frac{\mathrm{d}v_c}{\mathrm{d}t} = -i_{\text{sec}}. \tag{20}$$

The current and voltage ripples are given by the solution to the system of equations in (20). The inverter current entering the primary winding of the transformer is given by

$$i_{\text{inv}}(t) = \frac{V_{\text{dc}} - v_{\text{AC}}}{L_m}t + \frac{N^2}{(N-1)\omega L_m} \times \left(\frac{V_{\text{dc}}}{N^2} + \frac{v_{\text{AC}}(N-1)}{N^2} - \frac{v_{c0}}{N}\right)\sin(\omega t) + i_{\text{inv0}} + \frac{i_{c0}}{N}(1 - \cos(\omega t)) \tag{21}$$

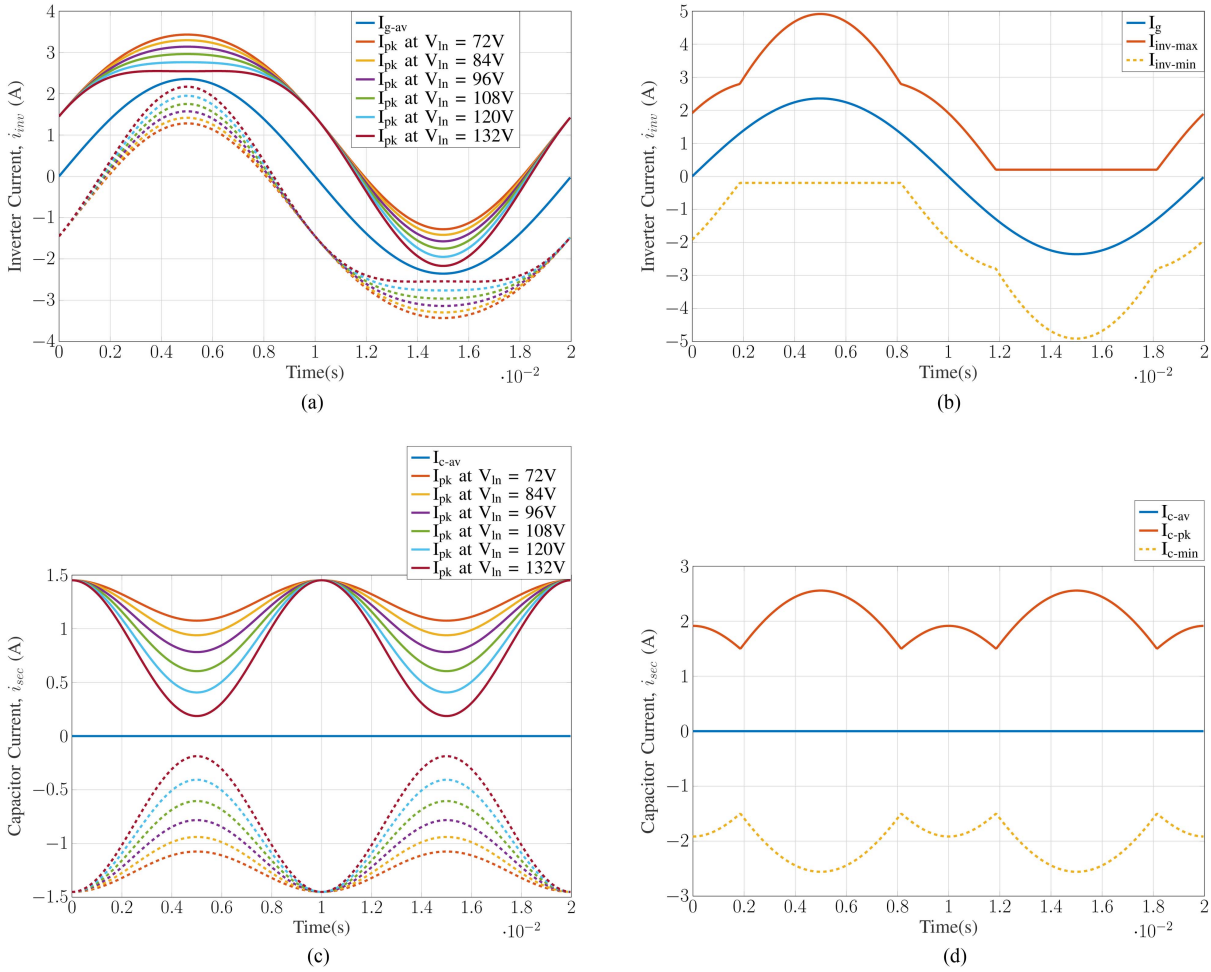

Fig. 7. Current envelops for inverter current and capacitor current under fixed frequency (66 kHz) and variable frequency operation. (a) Envelop for phase A inverter current i_{inv} using fixed frequency SPWM over a line cycle with voltage as a parameter (assuming same ac current at different voltages). (b) Envelop for phase A inverter current i_{inv} using variable frequency SPWM over a line cycle. Optimal switching frequency is selected in each switching cycle. (c) Envelop for phase A capacitor current i_{sec} waveform using fixed frequency SPWM over a line cycle with voltage as a parameter. (d) Envelop for capacitor current i_{sec} of phase A using variable frequency SPWM over a line cycle. Optimal switching frequency is selected in each switching cycle.

where the terms $i_{\text{inv}0}$, i_{c0}, and v_{c0} represent the initial values (at the beginning of the switching cycle, i.e., $t = 0$) of the transformer primary winding current, transformer secondary winding current, and the capacitor voltage, respectively, and ω is the resonant frequency of the output filter, which is given by

$$\omega = N\sqrt{\frac{1}{(N-1)L_m C}}. \tag{22}$$

The current through the secondary winding of the transformer is given by

$$i_{\text{sec}}(t) = i_{c0}\cos(\omega t) + \frac{N^2}{(N-1)\omega L_m} \times \left(v_{c0} - \frac{V_{\text{dc}}}{N} - \frac{v_{\text{AC}}(N-1)}{N}\right)\sin(\omega t) \tag{23}$$

and the output ac current is given by

$$i_{\text{ac}}(t) = \frac{V_{\text{dc}} - v_{\text{AC}}}{L_m}t + i_{\text{inv}0} + \frac{i_{c0}}{N}(1 + (N-1)\cos(\omega t)) + \frac{1}{\omega L_m} \times (Nv_{c0} - V_{\text{dc}} - (N-1)v_{\text{AC}})\sin(\omega t). \tag{24}$$

The voltage ripple on the capacitor due to the switching frequency current flowing through it is given by

$$v_c(t) = v_{c0}\cos(\omega t) - \frac{i_{c0}}{\omega C}\sin(\omega t) + \left(\frac{V_{\text{dc}}}{N} + \frac{v_{\text{AC}}(N-1)}{N}\right)(1 - \cos(\omega t)). \tag{25}$$

The largest current ripple happens at $d = 0.5$, and consequently the largest voltage ripple also appears at this point. Applying the initial conditions, i.e., $i_{\text{inv}}(0) = 0$, $i_{\text{sec}}(0) = 0$, and $v_c(\frac{T_s}{4}) = v_{\text{AC}}$, to the systems (21)–(25), the following initial

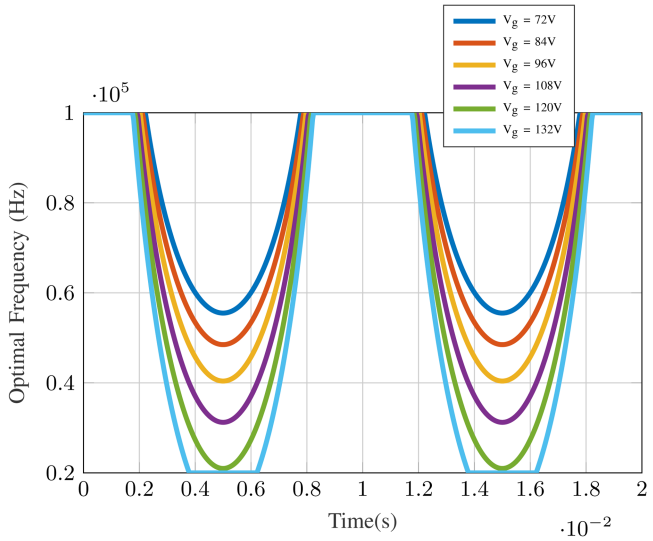

Fig. 8. Optimal frequency for phase A using SPWM over a line cycle with voltage as a parameter (assuming same ac current at different voltages).

TABLE I
PARAMETERS FOR PROTOTYPE OF THE PROPOSED INVERTER CIRCUIT

Parameter	Value
AC voltage v_{ac}	208 V
DC bus voltage V_{dc}	400 V
DC bus capacitance C_{DC}	15 μF
Switching frequency f_s	66.66–125 kHz
Line frequency f_{line}	50 Hz
Power P	600 W
MOSFET switch	Infineon IPB65R125CFD7
On state resistance at 150° C, R_{DS-on}	222 mΩ
Reverse recovery charge Q_{rr}	1040 nC
Filter capacitance value C	3.0 μF
Capacitor part no.	Kemet PHE840EY7100MD16R06L2
Transformer core	Magnetics Inc. (Kool Mu) 77083
Number of turns on the primary N_p	60
Number of turns on the secondary N_s	6
Transformer magnetizing inductance L_m	290 μH
Value of external inductance L_{ext}	26 μH
External inductor core	Ferroxcube RM8- 3C95
Air gap for L_{ext}	0.89 mm
Number of turns for L_{ext}	20

value of capacitor voltage is obtained:

$$v_{c0} = \left(\frac{V_{dc}}{N} - \frac{v_{AC}}{N}\right)\left(1 - \sec\left(\omega\frac{T_s}{4}\right)\right) + v_{AC}. \quad (26)$$

The peak–peak magnitude of voltage ripple on the capacitor will be twice the difference between the initial and average values. Similarly, the peak–peak values of the primary current i_{inv}, secondary current i_{sec}, and the ac current i_{ac} are given by

$$\begin{aligned}
v_{c_{pp}} &= 2\left(\frac{v_{AC}}{N} - \frac{V_{dc}}{N}\right)\left(\sec\left(\omega\frac{T_s}{4}\right) - 1\right)\\
i_{inv_{pp}} &= 2\left(\frac{V_{dc} - v_{AC}}{L_m}\frac{T_s}{4} - \frac{N^2}{(N-1)\omega L_m}\left(\frac{v_{c0}}{N}\right.\right.\\
&\quad \left.\left. - \frac{V_{dc}}{N^2} - \frac{v_{AC}(N-1)}{N^2}\right)\sin\left(\omega\frac{T_s}{4}\right)\right)\\
i_{sec_{pp}} &= 2\frac{N^2}{(N-1)\omega L_m}\left(v_{c0}\right.\\
&\quad \left. - \frac{V_{dc}}{N} - \frac{v_{AC}(N-1)}{N}\right)\sin\left(\omega\frac{T_s}{4}\right)\\
i_{ac_{pp}} &= 2\left(\frac{V_{dc} - v_{AC}}{L_m}\frac{T_s}{4} + \frac{1}{\omega L_m}(Nv_{c0}\right.\\
&\quad \left. - V_{dc} - (N-1)v_{AC})\sin\left(\omega\frac{T_s}{4}\right)\right). \quad (27)
\end{aligned}$$

The peak-to-peak value of voltage ripple on the capacitor is determined from (27) that varies based on the value of capacitance C. The magnitude of voltage ripple across the capacitor determines the magnitude of residual current ripple in the output current.

3) Analysis of Soft-Switching Characteristics and Optimal Dead Time Calculation: In the proposed method of soft switching, the switching current ripple provides the ZVS current i_{zvs} passing through its body diode at the turn ON instant. The value of ZVS current is obtained by analyzing the amount of current required to discharge switch output capacitance (C_{DS}) and charge the capacitance of the complimentary switch in the dead time t_{dead}. Assuming that the current during dead time remains nearly constant, the optimal value of current required to fully discharge the output capacitance of the MOSFET is

$$i_{zvs-opt} = 2C_{DS}\frac{V_{dc}}{t_{dead}}. \quad (28)$$

where $i_{zvs-opt}$ is the value of current required for achieving optimal ZVS.

The total value of current swing around the average value of ac current i_{ac} is $2(i_{ac} + i_{zvs})$. Hence, at the turn OFF instant of top MOSFET, the switch current can be given by

$$\begin{aligned}
i_{sw-off} &= 2i_{ac} + i_{zvs}\\
\Delta i_{inv} &= 2(i_{ac} + i_{zvs})\\
\Delta i_{inv} &= (V_{dc} - v_c)\frac{Nd.T_s}{(N-1)L_m}. \quad (29)
\end{aligned}$$

It is seen from (29) that the peak value of current required to achieve ZVS is close to twice the magnitude of the ac current. The peak value of ripple current varies over the line cycle and can be controlled by varying the switching frequency according to the phase angle of the ac voltage. The switching frequency f_s required for achieving optimum ZVS is given by

$$f_s = \frac{(V_{dc} - v_c)Nd}{2(N-1)L_m|(i_{ac} + i_{zvs})|}. \quad (30)$$

The switching frequency of each leg in the inverter is updated at the beginning of every switching cycle using a lookup table synchronized with the ac line cycle.

The current ripple magnitude as a function of duty ratio is shown in Fig. 6. The switching frequency is used as a parameter. Each curve is plotted with a constant frequency throughout the

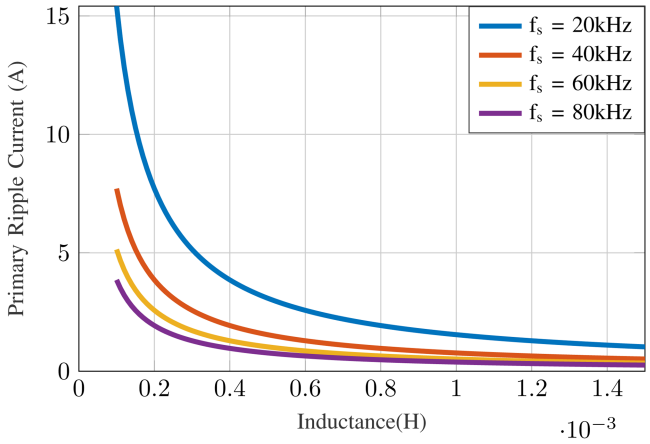

Fig. 9. Curve of current ripple magnitude as a function of transformer magnetizing inductance L_m referred to primary side, with $N = 10$.

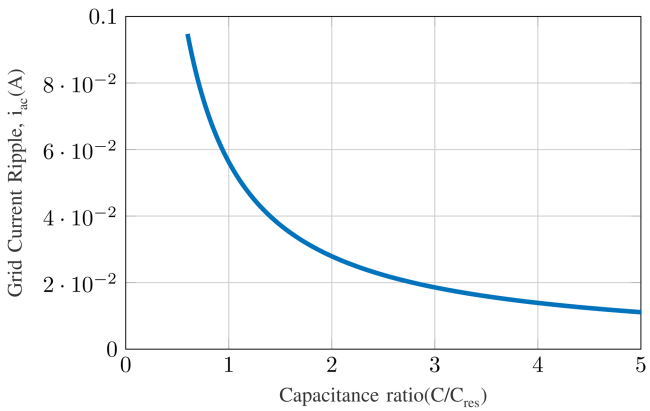

Fig. 10. Magnitude of ac current ripple as a function of capacitance ratio $f_s = 80$ kHz.

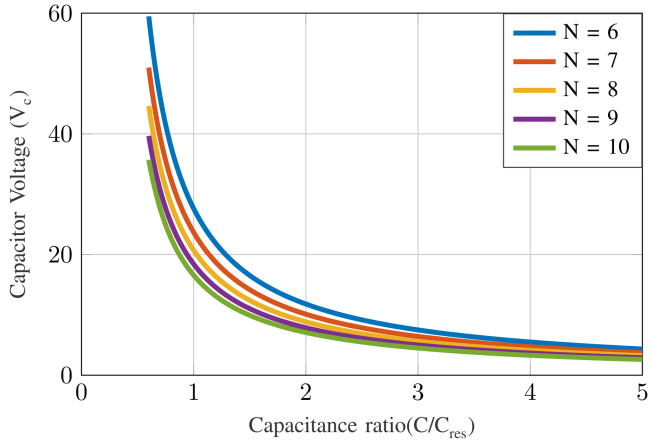

Fig. 11. Magnitude of voltage ripple on capacitor as a function of capacitance ratio, with N as a parameter, $f_s = 20$ kHz.

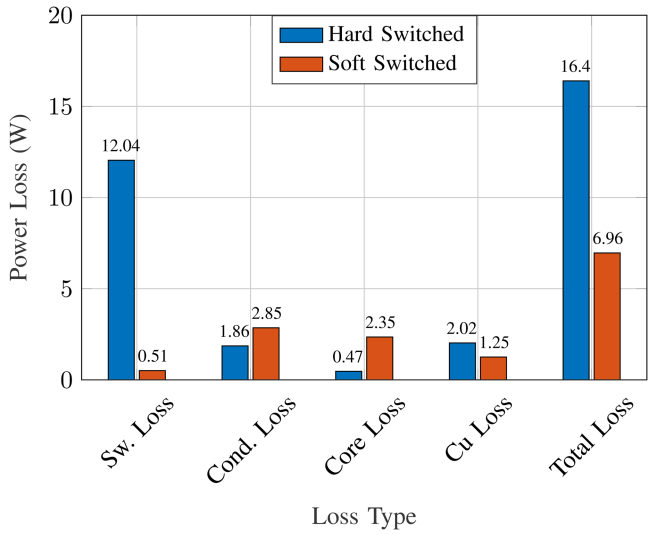

Fig. 12. Comparison of converter losses between a conventional hard-switched inverter and the proposed soft-switching inverter topology.

duty cycle axis. These curves show that the peak value of current ripple appears when the duty ratio is at 0.5. The current ripple magnitude reduces as the switching frequency is increased while maintaining a constant duty cycle.

Fig. 7(a) shows the envelopes for the inverter current i_{inv} over one line cycle for phase A current while employing the SPWM technique. In this modulation technique, the duty cycle changes with the magnitude of the ac voltage, which is superimposed on the neutral point voltage. Since the neutral point voltage is at midpoint of dc bus voltage, the duty cycle varies sinusoidally around 0.5. Correspondingly, the current ripple is at its maximum value at the voltage zero-crossing points, and it is minimum, near the peak value of ac voltage. As the root mean square (rms) value of ac voltage increases, the difference between the maximum and minimum value of current envelope increases. Fig. 7(b) shows the envelope for inverter current with variable frequency operation. The current ripple and the ZVS current magnitudes are observed to have been optimized over the line cycle. The current magnitude optimization results in achieving ZVS over the entire line cycle, whereas without variable frequency modulation, ZVS is achieved only in a fraction of the line cycle.

The transformer secondary-side current i_{sec} exhibits a similar variation in magnitude over a line cycle, as shown in Fig. 7(c) (this current envelope is shown for phase A only). The current i_{sec} comprises only the ripple current, since the low-frequency component is blocked by the filter capacitor. The circuit parameters chosen for deriving these curves are such that the circuit achieves ideal current ripple cancellation. It is observed that using SPWM along with variable frequency modulation, the magnitude of current ripple changes over the line cycle such that its magnitude is larger than the grid current. Therefore, its maximum value coincides with the peak value of grid current. Envelop of secondary current ripple using variable frequency operation is shown in Fig. 7(d). The magnitude of current ripple using variable frequency operation is optimized throughout the line cycle in a way that its magnitude is lower near the zero crossings, while it is larger near the peak value of grid voltage. Envelop of secondary-side current should follow the grid current magnitude in order to achieve current ripple cancellation throughout the line cycle.

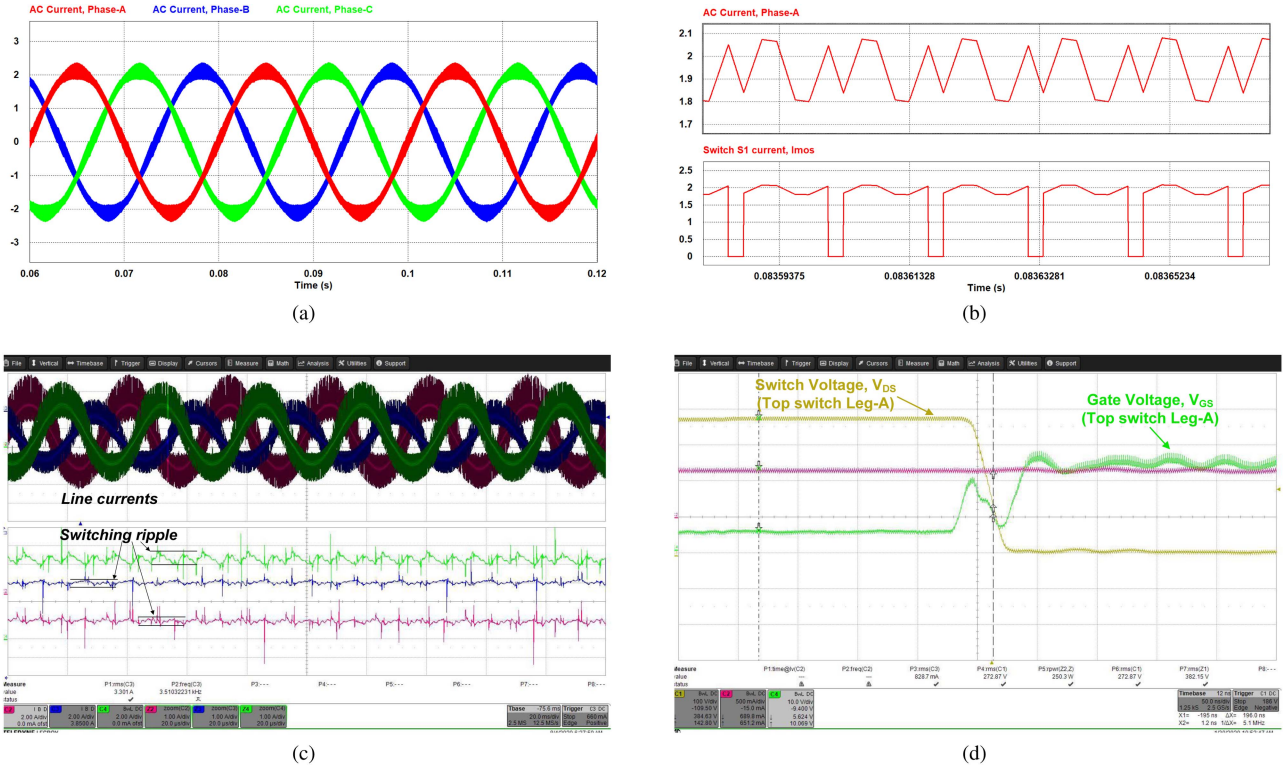

Fig. 13. Simulation and experimental waveforms of the hard-switched three-phase inverter. (a) Line cycle current waveforms (inverter current and ac current) for the three-phase inverter utilizing modified SPWM and inductive filter. (b) Switching cycle current waveforms for the three-phase inverter utilizing modified SPWM. Top: AC current and inverter current. Bottom: Switch current for top MOSFET. (c) Waveforms for the three-phase hard-switched inverter. Top: Line cycle scale for inverter current. Bottom: Zoom to switching cycle time scale for inverter current. (d) Switching cycle waveforms of top switch in positive-half line cycle showing hard-switched operation.

TABLE II
COMPARISON OF THE PROPOSED INVERTER CIRCUIT WITH OTHER SOFT-SWITCHED INVERTERS

Parameter	Proposed topology	Current ripple steering	*LCL* filter
Filter Type	Transformer + *LC*	CI + *C*	*LCL*
Filter Inductance	290 μH	1160 μH	290 μH
Second Inductance	26.1 μH	290 μH	86 μH
Size of magnetic elements	Small	Bulky	Bulky
Filter Capacitance	3.3 μF	0.1 μF	1 μF
Current Ripple Cancellation	Yes	Yes	No
Core losses*	2.35 W	3.1 W	1.96 W
Copper losses*	1.25 W	1.73 W	3.4 W
Peak Efficiency	98.7%	98.5%	98.4%

* Estimated values.

The variable frequency technique incorporated to optimize the ZVS performance limits the ZVS current to a minimum required value. The main concept is to modulate the size of peak-to-peak current ripple over the line cycle by changing the time period of the switching cycle. Consequently, the change in switching frequency is based on (30), assuming circuit parameters remain constant. The variation of the switching frequency over one line cycle is shown in Fig. 8 for different ac voltages. It can be observed that the higher ac voltages require lower minimum switching frequency for maintaining optimum ZVS. Similar change in switching frequency is required due to an increase in the output power. A higher output current would require a higher peak-to-peak current ripple to achieve ZVS, and hence a lower switching frequency is used for converter operation.

III. DESIGN OF CIRCUIT PARAMETERS

A. Design of Transformer

The transformer design is governed by the value of magnetizing inductance, the magnitude of current in the primary winding, and the range of operating frequencies used in the inverter. The value of inductance should be small enough such that lowest frequency operation is able to achieve ZVS at the highest value of load current. As a tradeoff, its value should be large enough that only an optimum ZVS current is obtained at the abovementioned operating point. Moreover, the turns ratio is chosen for optimizing the size of the proposed filter, which entails optimizing the size of filter capacitor while adjusting the dynamic response of grid current. The value of magnetizing inductance required for the current ripple cancellation technique is given by

$$L_m = \frac{N|V_{\text{AC-peak}}|(1-d)T_s}{2(N-1)(I_{\text{ac}}+I_{\text{zvs}})}. \tag{31}$$

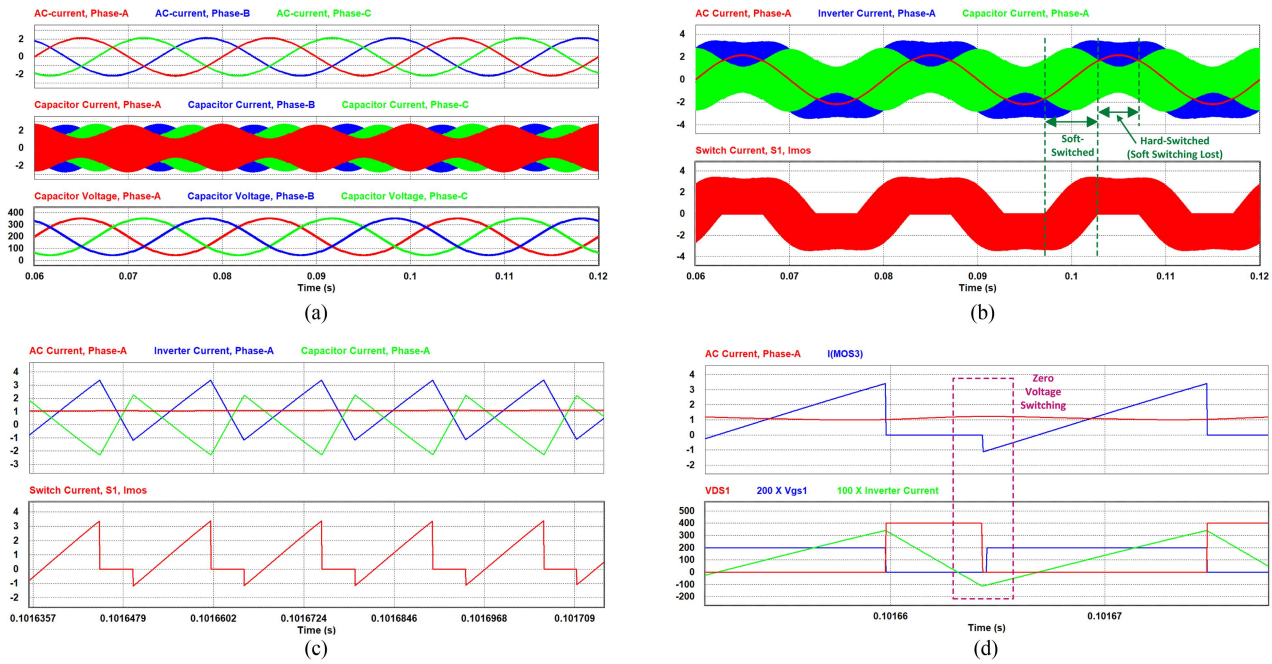

Fig. 14. Key waveforms of the soft-switched three-phase inverter with ripple cancellation in load current. (a) Switching cycle current waveforms for the three-phase inverter utilizing SPWM. Top: Load current in three phases, (middle) capacitor current in three-phases. Bottom: Capacitor voltage in the three phases. (b) Line cycle current waveforms and envelop shapes for the following. Top: Load current, capacitor current, and inverter current in phase A. Bottom: Switch current of top MOSFET of leg A. (c) Switching cycle current and voltage waveforms for the following. Top: Load current, capacitor current, and inverter current in phase A. Bottom: Switch current for top MOSFET of leg A. (d) Switching cycle current and voltage waveforms for the three-phase inverter utilizing SPWM. Top: Load current and switch current. Bottom: Switch voltage $V_{\rm DS}$, gate drive voltage V_{GS}, and inverter current $i_{\rm inv}$.

The value of inductance given by (31) is dependent on the power rating of the converter and the range of operating frequencies. In the present prototype, a transformer turns ratio of $N = 10$ and a minimum operating frequency of $f_s = 20\,\text{kHz}$ were selected. The values of converter operating parameters mentioned in Table I yield a value of 290μH for the transformer magnetizing inductance. Correspondingly, the ideal value of magnetizing inductance on the secondary side is $2.9\,\mu$H. The transformer primary-side peak current value is 5 A. A Kool mu core (Part No. 77083), from Magnetics Inc., was selected such that it does not saturate for the peak value of currents. The specifications of the transformer turns are mentioned in Table I. Fig. 9 shows the design curves for selecting the value of magnetizing inductance based on required current ripple magnitude and switching frequency.

B. Design of External Inductor

The current ripple developed in the secondary circuit depends on the value of external inductance. The value of external inductance required for ripple cancellation is determined from (14) to be $L_{\rm ext} = 26.1\mu$H.

C. Design of Capacitor

The design of capacitor requires the following two main criteria to be satisfied.

1) The magnitude of switching ripple on the capacitor voltage should be restricted to a minimum, as this ripple is responsible for the residual switching frequency ripple in output current.
2) The resonant frequency of the inductance in the secondary circuit and capacitor should be lower than the switching frequency of the converter.

The residual current ripple depends on the value of capacitance, and hence the design of this capacitor is critical. The capacitor design curves are generated by using results from (21)–(27). Fig. 10 shows the magnitude of current ripple injected into the load as a function of capacitance ratio ($\frac{C}{C_{\rm res}}$), where the capacitance $C_{\rm res}$ is the capacitance calculated using (21) for the selected minimum switching frequency. A capacitance corresponding to a ratio of 3 is selected to maintain the worst case voltage and ac current ripple under 10% of their respective maximum values.

Fig. 11 shows the curve of ripple voltage as a function of the capacitance. It can be seen that the voltage ripple on the capacitor decreases with an increase in capacitance value. However, at the same time, the physical size and cost of this capacitor must be taken into account while selecting the value. The capacitor value determines the magnitude of high-frequency ripple present in the ac current. A lower magnitude of capacitor voltage ripple would result in a lower magnitude of the current ripple. Therefore, a large capacitance value is selected. As a tradeoff, the higher the magnitude of the capacitor is, the higher is the magnitude of the low-frequency current through it due to lower impedance. Thus, the value of capacitor C is selected such that the magnitude of ripple voltage (peak-to-peak) remains in the range 5%–10% of the value of the low-frequency component, i.e.,

$$C = \frac{1}{2}\frac{I_{\text{ac}-\text{rip}-pk}}{2}\frac{T_s}{2}\frac{1}{(0.1 \times V_{\text{ac}-\text{peak}})}. \tag{32}$$

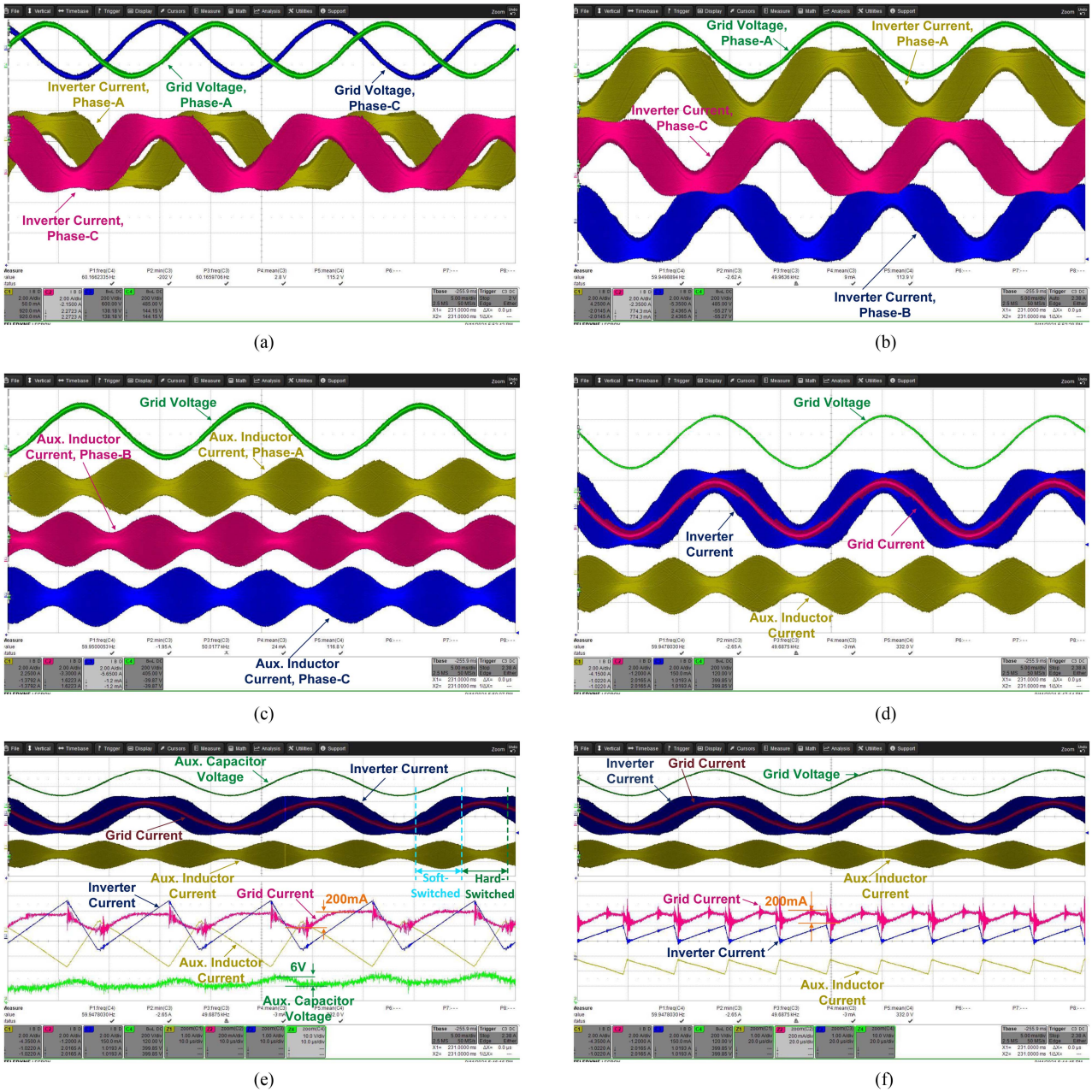

Fig. 15. Key waveforms of the fixed frequency operation of the proposed soft-switched three-phase inverter with ripple cancellation in ac current. (a) Line cycle waveforms of inverter current envelop and ac voltage for phases A and C of the three-phase inverter utilizing SPWM. (b) Line cycle current waveforms and envelop shapes for three inverter currents and ac voltage. (c) Line cycle waveforms for capacitor current envelop for the three phases and ac voltage. (d) Line cycle current envelops and voltage waveforms for one phase of the converter. (e) Top: Line cycle current envelops and capacitor voltage waveforms for one phase of the converter. Bottom: Switching cycle waveforms for currents and capacitor voltages. (f) Top: Line cycle current envelops and ac voltage waveforms for one phase of the converter. Bottom: Switching cycle waveforms for currents.

According to the second criterion listed above for the design of capacitor, resonant frequency of the circuit, given by (21), should be chosen lower than the minimum switching frequency to avoid any unwanted resonance by the PWM switching action. Hence, another condition on designing the capacitor is given by

$$\frac{1}{2\pi\sqrt{L_{\text{ext}}C}} \leq \frac{f_{s_{\min}}}{10}. \tag{33}$$

Practically, a capacitance lower than this value is chosen. Since the secondary circuit does not have any resistors except for the parasitic resistance of the components, even when the relationship specified by the (33) is satisfied, some controller damping is necessary to avoid exciting unwanted resonance in the system due to noise and system disturbances.

The proposed circuit provides soft switching and output current ripple cancellation. A net reduction in the inverter losses is achieved as compared to the hard-switched inverter. In this case, the benefit appears from the increased turns ratio that allows for optimizing the transformer design used for ripple cancellation. The process of optimizing the proposed filter comprises of

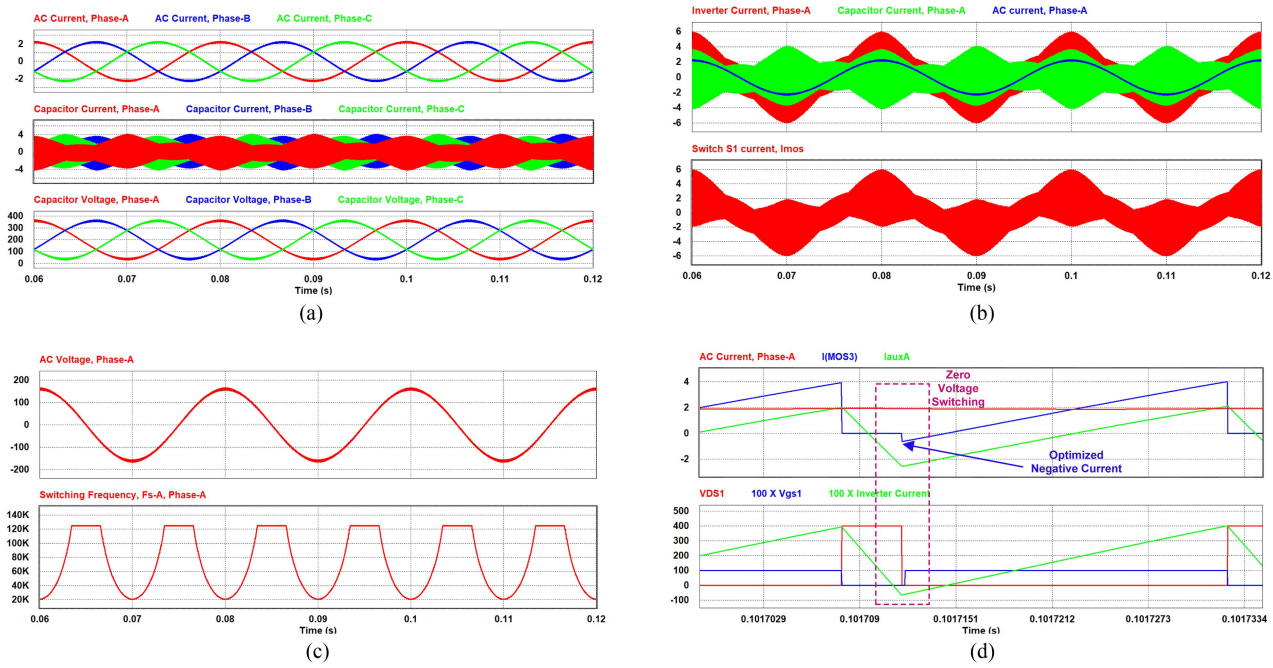

Fig. 16. Simulation waveforms of the proposed converter circuit utilizing variable frequency SPWM operation. (a) Line cycle current waveforms and current envelops for the three-phase inverter utilizing SPWM and variable frequency operation. Top: AC current in three phases and middle capacitor current in three-phases. Bottom: Voltage across the capacitor in three phases. (b) Line cycle current waveforms and envelop shapes with variable frequency SPWM. Top: AC current, inverter current, and capacitor current in phase A, Bottom: Switch current of top MOSFET in leg A. (c) Top: AC current in phase A. Bottom: Switching frequency of leg A. (d) Switching cycle waveform showing ZVS with optimized reverse current for soft switching. Top: AC current and switch current. Bottom: Switch voltage $v_{\rm DS}$, gate drive voltage v_{gs}, and inverter current $i_{\rm inv}$.

selecting the transformation ratio and correspondingly designing the external inductance and capacitance values. The details of achieving an optimized filter network using the proposed method will be presented in a future article. A comparison of losses with the hard-switched inverter, as shown in Fig. 12, shows that total losses in the inverter using the novel filter circuit are lower than a conventional hard-switched converter topology. Even though the switch rms currents increase, which increase the conduction losses of the converter, they are more than compensated by the reduction in switching losses. Therefore, the soft-switching technique utilizing the novel filter circuit prove to be more efficient as compared to a hard-switched inverter.

D. Comparison of the Proposed Inverter Topology With Conventional Soft-Switching Inverter Topologies

In this section, the proposed inverter circuit is compared with two other inverter topologies that do not require additional active circuits to achieve soft switching. The topologies used for comparison are the conventional *LCL* filter-based three-phase inverter operated in BCM for achieving ZVS [38], [46], [47] and the CI-based ripple steering inverter topology [35], [39]. The three topologies present very comparable cases, such that if designed for the microinverter application, same current waveform is present in the inverter switches. Therefore, their soft-switching performance and semiconductor losses are identical. The differences in the three topologies are given in Table II. All three of these topologies present third-order filtering of the inverter voltage using different filter architectures. The ripple steering inverter topology comprises a CI and a small capacitor. The CI decouples the line frequency and switching frequency components of the current in its two windings. However, the inductance value of the two windings cannot be chosen independently, which results in a bulky magnetic component and high magnetic losses. On the other hand, the conventional *LCL* filter utilizes two medium size magnetic components and a capacitor. Both the magnetic elements carry the line frequency current component, which makes both of them to be bulky in size. The proposed filter architecture, in comparison to the other two topologies, provides smallest magnetic components (one medium size transformer and one small external inductor). Only the transformer primary winding carries the line frequency component, whereas the secondary-side circuit of the transformer winding mainly carries the high-frequency component. The optimization of magnetic elements by utilizing the transformer turns ratio provides the main benefit in terms of small physical size of the inductor and lower magnetic losses.

IV. Simulation and Experimental Results

The proposed circuit was simulated on the powerSIM software for a power rating of 600 W using the circuit parameters given in Table I. A 208-V three-phase ac voltage [49], [50] is used for the prototype converter aimed at residential and commercial rooftop PV power generation systems. The key parameter waveforms are studied under various operating conditions. A conventional hard-switched three-phase full-bridge

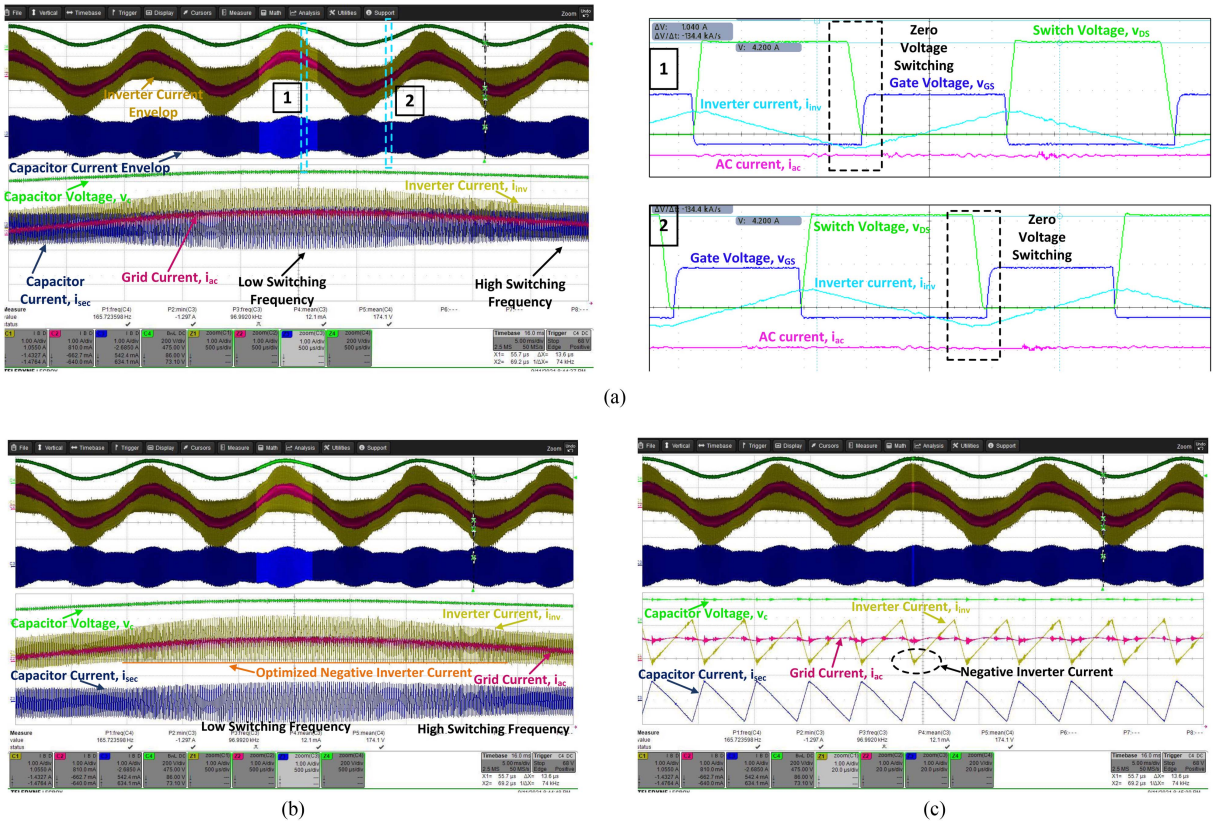

Fig. 17. Key waveforms of the variable frequency SPWM-operated soft-switched three-phase inverter with ripple cancellation in ac current using the current cancellation method. (a) Top: Line cycle current waveform envelops and ac voltage for variable frequency three-phase inverter utilizing SPWM. Bottom: Switching cycle waveforms for current and voltage showing capacitor current envelop always larger than ac current. Top right: Switch voltage, gate voltage, and inverter current showing ZVS performance close to peak of ac line cycle. Bottom right: Switch voltage, gate voltage, and inverter current showing ZVS performance close to zero crossing of ac line cycle. (b) Top: Line cycle waveforms for current envelop shapes using SPWM Bottom: Constant minimum inverter current and its envelop, ac current, and capacitor current. (c) Switching cycle current and voltage waveforms showing negative inverter current during switch turn ON, showing soft switching.

inverter has also been presented here for the comparison purposes. A lab prototype was prepared for experimental verification of the proposed soft-switching technique of the inverter. The voltage sensor for both the dc bus voltage as well as ac voltage uses potential dividers with appropriate scaling. The output of voltage divider is fed into an op-amp buffer and an analog-to-digital converter for digitizing the voltage signals. Digital signals on the ac side were isolated from dc side using a high-speed digital isolator $ISO7762$ from Texas Instruments and are acquired by the digital processor, cyclone $10LP$ series field programmable gate array (FPGA) ($10CL040YF484I7G$) from Intel [51]. Hall-effect current sensors from Allegro Microsystems ($ACS722LLC$) were used for sensing the ac current that provide a cheap solution for high-bandwidth (120 kHz) accurate current sensing as well as isolation. The FPGA is used for implementing the converter control system that includes dc bus voltage control, current control, fixed frequency modulation, and variable frequency modulation. The experimental results in this section are presented for the inverter operation with SPWM at steady-state. The focus of the experiments is on the steady-state circuit properties achieving soft switching and ripple cancellation. The transient performance of the circuit, its behavior under weak grid conditions, etc., will be presented in a future article that focuses on the control system development for the proposed converter topology.

A. *Hard-Switched Three-Phase Full-Bridge Inverter*

The simulation and experimental results for the hard-switched inverter operation using SPWM are shown in Fig. 13. The line currents for the three phases are shown in Fig. 13(a). The unity power factor mode of operation is investigated. The current ripple can be seen to be present throughout the line cycle due to the absence of capacitive filter. Fig. 13(b) shows the current ripple through the filter inductor (top waveform) and switch current of the top MOSFET (bottom waveform) for leg-A. The switch current in each switching cycle starts from zero instead of a negative value and directly jumps to the inductor current proving the hard-switching performance. These waveforms further show that the current ripple through the inductor is large (around 1 A) even after using a large value of inductance (2 mH). This ripple is injected in the load along with the low-frequency component of the line current. Fig. 13(d) shows the current envelop of the MOSFET current over couple of line cycles. The top waveform in this figure is the line current shown for reference of magnitude and phase angle. The experimental waveforms for

line current are shown in Fig. 13(c). The line currents of three phases in the line cycle time scale (top) and switching cycle time scale (bottom) validate the simulation results shown in Fig. 13.

B. Operation of the Proposed Inverter Circuit Using SPWM

Simulation results for the three-phase full-bridge inverter utilizing the proposed ripple cancellation circuit and fixed frequency SPWM are shown in Fig. 14. The inverter operation under unity power factor is presented here, thus the phase angle of current waveforms also depicts the phase angle of the ac voltage. The voltage difference across the inductor is large near the voltage zero crossings, and hence the large current ripple is observed at those points, whereas the small magnitude of ripple current is observed near the peak values of ac voltage. Due to this phase shifted behavior of the current ripple magnitude, the fixed frequency operation would result in achieving soft-switching operation for a larger portion of the line cycle in case of reactive power injection, i.e., power factor less than 1. Fig. 14(a) shows the current injected to the load (top) for all three phases, the current envelop of the three capacitor current waveforms (middle), and the voltage waveforms of the three capacitors (bottom). The capacitor voltage waveforms at steady-state are very close to the ac voltage, as was shown in the theoretical analysis. Fig. 14(b) shows the waveform of secondary-side current superimposed on the inverter current waveform and ac current waveform for phase A. It can be seen that the ac current has a negligible current ripple as compared to the inverter current, due to current ripple cancellation property of the proposed circuit. The bottom waveform of this figure shows the envelop of the MOSFET switch current, which can be seen to have negative current during the positive half line cycle depicting negative turn ON current. The negative turn ON current for MOSFETs provide the conditions for soft switching. Fig. 14(c) shows the zoomed version of the current waveforms on a switching time scale, where the top waveform shows the inverter current, capacitor current, and ac current. The slope of inverter current ripple and capacitor current ripple are negative of each other that add up to cancel the ripple in the ac current. A small magnitude of current ripple appearing in the ac current is due to the presence of voltage ripple on the capacitor. The MOSFET current waveform (bottom) shows that every switching cycle starts with a negative current showing ZVS operation. The bottom waveform of Fig. 14(d) shows the voltage ripple on the capacitor.

The experimental waveforms for the proposed inverter circuit using fixed frequency SPWM are shown in Fig. 15, and Fig. 15(a) shows ac voltages of two phases and their corresponding inverter currents. Large magnitude inverter current ripple is observed in this figure, due to small value of transformer magnetizing inductance used in the circuit. The three-phase circuit operation is shown in 15(b), where the inverter currents in three phases are presented. The current envelop for inverter current over a line cycle shows expected shape, due to the large magnitude current ripple superimposed on the low-frequency line current, as shown in the theoretical analysis. Fig. 15(c) shows capacitor current in the three phases. The envelop of current ripple is consistent with that shown in the analysis. The magnitude of current ripple near the zero-crossing of ac voltage has large magnitude, whereas

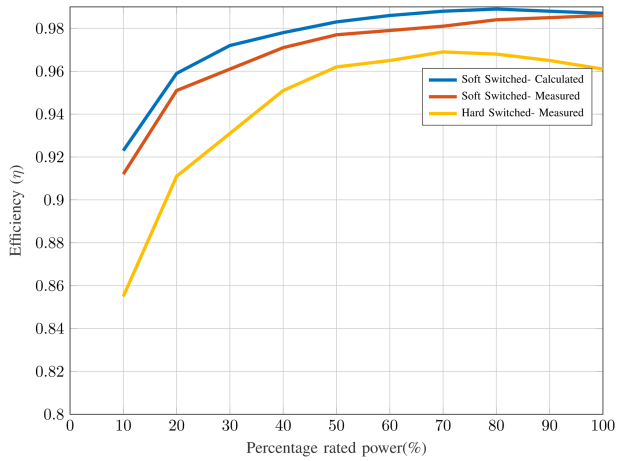

Fig. 18. Calculated and measured values of converter efficiency for the proposed soft-switched converter circuit.

near the peak value of ac voltage, the current ripple is smaller, due to low voltage difference across the primary winding of the transformer. Fig. 15(d) shows the voltages and currents at various points in the circuit for phase A. The ac current with a small current ripple (pink) is superimposed on the inverter current (blue) with large current ripple. The capacitor current (yellow) for this phase consists mainly of the high-frequency ripple current, whereas a negligible low-frequency component is present. Fig. 15(e) and (f) show the waveforms of these parameters (line current, inverter current, capacitor current, and capacitor voltage) on the switching frequency time scale close to zero crossings and peak values of ac voltage, respectively. It can be seen that the inverter current ripple (blue) is same in magnitude ($\sim$4 A) as the capacitor current ripple (yellow), but their slope is negative of each other. These two currents are added to form the line current (pink) that contains around 20 times lower ripple content (200 mA). The small switching component is observed in the ac current, due to deviation of the inductor values in the primary and secondary circuits from the theoretical values. A lower tolerance in the component values has a potential of reducing the magnitude of current ripple in the output current even further. The capacitor voltage waveform in Fig. 15(e) (green) is similar in shape to the ac voltage and contains very small high-frequency voltage ripple ($\sim$5 V). Fig. 15(f) shows these parameters close to the peak value of ac voltage and the current ripple magnitudes are significantly lower ($\sim$2 A). A similar reduction (as was observed near the zero crossings) in high-frequency current ripple is observed in the ac current. The fixed frequency operation of the converter shows that the current ripple has a bipolar nature near the zero crossings of ac voltage, since the instantaneous value of low-frequency component is small, and hence the inverter is soft-switched, whereas the current ripple near the peak value of ac voltage remains unipolar and does not provide the necessary current for soft switching. The inverter loses soft switching near the peak values of ac voltage under the unity power factor operation. The inverter soft switching is ensured in every switching cycle by the help of variable frequency operation, such that the necessary reverse current is generated.

The simulation waveforms for the variable frequency operation of the proposed soft-switched converter using SPWM are shown in Fig. 16(a)–(c). The top waveform in Fig. 16(a) shows the three ac currents with reduced switching ripple. The capacitor currents in the three phases are shown in the middle waveform of Fig. 16(a). The magnitude of capacitor current under variable frequency operation is significantly different from the fixed frequency operation. The magnitude of its envelop is higher than that of the ac current near the peak value of ac voltages. The bottom waveform shows the voltage across the capacitor in the three phases. These voltages are nearly equal to the output ac voltage. Fig. 16(b) shows currents in different sections of the circuit in phase A circuit in the top waveform. The ac current is superimposed on the capacitor current waveform and inverter current waveform, which shows a comparison of their magnitudes. The bottom waveform presents the current through primary side of transformer in Leg A. It can be seen that the switch current envelop has a negative minimum value during the positive half of the ac voltage (and vice versa in the negative half line cycle). The negative value of current envelop shows the presence of negative current in the MOSFET during turn ON. Fig. 16(c) shows the variation in switching frequency over a line cycle for unity power factor mode of operation. The minimum frequency is obtained at the peak value of ac current, i.e., maximum time duration is provided for the current ripple to become negative at the peak value of ac current. The minimum operating frequency is chosen to be close to 50 kHz, whereas the highest operating frequency is chosen as 125 kHz. Fig. 17(a)–(c) show the experimental results of the variable frequency operation of the proposed circuit. The inverter current envelop and capacitor current envelop have a similar shape and values as that obtained through simulations. The top waveform for Fig. 17(a) show the capacitor voltage (green), ac current (pink) superimposed on inverter current (yellow), and the capacitor current (blue). The inverter current envelop shows a bump near the peak values of ac voltage. This shows the region when the variable frequency operation is active. The bottom waveform shows the ac current superimposed on the capacitor current. The high-frequency capacitor current magnitude is larger than the ac current throughout the line cycle. The variation in switching frequency is observed in this image, with high switching frequency on the two ends of the image, whereas low switching frequency in the middle, closer to the peak values of the ac current. The variation in switching frequency as calculated using (30) would be different for the case of reactive power, since the current zero crossings will be phase-shifted from the voltage zero crossings. Therefore, the location of peak magnitude of current ripple will also shift from the case of unity power factor. The bottom waveform in Fig. 17(b) shows the ac current superimposed on the inverter current, where a constant value of negative current is observed in the positive half line cycle. In Fig. 17(c), the switching time scale waveforms for the three currents are shown. The negative value of inverter current shows ZVS performance at the peak value of ac current, while maintaining the ripple cancellation property.

The calculated and measured efficiency of the proposed converter are shown in Fig. 18. The measured efficiency of the proposed converter is also compared with the conventional hard-switched converter. The efficiency curves show that the proposed scheme of soft switching is able to improve the inverter efficiency by over 1.5%. The total harmonic distortion of the current injected into the grid was measured to be 2.6%, which is well within the requirements of the IEEE-1547 [40] standard used for grid-connected inverters. Therefore, the proposed inverter topology exhibits superior performance compared to the conventional inverter topologies.

V. Conclusion

A novel soft-switching dc–ac full-bridge inverter topology was introduced in this article that generates an ultralow ripple output current. The proposed circuit utilized a network of passive components to achieve soft switching for the inverter switches. The ZVS-based soft-switching operation for the inverter was achieved by increasing the magnitude of switching ripple in the inverter current. Moreover, the magnitude of ripple in the inverter current was optimized throughout a line cycle by employing variable frequency operation. The switching ripple presented in the inverter current was significantly attenuated from the output current, due to the ripple cancellation property of the proposed passive network. The simulation and experimental results presented in this article validated the theory and operation of the proposed circuit with soft switching and ultralow ripple ac current.

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