Investigation Into the Third Quadrant Characteristics of Silicon Carbide MOSFET

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***Abstract*—Owing to the superior performances, silicon carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs) attract a lot of attention. To increase the power density, it is desired to use the third quadrant (3rd-quad) characteristics of the MOSFET rather than the externally paralleled Schottky diode for freewheeling during the deadtime. It has been known that the 3rd-quad is far more than a body diode, and the MOS channel is also an important part of it. The channel may be not fully closed and, therefore, play a significant role in the reverse conduction even when the gate is zero or negatively biased. However, a comprehensive study of the 3rd-quad characteristics is still to be conducted. In this article, experiments and simulations are conducted and a physical model is developed to explain the 3rd-quad characteristics of the SiC MOSFET. It reveals how and why the 3rd-quad characteristics are affected by the gate voltage and the junction temperature. This article is helpful for not only the application of SiC MOSFET but also the device design.**

***Index Terms*—Body diode, MOSFET, silicon carbide, third quadrant (3rd-quad) characteristics.**

I. Introduction

THE use of silicon carbide (SiC) power metal-oxide-semiconductor field-effect transistor (MOSFET) is growing in applications such as PV grid inverters and electrical vehicle drives [1], [2], [3], [4], [5]. Compared with silicon insulated gate bipolar transistors, SiC power MOSFETs feature excellent switching characteristics such as low conduction loss [6], [7], [8]. To increase the power density, there is a strong desire to use the body diode for reverse freewheeling during the deadtime, which makes the study of the third quadrant (3rd-quad) characteristics important [9], [10].

However, there is a MOS structure parallel with the pn junction [11], [12]. There are two kinds of 3rd-quad gate bias. One may have the gate positively biased and therefore the MOS channel turned on for synchronous rectification, which is to reduce losses [13], [14]. However, to avoid the fault ride-through, a positive gate bias is not allowed during the deadtime. It is known that a zero or negative gate bias does not guarantee a closed channel in the 3rd-quad [15], [16], [17], [18], which means that the 3rd-quad is more than a body diode.

The channel takes part of the total current from the pn junction when the negative OFF-state gate voltage is higher (i.e., the negative OFF-state gate voltage is close to 0 V). The voltage drops on the p-base and across the pn junction go down. However, due to the current of pn junction goes down, fewer holes are injected into the n-drift region. This leads to weaker conduction modulation and, therefore, an increase of the voltage drop on the n-drift. The source-to-drain voltage is a result of the competition of the two. Therefore, the channel current plays a key role in the 3rd-quad characteristics. However, a comprehensive study of how the 3rd-quad characteristics are affected via MOS channel is to be conducted.

The MOS channel current is a function of the gate overdrive, which is defined as the difference of the gate bias and the threshold voltage [19]. This means that channel current could be affected not only by the threshold voltage but also by the gate bias and junction temperature.

Regarding the impact of gate voltage, it has been shown that 1.2 kV SiC MOSFET shows a lower source to drain voltage drop with higher OFF-state gate voltage [20], [21]. However, it is not true for all SiC MOSFETs. For 10 kV SiC MOSFETs, a higher OFF-state gate voltage results in a higher source to drain voltage drop at high junction temperatures and large current [22]. The influence of gate voltage on the 3rd-quad characteristics was modeled in [23], but it does not explain why the MOS channel may be formed in the 3rd-quad when the gate bias is zero or negative. In addition, it is reasonable to expect that a layout with balanced parasitic parameters (stray inductance and parasitic capacitance) for the parallel devices is preferred for the current sharing [24].

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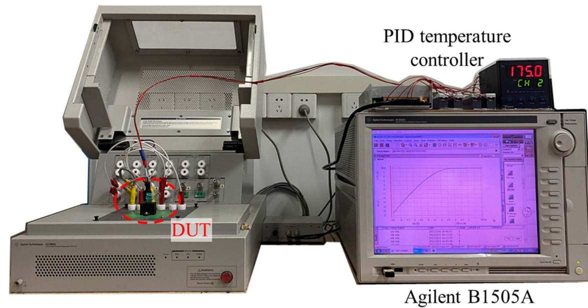


Fig. 1. Experimental platform for measuring the characteristics of the 3rd-quad. The heating platform consists of a 24 V power supply, a PID temperature controller (the control accuracy is within ±0.1 °C), a ceramic heating plate (maximum temperature 450 °C), a solid state relay, and a K-type thermocouple. The ceramic heating plate is attached to the back of the device by a clamp.

An increase of the junction temperature leads to a decrease in threshold voltage and, therefore, brings about lower channel resistance [25]. But, it does not mean that this channel gets more current from the body diode. This is because the pn junction shows a lower forward voltage drop and thus tends to take more current as the junction temperature increases [26]. Consequently, the final effect is the competition between the MOS channel and the pn junction.

In this article, experiments and simulations are conducted and a physical model is developed to answer the following basic questions.

1) Why the MOS channel may be not fully closed even when the gate is negatively biased in the 3rd-quad?
2) When the MOS channel is closed?
3) How the MOS channel affects the temperature coefficient of the reverse conduction voltage drop?

The rest of this article is organized as follows. Section II presents the 3rd-quad static characterization and physical model. Section III illustrates the influence of gate voltage on V_{SD}. Section IV discusses the possibility of a negative current temperature coefficient in the 3rd-quad. Finally, Section V concludes this article.

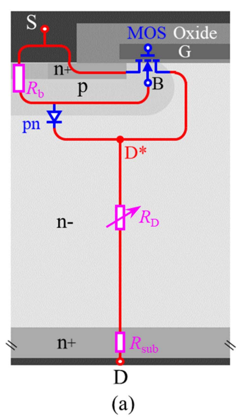
II. Third Quadrant Static Characterization and the Proposed Model

The drain-to-source current (I_{DS}) is a function of the drain-to-source voltage (V_{DS}) for a given gate-to-source voltage (V_{GS}) of a SiC MOSFET, and vice versa. If $V_{\mathrm{DS}} > 0$ V, then the current flows from the drain, through the device, to the source, and the device works in the 1st-quad. Meanwhile, if $V_{\mathrm{DS}} < 0$ V, I_{DS} is negative and the device works in the so called the 3rd-quad.

Experiments are conducted, and models are developed to reveal the underpinning physics of the 3rd-quad characteristics. The test system consists of an Agilent B1505A and a heating platform, as shown in Fig. 1. The device under test (DUT.P) is planar SiC MOSFET (SCT10N120AG), and type DUT.T is a trench SiC MOSFET (SCT3120AL). Their rated currents at $T_{\mathrm{c}} = 25$ °C are listed in Table I.

TABLE I
SiC MOSFETs Under Tests

DUT	Gate Structure	Rated current @ T_{c} = 25 °C	Minimum V_{GS}	Maximum T_{j}
DUT.P	Planar	12 A	–10 V	200 °C
DUT.T	Trench	21 A	–4 V	175 °C



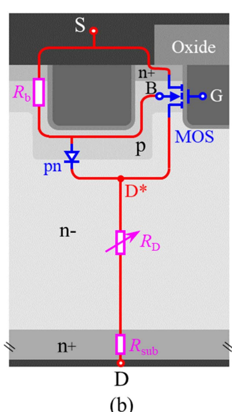


Fig. 2. Equivalent circuit models of the 3rd-quad characteristics of (a) DUT.P and (b) DUT.T. The model contains five parts: the MOS, the pn junction, the p-base region resistance (R_{b}), the drift region resistance (R_{D}), which is variable, and the substrate resistance (R_{sub}). Here, the source electrode is denoted by S, gate by G, drain by D, base by B, p-base region by p, n$^+$source by n$^+$, n-drift by n-, and substrate by sub.

A. Third Quadrant is More Than the Body Diode

A body diode exists in the SiC MOSFET, which is a pin diode and made up of the p-base, the n-drift, and the substrate regions. When $V_{\mathrm{DS}} < 0$ V, the diode may be turned on and contribute to the reverse current.

However, apart from the body diode, some other components are present in the device. The first component is the MOS structure (hereinafter referred to as MOS), as shown in Fig. 2. The second component is the parasitic npn, which is made up of the n+source, the p-base, and the n-drift regions. Therefore, the total source-to-drain voltage drop can be written as

$$V_{\mathrm{SD}} = V_{\mathrm{SD^*}} + I_{\mathrm{SD}} \times (R_D + R_{\mathrm{sub}}) \tag{1}$$

where D* is the top most part of the n-drift region, as shown in Fig. 2, R_{D} is the drift region resistance, R_{sub} is the substrate resistance, and I_{SD} is the total source-to-drain current, which is composed of three parts and can be written as

$$I_{\mathrm{SD}} = I_{\mathrm{pn}} + I_{\mathrm{ch3}} + I_{\mathrm{npn}} \tag{2}$$

where I_{pn} is the body diode current in the 3rd-quad, I_{ch3} is the channel current and I_{npn} is the parasitic npn current. Generally, I_{npn} is very small and ignored.

I_{ch3} is a function of the gate-to-source voltage V_{GS}. Accordingly, V_{GS} may modify the 3rd-quad I-V characteristics, as shown in Fig. 3, even when the gate is zero or negatively biased ($V_{\mathrm{GS}} \leq 0$ V). If V_{GS} is smaller (i.e., the gate is more negatively biased relative to the source), then the channel resistance is larger and V_{SD} is higher for a given I_{SD}. Consequently, the I-V curves

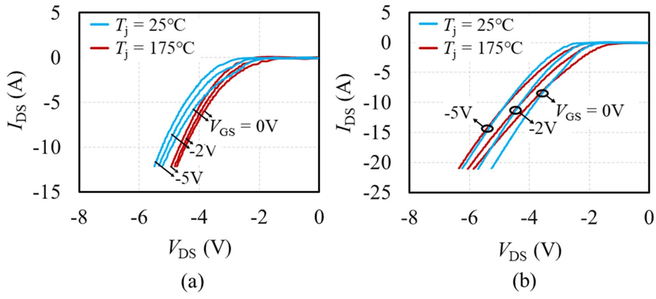


Fig. 3. Typical 3rd-quad I-V characteristics of DUT.P and DUT.T. (a) DUT.P with T_j of 25 and 175 °C, V_{GS} of 0, −2, and −5 V. (b) DUT.T with T_j of 25 and 175 °C, V_{GS} of 0, −2 and −5 V.

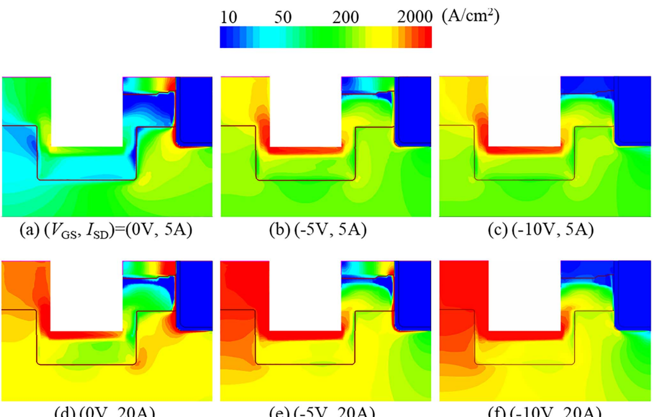


Fig. 4. Total current density distribution of DUT.T with V_{GS} of 0, −5 and −10 V, I_{SD} of 5 and 20 A. The doping concentrations of the p+, p-base, n+ and drift region are 5×10^{18} cm^{-3}, 2×10^{17} cm^{-3}, 2×10^{19} cm^{-3} and 1×10^{16} cm^{-3}, respectively. The thickness of the gate oxide is 50 nm, and the length of the channel is 0.5 μm. The TCAD simulation model was calibrated to match the experiment behavior of DUT.T, which could be used as a general case study.

shift to the left with the decrease in V_{GS}. This notion is true for both the planar and trench gate devices, whether at room or elevated temperatures.

The channel will be eventually closed with a further decrease in V_{GS}, as shown in Fig. 4. To investigate the critical V_{GS} when the channel is completely closed in the 3rd-quad, the minimum V_{GS} may be lower than the recommended V_{GS} of the datasheet. Once V_{GS} goes across a critical point which is roughly −10 V, the 3rd-quad characteristics degenerate to the forward conduction characteristics of a pin diode. V_{SD} remains constant when V_{GS} is lower than −10 V, as shown in Fig. 5. This notion implies that the I-V curve is not affected by V_{GS} anymore. Simulation analysis shows that the critical point is, but weakly, affected by I_{SD}, due to the body effect, which will be discussed in the following section [15].

The channel is not completely closed in the typical applications with an OFF-state gate voltage (V_{GS}) no lower than −5 V. This implies that: 1) $I_{ch3} > 0$ A, 2) V_{SD} is lower than that of the body diode, and 3) the 3rd-quad characteristics can be affected by V_{GS}.

B. V_{TH3} and Body Effect

As mentioned previously, I_{ch} may be nonzero in the 3rd-quad when $V_{GS} = 0$ V. On the other hand, the channel has to be

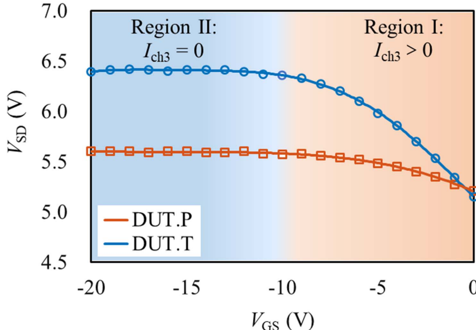


Fig. 5. Impact of V_{GS} on V_{SD}. The V_{SD} of DUT.P and DUT.T increase with the decrease of V_{GS}, and V_{SD} stops increasing when V_{GS} is about −10 V. V_{SD} is measured at I_{Dnom}.

completely closed, or the device cannot block a forward voltage of hundreds or thousands of volts when $V_{GS} = 0$ V. So, there raises a question, i.e., why the channel is formed in the 3rd-quad but closed in the 1st-quad for the same V_{GS}.

From the I-V characteristics point of view, the basic difference is the polarity of the drain-to-source voltage if the channel is not completely closed. Fig. 2 shows that the devices are not symmetrical.

In the 1st-quad, the channel current flows from the drain to the source. When $V_{GS} > V_{TH}$, the channel current is given by [19]

$$I_{ch1} = \frac{Z\mu_{ch}C_{OX}}{L_{ch}}\left[(V_{GS} - V_{TH}) \cdot V_{D^*S} - \frac{1}{2}V_{D^*S}^2\right] \quad (3)$$

where Z is the channel width, L_{ch} is the channel length, μ_{ch} is the channel mobility, C_{OX} is the gate oxide capacitance per unit area, and D* is the top most part of the n-drift region, as shown in Fig. 2.

However, $V_{SD} > 0$ V in the 3rd-quad, and the flow direction is contrary to that in the 1st-quad when the channel exists. The n-drift region is the real source of the electrons, and the n+ region is the real drain of the electrons. In comparison with the p-body is shorten by the source in the 1st-quad ($V_{BS} = 0$ V), the p-body is not shorted to intrinsic drain D* in the 3rd-quad, which may lead to $V_{BD^*} \neq 0$ V. Given that V_{TH3} is affected by V_{BD^*} [15], V_{TH3} is different from V_{TH}, which induces $I_{ch3} \neq I_{ch1}$. Thus, the channel current in the 3rd-quad has to be rewritten as

$$I_{ch3} = \frac{Z\mu_{ch}C_{OX}}{L_{ch}}\left[(V_{GD^*} - V_{TH3}) \cdot V_{SD^*} - \frac{1}{2}V_{SD^*}^2\right]. \quad (4)$$

Compared to the 1st-quad, two basic differences can be observed. First, the gate bias is the gate-to-D* voltage rather than the gate-to-source voltage V_{GS}. When V_{SD} increases for a given V_{GS}, V_{GD^*} keeps increasing and may eventually go over the threshold voltage. This condition is different from that of the 1st-quad, wherein the gate bias keeps to be constant (V_{GS}) no matter how high V_{DS} goes.

Second, the threshold voltage has to be revised due to the body effect. The body effect is induced by the body bias, which is defined to be the potential difference between the real body region (see point B shown in Fig. 2) and the real source of the electrons. The 1st-quad body bias, V_{BS} is always zero because the pn junction is reverse-biased and no current flows from the

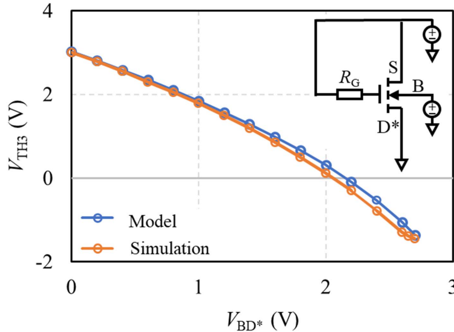
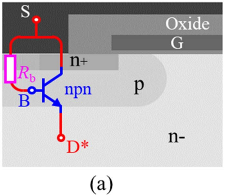
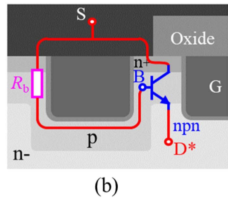


Fig. 6. Impact of V_{BD^*} on V_{TH3} is based on simulation and theoretical model, and the simulation measurement circuit of V_{TH3} under the influence of body effect is shown in the upper right corner. A p-base electrode is formed near the p-base region, and an adjustable voltage source is connected between B and D*. V_{TH3} is defined as the V_{GD^*} when the source-to-drain current reaches 10 mA, and the simulated V_{TH3}-V_{BD^*} curve is obtained by changing the adjustable voltage source (V_{BD^*}).





(a) (b)

Fig. 7. Parasitic npn transistor in the 3rd-quad of (a) DUT.P and (b) DUT.T. The base, emitter and collector of the parasitic npn is p-base (B), n-drift (D*), and n+, respectively.

p-base region to the source. Unlike the 1st-quad, the 3rd-quad body bias is B-to-D* voltage V_{BD^*}, and becomes positive when V_{SD} goes higher. According to the 1st-quad threshold voltage with substrate bias [19], [27], when a substrate bias (V_{BD^*}) is applied in the 3rd-quad, the threshold voltage in the 3rd-quad is given by

$$V_{\mathrm{TH3}} = V_{\mathrm{FB}} + 2\psi_{\mathrm{B}} + \frac{\sqrt{2\varepsilon_{\mathrm{S}} \cdot q \cdot N_{\mathrm{A}}}}{C_{\mathrm{OX}}}\sqrt{2\psi_{\mathrm{B}} - V_{\mathrm{BD}^*}} \quad (5)$$

where Ψ_{B} is the Fermi potential from intrinsic Fermi potential, N_{A} is the effective channel doping concentration, q is the elementary charge, ε_{s} is the silicon carbide dielectric constant, and V_{FB} is the flat band voltage, which is given by

$$V_{\mathrm{FB}} = \phi_{\mathrm{MS}} - \frac{Q_{\mathrm{f}} + Q_{\mathrm{it}}}{C_{\mathrm{OX}}} \quad (6)$$

where ϕ_{MS} is the work function difference between metal and semiconductor, Q_{f} is the fixed-oxide-charge density, and Q_{it} is the interface trap charge density.

The third term in (5) decreases with the increase in V_{BD^*}, eventually down to zero. Accordingly, V_{TH3} of DUT.T decreases, approaching the sum of the first two terms in (5), as shown in Fig. 6. It is worth noticing that V_{BD^*} does not go over $2\Psi_{\mathrm{B}}$, or the third term in (5) becomes imaginary and physically meaningless. The body diode is turned on because V_{BD^*} approaches $2\Psi_{\mathrm{B}}$ of ~3.0 V. The body diode current finally becomes prominent and generates a voltage drop on the n-drift and the substrate regions, which consumes the excess part of V_{SD}, i.e., $V_{\mathrm{D^*D}} = I_{\mathrm{SD}} \times (R_{\mathrm{D}} + R_{\mathrm{sub}})$.

As a result of the aforementioned two differences, the gate bias is much more prone to go over the threshold voltage in the 3rd-quad than in the 1st-quad. Specifically, the formation of MOS channel is easier in the 3rd-quad than in the 1st-quad. In a special case, when the gate electrode is shorted to the source electrode, the MOS channel is eventually formed as V_{SD} goes up, whereas the MOS channel can never be formed no matter how high V_{DS} goes. Similar behaviors can be observed even with a negative V_{GS}, as long as V_{GS} is no lower than a critical voltage, which is roughly -10 V and is a function of I_{SD} as mentioned previously.

C. Impact of Parasitic npn

It is well known that there is a parasitic npn transistor, which is suppressed to be activated in the 1st-quad by smart device designs. However, one can do nothing to prevent the activation of the parasitic npn in the 3rd-quad. This is because it is the p-base/n-drift rather than the p-base/n+ junction that plays the emitter junction of the 3rd-quad npn, as shown in Fig. 7. In the 3rd-quad, the p-base/n-drift junction, which is the pn junction of the body diode as well is forward biased. It is eventually turned ON once V_{SD} goes over the turn-ON voltage, which is roughly 2.7 V.

However, the activation of the 3rd-quad npn does not inevitably produce a significant collector current, which means I_{npn} is very small. Electrons are injected into the p-base region when the p-base/n+ junction is turned on. But only those who successfully pass through the p-base and divert into the n+ region contribute to I_{npn}, which is given by

$$I_{\mathrm{npn}} = \frac{\gamma\alpha_{\mathrm{T}}}{1 - \gamma\alpha_{\mathrm{T}}} \times I_{\mathrm{B}} \quad (7)$$

where I_{B} is the base current, γ is the emitter injection efficiency, and α_{T} is the base transport factor.

As shown in Fig. 4, the 3rd-quad I_{npn} is generally very small and negligible for the following two reasons. Unlike in the 1st-quad, γ of the 3rd-quad npn is extremely low. Because the doping concentration of the emitter (n-drift) is lower than that of the base (p-base) by several orders. Second, α_{T} is greatly limited by the low carrier lifetime in the p-base region, which is typically on the order of nanosecond.

III. Influence of Gate Voltage on 3rd-Quad Conduction Characteristics

When the 3rd-quad characteristics are utilized for freewheeling, voltages are applied to the gate electrode to control the device. A SiC MOSFET has two working states in the 3rd-quad. The first state is known as synchronous rectification, wherein the gate is biased to the ON-state gate voltage. As the MOS channel is fully open, the source-to-drain voltage drop can be much lower than that of a pin diode, resulting in a decrease in the device's power loss during the freewheeling. However, this working state is not allowed during the deadtime to avoid the fault ride-through. The second state can be called OFF-state

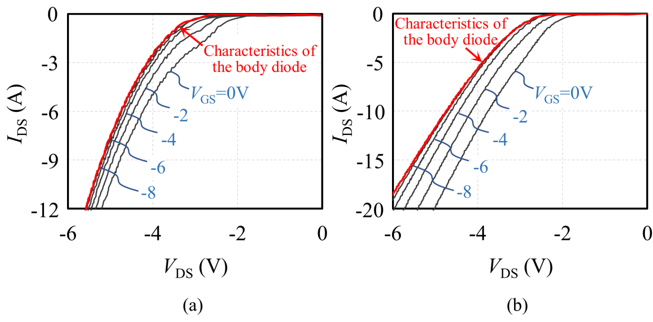


Fig. 8. Third quadrant I-V characteristics of (a) DUT.P and (b) DUT.T with V_{GS} of 0, −2, −4, −6, −8 V. I-V characteristic curves gradually overlap with the decrease of V_{GS}.

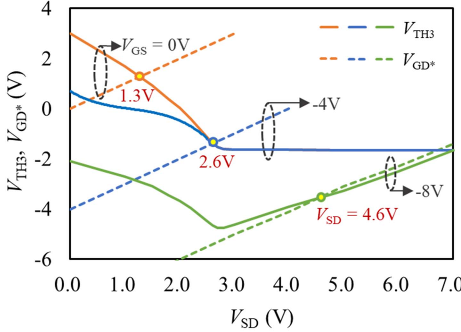


Fig. 9. Intersection points of V_{TH3} and $V_{\mathrm{GD^*}}$ are the reverse conduction voltage when the channel is formed. The solid lines are V_{TH3} of DUT.T under different V_{GS}, and the dash lines are $V_{\mathrm{GD^*}}$ under different V_{GS}.

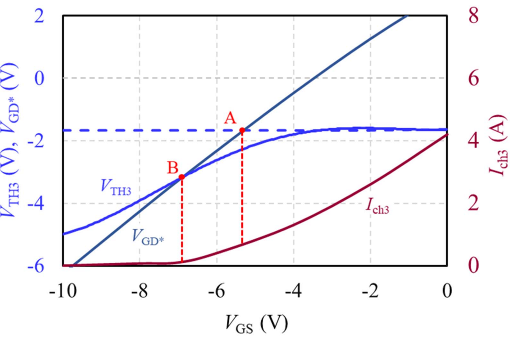


Fig. 10. I_{ch3} of DUT.T is extracted with $I_{\mathrm{SD}} = 5$ A. Dash line is V_{TH3}, which ignores the effect of Q_{it}, and the curve of V_{TH3} is V_{TH3}, which does not ignore the effect of Q_{it}. Point A is the intersection of $V_{\mathrm{GD^*}}$ and V_{TH3}, which ignores Q_{it}, and point B is the intersection of $V_{\mathrm{GD^*}}$ and V_{TH3}, which does not ignore Q_{it}.

rectification wherein the gate is biased to the OFF-state gate voltage, which may be zero or negative. As discussed in the previous section, a zero or negative gate bias does not guarantee that the MOS channel is completely closed in the 3rd-quad. Therefore, understanding how the gate voltage influences the 3rd-quad characteristics is important for making greater use of the device.

A. When Channel is Formed?

As previously mentioned, the channel current may exist in the 3rd-quad even when V_{GS} is negative. According to (4), I_{ch3} is a function of the difference between $V_{\mathrm{GD^*}}$ and V_{TH3}. Since $V_{\mathrm{GD^*}}$ is made up of V_{GS} and $V_{\mathrm{SD^*}}$, one can expect that the 3rd-quad channel current is affected by V_{GS}. Thus, there raises a question that when the MOS channel is formed.

As shown in Fig. 8, the MOS channel is closed when the gate electrode is biased so negatively that $V_{\mathrm{GD^*}}$ is always less than V_{TH3}. The 3rd-quad characteristics degenerate to the forward conduction characteristics of a pin diode, and the turn-ON voltage of which is about 2.8 V (DUT.P)/2.6 V (DUT.T). VGD* increases and may exceed VTH3 when VGS increases and gradually approaches zero. This notion implies that the MOS channel may be formed. The channel takes part of the total current from the body diode, causing the voltage drop on the body diode to decrease. Consequently, the I-V curves with V_{GS} higher than −8 V shift to the right, compared with that of the body diode (the red curve).

According to (1), $V_{\mathrm{SD^*}}$ increases as V_{SD} goes up, which results in two effects. The first effect is the increase of $V_{\mathrm{GD^*}}$ for a given V_{GS}, as shown in Fig. 9. The second effect is the decrease of V_{TH3} due to the body effect. When $V_{\mathrm{GD^*}}$ goes over V_{TH3}, the MOS channel is formed.

However, another factor has to be considered for a reasonable evaluation of V_{TH3}. According to (5), V_{TH3} is a function of both $V_{\mathrm{BD^*}}$ and V_{FB}. For a given I_{SD}, the body diode is forward biased, and $V_{\mathrm{BD^*}}$ is clamped to the turn-ON voltage of pn junction. Thus, the body effect induced by $V_{\mathrm{BD^*}}$ is no longer affected by V_{GS}. However, the flat band voltage V_{FB} is a function of V_{GS}, which causes V_{TH3} to decrease with decreasing V_{GS}, as shown in Fig. 10. Q_{it} increases under the influence of negative V_{GS} because the interface traps positive charges, resulting in the decrease in V_{FB} according to (6).

If V_{GS} is negative, then a negative electric field is formed across the channel interface. Q_{it} increases as the positive charges are trapped in the gate oxide and the interface, and V_{FB} decreases, which results in a decrease in V_{TH3}. Besides, the stronger the electric field (the lower V_{GS}), the more charges are trapped, resulting in a lower V_{TH3} in Fig. 10.

With the consideration of Q_{it}, $V_{\mathrm{GD^*}}$, and V_{TH3} intersect at point B rather than point A, as shown in Fig. 10. The gate bias induced trapping charges slow down the closing process of the MOS channel as V_{GS} becomes more negative. The gate voltage at which the MOS channel is just completely close is called the critical gate voltage, V_{CR3}. The process of SiC MOSFET is not mature enough compared with that of Si MOSFET, resulting in lots of traps existing in the oxide and interface. Fig. 10 shows a significant amount of N_{t} ($N_{\mathrm{t}} = Q_{\mathrm{t}}/\mathrm{q}$) that can go up to 1×10^{12} cm^{-2}, which leads to V_{TH3} going down to −5 V. This explains why one can still see the channel current even when V_{GS} is −7 V or lower.

Since $V_{\mathrm{GD^*}}$ is made up of V_{GS} and $V_{\mathrm{SD^*}}$, one can tell that V_{CR3} is a function of $V_{\mathrm{SD^*}}$ and, therefore, of I_{SD}, as shown in Fig. 11. The $|V_{\mathrm{GS}}|$-I_{SD} space ($V_{\mathrm{GS}} \leq 0$ V) is partitioned into two regions by a critical line. The first region has no channel current and is uncontrollable by V_{GS}, and I_{SD} is composed by I_{pn}. The other region is with a nonzero channel current and controllable by V_{GS}.

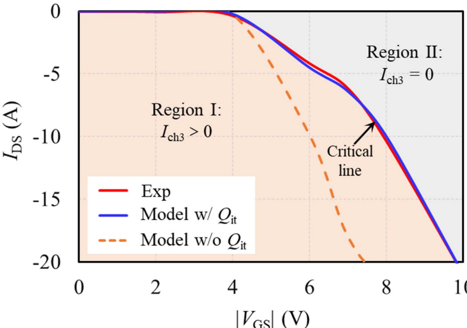


Fig. 11. I_{DS} of the curves is the conduction current when the channel of DUT.T is formed in the 3rd-quad.

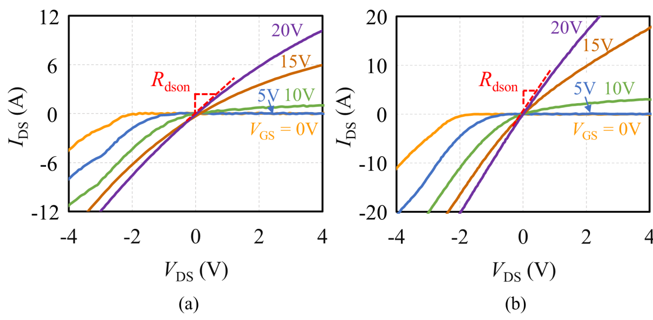


Fig. 12. I-V characteristics of (a) DUT.P and (b) DUT.T with V_{GS} of 0, 5, 10, 15, and 20 V, T_j of 25 °C. R_{dson} is the differential resistance.

For a given V_{GS}, the I-V curve may split from that of the body diode as V_{SD} goes up, as shown in Fig. 8. V_{GD^*} increases as V_{SD} goes up. When V_{GD^*} goes over V_{TH3}, the channel current is generated. Now, the source-to-drain current when the channel is formed is called critical I_{SD} ($I_{SD\text{-}C}$), and I_{ch3} is generated when I_{SD} is greater than $I_{SD\text{-}C}$. Based on the I-V characteristic of the pn junction and the critical condition for the formation of the channel, i.e., $V_{GD^*} = V_{TH3}$, the model of $I_{SD\text{-}C}$ is obtained by

$$I_{SD\text{-}C} = I_0 \exp\left(\frac{qV_{BD^*}}{\eta kT}\right) \tag{8}$$

where I_0 is the constant saturation current, η is the emission coefficient, which is used to simulate carrier generation–recombination in the depletion region of the pn junction, T is the temperature, and V_{BD^*} is given by

$$V_{BD^*} = 2\psi_B - \frac{(m-n)^2}{4} \tag{9}$$

where m and n are given by

$$m = \sqrt{4 \cdot (V_{GS} - V_{FB} + I_{SD} \cdot R_b) + n^2} \tag{10}$$

$$n = \frac{\sqrt{2\varepsilon_S \cdot q \cdot N_A}}{C_{OX}}. \tag{11}$$

According to (8)–(11), $I_{SD\text{-}C}$ increases as the V_{GS} becomes more negative, which is consistent with the experimental results, as shown in Fig. 11. It is worth noticing that the trapping charge Q_{it} plays an important role in the 3rd-quad and cannot be ignored. The effect of Q_{it} promotes the formation of the channel, and the channel can be formed at a lower V_{GS}. Accordingly, the $I_{SD\text{-}C}$ curve with Q_{it} shifts to the right in Fig. 11 compared with that of the model without Q_{it}.

Meanwhile, the turn-ON sequence of the MOS channel and body diode varied with V_{GS}. According to the critical line of I_{SD} in Fig. 11, $I_{SD\text{-}C}$ is nearby 0 A when $V_{GS} = 0$ V, and the MOS channel turns ON first, which lasted until V_{GS} decreases to -4 V. $V_{GS} = -4$ V is the critical point that the MOS channel and the body diode turn ON at the same time. Once V_{GS} is less than -4 V, $I_{SD\text{-}C}$ will exceed 0 A, and the body diode turns ON first. The theoretical analysis in this article is based on the SiC MOSFETs, but it is basically applicable to the silicon MOSFETs as well.

B. Channel Resistance Affected by V_{GS}

The I-V characteristics in the 1st-quad and 3rd-quad vary when V_{GS} is zero, as shown in Fig. 12. In the 1st-quad, the device is in OFF-state and the MOS channel can never be formed no matter how high V_{DS} goes. In the 3rd-quad, a diode-like characteristic wherein the MOS channel may be formed. The only question is which current path turns on first: the MOS channel or the body diode.

When V_{GS} is between 15 and 20 V, the MOS channel is fully open, regardless of whether it is in the 1st-quad or 3rd-quad. And it dominates the current conduction in the 3rd-quad in the vicinity of the origin. Therefore, it simply shows a resistive characteristic with the ON-state resistance given by [19] and [28]. When $V_{DS} = 0$ V, V_{BD^*} is 0 V, and V_{TH3} coincides with the 1st-quad threshold voltage.

Based on the analysis of the experimental results, the ON-state I-V characteristic is not just that of a pure resistor. Specifically, the MOS channel is not simply a resistor with constant resistance, although it is fully open. The derivative of the turn-ON conductance in the 3rd-quad is given by

$$\frac{\partial^2 I_{ch3}}{\partial V_{SD^*}^2} = \frac{Z\mu_{ch}C_{OX}}{L_{ch}} \cdot \left[1 - 2\frac{\partial V_{TH3}}{\partial V_{SD^*}} - \frac{\partial^2 V_{TH3}}{\partial V_{SD^*}^2} \cdot V_{SD^*}\right]. \tag{12}$$

According to (12), a positive derivative of the turn-ON conductance means that the channel conductance increases with increasing V_{SD^*}. Whether the derivative of the turn-ON conductance is positive or negative depends on the derivative of V_{TH3} and the second derivative of V_{TH3}.

When $V_{GS} = 0$ V, the derivative of V_{TH3} is negative in Fig. 9. Besides, the slope of the curve of V_{TH3}-V_{SD^*} decreases when V_{SD^*} increases, which means that the second derivative of V_{TH3} is negative. Therefore, the derivative of the turn-ON conductance is greater than zero. The 3rd-quad turn-ON conductance increases with increasing V_{SD}, which means the 3rd-quad turn-ON resistance decreases with the increase in V_{SD}. Besides, the result holds as the V_{GS} goes higher.

C. Controllability of Source-to-Drain Voltage

As mentioned previously, V_{SD} is a function of V_{GS}. Fig. 13 demonstrates that V_{SD} decreases with increasing V_{GS}. However, V_{SD} may not present a tendency of linear decrease all the time.

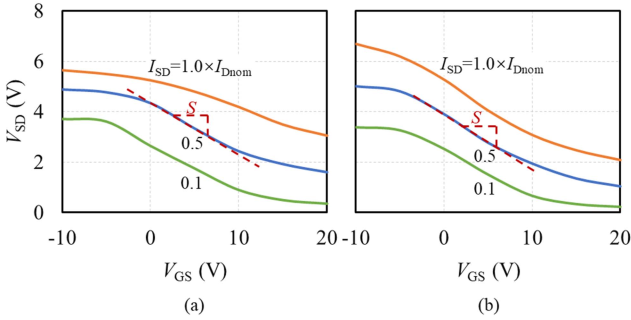


Fig. 13. Impact of the gate-to-source voltage V_{GS} on the source-to-drain voltage V_{SD} of (a) DUT.P and (b) DUT.T. The rated current, I_{Dnom}, of DUT.P and DUT.T are 12 A and 21 A, respectively. The ordinate of (b) is the same to that of (a).

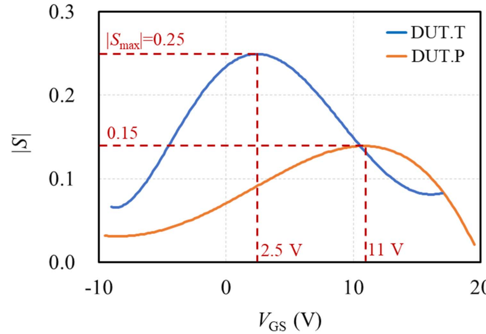


Fig. 14. Sensitivity of V_{SD} to V_{GS} as a function of V_{GS} at rated current and room temperature.

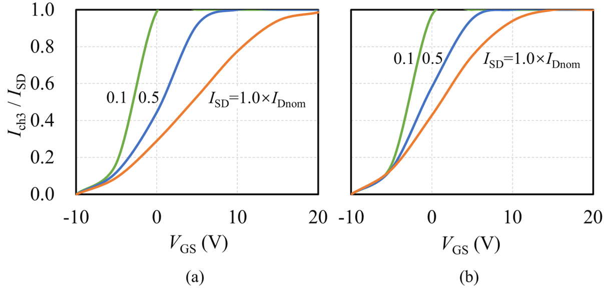


Fig. 15. Channel current ratio of (a) DUT.P and (b) DUT.T, as a function of V_{GS}. The rated current, I_{Dnom}, of DUT.P and DUT.T are 12 A and 21 A, respectively. The ordinate of (b) is the same to that of (a).

The descent speed of V_{SD} slows down as the V_{GS} increases from 0–20 V, and V_{GS} has a limited effect on V_{SD} when V_{GS} is large enough (V_{GS} is close to 20 V).

To better understand the controllability of the source-drain voltage, a parameter for a given I_{SD} is set to reflect the controllability of V_{GS} to V_{SD}. The sensitivity of V_{SD} to V_{GS}, S, is defined as $\mathrm{d}V_{SD}/\mathrm{d}V_{GS}$, which is the slope of the curve V_{SD}-V_{GS}, as shown in Fig. 13. Besides, the larger $|S|$ is, the stronger the control ability of V_{GS} to V_{SD} will be.

The effect of V_{GS} on S is shown in Fig. 14. The $|S|$ of DUT.P/DUT.T first increases and then decreases, and $|S|$ reaches the highest in V_{GS} = 11/2.5 V. At low V_{GS}, I_{SD} flows through the body diode and the MOS channel, as shown in Fig. 15. It can be seen from (1) that V_{SD} is made up of V_{SD^*} and the voltage drop on the drift region and substrate region. Besides, V_{SD^*} is made up of the voltage drops on R_b and across the pn junction. Therefore, for a given ΔV_{GS}, which is defined as the difference between V_{GS1} and V_{GS2} ($V_{GS1} > V_{GS2}$), ΔV_{SD} is given by

$$\Delta V_{SD} = \left(I_{ch3(VGS1)} - I_{ch3(VGS2)}\right) \times R_b + \frac{\eta k T}{q} \ln\left(\frac{1 - I_{ch3(VGS2)}/I_{SD}}{1 - I_{ch3(VGS1)}/I_{SD}}\right) \tag{13}$$

where $I_{ch3(VGS1)}$ is the channel current with $V_{GS} = V_{GS1}$, and $I_{ch3(VGS2)}$ is the channel current with $V_{GS} = V_{GS2}$.

It can be seen from Fig. 15 that the I_{ch3} at rated current of DUT.P/DUT.T grows faster and faster before V_{GS} reaches 11/2.5 V, which means ΔV_{SD} for a given ΔV_{GS} increases with increasing V_{GS} according to (13). Given that ΔV_{SD} is comparable to dV_{SD} when ΔV_{GS} approaches infinity, $|S|$ increases with the increase in V_{GS}. The ascending speed of I_{ch3}/I_{SD} slows down with the increase in V_{GS} to 20 V, resulting in ΔV_{SD} going down, which means $|S|$ decreases. Therefore, V_{GS} has an excellent control effect on V_{SD} when V_{GS} of DUT.P/DUT.T is close to 11/2.5 V. Besides, V_{GS} has a limited effect on V_{SD} when V_{GS} is close to -10 or 20 V.

D. *Control Method of the V_{GS}*

The channel can be formed in the 3rd-quad with a higher V_{GS}, which can reduce the conduction loss. Some data sheets recommended setting the OFF-state gate voltage to 0 V. $V_{GS} = 0$ V is a good choice for a single device if the device can be completely closed.

However, the increased V_{GS} may cause undesirable side effects for the parallel devices with different threshold voltages (threshold voltages of devices with different batches vary considerably, and SiC MOSFETs are likely to operate with V_{TH} mismatch, especially after long term of cycling) [29]. The influence of different V_{GS} on parallel devices is evaluated with a double pulse test circuit (DPT), as shown in Fig. 16. Two devices are parallel connected in the lower arm of the DPT, and their V_{TH} are different.

The freewheeling transient current sharing with different threshold voltage is shown in Fig. 17. As shown in Fig. 17(a), DUT1 with a lower threshold voltage takes most part of the total current when $V_{GS1} = V_{GS2} = 0$ V, and the difference of freewheeling current between DUT1 and DUT2 is 1.4 A. This situation is due to the channel formed in the 3rd-quad, and V_{SD} increases with the increase of V_{TH} according to (1) [25]. Thus, a device with a higher V_{TH} has a larger V_{SD}, and it gets less current.

When $V_{GS1} = V_{GS2} = -5$ V, the pn junction takes part of the total current from the channel, as shown in Fig. 4. The influence of threshold voltage on V_{SD} is weakened, and the difference of freewheeling current between DUT1 and DUT2 is reduced to 0.8 A. Therefore, an appropriate negative gate voltage is conducive to parallel applications. However, the additional losses should be taken into consideration. Besides, a very large negative gate voltage causes the threshold voltage drift and degrades the long-term reliability of the gate oxide, which may shorten the device lifetime [30].

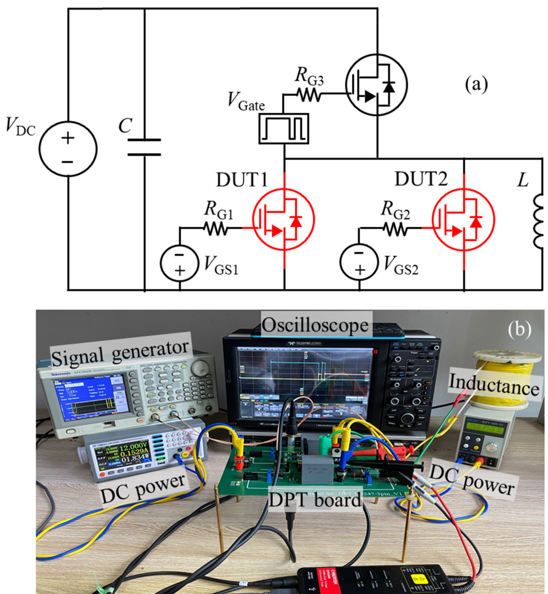


Fig. 16. (a) Circuit diagram of DPT. The input voltage V_{dc} is 300 V, and the gate-to-source voltage bias of the upper bridge arm V_{Gate} is 15 and −5 V. The gate resistance R_{G1} and OFF-state gate voltage V_{GS1} of DUT1 are the same as those of DUT2. (b) Experimental setup of DPT.

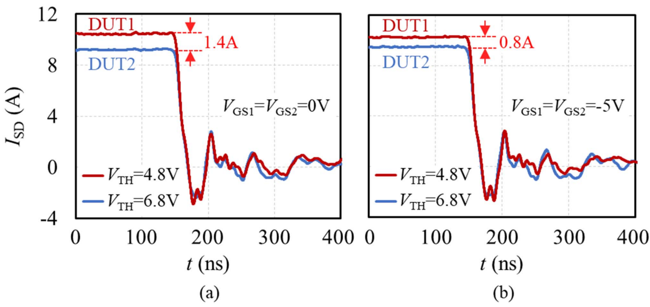


Fig. 17. Freewheeling current sharing performance of DUT.T with V_{TH} mismatch under (a) $V_{GS1} = V_{GS2} = 0$ V and (b) $V_{GS1} = V_{GS2} = -5$ V. The total current of DUT1 and DUT2 is 20 A. The ordinate of (b) is the same to that of (a).

IV. Influence of T_j on 3rd-Quad Conduction Characteristics

When the junction temperature of the devices was changed, the voltage drop across the MOS channel, and the voltage of the body diode will decrease. Besides, the change of voltage caused by T_j of the body diode and MOS channel is different. As pointed out in the previous sections, we have found that there are three conduction modes for the 3rd-quad at different gate voltages. The first mode is the channel is fully formed and all I_{DS} flows through the channel when the positive V_{GS} is large enough. The second mode is that the channel is partially formed, i.e., I_{SD} flows through the channel and body diode. The third mode is that the channel is completely closed and all I_{SD} flows through the body diode when V_{GS} is negative enough. Therefore, the effect of T_j on the 3rd-quad characteristics may vary with V_{GS}.

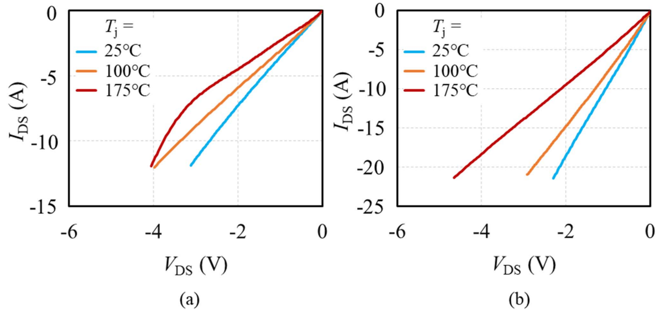


Fig. 18. Third-quad I-V characteristics of (a) DUT.P and (b) DUT.T with the MOS channel fully open ($V_{GS} = 20$ V).

A. Channel Fully Formed

At room temperature, when V_{GS} is between 15 and 20 V, V_{SD} of DUT.T increases linearly with the increase of I_{SD}. This means the MOS channel is fully open, and all I_{SD} flows through the channel. In Fig. 18(a), the kink in the I-V curve under $T_j = 175$ °C indicates that the body diode is turned ON. Besides, due to the difference in device structure, the body diode of planar MOSFET is easier to turn ON than that of trench MOSFET at high temperature [22]. The temperature coefficient of V_{SD} is positive. However, it is known that an increase in T_j leads to a lower V_{TH3} and a decrease in V_{SD}.

When the channel is fully formed, V_{SD} is made up of the voltage drops on the channel resistance (R_{ch}), R_D, and R_{sub}. When T_j increases, the change of V_{SD} for a given I_{SD} mainly depends on R_{ch} and R_D.

It is known that R_{ch} and R_D increase with decreasing mobility in the MOS channel and drift region, and mobility is sensitive to T_j [19], [31]. Therefore, the main physical mechanisms for a positive temperature coefficient in the 3rd-quad when the channel is fully formed come for two reasons. The first mechanism is related to the temperature dependence of V_{TH3}. The V_{SD} decreases with T_j due to the negative temperature coefficient of V_{TH3}. The second mechanism is related to the temperature dependence of mobility. As T_j increases, the scattering of carrier becomes stronger, resulting in a decrease in mobility, which leads to an increase in R_{ch} and R_D. Thus, the V_{SD} increases with T_j. The only question is which mechanism dominates the temperature coefficient of the V_{SD}.

Since V_{GS} is very large (V_{GS} >15 V) when the channel is fully formed, temperature induced changes in V_{TH3} has a limited effect on R_{ch}. Therefore, the effect of T_j on the mobility dominates the temperature coefficient of V_{SD}, which results in a positive temperature coefficient for the 3rd-quad when the channel is fully formed.

B. Channel Partially Formed

As mentioned previously, when $I_{SD} = I_{Dnom}$ and V_{GS} is between −10 and 10 V, the MOS channel is partially formed. The influence of T_j on V_{SD} is shown in Fig. 19. When V_{GS} of DUT.P is less than 10 V, the temperature coefficient of V_{SD} in the 3rd-quad is negative. However, the temperature coefficient of DUT.T is positive, as shown in Fig. 19(b) [32]. Thus, there

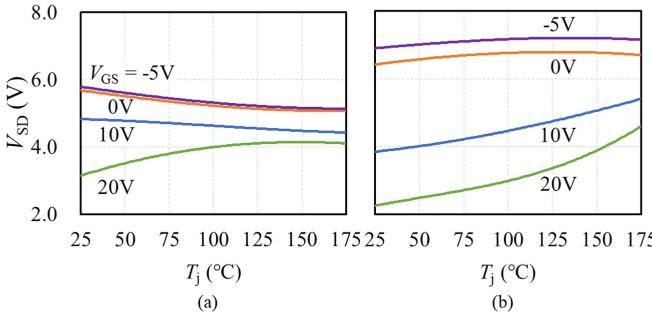


Fig. 19. Impact of the junction temperature on V_{SD} of (a) DUT.P and (b) DUT.T at rated current. The ordinate of (b) is the same to that of (a).

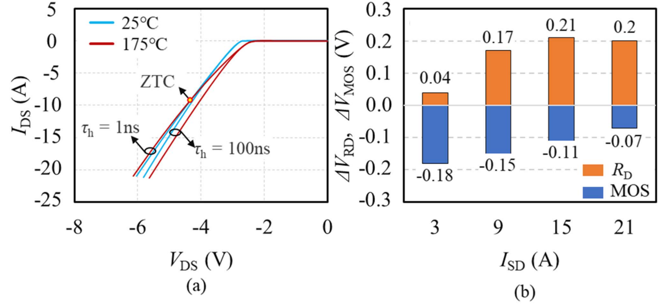


Fig. 20. (a) Third quadrant I-V characteristics of DUT.T with V_{GS} of -5 V, τ_h of 1 and 100 ns, and the intersection is called the zero-temperature coefficient (ZTC) point. (b) $\Delta V_{RD}/\Delta V_{MOS}$ of R_D/MOS is obtained at different I_{SD} with τ_h of 1 ns and V_{GS} of -5 V. ΔV_{RD} is the difference between V_{RD} with 175 °C and V_{RD} with 25 °C, i.e., $\Delta V_{RD} = V_{RD}$ (175 °C) – V_{RD} (25 °C).

raises a question of what causes the temperature coefficient of DUT.T and DUT.P to be different when the MOS channel is partially formed.

When the MOS channel is partially formed, the temperature coefficient of V_{SD} in the 3rd-quad is mainly affected by the MOS, pn junction, and R_D according to (1). These components are divided into two parts. The first includes the pn junction and MOS in parallel, and the temperature coefficient is determined by the dominant one of the two components. The second part is R_D.

Compared with the R_D with a positive temperature coefficient when the channel is fully formed, the temperature coefficient of R_D is more complicated when the MOS channel is partially formed. Because the carrier of the I_{SD} is bipolar, and the lifetime of carrier is affected by T_j. At low current, the lifetime of carrier increases as T_j goes higher, which leads to the R_D decreasing with temperature. Thus, the temperature coefficient of R_D is negative. While at high current, as T_j goes higher, in addition to an increase in carrier lifetime, the mobility of the drift region decreases, which leads to an increase of R_D. The temperature coefficient may change from negative to positive.

When I_{SD} is small, the voltage drop across R_D is negligible compared to that across the MOS. Thus, the 3rd-quad temperature coefficient of the SiC MOSFET is dominated by the MOS and pn junction. Coupled with the MOS and pn junction of a negative temperature coefficient [26]. Consequently, the temperature coefficient of DUT.P and DUT.T are negative, as shown in Fig. 3. With the increase of I_{SD}, the 3rd-quad temperature coefficient is dominated by the drift region. When $I_{SD} = I_{Dnom}$, the temperature coefficient of DUT.T is positive, as shown in Fig. 19(b), which is different from the negative temperature coefficient of DUT.P in Fig. 19(a). The difference is because of the different minority carrier lifetimes in DUT.P and DUT.T, which may be attributed to the type and number of recombination centers of the devices. It is known that the minority carrier lifetime decreases with the increase in the number of recombination centers. There is always some variation in the number of recombination centers for different devices because of the different manufacturing processes of different manufacturers, which leads to different minority carrier lifetimes of devices. A small lifetime of minority carriers causes the mobility of the drift region to decrease significantly with temperature.

Simulation results of DUT.T are shown in Fig. 20, and the I-V curves of the 3rd-quad are illustrated with different minority

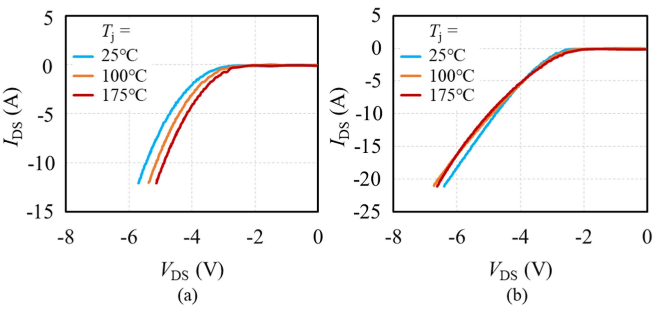


Fig. 21. Third-quad I-V characteristics of (a) DUT.P and (b) DUT.T with the MOS channel fully closed ($V_{GS} = -10$ V).

carrier lifetimes (τ_h). When τ_h in the drift region is 100 ns, the temperature coefficient is always negative. When τ_h is 1 ns, the temperature coefficient changes from negative to positive with the increase of I_{SD}.

Therefore, when τ_h of DUT.T is very small, coupled with a high current density, the carrier mobility decreases significantly with temperature. The temperature coefficient of DUT.T is dominated by the mobility of the drift region, and it is positive. However, when τ_h in the DUT.P drift region is long, the temperature coefficient of DUT.P, which is negative is dominated by the lifetime of carrier.

C. Channel Completely Closed

The channel is completely closed when V_{GS} is less than -10 V, and all I_{SD} flows through the body diode. Thus, the temperature coefficient of V_{SD} in the 3rd-quad is affected by the pn junction and R_D. The voltage drop of pn junction decreases with T_j due to the positive temperature coefficient of intrinsic carrier concentration.

When the channel is fully formed, the carriers of I_{SD} are unipolar, and the temperature coefficient of R_D is positive due to mobility decreases with T_j. As V_{GS} becomes more negative, the channel is gradually closed. The body diode takes part of the total current from the channel and the bipolar carriers of the I_{SD} increase. When the channel is completely closed, the lifetime of bipolar carriers increases with increasing T_j, resulting in a decrease in R_D. Coupled with the pn junction with

a negative temperature coefficient, the V_{SD} of DUT.P decreases with increasing T_j, as shown in Fig. 21(a). However, as shown in Fig. 21(b), the temperature coefficient of DUT.T for a given I_{SD} remains positive as V_{GS} is reduced to -10 V. This is because the τ_h of DUT.T is very small, resulting in the temperature coefficient being dominated by the mobility.

V. Conclusion

The 3rd-quad static conduction characteristics of the SiC MOSFET are studied by experiments and simulations in this article, and a physical model is developed to explain the characteristics. The MOS channel is not fully closed in the 3rd-quad for the following two reasons. The first reason is the increase of the gate potential for a given V_{GS}. The second reason is the decrease of the threshold voltage in the 3rd-quad (V_{TH3}) due to the body effect. The MOS channel is formed when the gate potential goes over V_{TH3}. Besides, the gate bias induced trapping charges to slow down the closing process of the MOS channel as V_{GS} goes down from zero. The channel is closed when the source-to-drain current (I_{SD}) is less than the critical I_{SD}, and the channel of DUT.P and DUT.T could not be formed when V_{GS} is smaller than -10 V. A negative V_{GS} is conducive to parallel applications, but the additional losses should be taken into consideration. The effect of the MOS channel on the temperature coefficient of V_{SD} varies with V_{GS}. The larger is the channel current, i.e., the larger is V_{GS}, the larger is the temperature coefficient of V_{SD}. This article provides a reference for understanding the 3rd-quad behavior of the SiC MOSFETs and a guideline for circuit applications as well as chip design.

References

[1] Z. Liang, P. Ning, and F. Wang, "Development of advanced all-SiC power modules," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2289–2295, May 2014.

[2] P. Yi, P. K. S. Murthy, and L. Wei, "Performance evaluation of SiC MOSFETs with long power cable and induction motor," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–7.

[3] H. Liu, H. Wu, Y. Lu, Y. Xing, and K. Sun, "A high efficiency inverter based on SiC MOSFET without externally antiparalleled diodes," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 163–167.

[4] J. Jordán et al., "A comparative performance study of a 1200V Si and SiC MOSFET intrinsic diode on an induction heating inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2550–2562, May 2014.

[5] S. Yin, K. J. Tseng, C. F. Tong, R. Simanjorang, C. J. Gajanayake, and A. K. Gupta, "A 99% efficiency SiC three-phase inverter using synchronous rectification," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 2942–2949.

[6] T. Kimoto, "Material science and device physics in SiC technology for high-voltage power devices," (in Japanese) *J. Appl. Phys.*, vol. 54, no. 4, Mar. 2015, Art. no. 040103.

[7] T. Kimoto and J. A. Cooper, *Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices, and Applications.* Singapore: Wiley, Nov. 2014.

[8] Q. J. Zhang et al., "Latest results on 1200 V 4H-SiC CIMOSFETs with Rsp, on of 3.9 mΩ·cm2 at 150 °C," in *Proc. IEEE 27th Int. Symp. Power Semicond. Devices IC's*, 2015, pp. 89–92.

[9] M. Zhang, J. Wei, X. Zhou, H. Jiang, B. Li, and K. J. Chen, "Simulation study of a power MOSFET with built-in channel diode for enhanced reverse recovery performance," *IEEE Electron. Device Lett.*, vol. 40, no. 1, pp. 79–82, Jan. 2019.

[10] X. Deng, X. Xu, X. Li, X. Li, Y. Wen, and W. Chen, "A novel SiC MOSFET embedding low barrier diode with enhanced third quadrant and switching performance," *IEEE Electron. Device Lett.*, vol. 41, no. 10, pp. 1472–1475, Oct. 2020.

[11] L. Tang et al., "The influence of dynamic threshold voltage drift on third quadrant characteristics of SiC MOSFET," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia*, 2021, pp. 483–487.

[12] C. Li, Z. Lu, H. Wu, W. Li, X. He, and S. Li, "Junction temperature measurement based on electroluminescence effect in body diode of SiC power MOSFET," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 338–343.

[13] S. Yin, Y. Liu, Y. Liu, K. J. Tseng, J. Pou, and R. Simanjorang, "Comparison of SiC voltage source inverters using synchronous rectification and freewheeling diode," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1051–1061, Feb. 2018.

[14] B. Li, M. Chen, X. Wang, N. Chen, X. Sun, and D. Zhang, "An optimized digital synchronous rectification scheme based on time-domain model of resonant CLLC circuit," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10933–10948, Sep. 2021.

[15] G. Doln, S. Sapp, A. Elbaiaway, and C. F. Wheatley, "The influence of body effect and threshold voltage reduction on trench MOSFET body diode characteristics," in *Proc. 16th Int. Symp. Power Semicond. Devices ICs*, 2004, pp. 217–220.

[16] K. Han and B. J. Baliga, "Comprehensive physics of third quadrant characteristics for accumulation- and inversion-channel 1.2-kV 4H-SiC MOSFETs," *IEEE Trans. Electron. Devices*, vol. 66, no. 9, pp. 3916–3921, Sep. 2019.

[17] X. Jiang et al., "Investigation on degradation of SiC MOSFET under surge current stress of body diode," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 77–89, Mar. 2020.

[18] V. Pala et al., "Physics of bipolar, unipolar and intermediate conduction modes in silicon carbide MOSFET body diodes," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs*, 2016, pp. 227–230.

[19] S. M. Sze, *Physics of Semiconductor Devices*. Hoboken, NJ USA: Wiley, 1981.

[20] R. Callanan, J. Rice, and J. Palmour, "Third quadrant behavior of SiC MOSFETs," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 1250–1253.

[21] K. Peng, S. Eskandari, and E. Santi, "Characterization and modeling of SiC MOSFET body diode," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 2127–2135.

[22] R. Zhang, X. Lin, J. Liu, S. Mocevic, D. Dong, and Y. Zhang, "Third quadrant conduction loss of 1.2–10 kV SiC MOSFETs: Impact of gate bias control," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2033–2043, Feb. 2021.

[23] A. U. Rashid, M. M. Hossain, A. I. Emon, and H. A. Mantooth, "Datasheet-driven compact model of silicon carbide power MOSFET including third-quadrant behavior," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11748–11762, Oct. 2021, doi: 10.1109/TPEL.2021.3062737.

[24] Z. Zeng, X. Zhang, and X. Li, "Layout-dominated dynamic current imbalance in multichip power module: Mechanism modeling and comparative evaluation," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11199–11214, Nov. 2019.

[25] J. A. O. González and O. Alatise, "A novel non-intrusive technique for BTI characterization in SiC mosfets," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5737–5747, Jun. 2019.

[26] J. Qi et al., "Comparative temperature dependent evaluation and analysis of 1.2-kV SiC power diodes for extreme temperature applications," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13384–13399, Dec. 2020.

[27] S. Khandelwal et al., "Analysis and modeling of vertical non-uniform doping in bulk MOSFETs for circuit simulation," in *Proc. 8th Int. Caribbean Conf. Devices, Circuits Syst.*, 2012, pp. 1–5.

[28] B. J. Baliga, *Silicon Carbide Power Devices*. Singapore: World Scientific, Jan. 2006.

[29] H. Li et al., "Influences of device and circuit mismatches on paralleling silicon carbide MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 621–634, Jan. 2016.

[30] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETs," *IEEE Trans. Electron. Devices*, vol. 62, no. 2, pp. 316–323, Feb. 2015, doi: 10.1109/TED.2014.2356172.

[31] J. Lutz et al., *Semiconductor Power Devices: Physics, Characteristics, Reliability*. Berlin, Germany, Springer, 2011.

[32] Z. Zhu, H. Xu, L. Liu, N. Ren, and K. Sheng, "Investigation on surge current capability of 4H-SiC trench-gate MOSFETs in third quadrant under various V_{GS} Biases," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 6361–6369, Oct. 2021.

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