Improved SiC MOSFET Model Considering Channel Dynamics of Transfer Characteristics

Ning Wang, Jianzhong Zhang, *Senior Member, IEEE*, and Fujin Deng, *Senior Member, IEEE*

***Abstract*—An improved SiC MOSFET model is proposed in this article, which predicts the dynamics accurately in the wide operation range of the SiC MOSFET. The temperature-sensitive effect (TSE), the short channel effect (SCE), and the interface state effect are comprehensively taken into consideration in the modeling of the transfer characteristics. A dynamic test platform of transfer characteristics is designed to extract data better than the datasheet. The turn-ON and turn-OFF processes of the SiC MOSFET are decoupled, and the nonlinear interterminal capacitances are also modeled thoroughly. To verify the convergence and accuracy of the proposed model, a 400 V/30 A double pulse test is fulfilled, and the complex converters are also simulated with the proposed model. The results show that the proposed model has good convergence and accuracy in predicting the switching trajectory of the SiC MOSFET, which would be favorable for observing the dynamics in the high-speed switching processes of the SiC MOSFET.**

***Index Terms*—Device model, dynamic characteristic, SiC MOSFET , transfer characteristic.**

I. Introduction

DUE to the lower on-resistance and the faster switching speed, the silicon carbide (SiC) MOSFET is a promising replacement for the silicon IGBT in high-voltage and high-power applications, such as photovoltaic systems, electric vehicles, and solid-state transformers [1]. With the development of device technologies, the modeling of the SiC MOSFET has become a significant topic in recent years [2], [3]. On the one hand, the reliability issues during the high-speed switching processes of the SiC MOSFET need to be predicted in advance, such as crosstalk phenomena [4], electrical stresses [5], and electromagnetic interferences (EMI) [6]. On the other hand, to fully exploit the potential of the SiC MOSFET and further improve the performance of the system, the ON-state loss, the switching loss [7], and the dead time [8] should also be calculated ahead of time. Therefore, a dynamic model of the SiC MOSFET with high accuracy is of vital importance.

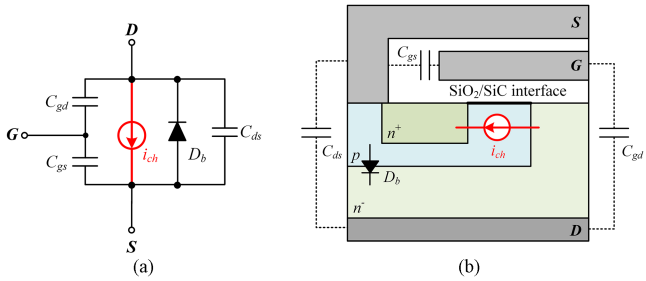

Fig. 1. SiC MOSFET model. (a) Simplified small-signal model. (b) Typical VDMOSFET structure.

The simplified small-signal model of the SiC MOSFET is shown in Fig. 1(a), where $i_{\rm ch}$ is the channel current, C_{gs}, $C_{gd,}$ and C_{ds} are three interterminal capacitances between terminals, and D_b is the body diode, and all of these parameters could be positioned in the typical vertical double-diffused (VD) MOSFET structure shown in Fig. 1(b). The modeling of the interterminal capacitances and the channel current are the most complex parts when modeling the SiC MOSFET because both of them have nonlinear features. The nonlinear features of the interterminal capacitances are well-known about the thickness of the depletion layer inside the SiC MOSFET varies with the terminal voltage. In recent studies, the model of the interterminal capacitance is no longer limited to the C–v_{ds} curves provided in the datasheets, and the influence of the gate–source voltage v_{gs} is taken into consideration. A hyperbolic-tangent-based function is adopted in [9] to describe the impact of v_{gs} on C_{gs}, where the value of C_{gs} is not treated as constant anymore. In [10], the exponential function with correction factor is applied to model C_{ds}, where v_{ds} and v_{gs} are taken as variables for the exponential function and the correction factor, respectively. It could be found that the interterminal capacitances are mainly voltage-dependent, and the impacts of other physical quantities are trivial [11], so the modeling of the interterminal capacitances is becoming more perfect.

When the SiC MOSFET operates in the saturation region, the channel current $i_{\rm ch}$ is controlled by the gate–source voltage v_{gs}, and the transfer characteristic shows the relationship of v_{gs} and $i_{\rm ch}$. Different from the modeling of the interterminal capacitances of the SiC MOSFET, the studies on the transfer characteristic model are inadequate. Most of the literature tried to apply different functions to make the model better fit the

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The authors are with the School of Electrical Engineering, Southeast University, Nanjing 210096, China (e-mail: ningwangedu@163.com; jiz@seu.edu.cn; fdeng@seu.edu.cn).

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transfer characteristic curve provided in the datasheet, including the quadratic polynomial function [12], [13], the exponential function [14], and the hyperbolic tangent function [15]. In [12], [13], [14], [15], and [16], the junction temperature T_j is taken as an independent variable in the fitting function. However, only two or three temperature points are available in the datasheet, which is far from enough. In general, the datasheet-driven model of the SiC MOSFET has limited accuracy.

In this article, an improved model of the SiC MOSFET considering the channel dynamics of the transfer characteristic is proposed. The innovations of this article are as follows:

1) The proposed model takes three channel dynamics into consideration, including the TSE, the SCE, and the interface state effect (ISE).
2) The dynamic test platform (DTP) of transfer characteristics is designed to extract data, where the turn-ON and the turn-OFF transfer characteristics can be modeled separately.
3) The general embedding method is presented to ensure that measurement-based data could be effectively applied in the Spice software.
4) The nonlinear interterminal capacitances are also comprehensively modeled by expanding the data of the C–v curves provided in the datasheet.

This article is organized as follows. In Section II, the features of the transfer characteristics of the SiC MOSFET are discussed and analyzed in detail. In Section III, the transfer characteristic is modeled based on the DTP. In Section IV, the simulation and experiment validations are carried out. Finally, Section V concludes this article.

II. Transfer Characteristics

A. Curve of Transfer Characteristic

In a typical VD MOSFET structure, the channel is formed at the top of the p-base, which is between the $n+$ doped region and the $n-$ drift layer. If the drain–source voltage v_{ds} is very small compared to the gate–source voltage v_{gs}, the SiC MOSFET operates in the linear region and the channel can be equivalent to a voltage-controlled resistor. If the drain–source voltage v_{ds} are relatively higher than the gate–source voltage v_{gs}, the SiC MOSFET operates in the saturation region and the channel can be treated as a voltage-controlled current source. Since the dynamic characteristics of the SiC MOSFET are defined in the transition between the cutoff region and the linear region [5], the channel is modeled as a current source in this article.

The turn-ON and the turn-OFF processes of the channel are not abrupt because the carriers could not appear or disappear instant. The transfer characteristic curve of the SiC MOSFET can well present the transformation process of the channel, as shown in Fig. 2. During the switching processes, the SiC MOSFET goes through four states with the change of v_{gs}, namely the accumulation state, the depletion state, the weak inversion state, and the strong inversion state. In the accumulation state, v_{gs} is negative, so the SiC MOSFET could be turned off reliably. The negative charge in the metal will attract the holes in the p-base towards the

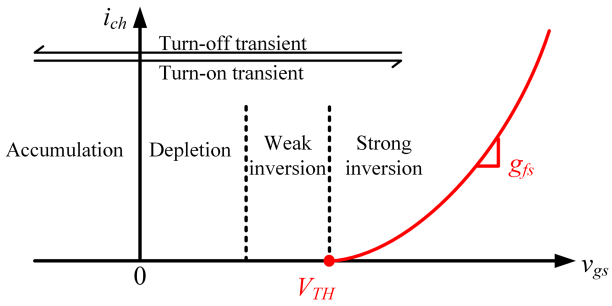


Fig. 2. Transfer characteristic curve of SiC MOSFET.

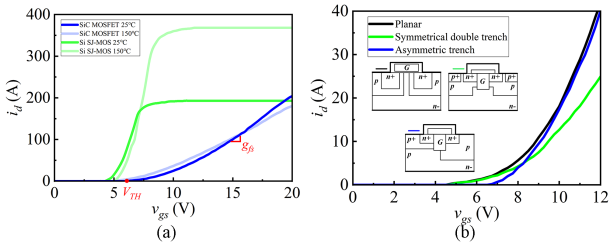


Fig. 3. Comparisons of transfer characteristic curves in different MOSFETs. (a) SiC MOSFET (IMZA65R039M1H) and SJ-MOS (IPW65R041CFD7). (b) SiC planar MOSFET (C2M0080120D), SiC symmetrical double trench MOSFET (SCT2080KE), and SiC asymmetric trench MOSFET (AIMW120R060M1H).

SiO_2/SiC interface, which leads to the accumulation of majority carriers on the semiconductor surface. As v_{gs} increase towards 0 V, the concentration of the accumulated holes will decrease. Once v_{gs} is positive, the holes will be repelled away from the SiO_2/SiC interface, and the p-base will enter the depletion state. With the increase of v_{gs}, the concentration of electrons will increase, so the p-base could conduct a weak current (μA level) in the weak inversion state. Once the concentration of electrons is higher than that of holes, the channel is formed, which has sufficient conductivity (mA to A level). In the strong inversion state, the channel can be treated as a current source mainly controlled by v_{gs}. As shown in Fig. 2, the threshold voltage V_{TH} is the gate–source voltage where the channel could conduct a certain value of current. The transconductance g_{fs} is the local tangent slope on the transfer characteristic curve, and g_{fs} characterize the conductivity of the channel in the strong inversion state.

The transfer characteristics depend on the semiconductor materials and the fabrication technologies of the power devices, so they vary widely among different power devices. It can be seen in Fig. 3(a) that the shape of the transfer characteristic curves is quite different between the SiC MOSFET and the Si super junction MOSFETs (SJ-MOS), whereas their continuous current capacity is similar. As shown in Fig. 3(b), the different gate technologies have great impacts on the transfer characteristic curves too. Therefore, the large difference in the transfer characteristic of the MOSFETs calls for the acquisition of a detailed and targeted model.

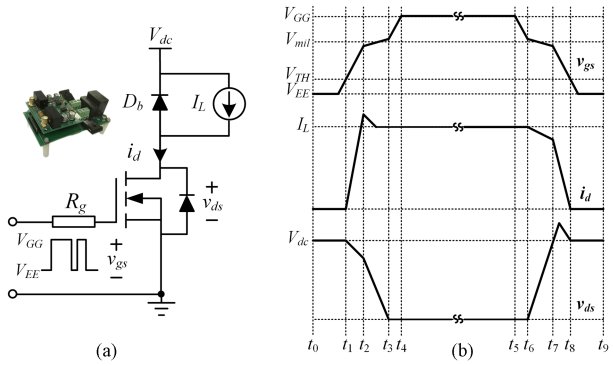


Fig. 4. Switching trajectory of SiC MOSFET. (a) DPT circuit and prototype. (b) Switching trajectory.

B. Switching Trajectory

The transfer characteristics directly determine the dynamic features by influencing the switching trajectory of the SiC MOSFET. Fig. 4 shows the switching trajectory waveforms of the drain current i_d, the gate–source voltage v_{gs}, and the drain–source voltage v_{ds} in the switching processes, where $V_{\rm dc}$ is the blocking voltage of the SiC MOSFET, I_L is the load current, R_g is the total gate resistance, V_{GG} is the positive driving voltage, and V_{EE} is the negative driving voltage. The switching trajectory could be obtained from the double pulse test (DPT) platform. It should be noted that the body diode of the SiC MOSFET is served as the freewheeling diode D_b in the DPT.

The turn-ON trajectory can be divided into four periods, namely the delay period (t_0,t_1), *di*/*dt* period (t_1,t_2), *dv*/*dt* period (t_2,t_3), and ON-state (t_3,t_4). The turn-OFF trajectory also has four periods, namely the delay period (t_5,t_6), *dv*/*dt* period (t_6,t_7), *di*/*dt* period (t_7,t_8) and OFF-state (t_8,t_9). The slew rate of the drain current *di*/*dt* and the slew rate of the drain–source voltage *dv*/*dt* are the most important parameters to characterize the switching processes of the SiC MOSFET, and they can be calculated from

$$\left(\frac{di}{dt}\right)_{\rm ON} = \frac{g_{fs}(V_{GG}-V_{\rm TH})}{R_gC_{gs}+g_{fs}L_s} \tag{1}$$

$$\left(\frac{di}{dt}\right)_{\rm OFF} = \frac{g_{fs}(V_{EE}+V_{\rm TH})+I_L}{R_gC_{gs}+g_{fs}L_s} \tag{2}$$

$$\left(\frac{dv}{dt}\right)_{\rm ON} = \frac{g_{fs}(V_{GG}-V_{\rm TH})-I_L}{R_gC_{gd}g_{fs}} \tag{3}$$

$$\left(\frac{dv}{dt}\right)_{\rm OFF} = \frac{g_{fs}(V_{\rm TH}-V_{EE})+I_L}{R_gC_{gd}g_{fs}}. \tag{4}$$

It is obvious that $V_{\rm TH}$ and g_{fs} have significant influences on the calculation of *di*/*dt* and *dv*/*dt*. It is well-known that *di*/*dt* is the main factor of the turn-ON current overshoot, the turn-OFF voltage overshoot, and the differential mode EMI. At the same time, *dv*/*dt* is the source of crosstalk phenomena and the common mode EMI. In addition, the value of *di*/*dt* and *dv*/*dt* directly impacts the evaluation of the switching losses. Therefore, the transfer characteristics of the SiC MOSFET should be accurately modeled during the prediction of the dynamic characteristics of the SiC MOSFET.

C. Channel Dynamics

The transfer characteristic curves are provided in the datasheet, but they are insufficient as the operating range of the SiC MOSFET is much wide than that of the datasheet. When the SiC MOSFET operates in the practical application, the channel dynamics should be considered in the model, such as the TSE, the SCE, and the ISE.

The TSE of the channel can be attributed to the positive temperature sensitivity of the carrier concentration. At the same time, since the Coulomb scattering is stronger than the phonon scattering within the normal operating temperature range of the SiC MOSFET, the field effect mobility also has a positive temperature coefficient [18], [19], [20]. As a result, more inversion electrons will appear in the channel when the temperature is higher, so $V_{\rm TH}$ will decrease and g_{fs} will increase. The manufacturers usually provide the transfer characteristic curves at two or three temperature points, which are far from enough. Therefore, to increase the accuracy of the interpolation algorithm, it is necessary to extract the data of the transfer characteristics from more temperature points.

The SCE is due to the drain-induced barrier lowering effect (DIBL), which is more obvious in the SiC MOSFET than in the Si MOSFET [21], [22], [23]. Compared with the Si material, the channel mobility based on the SiC material is relatively lower, so the channel resistance tends to be higher. Shortening the channel length is one of the most effective ways to overcome this defect. However, when the channel length is reduced to a level comparable to the width of the drain depletion layer, the SCE will cause the following three negative effects.

1) The shift in the transfer characteristic curve.
2) Degradation of the sub-threshold properties.
3) Unsaturation of the drain current [22].

In terms of the transfer characteristic discussed in this article, the transfer characteristic curve will shift to the right when the SiC MOSFET is turned on. It can be explained as the decrease of v_{ds} making the drain depletion thinner, and the holes are not sufficiently repelled, so more electrons are required to form the channel. As a result, $V_{\rm TH}$ will increase and g_{fs} will decrease in the turn-ON *dv*/*dt* period (t_2,t_3). On the contrary, $V_{\rm TH}$ will decrease and g_{fs} will increase in the turn-OFF *dv*/*dt* period (t_6,t_7). As shown in Fig. 5, one of the most observable impacts of the SCE on the switching trajectory is that the "Miller ramp" replaces the "Miller plateau" [5], [9]. To predict the dynamic characteristics of the SiC MOSFET more accurately, the SCE should be taken into consideration in the model. The Miller voltage $V_{\rm mil}$ has the following relationship:

$$V_{\rm mil}+\Delta V_{\rm mil} = (V_{\rm TH}+\Delta V_{\rm TH}) + \frac{I_L}{g_{fs}+\Delta g_{fs}} \tag{5}$$

where $\Delta V_{\rm mil}$, $\Delta V_{\rm TH}$, and Δg_{fs} are variance of $V_{\rm mil}$, $V_{\rm TH}$, and g_{fs} caused by the SCE, respectively.

The ISE has a more significant impact on the transfer characteristics of the SiC MOSFET than the Si MOSFET because the

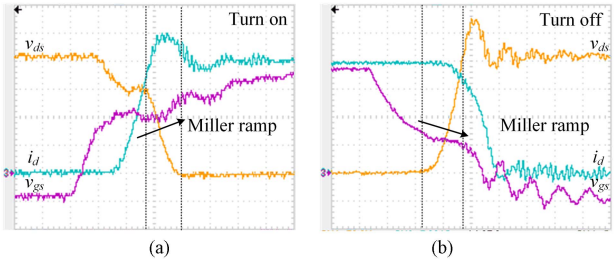


Fig. 5. Switching trajectory of SiC MOSFET (C2M0080120D, $V_{\rm dc} = 400$ V, $I_L = 20$ A, $R_g = 10\ \Omega$, $T_j = 25$ °C). (a) Turn-ON. (b) Turn-OFF. v_{gs} (5 V/div), v_{ds} (100 V/div), i_d (5 A/div), and time (25 ns/div).

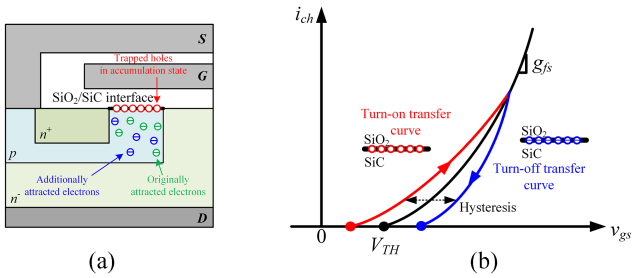


Fig. 6. ISE of SiC MOSFET. (a) ISE in turn-ON process. (b) Hysteresis of transfer characteristic.

SiO_2/SiC interface is more complex than the SiO_2/Si interface. On the one hand, the existence of carbon in the SiC material brings point defects. On the other hand, the high bandgap of the SiC material gives these point defects at a range of high energy levels. The density of the SiO_2/SiC interface state could reach 10^{11}–10^{12} cm^{-2}/eV, which is two or three orders of magnitude larger than that of the SiO_2/Si interface state [24], [25]. When the channel switches between the accumulation state and the strong inversion state, the charges trapped in the interface will change the number of electrons by the Coulomb force. In consequence, the shift will occur in the transfer characteristic curve of the SiC MOSFET.

As shown in Fig. 6(a), a large number of holes will be trapped on the SiO_2/SiC interface when the channel is in the accumulation state, and the number of the trapped holes will increase with a lower negative v_{gs}. Once the channel enters the inversion states, these trapped holes will attract more additional electrons to form the channel, so $V_{\rm TH}$ will decrease and g_{fs} will increase. Likewise, since the SiO_2/SiC interface traps a lot of electrons before the channel is turned OFF, $V_{\rm TH}$ will increase, and g_{fs} will decrease in the turn-OFF process of the SiC MOSFET. It can be seen in Fig. 6(b) that the ISE makes the difference between the turn-ON and the turn-OFF transfer characteristics, and this phenomenon can be called the "hysteresis of transfer characteristic."

The hysteresis of the transfer characteristic is recoverable, and it exists in each switching process. In the conventional model, which neglects the ISE, the negative initial voltage V_{EE} will not influence the value of the turn-ON *di*/*dt* and *dv*/*dt*, and the positive initial voltage V_{GG} has a trivial impact on the turn-OFF *di*/*dt* and *dv*/*dt*. However, as shown in Fig. 7, the experimental slew rate

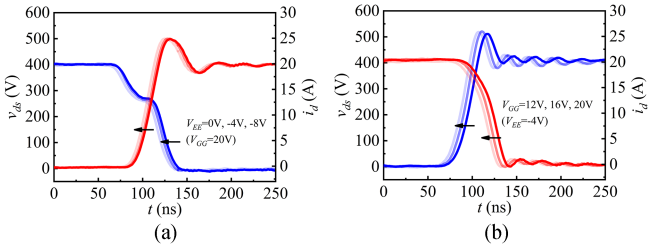


Fig. 7. Switching trajectory of SiC MOSFET with different initial driving voltages (C2M0080120D, $V_{\rm dc} = 400$ V, $I_L = 20$ A, $R_g = 10\ \Omega$, $T_j = 25$ °C). (a) Turn-ON process with $V_{GG} = 20$ V, $V_{EE} = 0$ V, -4 V, and -8 V. (b) Turn-OFF process with $V_{EE} = -4$ V, $V_{GG} = 12$ V, 16 V, and 20 V. (Arrows indicate the changing direction of the initial gate voltage.)

of i_d and v_{ds} will increase when the absolute value of the initial gate–source voltages increases. Therefore, the ISE should be considered in the transfer characteristic model. In detail, the turn-ON and the turn-OFF transfer characteristics should be modeled separately, and the value of V_{GG} and V_{EE} should be determined meantime.

TSE, SCE, and ISE are three critical physical effects for the design, application, and evaluation of the SiC MOSFET. The dynamic transfer characteristics considering the TSE, SCE, and ISE can be approximately expressed as follows:

$$V_{\rm TH} = \underbrace{\frac{1}{C_{ox}}\sqrt{4\varepsilon_{\rm SiC}kT\ln\left(\frac{N_A}{n_i}\right)} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right)}_{\rm TSE} \underbrace{-\frac{4\varepsilon_{\rm SiC}t_{ox}\Psi_B}{C_{ox}L}}_{\rm SCE} \underbrace{-\frac{Q_{ox}}{C_{ox}}}_{\rm ISE} \tag{6}$$

$$g_m = \frac{W\mu_{ni}C_{ox}}{L}\left(v_{gs} - V_{TH}\right)\left(1 + \lambda v_{ds}\right) \tag{7}$$

where $\varepsilon_{\rm SiC}$ is the dielectric constant of the SiC material, k is the Boltzmann's constant, T is the temperature, N_A is the doping density, n_i is the intrinsic carrier concentration, C_{ox} is the specific oxide capacitance, q is the fundamental charge, t_{ox} is the oxide thickness, ψ_B is the bulk potential, W is the channel width, L is the channel length, Q_{ox} is the total effective oxide charge, μ_{ni} is the electron channel mobility, and λ is the channel modulation factor.

It is difficult to directly apply the physics-based equations to model the transfer characteristics because the parameters inside the SiC MOSFET might be unavailable to the users. Therefore, a measurement-based method is proposed in this article to extract the detailed dynamic transfer characteristics for the SiC MOSFET.

III. Improved Model

A. Test Platform of Dynamic Transfer Characteristic

The DTP is shown in Fig. 8, which consists of two isolated push-pull gate drivers U_1 and U_2, PNP transistor Q_1, power supplies V_{GG1}, V_{EE1}, V_{GG2}, V_{EE2}, and V_{GG1}', driving resistors R_1, R_2, and R_3, high-speed switching diode D_1. It should be noted that the value of V_{GG1}, V_{GG1}', and $V_{\rm dc}$ is adjustable, and the junction temperature of the SiC MOSFET could be controlled

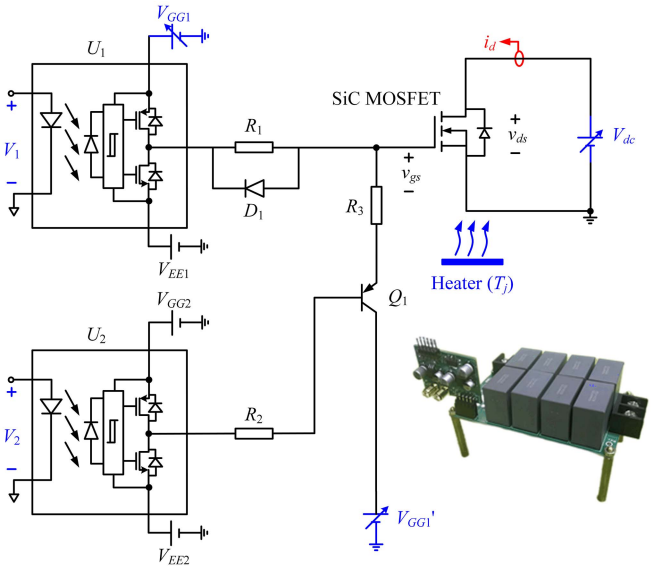


Fig. 8. DTP circuit and prototype.

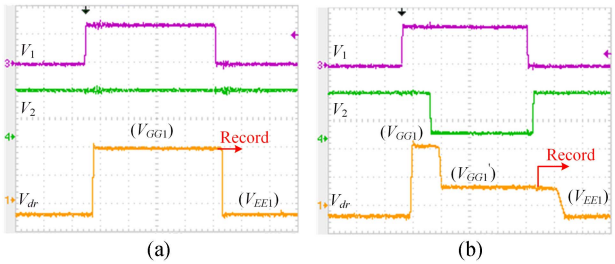


Fig. 9. Operation principle of DTP ($V_{GG1} = 20$ V, $V_{EE1} = -4$ V, $V_{GG1}{}' = 7$ V, without load). (a) Turn-ON process test. (b) Turn-OFF process test. V_1 and V_2 (2 V/div), V_{dr} (10 V/div), and time (250 ns/div).

by the heater. The effective driving voltage V_{dr} of the SiC MOSFET can be expressed as

$$V_{dr} = \begin{cases} V_{GG1} & V_1 = 1, V_2 = 1 \\ V_{EE1} & V_1 = 0, V_2 = 1 \\ V'_{GG1} & V_1 = 1, V_2 = 0 \end{cases} \tag{8}$$

where V_1 and V_2 are the driving signals. The extraction of the dynamic transfer characteristics is realized by obtaining the value of i_d at a fixed gate–source voltage v_{gs}. As shown in Fig. 9(a), when extracting the turn-ON transfer characteristic, the signal V_2 should be set at a high level, and V_1 is a pulse signal with 1 μs which could reduce the impact of the self-heating effect. It can be seen that V_{dr} will be switched between V_{EE1} and V_{GG1}, and the value of i_d at different V_{GG1} could be obtained, as shown in Fig. 10(a). Then the turn-ON transfer characteristic at a fixed $V_{\rm dc}$ could be obtained. Since there have some differences between the turn-ON and turn-OFF transfer characteristics, the data of the turn-OFF transfer characteristic should be extracted in another way. Fig. 9(b) shows the signals V_1 and V_2 for the turn-OFF process, where V_2 should turn to a low level after a certain delay. So, the effective driving voltage V_{dr} jumps to V_{GG1} first, keeps at V_{GG1}' second, and decreases to V_{EE1} finally. As a result, the SiC MOSFET is turned on sufficiently by V_{GG1}, then keeps in the

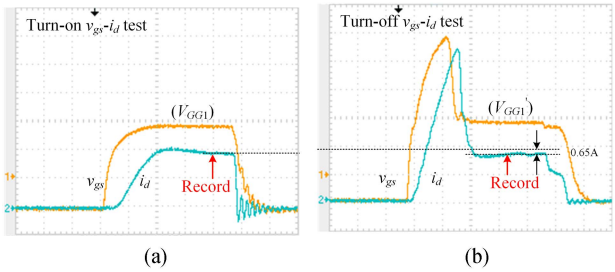


Fig. 10. Transfer characteristic measurement (C2M0080120D, $V_{\rm dc} = 20$ V, $T_j = 25$ °C, $v_{gs} = 7$ V). (a) Turn-ON process test. (b) Turn-OFF process test. v_{gs} (5 V/div), i_d (2 A/div), and time (250 ns/div).

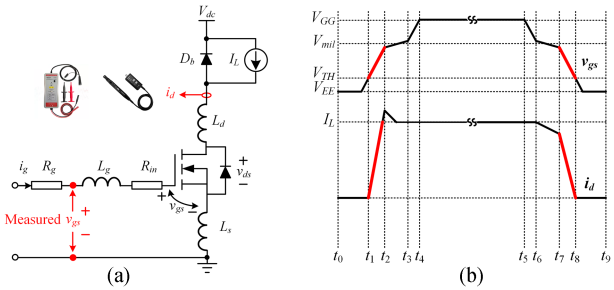


Fig. 11. Dynamic transfer characteristics proposed in [29] and [30]. (a) DPT circuit. (b) Relationship between v_{gs} and i_d.

strong inversion state at V_{GG1}', and the SiC MOSFET is turned OFF by V_{EE1} finally. The channel will conduct a certain current at V_{GG1}', and the conducted current at V_{GG1}' is recorded, as shown in Fig. 10(b). Therefore, the turn-OFF process of the SiC MOSFET could be reasonably emulated, and the turn-OFF transfer characteristic at a fixed $V_{\rm dc}$ could be obtained.

It is obvious in Fig. 10 that the current conducted by the channel in the turn-ON process and the turn-OFF process are different. When both V_{GG1} and V_{GG1}' are 7 V, and the blocking voltage $V_{\rm dc}$ is 20 V, the measured current in the turn-ON process is 0.65 A higher than that in the turn-OFF process, which is due to the ISE. Therefore, it is necessary to model the turn-ON and turn-OFF transfer characteristics separately.

It should be noted that each test process will increase the junction temperature of the SiC MOSFET, so sufficient interval time is necessary to keep the device in thermal equilibrium, especially in the turn-OFF test. Compared with the datasheet-driven parameters extraction method, the measurement-based method is more flexible and comprehensive. On the one hand, the DTP expands the measurement range of the curve tracer. On the other hand, the turn-ON and turn-OFF transfer characteristics could be measured separately in a convenient way.

The dynamic transfer characteristics of the SiC MOSFET could be tested by the DPT proposed in [29] and [30]. In [29] and [30], the relationship between v_{gs} and i_d in the *di*/*dt* period is researched. However, the solution based on the DPT has limited accuracy due to the following factors. First, the parasitic resistance and inductance in the DPT will lead to inevitable errors in the test of the transfer characteristics. Fig. 11 shows the parasitic gate resistance R_{in}, the parasitic gate inductance L_g, the parasitic source inductance L_s and the parasitic drain

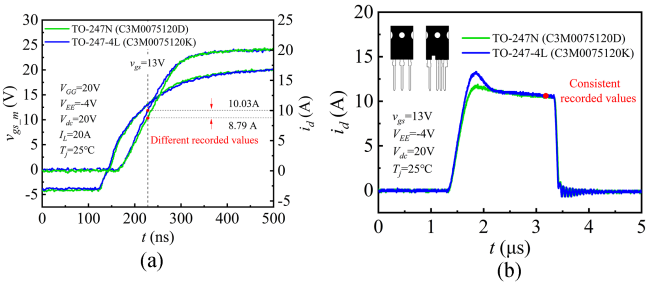


Fig. 12. Tested results of dynamic transfer characteristics in different packages based on (a) DPT. (b) DTP. (v_{gs_m} is measured v_{gs}.)

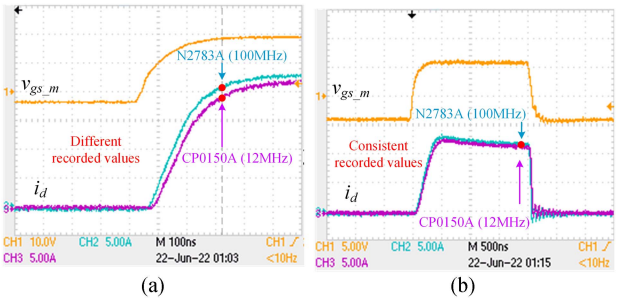


Fig. 13. Tested results of dynamic transfer characteristics by current probes with different bandwidth based on (a) DPT. (b) DTP.

inductance L_d. The voltage drop on the parasitic parameters could never be eliminated, and it will significantly influence the switching trajectory of the SiC MOSFET, especially in different packages with changing parasitic effects. Fig. 12(a) shows the tested results of dynamic transfer characteristics in different packages, where the measured i_d in the TO-247N package is 1.24 A lower than that in the TO-247-4L package under the same v_{gs} based on the DPT. This is unacceptable for testing the transfer characteristics. Second, the solution in [29] and [30] requires the strict and accurate correction for the time offset between the voltage probe and the current probe, where the dedicated calibration equipment is very expensive. Third, two probes with high bandwidth are required in the solution based on the DPT. Obviously, the measured i_d by low bandwidth probe CP0150A (12 MHz) has a more significant attenuation compared to that by high bandwidth probe N2783A(100 MHz), as shown in Fig. 13(a). The measurement errors would lead to the inaccuracy of the transfer characteristics.

The proposed extraction method of the transfer characteristics based on the DTP in this article could have higher accuracy than the existing solution as shown in [29] and [30]. Different from the existing solutions, the measurement of i_d based on the DTP is carried out at the stable state where i_g, di_g/dt, and di_d/dt are close to zero. Then the voltage drops on the parasitic parameters are trivial. Fig. 12(b) shows the tested results of the dynamic transfer characteristic at different packages, and good consistency could be achieved for the proposed solution based on the DTP. Furthermore, the proposed DTP only needs one current probe and then no time offset should be corrected. Fig. 13(b) shows only minor attenuation in the measured i_d when the bandwidth of the current probe is relatively low. Therefore,

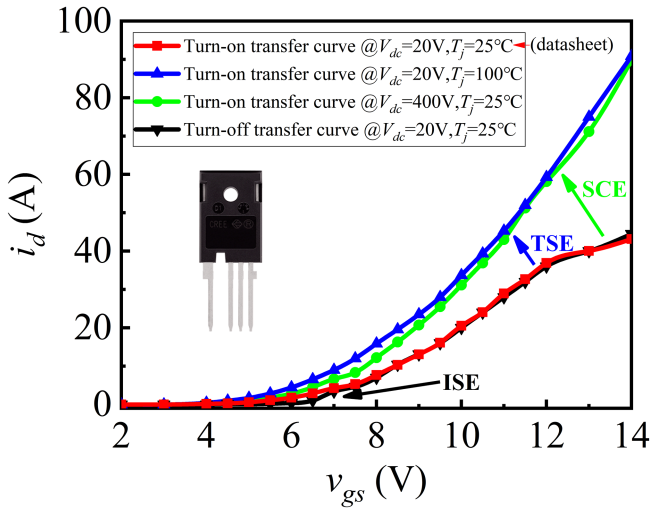


Fig. 14. Transfer characteristic curves at different operation points (C2M0080120D).

the good consistency and accuracy of the proposed extraction method of the transfer characteristics based on the DTP could be achieved.

B. Transfer Characteristic Model

To take the SCE into consideration, the dynamic transfer characteristic test should be repeated at different blocking voltages by adjusting $V_{\rm dc}$. Meanwhile, to consider the TSE, the test should be carried out at different junction temperatures by fully heating the SiC MOSFET to the specified temperature T_j, and then the junction temperature could be measured on the outside of the package. It is shown in Fig. 14 that the transfer characteristics in the practical applications are more complex than the curves provided in the datasheet. When the junction temperature increases from 25 °C to 100 °C, the transfer characteristic curve will shift to the left due to the TSE. Likewise, the SiC MOSFET will have a lower $V_{\rm TH}$ and higher g_{fs} due to the SCE if the blocking voltage increases from 20V to 400 V. It can also be seen that the turn-ON transfer characteristic curve shows a difference from the turn-OFF curve, which confirms the results about the ISE shown in Fig. 6. It should be noted that the negative initial voltage V_{EE} in the turn-ON process is -4 V, and the positive initial voltage V_{GG} in the turn-OFF process is 20 V in this article.

The complete test data of the transfer characteristics for the SiC MOSFET is shown in Fig. 15. Three junction temperatures $T_j = 25$ °C, $T_j = 100$ °C, and $T_j = 175$ °C, are selected in the proposed model, and the blocking voltage $V_{\rm dc}$ varies from 10 to 400 V. It is also convenient for the users to obtain data at other T_j or $V_{\rm dc}$ for modeling the dynamic transfer characteristic.

The Spice software lacks the plugins for the 3-D lookup table, so it is not friendly to the discrete data shown in Fig. 15. Therefore, a general embedding method is adopted to ensure good implementation of the measured data in the Spice software, as shown in Fig. 16. The curve fitting in MATLAB Toolbox is used to match the discrete data with the specific fitting function.

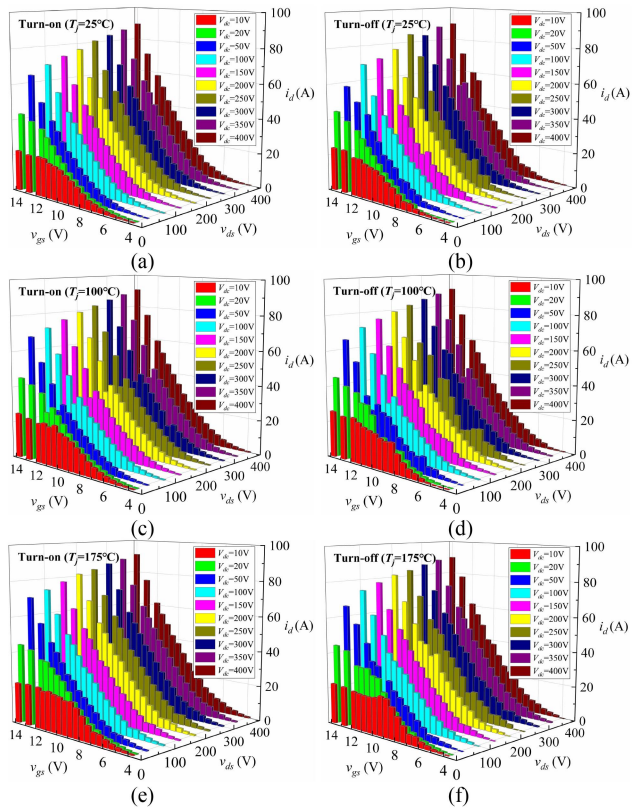


Fig. 15. Transfer characteristic of SiC MOSFET (C2M0080120D). (a) Turn-ON tested data at 25 °C. (b) Turn-OFF tested data at 25 °C. (c) Turn-ON tested data at 100 °C. (d) Turn-OFF tested data at 100 °C. (e) Turn-ON tested data at 175 °C. (f) Turn-OFF tested data at 175 °C.

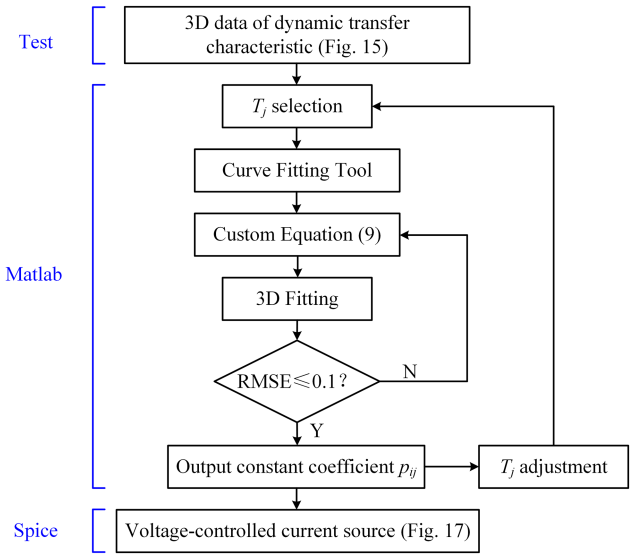


Fig. 16. General embedding method from test to Spice.

In this article, the fifth order bivariate polynomial is adopted, and it has

$$i_{ch}(v_{gs}, v_{ds})_{T_j=n^\circ\mathrm{C}} = \sum_{\substack{i=0 \\ j=0}}^{5} p_{ij} v_{gs}^i v_{ds}^j \tag{9}$$

TABLE I
COEFFICIENTS OF VOLTAGE-CONTROLLED CURRENT SOURCE

	T_j=25°C		T_j=100°C		T_j=175°C	
	on	off	on	off	on	off
p_{00}	12.660	12.490	15.760	15.350	17.740	17.870
p_{10}	20.020	18.540	17.900	17.730	22.760	22.790
p_{01}	3.285	3.275	3.190	2.080	3.444	2.974
p_{20}	8.955	8.545	5.443	6.032	7.262	6.649
p_{11}	−0.494	0.289	−1.062	−0.653	−1.514	−0.947
p_{02}	4.746	4.457	4.495	4.339	5.994	4.702
p_{30}	−1.083	0.154	0.824	1.130	−2.002	−1.735
p_{21}	−0.075	0.271	0.053	0.226	−0.208	0.725
p_{12}	2.756	3.591	3.014	2.905	3.051	2.415
p_{03}	−3.203	−2.441	−3.337	−1.531	−3.700	−2.500
p_{40}	−0.549	−0.387	0.4898	0.309	−0.248	−0.045
p_{31}	0.487	0.543	0.678	0.637	0.505	0.563
p_{22}	−1.693	−1.430	−1.707	−1.667	−2.104	−2.097
p_{13}	2.836	2.327	2.841	2.614	3.639	3.300
p_{04}	−2.711	−2.517	−2.490	−2.365	−3.422	−2.685
p_{50}	0.369	0.119	−0.008	−0.091	0.476	0.395
p_{41}	−0.002	0.019	−0.071	−0.087	−1.001	−0.394
p_{32}	−0.573	−0.889	−0.846	−0.795	−0.460	−0.450
p_{23}	1.327	1.081	1.352	1.240	1.585	1.587
p_{14}	−1.931	−1.846	−1.759	−1.652	−2.479	−2.060
p_{05}	1.635	1.291	1.670	1.113	1.980	1.367

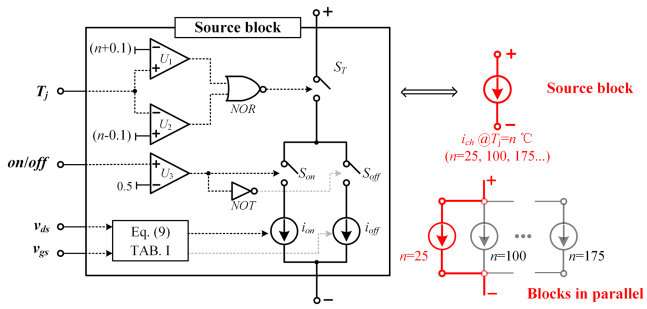


Fig. 17. Model of dynamic transfer characteristic in Spice software.

where p_{ij} are the coefficients and could be determined by the implementation of the 3-D fitting in the MATLAB, $i_{\mathrm{ch}}(v_{gs},v_{ds})$ is the channel current at various gate–source voltage and drain–source voltage, and the footnote $T_j = n°\mathrm{C}$ is the junction temperature. Table I shows the detailed coefficients in (9). Then, in the Spice software, the dynamic transfer characteristics of the SiC MOSFET could be modeled as the voltage-controlled current source. Fig. 17 shows the implementation of the dynamic transfer characteristic in the Spice software. There are several parallel-connected blocks corresponding to different junction temperature T_j and only one of the blocks at a specific T_j would be enabled during the simulation. The ON/OFF terminal in the Spice software is connected with the pulsewidth modulation (PWM) signal. Then, the voltage level of the PWM signal decides the turn-ON or turn-OFF process of the SiC MOSFET, where the high voltage corresponds to turn-ON process and the low voltage corresponds to turn-OFF process. The current source i_{ON} serves as the channel current of the SiC MOSFET in the turn-ON process, and i_{OFF} serves as the channel current of the SiC MOSFET in the turn-OFF process. The comparators U_1 and U_2 judge the T_j location according to n and trigger the switch S_T. So, only the source block at specific T_j would be enabled.

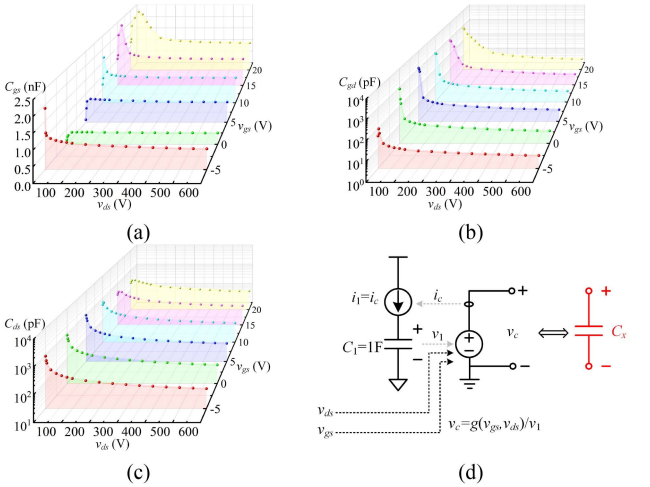


Fig. 18. Model of dynamic interterminal capacitance (C2M0080120D). (a) C_{gs}. (b) C_{gd}. (c) C_{ds}. (d) Implement of dynamic interterminal capacitance model in Spice software (C_x could be C_{gs}, C_{gd}, or C_{ds}).

C. Interterminal Capacitance Model

The interterminal capacitance model also plays an important role in predicting the dynamic characteristics of the SiC MOSFET. The C–v curves provided in the datasheet are widely applied to the conventional model of interterminal capacitances [26]. However, the C–v curves are only obtained at $v_{gs} = 0$ V, where the dynamic behaviors of the SiC MOSFET in the high-speed switching process are neglected. Since the parasitic capacitance of the p-base varies a lot when the channel changes from the accumulation state to the strong inversion state, the capacitance C_{gs} will change with v_{gs}. When v_{gs} is comparable to v_{ds}, the change in v_{gs} will have a great impact on the capacitance C_{gd}, which cannot be ignored anymore. The capacitance C_{ds} will decrease at higher v_{gs} because the equivalent area of the drain body junction and the carrier concentration at the bottom of the n-drift layer will reduce when v_{gs} increases. Therefore, to achieve high accuracy, the influences of v_{gs} on the three interterminal capacitances must be modeled.

The finite element analysis of the device is an effective way to extract the interterminal capacitances under the dynamic processes [27], [28]. As shown in Fig. 18(a)–(c), every single C–v curve in the datasheet is expanded to multiple curves at different v_{gs}, and it is obvious that the curves are different from each other, especially at low v_{ds}. The model of dynamic interterminal capacitance could be implemented by the voltage-controlled capacitance in the Spice software, which is shown in Fig. 18(d). Since the linear capacitance C_1 is adopted, good convergence could be achieved because no complex calculation parts are required. It should be noted that $g(v_{gs},v_{ds})$ is the fitting function according to the data in Fig. 18(a)–(c), and the detailed coefficients can also be obtained by the general embedding method in Fig. 16. The physical parameters of the SiC MOSFET (C2M0080120D) are same as [31], which might be easy to be collected for the different devices by cooperation with the manufacturers.

TABLE II
INFORMATION OF DPT

	Name	Information
Tested power device	SiC MOSFET	C2M0080120D (1200V/36A)
Driving parameters	R_g	10–60 Ω
	I_L	5–30 A
	V_{dc}	100–400 V
	T_j	25–175 °C
	V_{GG}/V_{EE}	20 V/–4 V
Parasitic parameters	L_{loop}	82.5 nH from ANSYS Q3D
	L_s	9.0 nH from ANSYS Q3D
Test equipment	Current probe	TCP305A
	Voltage probe	SI-9002
	Oscilloscope	TPS2024B

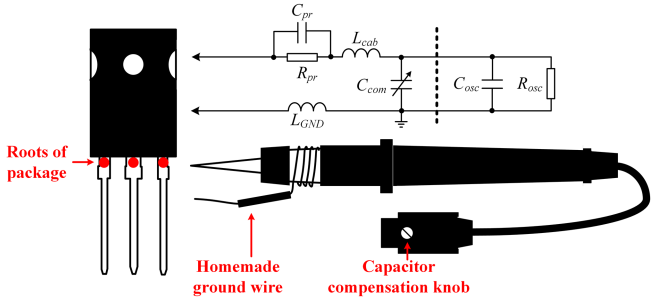


Fig. 19. Measurement of voltages between terminals of SiC MOSFET.

IV. Experiment Validation

A. Double Pulse Test (DPT) Platform

The DPT platform shown in Fig. 4(a) is implemented to validate the proposed model. The detailed information on the DPT is listed in Table II. It is significant to reduce the measurement errors of the voltage between the SiC MOSFET terminals. So, three critical steps are adopted in the implementation of the DPT, as shown in Fig. 19. First, the impedances of the probe and the oscilloscope should be matched ($R_{\rm pr}C_{\rm pr} = R_{\rm osc}C_{\rm osc}$) to ensure enough high-frequency response by tuning the capacitance compensation knob (see Fig. 19). Second, the homemade ground wire should be wrapped around the metal ground of the probe to minimize the parasitic inductance $L_{\rm GND}$, which is effective to reduce the additional oscillations. Third, the probes must be placed at the roots of the package as close as possible to reduce the errors caused by the parasitic inductance of the pins. Furthermore, the alignment should be carried out in the computer because the inherent offset and delay of the probes should be deducted in advance.

B. Accuracy Validation

In this article, Pspice16.6 is applied as the Spice software, and the computer configuration is Intel Core i5-7th Gen. To quantify the accuracy of the proposed model, all the errors between the experimental result $x_{\rm exp}$ and the simulated result $x_{\rm sim}$ will be expressed as the relative error; it has

$$\Delta\% = \left| \frac{x_{\rm exp} - x_{\rm sim}}{x_{\rm exp}} \right| \times 100\%. \tag{10}$$

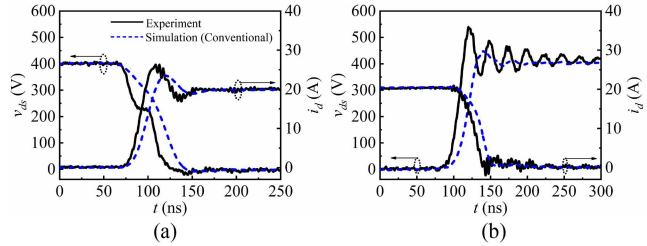


Fig. 20. Comparison of experimental and simulated switching trajectory when applying conventional model ($R_g = 10\ \Omega$, $I_L = 20$ A, $V_{\rm dc} = 400$ V, $T_j = 25$ °C). (a) Turn-ON process. (b) Turn-OFF process.

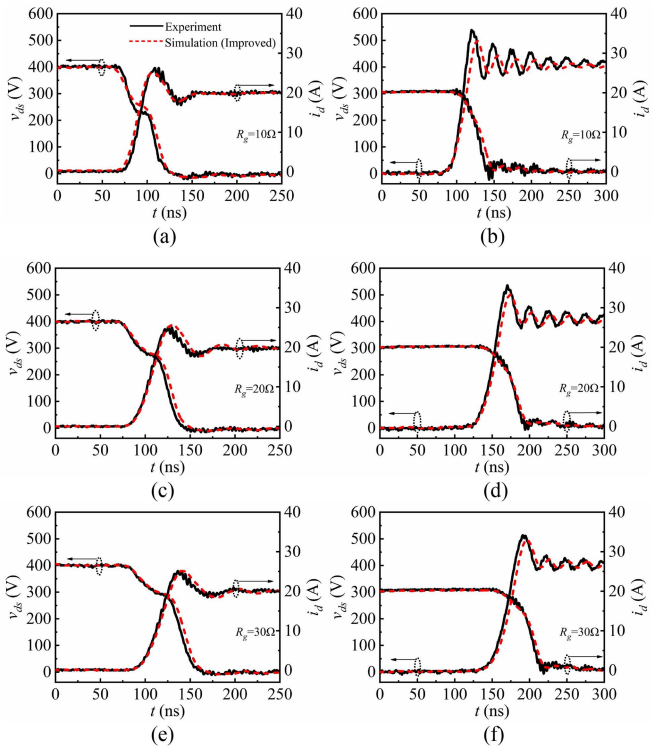


Fig. 21. Comparison of experimental and simulated switching trajectory with different R_g when applying the proposed model ($I_L = 20$ A, $V_{\rm dc} = 400$ V, $T_j = 25$ °C). (a) Turn-ON with $R_g = 10\ \Omega$. (b) Turn-OFF with $R_g = 10\ \Omega$. (c) Turn-ON with $R_g = 20\ \Omega$. (d) Turn-OFF with $R_g = 20\ \Omega$. (e) Turn-ON with $R_g = 30\ \Omega$. (f) Turn-OFF with $R_g = 30\ \Omega$.

The conventional model provided by the CREE neglects the channel dynamics, so there have obvious errors in predicting the switching trajectory of the SiC MOSFET. As shown in Fig. 20, taking the turn-ON *di*/*dt* as the comparison object, $\Delta\%$ reaches 23.9%, which is unacceptable.

The improved SiC MOSFET model with transfer characteristics considering the channel dynamics has higher accuracy than the conventional model. Meanwhile, the dynamic model of the interterminal capacitances could also improve the correctness of predicting the switching characteristics of the SiC MOSFET. As shown in Fig. 21, the simulated switching trajectory by the proposed model has great agreement with the experimental switching trajectory at different driving speeds. It is easy to find that the relative error of the turn-ON *di*/*dt* is only 3.6% in Fig. 21(a), which is far lower than that with the conventional

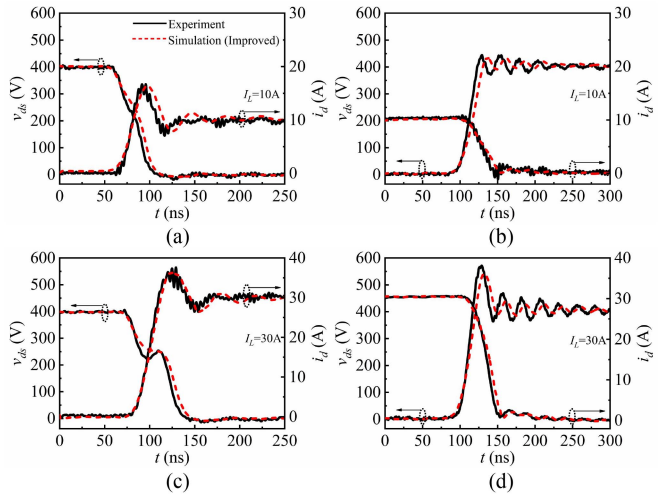


Fig. 22. Comparison of experimental and simulated switching trajectory with different I_L when applying the proposed model ($R_g = 10\ \Omega$, $V_{\rm dc} = 400$ V, $T_j = 25$ °C). (a) Turn-ON with $I_L = 10$ A. (b) Turn-OFF with $I_L = 10$ A. (c) Turn-ON with $I_L = 30$ A. (d) Turn-OFF with $I_L = 30$ A.

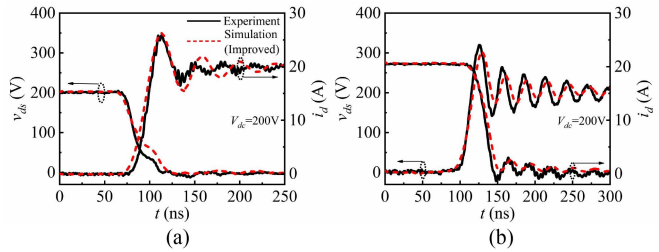


Fig. 23. Comparison of experimental and simulated switching trajectory with another blocking voltage when applying the proposed model ($R_g = 10\ \Omega$, $I_L = 20$ A, $V_{\rm dc} = 200$ V, $T_j = 25$ °C). (a) Turn-ON process. (b) Turn-OFF process.

model. As shown in Fig. 22, the proposed model also has relatively high accuracy with different load currents.

The blocking voltage $V_{\rm dc}$ will have a significant impact on the switching trajectory of the SiC MOSFET. On the one hand, the transfer characteristics of the SiC MOSFET vary at different v_{ds} due to the SCE. On the other hand, the interterminal capacitance will change when the voltages between terminals are different. As shown in Fig. 23, the proposed model could keep high accuracy at different $V_{\rm dc}$.

Since the proposed model takes TSE into consideration, the simulated results could agree with the experimental results well at a different temperature, as shown in Fig. 24. Fig. 24 shows the proposed model could have good accuracy with the junction temperature $T_j = 100$ °C, 125 °C, and 175 °C.

To intuitively demonstrate the advantages of the proposed model in terms of accuracy, this article takes the average of four relative errors of $(di/dt)_{\rm ON}$, $(dv/dt)_{\rm ON}$, $(di/dt)_{\rm OFF}$, and $(dv/dt)_{\rm OFF}$ for the comparisons, the average relative error is expressed as $\Delta_w\%$. As shown in Fig. 25, the improved model of the SiC MOSFET could get higher accuracy than the conventional model in the wide operation range.

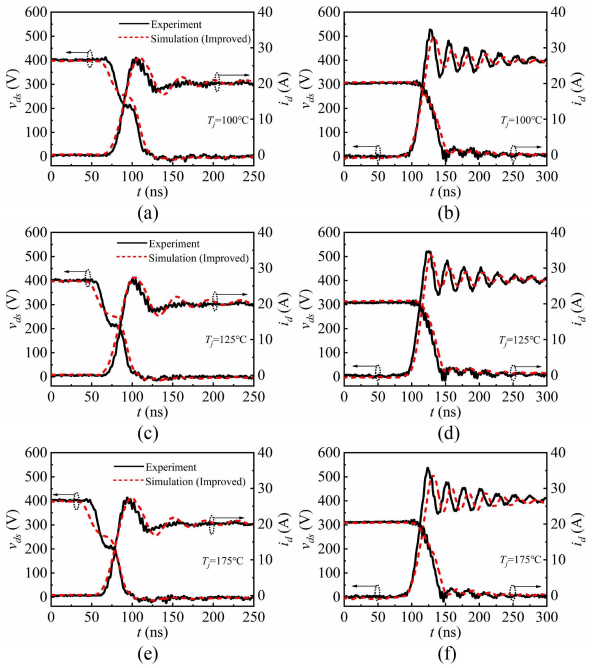


Fig. 24. Comparison of experimental and simulated switching trajectory with different junction temperatures when applying the proposed model ($R_g = 10\ \Omega$, $I_L = 20$ A, $V_{\rm dc} = 400$ V). (a) Turn-ON with $T_j = 100$ °C. (b) Turn-OFF with $T_j = 100$ °C. (c) Turn-ON with $T_j = 125$ °C. (d) Turn-OFF with $T_j = 125$ °C. (e) Turn-ON with $T_j = 175$ °C. (f) Turn-OFF with $T_j = 175$ °C.

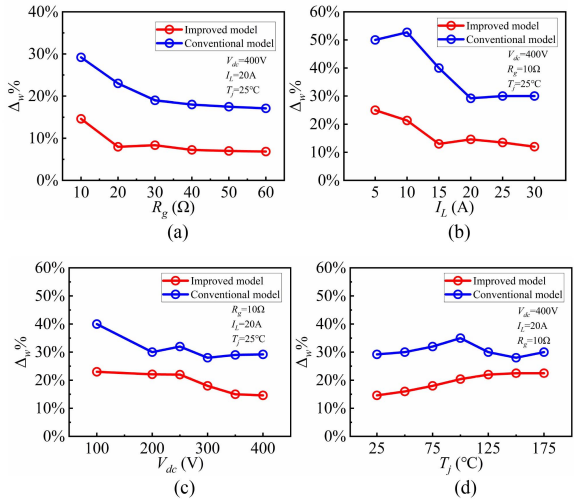


Fig. 25. Comparisons of accuracy in wide operation range of SiC MOSFET. (a) Different R_g. (b) Different I_L. (c) Different $V_{\rm dc}$. (d) Different T_j.

C. Convergence Validation

Besides the accuracy, convergence performance and simulation duration are two other important issues during the evaluation of the device model. It is widely known that the simulation accuracy will increase with the decrease of the maximum simulation step in the Spice software. Meanwhile, the divergence problem might occur in a short simulation step [15]. Fig. 26 shows the proposed model could achieve good convergence close to the conventional model even at the simulation step of 0.01ns. It is obvious that the general embedding method based on the fitting functions in Fig. 16 is easier and faster to converge than the method applying the lookup table, and the model based on the lookup table could not converge at the simulation step of 0.01 ns.

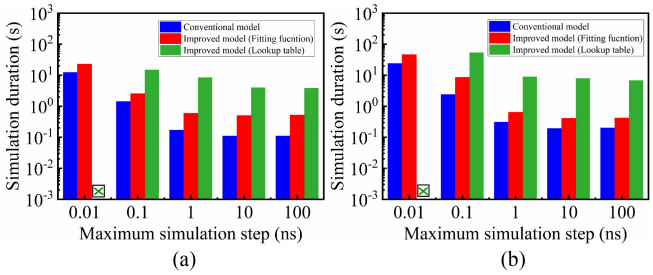


Fig. 26. Convergence validation of different models in Pspice16.6 (running time is 1 μs). (a) One DPT circuit. (b) Two DPT circuits.

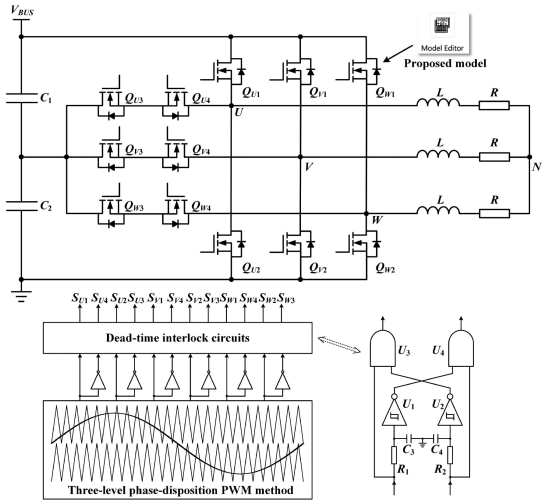
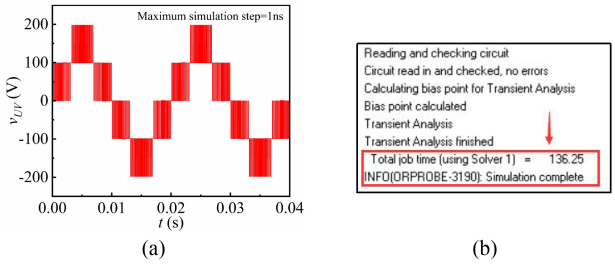


Fig. 27. Three-level T-type inverter with improved SiC MOSFET model.

TABLE III
INFORMATION OF THREE-LEVEL T-TYPE INVERTER

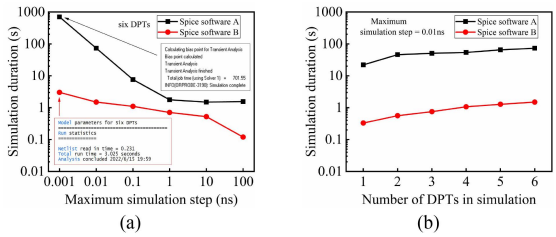
Name	Information
Bus voltage	V_{BUS}=200 V
Bus capacitor	C_1=C_2=680 μF
Load inductor	L=3 mH
Load resistor	R=15 Ω
Modulation method	Phase-disposition PWM
Switching frequency	5 kHz
Output frequency	50 Hz
Modulation ratio	α=0.8
Dead-time interlock circuit	U_1 and U_2 (SN74LVC1G14) U_3 and U_4 (SN74LVC1G08) R_1=R_2=100Ω C_3=C_4=100pF

It is necessary to ensure that the proposed model has good convergence in the system-level simulation. Fig. 27 shows the three-level T-type inverter with the improved SiC MOSFET model. The detailed information on the three-level T-type inverter is shown in Table III. It should be noted that six dead-time interlock circuits are included in the simulation to ensure the operation of the inverter in safety. Fig. 28(a) shows the output line voltage $v_{\rm UV}$ and Fig. 28(b) shows the convergence report of the proposed



(a) (b)

Fig. 28. Simulation results of the proposed model. (a) Output line voltage waveform. (b) Convergence report.



(a) (b)

Fig. 29. Simulation results of the proposed model in various Spice software at (a) different maximum simulation steps. (b) Different number of simulated DPTs. (Pspice16.6 and Simetrix9.0 are Spice software A and B, respectively.)

model in Pspice16.6. It can be seen that the simulation duration of the three-level T-type inverter is 136.25 s (running time = 0.04 s, maximum simulation step = 1 ns), and no divergence problems occur. Therefore, the convergence of the proposed model in the system-level complex topology has been validated well.

D. Generality Validation

It is valuable to show the proposed model has good generality in various Spice software. Besides Pspice16.6, a more state-of-art tool, Simetrix9.0, is also adopted in the same computer configuration for validation of the device model. The simulation results in different software are shown in Fig. 29. Obviously, no divergence problems would occur in the Spice software, even if the maximum simulation step is as short as 1 ps and the number of DPTs is as large as six. It also shows that Simetrix9.0 has a higher simulation speed, which is beneficial for the simulation of the complex converter.

To verify the performance of the improved model of the SiC MOSFET, the device model is also applied to soft-switching applications. Fig. 30 shows the neutral point clamped (NPC) full-bridge three-level LLC resonant converter with an improved SiC MOSFET model. The simulation results in Simetrix9.0 is shown in Fig. 31, where the resonant converter works well and the simulation duration is only 30.55 s (running time = 0.04 s, maximum simulation step = 1 ns). Therefore, the proposed model of the SiC MOSFET also has the potential for soft-switching resonant converters.

V. Conclusion

An improved SiC MOSFET model considering the channel dynamics of transfer characteristics is proposed in this article, which predicts the dynamic characteristics of the SiC MOSFET

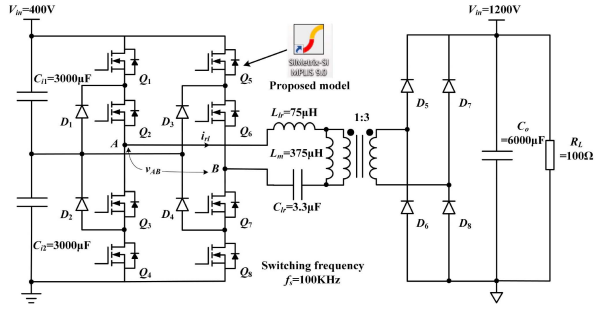
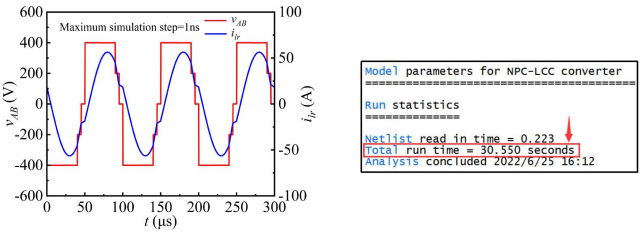


Fig. 30. NPC full-bridge three-level LLC resonant converter with improved SiC MOSFET model.



(a) (b)

Fig. 31. Simulation results of the proposed model. (a) Voltage and current of the resonant network. (b) Convergence report.

in high accuracy and good convergence. The dynamic effects, TSE, SCE, and ISE are taken into consideration in the proposed model. The measurement method based on the DTP and the implemented method in the Spice software are discussed in detail. Furthermore, the nonlinearity of the interterminal capacitances is also included in the model. The performance of the proposed model is validated in the DPT and comparisons with the conventional model are carried out. The simulation results have good agreement with the experimental results in different switching speeds, load currents, blocking voltages, and junction temperatures. Finally, two complex converters are simulated with the proposed model, and good convergence has been proven in a small maximum simulation step. Therefore, the proposed model could predict the dynamic characteristics of the SiC MOSFET at the converter system level.

References

[1] X. She, A. Q. Huang, Ó. Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017.

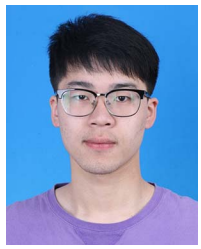
[2] H. A. Mantooth, K. Peng, E. Santi, and J. L. Hudgins, "Modeling of wide bandgap power semiconductor devices—Part I," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 423–433, Feb. 2015.

[3] N. Wang and J. Zhang, "Nonlinear capacitance model of SiC MOSFET considering envelope of switching trajectory," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 7977–7988, Jul. 2022.

[4] H. Li, Y. Jiang, Z. Qiu, Y. Wang, and Y. Ding, "A predictive algorithm for crosstalk peaks of SiC MOSFET by considering the nonlinearity of gate-drain capacitance," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2823–2834, Mar. 2021.

[5] J. Wang, H. S. Chung, and R. T. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan. 2013.

[6] X. Chen, W. Chen, X. Yang, Y. Ren, and L. Qiao, "Common-mode EMI mathematical modeling based on inductive coupling theory in a power module with parallel-connected SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6644–6666, Jun. 2021.
[7] S. K. Roy and K. Basu, "Analytical estimation of turn on switching loss of SiC MOSFET and Schottky diode pair from datasheet parameters," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9118–9130, Sep. 2019.
[8] L. Zhang, X. Yuan, J. Zhang, X. Wu, Y. Zhang, and C. Wei, "Modeling and implementation of optimal asymmetric variable dead-time setting for SiC MOSFET-based three-phase two-level inverters," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 11645–11660, Dec. 2019.
[9] Z. Duan, T. Fan, X. Wen, and D. Zhang, "Improved SiC power MOSFET model considering nonlinear junction capacitances," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2509–2517, Mar. 2018.
[10] K. Chen, Z. Zhao, L. Yuan, T. Lu, and F. He, "The impact of nonlinear junction capacitance on switching transient and its modeling for SiC MOSFET," *IEEE Trans. Electron. Devices*, vol. 62, no. 2, pp. 333–338, Feb. 2015.
[11] S. Jimenez, A. Lemmon, B. Nelson, and B. Deboi, "Comprehensive characterization of MOSFET intrinsic capacitances," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 1524–1530.
[12] W. Jouha, A. E. Oualkadi, P. Dherbécourt, E. Joubert, and M. Masmoudi, "Silicon carbide power MOSFET model: An accurate parameter extraction method based on the Levenberg–Marquardt algorithm," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9130–9133, Nov. 2018.
[13] V. Talesara et al., "Dynamic switching of SiC power MOSFETs based on analytical subcircuit model," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9680–9689, Sep. 2020.
[14] D. Christen and J. Biela, "Analytical switching loss modeling based on datasheet parameters for mosfets in a half-bridge," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3700–3710, Apr. 2019.
[15] H. Li, X. Zhao, K. Sun, Z. Zhao, G. Cao, and T. Q. Zheng, "A non-segmented PSpice model of SiC MOSFET with temperature-dependent parameters," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4603–4612, May 2019.
[16] K. Sun, H. Wu, J. Lu, Y. Xing, and L. Huang, "Improved modeling of medium voltage SiC MOSFET within wide temperature range," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2229–2237, May 2014.
[17] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed. New York, NY, USA: Kluwer Academic, 2004.
[18] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York, NY, USA: Springer, 2008.
[19] M. Riccio, V. d'Alessandro, G. Romano, L. Maresca, G. Breglio, and A. Irace, "A temperature-dependent SPICE model of SiC power MOSFETs for within and out-of-SOA simulations," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 8020–8029, Sep. 2018.
[20] C. Unger and M. Pfost, "Thermal stability of SiC-MOSFETS at high temperatures," *IEEE Trans. Electron Devices*, vol. 66, no. 11, pp. 4666–4672, Nov. 2019.
[21] Z. Dong, X. Wu, H. Xu, N. Ren, and K. Sheng, "Accurate analytical switching-on loss model of SiC MOSFET considering dynamic transfer characteristic and Q_{gd}," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12264–12273, Nov. 2020.
[22] M. Noborio, Y. Kanzaki, J. Suda, and T. Kimoto, "Experimental and theoretical investigations on short-channel effects in 4H-SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 1954–1962, Sep. 2005.
[23] K. Tachiki, T. Ono, T. Kobayashi, and T. Kimoto, "Short-channel effects in SiC MOSFETs based on analyses of saturation drain current," *IEEE Trans. Electron Devices*, vol. 68, no. 3, pp. 1382–1384, Mar. 2021.
[24] C. Unger and M. Pfost, "A comparison of the transient behavior of the drain current hysteresis in SiC-MOSFETs," in *Proc. IEEE Int. Conf. Elect. Syst. Aircr., Railway, Ship Propulsion Road Veh. Int. Transp. Electrific. Conf.*, 2018, pp. 1–5.
[25] Y. Cai et al., "Effect of threshold voltage hysteresis on switching characteristics of silicon carbide MOSFETs," *IEEE Trans. Electron Devices*, vol. 68, no. 10, pp. 5014–5021, Oct. 2021.
[26] Wolfspeed, "C2M0080120D: Silicon carbide power MOSFET," 2019. [Online]. Available: https://www.wolfspeed.com/media/downloads/167/C2M0080120D.pdf
[27] R. Stark, A. Tsibizov, N. Nain, U. Grossner, and I. Kovacevic-Badstuebner, "Accuracy of three interterminal capacitance models for SiC power MOSFETs under fast switching," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9398–9410, Aug. 2021.
[28] A. Agarwal, K. Han, and B. J. Baliga, "Impact of cell topology on characteristics of 600V 4H-SiC planar MOSFETs," *IEEE Electron Device Lett.*, vol. 40, no. 5, pp. 773–776, May 2019.
[29] H. Sakairi, T. Yanagi, H. Otake, N. Kuroda, H. Tanigawa, and K. Nakahara, "Measurement methodology for accurate modeling of SiC MOSFET switching behavior over wide voltage and current ranges," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7314–7325, Sep. 2018.
[30] P. Hofstetter, R. W. Maier, and M. M. Bakran, "Influence of the threshold voltage hysteresis and the drain induced barrier lowering on the dynamic transfer characteristic of SiC power MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf.*, 2019, pp. 944–950.
[31] A. Tsibizov, I. Kovačević-Badstübner, B. Kakarla, and U. Grossner, "Accurate temperature estimation of SiC power MOSFETs under extreme operating conditions," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1855–1865, Feb. 2020.



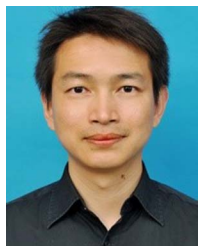
Ning Wang received the B.E. degree in electrical engineering from Jiangsu University, Zhenjiang, China, in 2020. He is currently working toward the Ph.D. degree with the Department of Electrical Engineering, Southeast University, Nanjing, China.

His research interests include the modeling for the electromagnetic transients of power electronics devices and novel active gate driver designs.

Jianzhong Zhang (Senior Member, IEEE) received the M.Sc. and Ph.D. degrees in electrical engineering from the Department of Electrical Engineering, Southeast University, Nanjing, China, in 2005 and 2008, respectively.

From 2006 to 2007, he was a visiting scholar with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. Since 2008, he has been with Southeast University, Nanjing, China, where he is currently a Research Professor with the School of Electrical Engineering. He was a Visiting Professor with Worcester Polytechnic Institute, Worcester, MA, USA, and the University of British Columbia, Vancouver, BC, Canada, from July 2012 to Aug. 2017, respectively. His research interests include power electronics, electrical machines, and renewable power generation.

Dr. Zhang was the recipient of the Institution Premium Award at the Institutions of Engineering and Technology, U.K.



Fujin Deng (Senior Member, IEEE) received the B.Eng. degree in electrical engineering from China University of Mining and Technology, Jiangsu, China, in 2005, the M.Sc. degree in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2008, and the Ph.D. degree in energy technology from the Department of Energy Technology, Aalborg University, Aalborg, Denmark, in 2012.

From 2013 to 2015 and from 2015 to 2017, he was a Postdoctoral Researcher and an Assistant Professor, respectively, with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. He joined the Southeast University in 2017 as a Professor in the School of Electrical Engineering, Southeast University, Nanjing, China. His main research interests include wind power generation, multilevel converters, high-voltage direct-current technology, dc grids, and offshore wind farm-power systems dynamics.