Design and Analysis of Modular Multilevel Reconfigurable Battery Converters for Variable Bus Voltage Powertrains

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***Abstract*—Larger battery packs, an efficient battery management system, highly efficient electromechanical conversion, and fast battery charging are the key factors for extending the drive range of electric vehicles and the expansion of electromobility. We present a novel highly stable modular multilevel powertrain design with a variable dc-bus voltage, active inner battery energy flow control, and reduced filter size. The underlying powertrain design replaces conventional hard-wired batteries by a modular multilevel architecture, thus modularizing the battery pack and increasing the energy efficiency, reducing the output filter size, and providing full control over the output voltage and energy flow of the battery cells. We analyse the large-signal stability of the proposed system and compare it to dc/dc-dc/ac conventional multiconverter powertrains, demonstrating better stability and lower filter requirements. Further, we experimentally evaluate the proposed system structure. In the experimental setup, we achieve stable converter operation with the output filter capacitor reduced by a factor of 24 and the filter inductor reduced by a factor of 17 compared to dc-dc-dc-ac reference system, thereby leading to a significant reduction of system cost, size, and weight.**

***Index Terms*—Efficiency, electric vehicle (EV), fast charging, inverter, multilevel converter, reconfigurable battery, variable dc bus.**

I. Introduction

MODERN electric vehicle (EV) powertrains rely on large-scale batteries, maximal utilization of the installed capacity, and highly efficient electromechanical energy conversion to extend the EV drive range. The drive range may be among the key parameters catalysing the shift to electromobility.

At present, EV manufacturers tend to increase the dc-link voltage up to 800 V to minimize the charging time and the conduction losses [1]. Although high dc-bus voltages allow faster and more efficient charging, long series-connected battery-cell strings suffer from a substantial loss of the usable or inaccessibility of the physical capacity due to cell-to-cell variation [2]–[4]. Furthermore, the switching losses in the inverter increase [5]–[7], and so do the magnetic losses in the motor iron [8]. Both loss mechanisms are negligible at high-speed and high-torque operating regions with a high modulation index. However, the efficiency of high-voltage powertrain drops in the low-speed and low-torque operating points, which may dominate in urban driving cycles, such as FTP-75 and ECE-15.

In the literature, several techniques increasing the efficiency in the urban driving cycle are investigated [9]–[14]. These techniques typically implement a dc–dc converter between the battery pack and the inverter to gain control over the dc-link voltage supplying the inverter. Bidirectional non-isolated boost converters are among the most studied topologies in the field [15]. The battery located at the low-voltage side of the dc–dc converter enables shorter series-connected cell strings, thus effectively addressing an average capacity drop caused by cell-to-cell parameter variation.

However, such a configuration does not allow fast and/or efficient direct battery charging from a high-voltage charger. Furthermore, powertrain systems with multiple conversion stages struggle with stability concerns. The traction inverter with tight torque control represents a constant power load (CPL) for the dc link. CPLs are known for their destabilizing character and exacerbate the design. Particularly, the filter design plays a key role in the stability of such a system. Besides various complex active stabilization techniques [16]–[20], proper filter design can guarantee a stable system under certain conditions. Unfortunately, such a design results in oversizing the filter capacitor and a bulky as well as expensive filter [21].

Moreover, the dc–dc converter requires active components rated for the dc bus voltage and the maximal current rating of the motor. High-voltage semiconductor switches operate at low switching dynamics; otherwise the switching loss will be intolerable. Therefore, such a topology requires a large filtering

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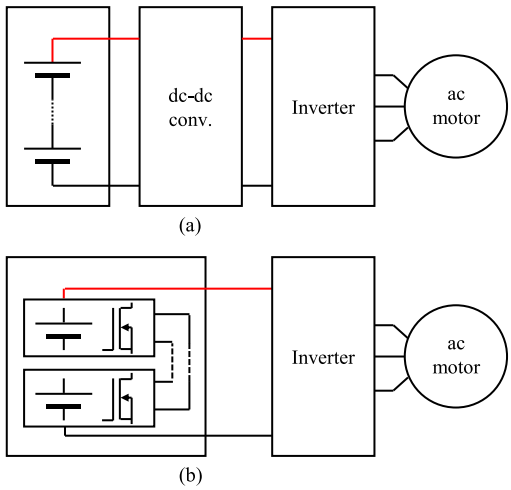

Fig. 1. Variable dc-link voltage powertrain. (a) Conventional solution and (b) reconfigurable solution.

inductor to sufficiently reduce the current ripple and for safe and stable operation.

We present a novel variable dc voltage powertrain system based on a modular reconfigurable dc battery pack, which increases the energy efficiency of the battery, improves the system stability and reliability, reduces the filter size, and provides wide charging capability.

This article describes conventional variable voltage powertrain systems and discusses their design and limitations in Section II. Section III presents the concept of modular multilevel reconfigurable battery converter and evaluates its implementation in powertrain systems. Benefits and design rules of the reconfigurable battery are discussed in Section IV and experimentally evaluated in Section V. Section VI summarizes the implementation of the modular battery system.

II. EV Powertrain Architecture

Most conventional powertrain systems comprise a hard-wired battery pack, an inverter, and an ac motor. The unchangeable battery pack provides a fixed voltage common for the drive and the charging. Particularly in drive operation, a high dc-link voltage implies low conduction losses and high efficiency in high-speed operating points. The low-speed region, on the other hand, suffers from unnecessarily high inverter switching and motor iron losses [8]. Furthermore, all loads have to manage the large voltage differences between full and depleted batteries.

Multiple converter powertrain systems, such as a wide range of vehicles from various brands based on Toyota's Hybrid Synergy Drive employ a nonisolated bidirectional dc–dc converter between the battery and the inverter [see Fig. 1(a)]. The converter provides control over the inverter dc link voltage and decouples it from the battery voltage.

A. System Model

Typically, the battery is located on the low-voltage side of the converter, which is operated in the step-up mode in drive operation (see Fig. 2). Applying the state-space averaging method, the circuit can be described as

$$\begin{aligned}\frac{\mathrm{d}i_L}{\mathrm{d}t} &= -\frac{r_\mathrm{L}}{L}i_L - (1-d)\frac{v_\mathrm{o}}{L} + \frac{1}{L}v_i \\ \frac{\mathrm{d}v_\mathrm{o}}{\mathrm{d}t} &= (1-d)\frac{1}{C}i_L - \frac{1}{C}i_\mathrm{o},\end{aligned} \tag{1}$$

where i_L is the inductor current, r_L is the inductor series resistance, L is the inductance, d is the duty ratio, v_o is the output voltage, v_i is the input voltage, C is the output capacitance, and i_o is the output current.

A tightly regulated power inverter behaves as a constant-power load. Considering the dc bus loaded by a mix of load types, the output current is expressed as

$$i_o = \frac{p_\mathrm{cpl}}{v_o} + \frac{v_\mathrm{o}}{R_o} \tag{2}$$

where p_cpl is the output power of the powertrain and R_o the resistive load.

The boost converter implements a cascaded control structure with an inner current loop and an outer voltage loop. The voltage loop is described as

$$\begin{aligned}\frac{\mathrm{d}y_1}{\mathrm{d}t} &= v_\mathrm{o,ref} - v_\mathrm{o} \\ i_\mathrm{L,ref} &= k_\mathrm{vp}\left(v_\mathrm{o,ref} - v_\mathrm{o}\right) + k_{vi}y_1\end{aligned} \tag{3}$$

where y_1 is the integrated voltage error, k_{vp} is the proportional gain, k_{vi} is the integral gain and $i_\mathrm{L,ref}$ is the inductor current reference. Similarly, the current loop is described as

$$\begin{aligned}\frac{\mathrm{d}y_2}{\mathrm{d}t} &= i_\mathrm{L,ref} - i_L \\ d &= k_{ip}\left(i_\mathrm{L,ref} - i_L\right) + k_{ii}y_2,\end{aligned} \tag{4}$$

where y_2 is the integrated current error, k_{ip} is the proportional gain, and k_{vi} is the integral gain.

The model described by (1)–(4) has four state variables i_L, v_o, y_1, and y_2. Let all time derivatives in (1)–(4) be equal to zero and consider a constant input voltage V_i, the steady-state values of the state variables are

$$\begin{aligned}I_{L0} &= k_{vi}Y_{10} \\ V_{o0} &= V_\mathrm{o,ref}\,Y_{10} = \frac{V_i - \sqrt{V_i^2 - 4r_L\left(p_\mathrm{cpl} + \frac{V_\mathrm{o,ref}^2}{R_o}\right)}}{2r_\mathrm{L}k_\mathrm{vi}} \\ Y_{20} &= \frac{2V_\mathrm{o0} - V_i - \sqrt{V_i^2 - 4r_L\left(p_\mathrm{cpl} + \frac{V_\mathrm{o,ref}^2}{R_o}\right)}}{2k_{ii}V_{o0}}, \\ D_\mathrm{o} &= k_\mathrm{ii}Y_{20}.\end{aligned} \tag{5}$$

The abovementioned conditions apply for a fixed output voltage of the battery defined by the series–parallel configuration of battery cells.

B. Filter Design

The boost-converter filter comprises an inductor on the input and a capacitor on the output side of the converter. The typical

design approach sizes the inductor and the capacitor to achieve desired current and voltage ripple [22]. Specifically, we set the inductor current and voltage ripple to 10 % and 1 %, respectively. Considering the design rules in the literature [22] and parameters in Table I, we calculate the inductor size as

$$L > V_i^2 \frac{(V_o - V_i)}{2p_o f_{sw} V_o \cdot \Delta i_L} \tag{6}$$

where p_o is the output power, which is the sum power of the resistive load and constant-power load.

To simplify the output capacitor design, we replace the constant-power load with an equivalent resistive load. The output capacitor is calculated as

$$C > \frac{(V_o - V_i)\, p_o}{2V_o^3 f_{sw} \cdot \Delta v_o}\,. \tag{7}$$

C. Charging Capability

The boost-based converter system can be charged either directly from a battery charger, or through the dc–dc converter. The converter allows charging from any voltage source (controlled or not) with an output voltage higher than the battery terminal voltage and lower than the maximal dc-link voltage. The converter can control the charging current, and therefore it allows charging from un-controlled or voltage-controlled sources, thus extending the charging capability of the system.

However, the dc–dc converter is typically rated for the power of the drivetrain, which can be significantly lower than the power of latest fast EV chargers [23]. Such a power rating forms a bottleneck for the system and does not allow fast high-voltage charging.

TABLE I
SYSTEM AND CONTROL PARAMETERS

Parameters	Description	Values
V_i	Input voltage	48 V
V_o	Output voltage	100 V
P_{CPL}	Output power	500 W
R_o	Resistive load	100 Ω
f_{sw}	Switching rate	12.5 kHz
Δi_L	Inductor current ripple	10 %
Δv_o	Output voltage ripple	1 %
L	Filter inductor	799 µH
r_L	Inductor series resistance	0.1 Ω
C	Filtering capacitor	168 µF
K_{vp}	Voltage loop proportional gain	1.80
K_{vi}	Voltage loop integral gain	486
K_{ip}	Current loop proportional gain	0.1
K_{ii}	Current loop integral gain	110

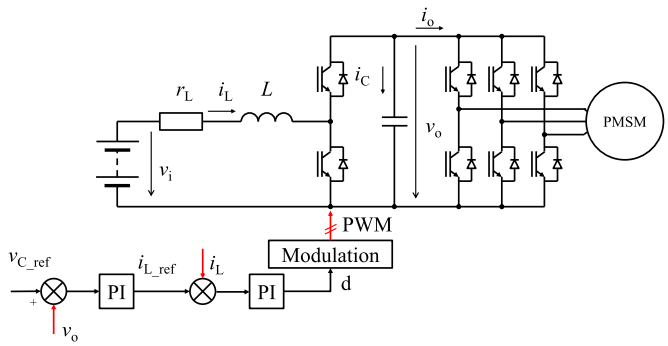

Fig. 2. Powertrain architecture based on a boost converter as for example in Toyota's hybrid synergy drive serves as the reference topology here.

III. Modular Multilevel Battery Converter Architecture

The proposed powertrain system replaces the conventional battery system and the bidirectional dc–dc converter with a modular reconfigurable battery [see Fig. 1(b)]. Reconfigurable batteries combine battery cells and power electronics to form a battery pack. There are several different reconfigurable topologies [24], [25]. In general, we recognise two groups: topologies connecting neighbouring modules only [26]–[28]; and topologies connecting even nonneighbouring ones [29]–[31]. Connecting nonneighbouring modules provides limited scalability of the system and typically introduces a need for high-voltage module components, such as semiconductors. The second group implements structures well known from the field of modular multilevel converters, which provide connection only between neighbouring modules. Semiconductor switches in these topologies are rated for the maximum voltage of one module, thus providing good scalability.

The simplest module topology for a dc reconfigurable battery is a half-bridge, where each module can connect in series or be bypassed. Alternatively, Fig. 3(b) depicts a three-switch topology providing series, parallel, and bypass connections with minimum number of switches. The general behaviour of the parallel and bypass connections (as well as the two mentioned topologies) from the output perspective are identical. Neither bypassing a module nor connecting modules in parallel increases the overall number of series-connected modules. However, since the parallel connection can concurrently offer load sharing, lower equivalent resistance, and balancing, the three-switch topology may be the preferred choice in many applications [32], [33].

Such a modular battery pack benefits from higher degrees of freedom to control the terminal voltage in fixed discrete levels or a combination of fixed and pulse-width modulated ones. The resultant circuit is in essence a multilevel buck converter [see Fig. 3(a)] [34], [35]. Switch Q_2 is in the three-switch topology complementary to both switches Q_1 and Q_3. In basic operation, we consider just 3 different switch states, as described in Fig. 4. The module configuration is applied with respect to all other modules in the battery pack to achieve demanded instantaneous terminal voltage.

Typically, such a multilevel converter synthesizes the output voltage from discrete voltage levels, implementing any of the known multilevel modulation techniques [14], [36]–[40]. Practically, phase-shifted carrier pulse-width modulation is among the highly popular multilevel modulation techniques for its simplicity and yet exceptional [41]–[44]. It evenly distributes conduction times, increases effective output frequency, and guarantees periodical switching of all modules. Thus, it allows convenient output filter sizing and bootstrapping of the gate driver supply voltage.

Considering the same mixed load conditions as for the boost converter (2), we describe the circuit as

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = d\frac{V_i}{L} - \frac{v_\mathrm{o}}{L} - \frac{r_L i_L}{L}$$
$$\frac{\mathrm{d}v_\mathrm{o}}{\mathrm{d}t} = \frac{i_L}{C} - \frac{i_\mathrm{o}}{C}\,. \tag{8}$$

We also implement the cascaded control structure with the outer voltage loop (3) and the inner current loop (4), like the conventional multiconverter powertrain solution. Hence, the state-space variables remain unchanged, i.e., i_L, v_o, y_1, and y_2, but their steady-state values differ:

$$V_{o0} = V_{o,\mathrm{ref}}$$
$$I_{L0} = \frac{p_\mathrm{cpl}}{V_{o0}} + \frac{V_{o0}}{R_o}$$
$$Y_{10} = \frac{I_{L0}}{k_{vi}}$$
$$Y_{20} = \frac{(V_{\mathrm{o}0} + r_L I_{L0})}{k_{ii} V_i}$$
$$D_0 = k_{ii} Y_{20}. \tag{9}$$

A. Modularization

The modular feature of the reconfigurable battery introduces several convenient design improvements and features, such as high energy efficiency [29], [45], [46] and increased fault tolerance [29], [47], [48].

Indeed, equipping each battery cell with power electronics may offer the best energy utilization [29], but such an extreme degree of modularization would be highly ineffective, costly, and unnecessary for breaking the statistics of the cell parameter spread. Instead, we propose small series-parallel groups of cells to form modules, e.g., <60 V.

The series-parallel configuration determines the module installed ampere-hour capacity. Whereas the physically installed ampere-hour capacity stays constant with an increasing number of series-connected cells, the practically available capacity follows the law of the minimum, because the smallest cell determines the usable capacitance—when the first cell is empty, the entire pack has to be considered so. Thus, as the cell-to-cell parameter spread leads to a higher chance of small cells the more cells are in the pack, the overall available capacitance suffers.

Large-scale batteries always implement a BMS to minimize the state-of-charge disbalance, but most BMS cannot overcome the limitation of the smallest cell. The reconfigurable battery however can exchange charge, energy, and power between modules to increase usable capacity and efficiency. The energy efficiency of the reconfigurable battery is further analysed in Section IV.

B. Filter Size Reduction

High power density is among the key parameters of modern power converters. The rapidly developing semiconductor integration is constantly reducing the converter size. However, passive filter components, such as inductors and capacitors, dominate the size in two-level converters [49]–[51] and make a further increase of power density difficult.

TABLE II
SYSTEM AND CONTROL PARAMETERS

Parameters	Description	Values
V_i	Input voltage	120 V
V_o	Output voltage	100 V
P_CPL	Output constant power load	500 W
$\mathrm{R_o}$	Resistive load	100 Ω
Δi_L	Inductor current ripple	10 %
Δv_o	Output voltage ripple	1 %
f_sw	Switching rate	12.5 kHz
L	Filter inductor	47 µH
r_L	Inductor series resistance	0.01 Ω
C	Filtering capacitor	168 / 2.2 µF
K_vp	Voltage loop proportional gain	2.34
K_vi	Voltage loop integral gain	550
K_ip	Current loop proportional gain	0.005
K_ii	Current loop integral gain	50

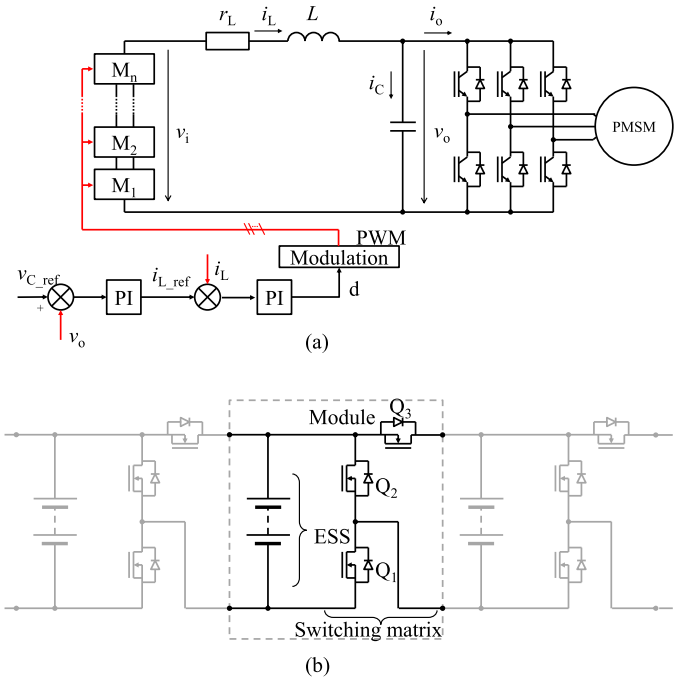

Fig. 3. Multilevel converter circuit diagrams of (a) the macrotopology and (b) the microtopology.

High output-voltage quality and low output-filter requirements are typical features of multilevel converters [34], [36]. Both features follow from a higher output-voltage resolution and higher switching rate.

Unlike conventional two-level converters, reconfigurable battery converters provide multiple discrete voltage levels at their terminals reflecting the module voltages. The reconfigurable battery modulates the demanded voltage using the two nearest levels

$$V_{\mathrm{bt},h} = V_\mathrm{mod} \cdot \left\lceil \frac{V_o}{V_\mathrm{mod}} \right\rceil \quad \text{and upright}$$

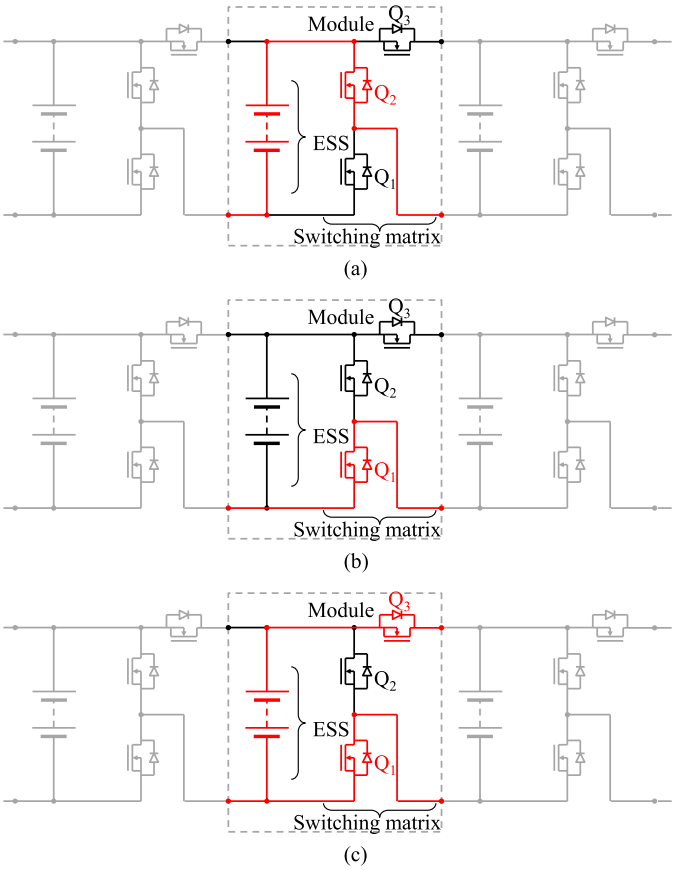

Fig. 4. Operational principle of the three-switch module topology. (a) Q_2 is ON, and the module is connected in series. (b) Q_1 is ON, and the module with all parallel connected modules on the left side are bypassed. (c) Q_1 and Q_3 are ON, and the module is connected in parallel with the neighboring module on the right side.

$$V_{\mathrm{bt,l}} = V_{\mathrm{mod}} \cdot \left\lfloor \frac{V_o}{V_{\mathrm{mod}}} \right\rfloor$$

where $V_{\mathrm{bt,h}}$ is the nearest higher voltage, $V_{\mathrm{bt,l}}$ is the nearest lower voltage, V_{mod} is the module voltage and V_{o} is the desired output voltage.

Lower voltage ratings of components in multilevel converters allow the implementation of semiconductor switches with higher dynamics, thus an increase of the switching rate. Beside the transistor switching rate, a proper multilevel modulation technique can further increase the effective switching rate of the converter. For example, the phase-shifted carrier pulsewidth modulation (PS-PWM) can increase the effective switching rate of the system, thus further decreasing the filter size [34], [52]. The effective switching rate depends on the number of modules in the system as

$$f_{\mathrm{sw}} = k \cdot f_{\mathrm{sw,mod}}$$

where f_{sw} is the effective switching rate, $f_{\mathrm{sw,mod}}$ the module switching rate and k the number of modules in the system.

Considering PS-PWM, design of the filtering inductor follows rules like a conventional buck converter (except for the increased equivalent switching frequency) described in [22]:

$$L = \frac{(V_{\mathrm{bt},h} - V_o)^2 V_o}{2V_{\mathrm{mod}} f_{\mathrm{sw}} p_{\mathrm{o}} \cdot \Delta i_L}. \tag{10}$$

Similarly, we design the output capacitor as

$$C = \frac{p_o \cdot \Delta i_L}{8V_o^2 f_{\mathrm{sw}} \cdot \Delta v_o}. \tag{11}$$

The inductor and capacitor sizes are proportional to the module voltage. The smaller the module voltage, the closer we can approximate the output voltage, and thus reduce the inductor and the capacitor sizes.

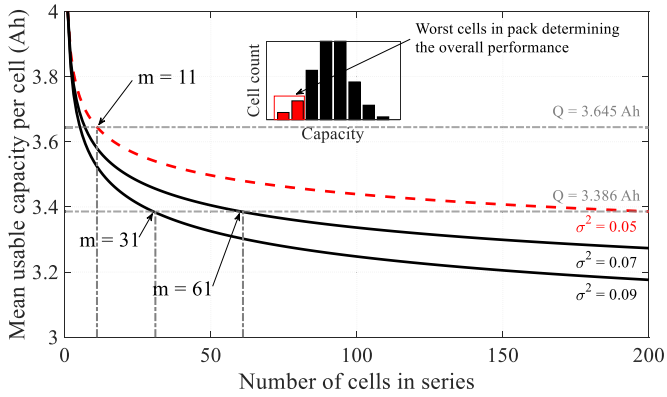

Fig. 5. Average capacity drop of series-connected strings of cells with different quality ($\mu = 4$ Ah, $\sigma^2 = 0.05$, $\sigma^2 = 0.07$, and $\sigma^2 = 0.09$).

C. Stability Improvement

The filter design is among the key factors influencing the stability of multiconverter systems [21]. Indeed, a large filtering inductor reduces the current ripple and increases the output voltage quality; on the other hand, it reduces the system stability. The stability can be improved by oversizing the output capacitor. Such an approach, particularly for high-power high-voltage systems, results in a bulky and expensive filter.

The convenient filter sizing in multilevel topologies guarantees small filters and increased stability, as analysed in Section IV.

D. Charging Capability

The dynamically reconfigurable framework of the battery provides two options for charging: a dynamic charging mode and a steady charging mode. The dynamic mode is in principle equivalent to charging the battery through the dc–dc converter in the reference topology. As the output voltage and the charging current are controlled by the converter, the battery can be charged from uncontrolled voltage sources. In contrast to the boost converter, the source voltage must be lower than the maximal battery output voltage.

The steady mode allows setting the battery to a specific series–parallel configuration to adjust the battery terminal voltage according to the charger capability. The battery pack can be charged from a controlled voltage source directly without

switching or with low-dynamic switching [26]. The absence of switching loss leaves more space for conduction losses, thus increases current capability of the system allowing fast charging [53].

IV. Benefits of the Proposed Powertrain Architecture

A. Modularization Statistics

Energy efficiency of long series-connected battery strings, typical for large batteries, strongly relies on effective BMS providing either passive or active balancing. Passive balancing represents a simple and cost-effective solution to increase utilization of the battery installed. Nevertheless, such a solution does not effectively overcome the average capacity drop in large batteries caused by cell-to-cell parameter variation. Unlike active balancing, the passive technique is not capable of charge redistribution among cells in the battery pack. The usable capacity of a battery pack implementing passive balancing technique is

$$Q_{BP} = \min\{Q_{B1},\ Q_{B2}, \ldots,\ Q_{Bm}\} \tag{12}$$

where Q_{BP} is the usable capacity of the battery pack, m is number of cells in series, and Q_{B1} to Q_{Bm} are ampere-hour capacities of individual battery cells.

To fully utilize the installed capacity, the battery pack needs to actively redistribute the charge in the battery pack during runtime, respectively active balancing technique described as

$$Q_{BP} = \mathrm{mean}\{Q_{B1},\ Q_{B2}, \ldots,\ Q_{Bm}\}. \tag{13}$$

The proposed multilevel topology provides a degree of freedom to actively control the energy flow through individual modules, thus performing active balancing on the module level [46], [54], [55]. In addition to the module balancing, each module implements a local passive BMS to perform balancing on the cell level. The combination of the passive technique on the cell level and active balancing on the module level forms a hybrid balancing depending on the degree of modularization, respectively, on the module size, as described by

$$Q_{BP} = \mathrm{mean}\{\min\{Q_{B1},\ \ldots, Q_{Bn}\},\ \ldots,\ \min\{Q_{B(m-n)}, \ldots, Q_{Bm}\}\} \tag{14}$$

where n is number of cells in a module and represents the module size.

Considering a normal distribution of cell ampere-hour capacity, the mean capacity of m series-connected cells combined with passive balancing is expressed as

$$E(Q_n) = \int_{-\infty}^{\infty} Q \cdot f(Q,\mu,\sigma) \cdot (1 - F(Q,\mu,\sigma))^{n-1} \mathrm{d}Q \tag{15}$$

where Q is the ampere-hour capacity, f is the cell capacity distribution function, F is the cell capacity cumulated distribution function, μ is the mean value, σ is the standard deviation, and n is the number cells in series.

Indeed, large batteries require higher quality cells to minimize the average capacity drop due to the limitation to the weakest cell. Nevertheless, minimizing manufacturing tolerances and preselecting cells is extremely costly and does not fully eliminate the effect. Furthermore, even perfectly matched cells develop parameter variation during the lifetime [56].

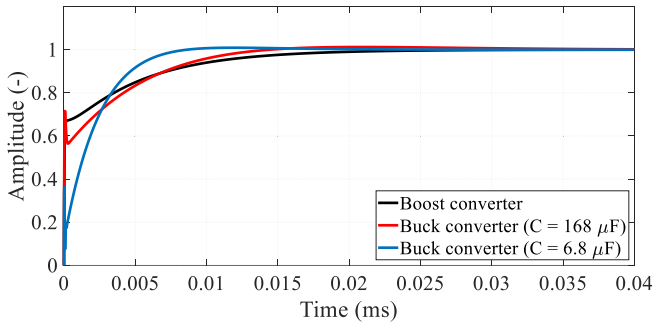

Fig. 6. Step-response comparison of the reference boost converter ($L = 799$ μH and $C = 168$ μF) (black line), the multilevel converter with equal output capacitor ($L = 47$ μH and $C = 168$ μF) (red line), and the multilevel converter with proper output filter size ($L = 47$ μH and $C = 6.8$ μF) (blue line).

The proposed architecture breaks long series strings into shorter segments increasing their average capacity, as described in Fig. 5. Therefore, the proposed multilevel topology can reach a higher average capacity compared to the conventional solution considering the same high-quality cells. More interestingly, a reconfigurable battery can achieve the same average capacity implementing even lower-quality cells (see Fig. 5).

Furthermore, a proper control strategy of such a reconfigurable battery pack can increase the battery lifetime [57].

B. Stability Improvement

The proposed multilevel topology implements lower-voltage semiconductor switches matching the module voltage, which allow higher switching rates and provide better dynamics compared to the boost converter with high-voltage semiconductors. To yield a fair comparison, we limit the switching rate of the proposed system to 12.5 kHz and tune the regulators of both systems to match their output voltage step responses in speed to set equal conditions (see Fig. 6).

The large-signal stability of the conventional boost converter and the proposed multilevel topology loaded by a CPL and a resistive load are studied by estimating the domain of attraction using the second Lyapunov method and Takagi–Sugeno (TS) multimodeling. The method yields the largest attraction domain among nonlinear system stability analysis tools and is suitable for nonlinear systems with multiplication, division, exponential, and square-root nonlinearities [58].

The TS multimodel deduces a set of r linear local models from the nonlinear system and interconnects them by nonlinear scalar membership functions $\boldsymbol{F}$ verifying the property of the convex sum. Considering q nonlinearities of the modeled system ($f_{\mathrm{j}}(x) = 1, 2, \ldots, q$), the resulting TS model has at least $r = 2^q$ rules. With enough local linear models, the obtained TS model is strictly equivalent to the nonlinear model [58].

Shifting the operating point to the origin and assuming constant inputs ($u(t) = 0$), we obtain the TS autonomous model

as

$$\dot{\boldsymbol{x}} = \sum_{i=1}^{r} \left[\boldsymbol{F_i}(\boldsymbol{x})\boldsymbol{A_i}(\boldsymbol{x})\right] \cdot \boldsymbol{x}. \tag{16}$$

The system is asymptotically stable if there exists a feasible solution of the linear matrix inequality (LMI)

$$\begin{aligned} &\boldsymbol{P} = \boldsymbol{P}^T > 0 \\ &\boldsymbol{A}_{\mathrm{i}}^T \cdot \boldsymbol{P} + \boldsymbol{P} \cdot \boldsymbol{A}_{\mathrm{i}} < 0 \ \ \forall i \in \{1,\ 2,\ \ldots, r\}. \end{aligned} \tag{17}$$

The existence of the matrix $\mathbf{P}$ is conditioned by matrix $\mathbf{A_i}$ fulfilling Hurwitz and $\boldsymbol{A} = \sum_{i=1}^{r} \boldsymbol{A}_i$ fulfilling Hurwitz. When these two conditions are fulfilled and there is a feasible solution of LMI (17), the Lyapunov quadratic function is completely known as

$$V(\boldsymbol{x}) = \boldsymbol{x}^T \cdot \boldsymbol{P} \cdot \boldsymbol{x}. \tag{18}$$

Importantly, no knowledge of membership functions is required for the determination of $V(\boldsymbol{x})$.

In what follows, we combine the TS method with phase portraits of both systems for visual stability analysis. We use a combination of states to generate a set of phase portraits to determine without loss of information the complete behaviour of the immediate system dynamics for the set of initial conditions (5) and (9) [59].

1) Boost Converter: The autonomous model (16) of the powertrain system implementing boost converter was obtained from (1)–(4) and shifting the operating point (5) to the origin, as

$$\begin{aligned} x_1 &= i_L - I_{L0} \\ x_2 &= v_o - V_{o0} \\ x_3 &= y_1 - Y_{10} \\ x_4 &= y_2 - Y_{20} \end{aligned} \tag{20}$$

where $\boldsymbol{x} = [x_1,\ x_2,\ x_3,\ x_4]$ is the new state-space variable vector describing the deviation from the origin, respectively the operating point. The model (19) has three nonlinearities ($q = 3$), therefore there are $r = 2^3 = 8$ rules, thus eight linear models

$$\dot{\mathbf{x}} = \left[\boldsymbol{F}_i\left(x_1, x_2\right)\boldsymbol{A}_i\left(x_1, x_2\right)\right] \cdot \boldsymbol{x} \tag{21}$$

with

$$\begin{aligned} f_1 &= x_1 \\ f_2 &= x_2 + V_{o0} \\ f_3 &= \frac{1}{x_2 + V_{o0}}\ . \end{aligned} \tag{22}$$

The LMI problem (17) can be formulated as

$$\begin{aligned} &\boldsymbol{P} = \boldsymbol{P}^T > 0 \\ &\boldsymbol{A}(x_{1\min}, x_{2\min})^T \cdot \boldsymbol{P} + \boldsymbol{P} \cdot \boldsymbol{A}\left(x_{1\min},\ x_{2\min}\right) < 0 \\ &\boldsymbol{A}(x_{1\min}, x_{2\max})^T \cdot \boldsymbol{P} + \boldsymbol{P} \cdot \boldsymbol{A}\left(x_{1\min},\ x_{2\max}\right) < 0 \\ &\boldsymbol{A}(x_{1\max}, x_{2\min})^T \cdot \boldsymbol{P} + \boldsymbol{P} \cdot \boldsymbol{A}\left(x_{1\max},\ x_{2\min}\right) < 0 \\ &\boldsymbol{A}(x_{1\max}, x_{2\max})^T \cdot \boldsymbol{P} + \boldsymbol{P} \cdot \boldsymbol{A}\left(x_{1\max},\ x_{2\max}\right) < 0 \end{aligned} \tag{23}$$

where matrix functions $\mathbf{A}$ are obtained by replacing nonlinearities f_1, f_2, and f_3 with their minimal and maximal values. Estimation of the largest possible domain of attraction is an optimization task searching for the largest intervals $I_1 = [x_{1\min}\ x_{1\max}]$ and $I_2 = [x_{2\min}\ x_{2\max}]$ which provides a Hurwitz matrix $\mathbf{A}$ and a feasible solution of LMI (23). A MATLAB program has been developed with model parameters given in Table I and fixed x_1 interval $I_1 = [-0.78\ 0.78]$. Solving LMI (23) and searching for the largest interval I_1, we obtained a positive definite matrix

$$P = \begin{bmatrix} 38.12 & 50.73 & -2.05 \cdot 10^4 & -2.39 \cdot 10^4 \\ 50.73 & 93.02 & -3.79 \cdot 10^4 & -4.54 \cdot 10^4 \\ -2.05 \cdot 10^4 & -3.79 \cdot 10^4 & 8.07 \cdot 10^7 & -2.06 \cdot 10^7 \\ -2.39 \cdot 10^4 & -4.54 \cdot 10^4 & -2.06 \cdot 10^7 & 6.99 \cdot 10^7 \end{bmatrix} \tag{24}$$

for the x_2 interval $I_2 = [-0.64\ 0.64]$. The Lyapunov quadratic function is obtained from (19) shown at the bottom of this page. The border of the attraction domain is obtained by inserting a point lying on the border into (18).

There are two candidate points $x_{\min}^1$ and $x_{\min}^2$: point of tangency of the Lyapunov function V(x) and plain $x_1 = x_{1\min}$; and point of tangency of the Lyapunov function V(x) and plain $x_2 = x_{2\min}$. We find point $x_{\min}^1$ by inserting plain $x_1 = x_{1\mathrm{mim}}$ into $V(x)$, putting the gradient equal to zero (25), and solving the set of equations describing each coordinate

$$\nabla V\left(x\right) = 0. \tag{25}$$

Similarly, we find point $x_{\min}^2$ on plain $x_2 = x_{2\min}$. Coordinate x_1 of point $x_{\min}^2$ lies outside the I_1 interval; thus the domain of attraction border is

$$V\left(x\right) = V\left(x_{\min}^1\right) => V\left(x\right) - 6.1 = 0. \tag{26}$$

The estimated domain of attraction and phase portraits of each state combination are displayed in Fig. 7 (further figures given in an online supplement).

2) Multilevel Topology: Similarly, we derive the autonomous model (27) from (2), (3), (4), and (8), and shifting the operating point (9) to the origin (20)

$$\dot{\boldsymbol{x}} = \begin{bmatrix} \frac{-r_L - V_i k_{ip}}{L} & \frac{-k_{ip}k_{vp}V_i - 1}{L} & \frac{k_{ip}k_{vi}V_i}{L} & \frac{V_i}{L}k_{ii} \\ \frac{1}{C} & \frac{1}{C}\frac{p_{\mathrm{CPL}}}{V_{o0}}f_1 - \frac{1}{C}\frac{1}{R_o} & 0 & 0 \\ 0 & -1 & 0 & 0 \\ -1 & -k_{vp} & k_{vi} & 0 \end{bmatrix} \cdot \boldsymbol{x}. \tag{27}$$

$$\dot{\boldsymbol{x}} = \begin{bmatrix} \frac{-r_L - k_{ip}f_2}{L} & \frac{-1 + k_{ii}Y_{20} - k_{vp}k_{ip}f_2}{L} & \frac{k_{vi}k_{ip}f_2}{L} & \frac{k_{ii}f_2}{L} \\ \frac{1 + k_{ip}f_1 - k_{ii}Y_{20} + k_{ip}I_{\mathrm{L0}}}{C} & \frac{k_{vp}k_{ip}f_1 + k_{vp}k_{ip}I_{\mathrm{L0}}}{C} - \frac{1}{CR_o} + \frac{p_{\mathrm{CPL}}}{CV_{o0}f_3} & \frac{-k_{vi}k_{ip}f_1 - k_{vi}k_{ip}I_{\mathrm{L0}}}{C} & \frac{-k_{ii}f_1 - k_{ii}I_{\mathrm{L0}}}{C} \\ 0 & -1 & 0 & 0 \\ -1 & -k_{vp} & k_{vi} & 0 \end{bmatrix} \cdot \boldsymbol{x}. \tag{19}$$

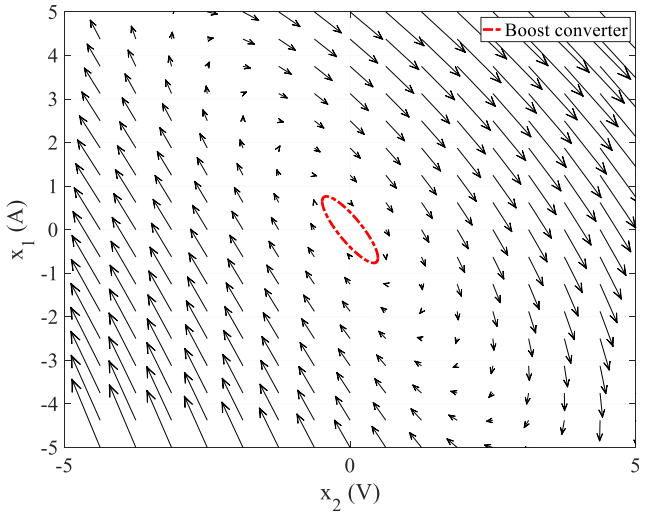

Fig. 7. Boost converter: domain of attraction (red line) and phase portrait of x_1, x_2 state combination around the origin ($x_3 = 0$ and $x_4 = 0$).

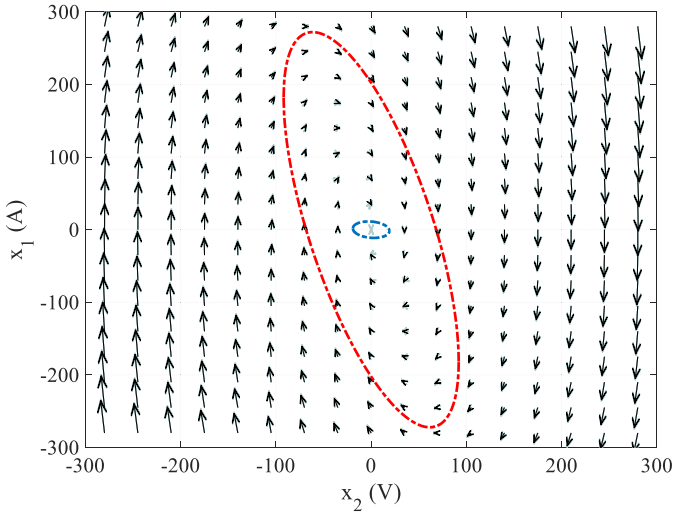

Fig. 8. Multilevel topology: domain of attraction comparison of different output-filter capacitors: $C = 168$ µF (red) and $C = 6.8$ µF (blue). Phase portrait of x_1, x_2 state combination plotted only for output filter capacitor C = 168 µF, and $x_3 = 0$, $x_4 = 0$.

The model (27) has one nonlinearity ($q = 1$), and therefore there are $r = 2^1 = 2$ rules, thus two linear models

$$\dot{\mathbf{x}} = [\boldsymbol{F}_i(x_2)\, \boldsymbol{A}_i(x_2)] \cdot \boldsymbol{x} \tag{28}$$

with

$$f_1 = \frac{1}{x_2 + V_{o0}}. \tag{29}$$

The LMI problem (17) can be formulated as

$$\begin{aligned} &\boldsymbol{P} = \boldsymbol{P}^T > 0 \\ &\boldsymbol{A}(x_{2\min})^T \cdot \boldsymbol{P} + \boldsymbol{P} \cdot \boldsymbol{A}(x_{2\min}) < 0 \\ &\boldsymbol{A}(x_{2\max})^T \cdot \boldsymbol{P} + \boldsymbol{P} \cdot \boldsymbol{A}(x_{2\max}) < 0 \end{aligned} \tag{30}$$

where the matrix function $\boldsymbol{A}$ is obtained by replacing nonlinearity f_1 with its minimal and maximal values. Estimation of the largest possible domain of attraction is an optimization task searching for the largest interval $I_2 = [x_{2\min}\ x_{2\max}]$ which provides Hurwitz matrix A and a feasible solution of LMI (30). A MATLAB program has been developed with model parameters given in Table II. Solving LMI (30) and searching for the largest interval I_1, we obtained a positive definite matrix

$$P = \begin{bmatrix} 1.12 & 2.21 & -533.18 & -85.10 \\ 2.21 & 4.63 & -3.95 \cdot 10^3 & -5.13 \cdot 10^3 \\ -533.18 & -3.95 \cdot 10^3 & 3.22 \cdot 10^7 & -1.33 \cdot 10^7 \\ -85.10 & -5.13 \cdot 10^3 & -1.33 \cdot 10^7 & 1.07 \cdot 10^7 \end{bmatrix}. \tag{31}$$

For the x_2 interval $I_2 = [-97.9\ 97.9]$. The Lyapunov quadratic function is obtained from (18). The border of the attraction domain is obtained by (18) with a point lying on the border.

Unlike the boost converter analysis, there is just one possible point $x^1_{\min}$ which is a point of tangency of the Lyapunov function $V(x)$ and plain $x_2 = x_{2\min}$ per

$$V(x) = V\left(x^1_{\min}\right) => V(x) - 45633.2 = 0. \tag{32}$$

The large signal stability of the proposed multilevel system is in Fig. 8. The multilevel topology exhibits a significantly larger domain of attraction compared to the boost converter.

C. Filter Size Reduction

Proper filter design guarantees system stability with sufficient domain of attraction. Both filter components, the filtering inductor and the output capacitor, directly affect the stability region. Increasing the output capacitance increases the stability, whereas increasing the inductor size destabilizes the system [60].

The large-signal stability analysis of the boost converter and the multilevel topology demonstrates a multiple times larger stability region of the proposed multilevel solution. The analysis considers the same output-capacitor size. Nevertheless, the multilevel topology does not require such a bulky output filter. Reducing the output-capacitor size, we find a positive definite matrix P as

$$P = \begin{bmatrix} 11.66 & 1.03 & -202.45 & -286.32 \\ 1.03 & 4.02 & -713.02 & -9.82 \cdot 10^3 \\ -202.45 & -713.02 & 5.73 \cdot 10^7 & -2.15 \cdot 10^7 \\ -286.32 & -9.82 \cdot 10^3 & -2.15 \cdot 10^7 & 4.15 \cdot 10^7 \end{bmatrix} \tag{33}$$

for an output capacitance C = 6.8 µF and $I_2 = [-40.2\ 40.2]$. The corresponding border of the domain of attraction

$$V(x) - 1462.7 = 0 \tag{34}$$

is compared to the boost converter solution implementing an output capacitor $C = 168$ µF (see Fig. 8, further plots in the online supplement).

The multilevel topology exhibits a significantly larger domain of attraction compared to the reference boost converter, with the output capacitor reduced by a factor of 24.

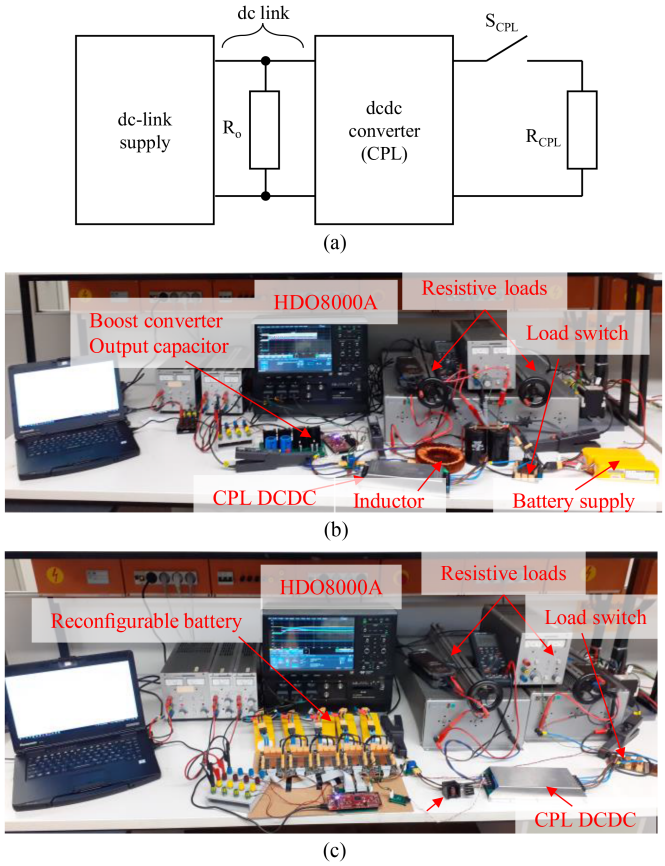

Fig. 9. Experimental setup to evaluate stability. (a) Block diagram. (b) Reference boost converter. (c) reconfigurable battery.

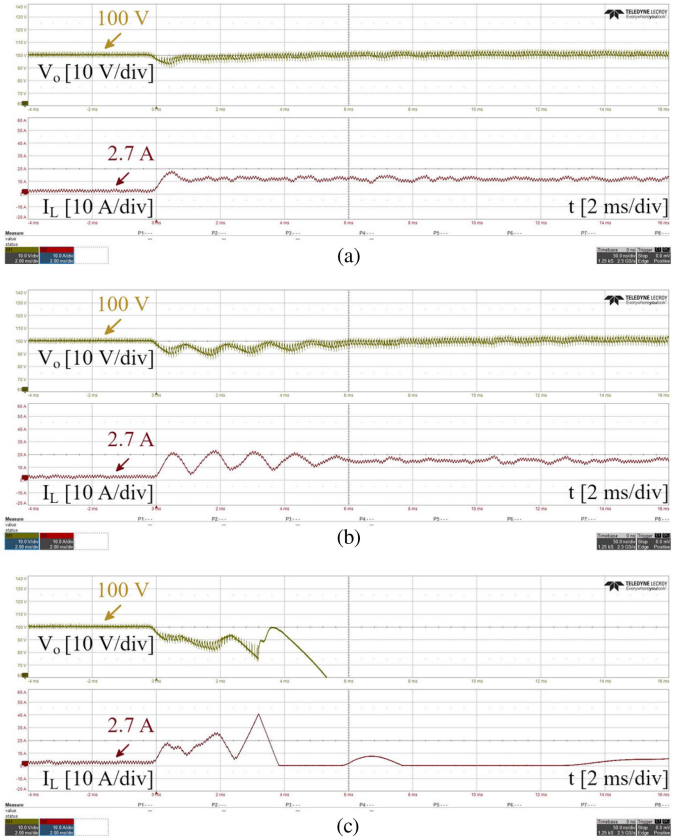

Fig. 10. Step response of the boost converter ($L = 799$ µH and $C = 168$ µF) constantly loaded by $R_{load} = 100\ \Omega$ and constant-power load steps of (a) $P_{CPL} = 350$ W. (b) $P_{CPL} = 450$ W, and (c) $P_{CPL} = 550$ W, instability and diverting voltage clearly visible. Scaling of the voltage plots 10 V/div, current plots 10 A/div, time scale 2 ms/div.

V. Experimental Results

A. Experimental Setup

We developed an experimental reference setup implementing a boost converter and a setup implementing the proposed reconfigurable topology. Both setups are supplied from multiple 24 V, 6200 mAh, 40 C battery packs (Zippy Technology Corp., Taiwan).

We loaded both setups with a resistor $R_o = 100\ \Omega$ and a dc–dc load converter CFB600W-110S (Cincon, Taiwan) with an input voltage range of 43 to 160 V, 48 V output voltage, 600 W output power and 500 µs settling time. The dc–dc load converter is operated in a constant-output-voltage mode and is loaded by a resistor R_{CPL}, which determines the output power. In such a configuration, the dc–dc load converter consumes a constant power from the input's perspective. Further, we equipped the output circuit with a semiconductor switch IPT015N10N5 (Infineon, Germany) to generate sharp load steps [see Fig. 9(a)].

For both setups, we developed the control algorithm in C and implemented it on a TMS320F28379D (Texas Instruments, TX, USA). The current feedback is based on the current transducer LES 15-NP (LEM, Switzerland) and the voltage feedback on TLC2272 (Texas Instruments, USA).

The reference setup comprises a 48 V battery pack (12s2p), a boost converter of 650 V, 40 A transistors IKW40N65H5 (Infineon, Germany), a custom filtering inductor 799 µH wound on a Kool Mµ core 77336A7 (Magnetics, USA PA), and 168 µF of three electrolytic output capacitors EKXJ201ELL560MJ25S (United Chemi-Con, IL, USA) [see Fig. 9(b)]. The control algorithm contains an inner current loop and an outer voltage loop (see Fig. 2).

The second setup evaluates a reconfigurable battery of five modules, each with a 24 V battery and a three-switch power electronic topology implementing IPT015N10N5 (Infineon, Germany). The output filter uses a 47 µH inductor 7443783533470 (Wuerth, Germany) and a 6.8 µF output capacitor 672D685H150CG5C (Vishay, PA USA) [see Fig. 9(c)]. Like in the reference setup control algorithm, there is an inner current and an outer voltage loop [see Fig. 3(a)].

We used a 12-bit oscilloscope HDO8000A (Teledyne Lecroy, NY, USA), wide-bandwidth differential probes HVD3206A (Teledyne Lecroy, NY, USA), and current clamps P01120043A (Chauvin Arnoux, France) for all measurements, including the dc-link voltage, the voltage across load resistor R_{CPL}, current flowing through load resistor R_{CPL}, and the inductor current.

B. Test Procedure

The test procedure is the same for each setup. We operate the setup at the nominal operating voltage $V_o = 100$ V and load

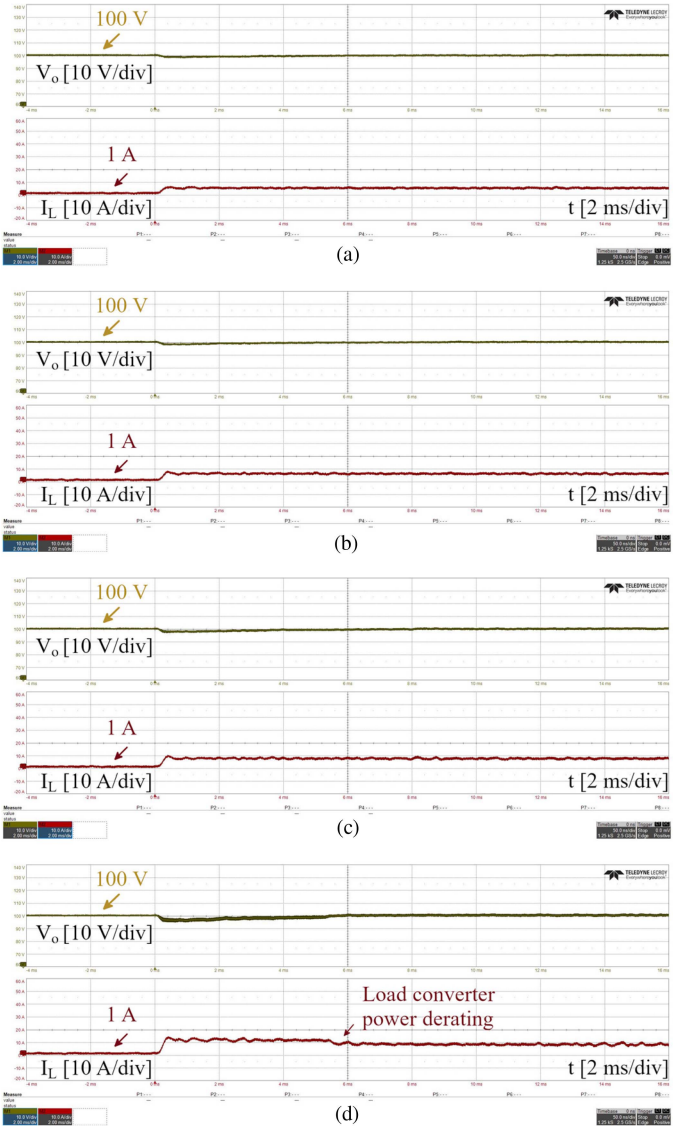

Fig. 11. Step response of the reconfigurable multilevel battery topology ($L = 47$ μH and $C = 168$ μF) constantly loaded by $R_{\text{load}} = 100\ \Omega$ and constant-power load steps of (a) $P_{\text{CPL}} = 350$ W, (b) $P_{\text{CPL}} = 450$ W, (c) $P_{\text{CPL}} = 550$ W, and (d) $P_{\text{CPL}} = 850$ W. Scaling of the voltage plots 10 V/div, current plots 10 A/div, time scale 2 ms/div.

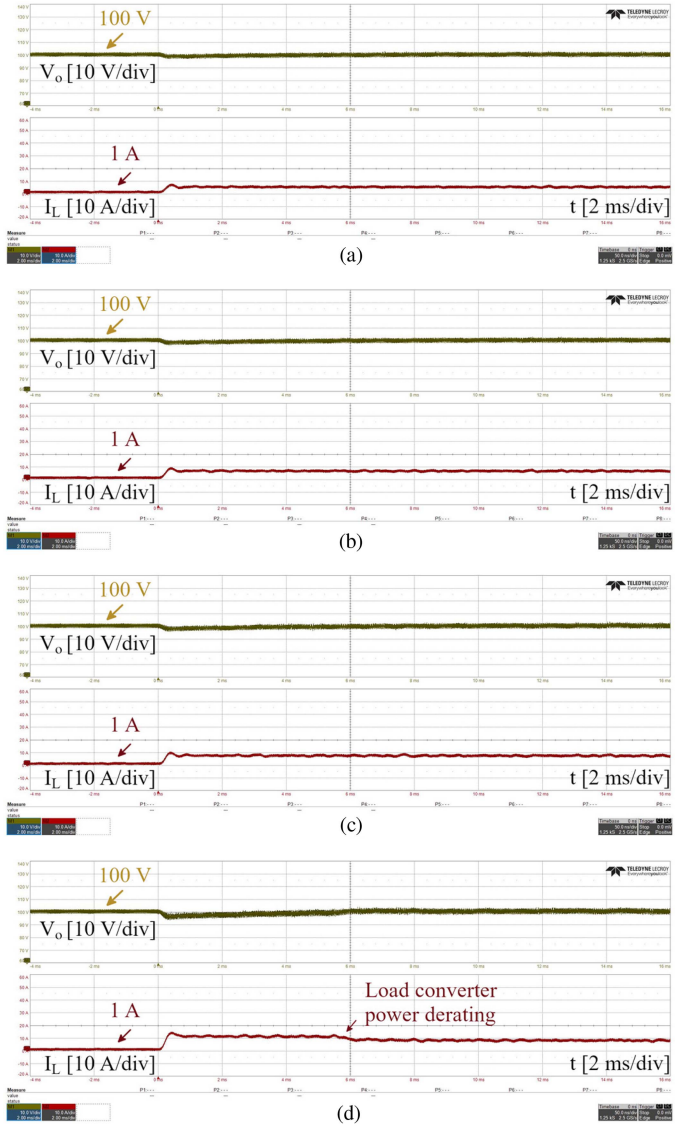

Fig. 12. Step response of the reconfigurable multilevel battery topology ($L = 47$ μH and $C = 6.8$ μF) constantly loaded by $R_{\text{load}} = 100\ \Omega$ and constant-power load steps of (a) $P_{CPL} = 350$ W, (b) $P_{\text{CPL}} = 450$ W, (c) $P_{\text{CPL}} = 550$ W, and (d) $P_{\text{CPL}} = 850$ W. Scaling of the voltage plots 10 V/div, current plots 10 A/div, time scale 2 ms/div.

the dc link with: the resistor $R_o = 100\ \Omega$ resulting in 100 W resistive load; and the dc–dc converter with no load (S_{CPL} is OFF). We set the output power of the dc–dc by setting resistor R_{CPL} according to

$$P_{\text{CPL}} \approx \frac{(48\ \text{V})^2}{R_{\text{CPL}}}. \tag{35}$$

Switching S_{CPL} ON generates load step of defined power with constant-power load characteristic, which evaluates stability of the dc-link supply.

We set the over-current protection of the converter to 40 A and the over-voltage protection to 140 V in the control algorithm. Upon exceeding these values, the controller turns all PWM outputs OFF, driving the system to the passive state.

We run three tests: evaluate the stability of the boost converter ($L = 799$ μH and $C = 168$ μF); evaluate the stability of the reconfigurable battery with the same output capacitor ($L = 47$ μH and $C = 168$ μF); evaluate the stability of the reconfigurable battery with reduced output capacitor ($L = 47$ μH and $C = 6.8$ μF).

C. Results

We experimentally tested both systems in response to CPL under load steps P_{CPL}: 350; 450; 550; and 850 W. The boost converter became unstable at load step $P_{\text{CPL}} = 550$ W and higher, triggering the over-current protection (see Fig. 10). The proposed reconfigurable topology with equivalent output capacitor was perfectly stable under all the tested load steps. Furthermore, the output voltage exhibits significantly higher output voltage

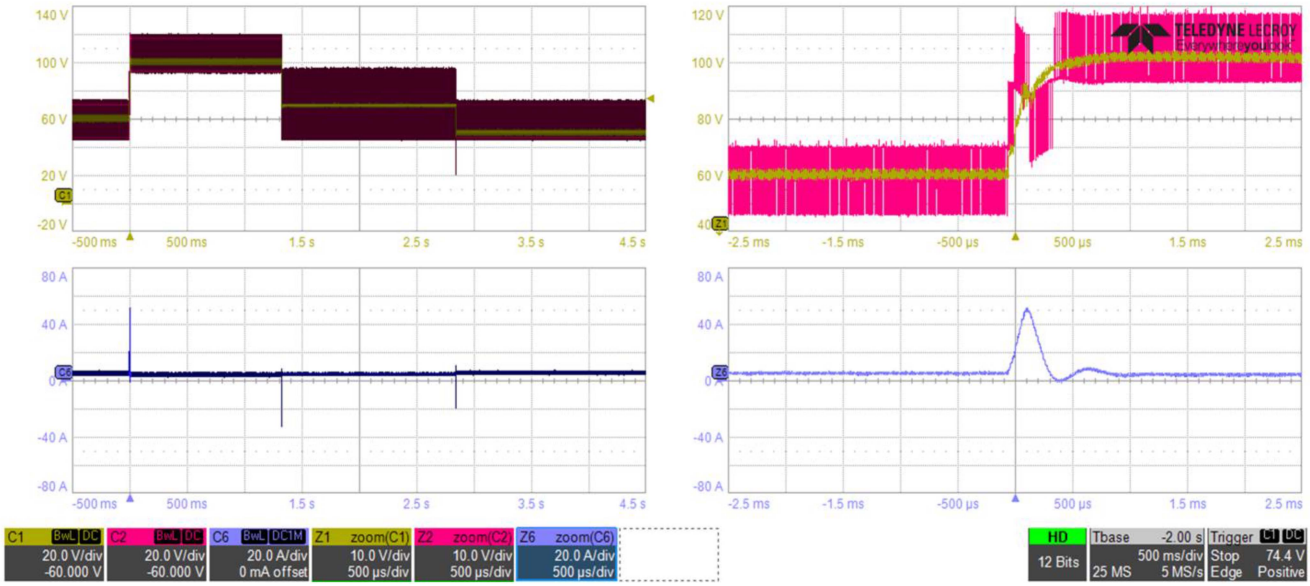

Fig. 13. Profile of the dc-link voltage generated by the multilevel converter ($L = 47$ µH and $C = 6.8$ µF) continuously loaded by $R_{\rm load} = 100\ \Omega$ and constant power load $P_{\rm CPL} = 200$ W. Oscillograms on the left side display dc-link voltage $V_{\rm o}$, modulated battery terminal voltage $V_{\rm bat}$, and inductor current I_L. The output voltage profile comprises the following transitions: 60 V $\rightarrow$ 100 V $\rightarrow$ 70 V $\rightarrow$ 50 V. Oscillograms on the right-side display details of the transient from 60 to 100 V. Scaling of voltage plots is 20 V/div; of current plot 20 A/div, the time scale is 500 ms/div (left-side oscillograms) and 500 µs/div (right-side oscillograms).

quality compared to the boost converter (see Fig. 11). Finally, we reduced the output filter of the reconfigurable battery to 6.8 µF and we observed no stability issues (see Fig. 12).

In addition to the stability comparison, we evaluated the variable output voltage feature of the reconfigurable battery. We generated an output voltage profile with multiple output voltage transients (see Fig. 13)

VI. Conclusion

In this article, we propose a reconfigurable battery converter to replace the conventional variable voltage powertrain of a hard-wired battery pack and bidirectional dc–dc to increase energy efficiency, reduce dc-link filter size, improve stability, and extend battery charging capability.

The proposed powertrain system modularizes the battery and implements a dynamically reconfigurable framework providing active balancing of battery modules. We setup a statistical model and evaluated capacity gain and benefits of modularisation. Breaking long hard-wired series-connected battery strings into shorter segments reduces the average capacity drop. The higher energy efficiency and balancing ability of the system allow implementation of cheaper, lower quality, or second-life cells.

Multilevel output voltage in combination with a proper control strategy interleaving and phase-shifting module operation guaranties high output voltage quality and significantly simplifies the dc-link filter design. The buck-converter character of the reconfigurable battery further increases stability of the powertrain.

We designed a reference powertrain system implementing the boost converter, set the same switching rate, tuned both systems up to the same speed matching their step responses and evaluated the large-signal stability including the domain of attraction. The proposed powertrain system exhibits a multiple times larger domain of attraction compared to the reference system.

Further, we built two experimental setups: the reference boost converter and the proposed reconfigurable system. We experimentally evaluated the stability of both systems under mixed load conditions by load steps at nominal output voltage. The reference boost converter became unstable at a load step of $P_{\rm CPL} = 550$ W. The proposed reconfigurable system implementing the same output capacitor was stable across the entire test range of $0 \leq P_{\rm CPL} \leq 850$ W.

Finally, we reduced the output capacitor of the reconfigurable battery by a factor of 24 and evaluated the stability. The system output voltage quality matched the output quality of the reference boost converter, but was perfectly stable across the entire test range of $0 \leq P_{\rm CPL} \leq 850$ W.

In the experimental setup, we manage to reduce the inductor a size by factor of 17 and the capacitor size by a factor of 24 and to significantly increase the stability compared to the reference system implementing a boost converter.

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