DC-Link Capacitance Reduction in PFC Rectifiers Employing PI+Notch Voltage Controllers

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***Abstract*—It is well-known that adding a notch filter in series with the typically employed type-II (or PI) regulator allows improving the tradeoff between dc-link voltage dynamics and grid-side current total harmonic distortion (THD) in practical single-phase power factor correction rectifiers. The article demonstrates that notch filter utilization alternatively allows reducing the value of dc-link capacitance in case hold-up time requirement is absent. The revealed value of minimum capacitance is expressed by explicit function of possible mains frequency values range, maximum expected grid voltage magnitude, rated system power, dc-link voltage set point, maximum tolerable grid-side current THD, and the desired phase margin (PM) of dc-link voltage loop. It is demonstrated that the proposed approach yields fourfold reduction of dc-link capacitance for typical values of 5% tolerable grid-side current THD under 40° PM constraint. Experimental results exhibit close-fitting resemblance to corresponding analytical predictions, verifying the proposed methodology.**

***Index Terms*—DC-link capacitance, PI+Notch controller, power factor correction, total harmonic distortion (THD), transient response.**

NOMENCLATURE

THD	Total harmonic distortion.
PFCR	Power factor correction rectifier.
PI	Proportional integrative.
PM	Phase margin.
LIC	Load interfacing converter.
RMS	Root mean square.

I. INTRODUCTION

CONSTANT growth of industrial and consumer electronics is putting more and more stress on the power grid, imposing strict constraints on the power quality [1], [2]. In order to respect modern grid codes in general and reduce THD in particular, active power factor correction techniques are widely used in off-grid power conversion systems. Various single-phase converter topologies can be used for this purpose [3], [4], [5], [6], [7], [8], all requiring a short-time energy storage component (typically a large electrolytic capacitor connected across dc-link terminals) to deal with instantaneous power mismatch and deliver hold-up energy when needed [9]. In case hold-up ability is necessary in certain application and/or steady-state dc-link voltage ripple magnitude is restricted, the value of dc-link capacitance is determined by the amount of necessary hold-up energy and/or allowed steady-state dc-link voltage swing [10], [11]. However, if hold-up requirement and dc-link magnitude restrictions are absent, the value of dc-link capacitance is dictated by instantaneous power mismatch (in both transient [12] and steady-state [13] regimes), which are typically less demanding. Therefore, the value of dc-link capacitance may (and should) be reduced in such cases in order to increase reliability (by decreasing the number of parallel-connected devices or employing nonelectrolytic capacitors) and reduce the cost and physical size of the power conversion system [14], [15], [16]. Research in this direction is mainly carried out either by finding a compromise between grid-side power quality and the minimum possible capacitance [17], [18], [19], [20] or by active capacitance reduction [21], [22], [23]. The former group of works makes use of the fact that power quality standards typically limit the magnitude of specific harmonics rather than THD by allowing respective harmonic content to be present in mains-side current by means of additional circuitry and/or algorithm. On the other hand, the latter group of works utilizes an additional auxiliary bidirectional power converter to decouple the short-time energy storage and the DC bus. Both groups may potentially attain lower dc-link capacitance than the methodology proposed in this article yet require nonconventional or additional circuitry.

In order to examine a novel approach for dc-link capacitance reduction, the value of minimum attainable capacitance has been determined first for existing methodologies such as single-phase inverters with active power decoupling [24], three-phase inverters for photovoltaic systems [25], single-phase PFCRs employing line waveform shaping control [21], and single-phase PFCRs without hold-up ability requirement [26], operating in steady-state only. Recently, Strajnikov and Kuperman [27] have generalized the work in [26] by providing analytical expression for the minimum attainable dc-link capacitance in single-phase PFCRs employing classical PI (or type-II) voltage compensators [9] taking into account both steady-state and transient operation regimes. On the other hand, it was demonstrated in [28] that adding a notch filter in series with the typically employed PI (or type-II) voltage compensator allows improving dc-link voltage

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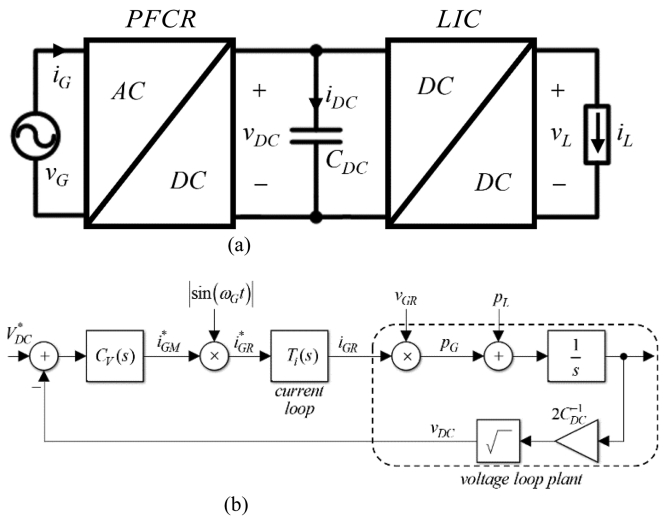

Fig. 1. Dual-stage grid-connected ac/dc power conversion system [12]. (a) Generalized topology. (b) Voltage loop structure.

dynamics without sacrificing grid-side current THD by increasing the voltage loop bandwidth. Based on this outcome, the article proposes to utilize the voltage loop bandwidth increase for dc-link capacitance reduction rather than for dc-link voltage dynamics enhancement (yet preserving the allowed dc-link voltage swing at all time). An analytical formulae for minimum dc-link capacitance is revealed, expressed by an explicit function of nominal mains frequency and corresponding uncertainty, maximum expected grid voltage magnitude, rated PFCR power, dc-link voltage set point, maximum tolerable grid-side current THD, and the desired dc-link voltage loop PM. Moreover, guidelines for systematic tuning of PI+Notch controller coefficients are provided and validated. It is shown that significant reduction of dc-link capacitance may be attained by utilizing PI+Notch controller instead of classical pure PI regulator. On the other hand, the following disadvantages of the proposed methodology must be emphasized.

1) Reduced dc-link capacitance implies increased dc-link ripple, which may not be tolerated in certain applications.
2) Increased dc-link voltage swing implies increased components' voltage stress and losses.

II. Power Balance in PFCR-Based System

A typical dual-stage PFCR-based grid-connected energy conversion system is shown in Fig. 1(a), consisting of grid-interfacing PFCR, bulk dc-link capacitance $C_{\rm DC}$, and load-interfacing dc–dc converter (LIC). Boost-topology PFCR under dual-loop dc-link voltage / grid-side current control is employed, where the energy balance is attained by regulating the average value of dc-link voltage to a set point $V^*_{\rm DC}$ using a voltage regulator $C_V(s)$, processing the dc-link voltage error to obtain the set point value of grid-side current magnitude $i^*_{GM}(t)$ [cf. Fig. 1(b)]. The latter is then multiplied by rectified unity-grid-voltage template $v^{-1}_{GM}(t)v_G(t)$ with $v_{GM}(t)$ denoting the magnitude of mains voltage $v_G(t)$ to form the rectified grid-side current reference $i^*_{GR}(t)$, tracked by the current loop. Typically, current loop is completely decoupled from the voltage loop in frequency domain, and may therefore be represented by complementary sensitivity function

$$T_i(s) \approx 1 \tag{1}$$

within the voltage loop bandwidth [29].

In practice, grid-side PFCR voltage and current are given by the following:

$$v_G(t) = v_{GM}(t)\sin(\omega_G t) + \underbrace{\sum\nolimits_{n>1} v_n(t)\sin(n\omega_G t)}_{\phi_v(t)}[\rm V] \tag{2}$$

and

$$i_G(t) = i_{GM}(t)\sin(\omega_G t) + \underbrace{\sum\nolimits_{n>1} i_n(t)\sin(n\omega_G t)}_{\phi_i(t)}[\rm A] \tag{3}$$

respectively, where ω_G [rad/s] signifies grid frequency, $v_{GM}(t)$, $i_{GM}(t)$ represent slow-varying first-harmonic voltage and current magnitudes, respectively [with $i_{GR}(t) = |i_G(t)|$ and $v_{GR}(t) = |v_G(t)|$ in Fig. 1(b)], and $\phi_v(t), \phi_i(t)$ denote corresponding residual harmonic content satisfying [27]

$$\sqrt{\textstyle\sum_{n>1} V_n^2} << V_{GM},\ \sqrt{\textstyle\sum_{n>1} I_n^2} << I_{GM} \tag{4}$$

with V_{GM}, I_{GM}, V_n, and I_n indicating steady-state values of $v_{GM}(t)$, $i_{GM}(t)$, $v_n(t)$, and $i_n(t)$, respectively. Obviously, in order to allow correct boost-topology PFCR operation

$$v_{\rm DC}(t) \geq v_{GR}(t) \tag{5}$$

must hold at all time. Instantaneous grid-side power is then given by the following:

$$p_G(t) = v_G(t)i_G(t) = p_{GM}(t) + \Delta p_G(t) + \phi_p(t)[\rm W] \tag{6}$$

with

$$\begin{aligned} p_{GM}(t) &= 0.5 v_{GM}(t) i_{GM}(t),\ \Delta p_G(t) = -p_{GM}(t)\cos(2\omega_G t)\,, \\ \phi_p(t) &= \phi_v(t) i_{GM}(t)\sin(\omega_G t) + \phi_i(t) v_{GM}(t)\sin(\omega_G t) \\ &\quad + \phi_v(t)\phi_i(t). \end{aligned} \tag{7}$$

Taking into account load-side terminals instantaneous power $p_L(t) = v_L(t)i_L(t)$ [W], there is [cf. Fig. 1(a)]

$$\begin{aligned} p_{\rm DC}(t) &= v_{\rm DC}(t) i_{\rm DC}(t) \\ &= p_{GM}(t)\eta_G + p_L(t)\eta_L^{-1} \\ &\quad + \Delta p_G(t)\eta_G + \phi_p(t)\eta_G \end{aligned} \tag{8}$$

where η_G and η_L symbolize PFCR and LIC efficiencies, respectively. According to (4), RMS values of residual harmonic components are significantly lower than of low-frequency power components in (6). Thus, the influence of $\phi_p(t)$ is disregarded further down.

III. Steady-State Performance

In steady state, $p_L(t)$ and $p_{GM}(t)$ are constant, i.e., power balance yields [cf. (7)]

$$P_{GM}\eta_G + P_L\eta_L^{-1} = 0 \Rightarrow I_{GM} = \frac{2\eta_L^{-1}\eta_G^{-1}P_L}{V_{GM}} \tag{9}$$

with P_{GM} and P_L indicating steady-state value of $p_{GM}(t)$ and $p_L(t)$, respectively. Corresponding steady-state instantaneous dc-link voltage is then given by the following [12]:

$$v_{\rm DC}^{ss}(t) = V_{{\rm DC},rms}^{*}\sqrt{1-\frac{\eta_S^{-1}\eta_G^{-1}P_L}{\omega_G\left(V_{{\rm DC},rms}^{*}\right)^2 C_{\rm DC}}\sin\left(2\omega_G t\right)} \tag{10}$$

with

$$V_{\rm DC,rms}^{*} \approx V_{\rm DC}^{*}\sqrt{1+\left(\frac{\eta_S^{-1}\eta_G^{-1}P_L}{2\sqrt{2}\omega_G C_{\rm DC}\left(V_{\rm DC}^{*}\right)^2}\right)^2}. \tag{11}$$

In should be emphasized that if steady-state operation only is assumed, then (5) is simplified as follows:

$$v_{DC}^{ss}(t) \geq v_{GR}(t) \tag{12}$$

to allow correct boost-topology PFCR operation. Substituting (2) and (10) into (12) and solving yields minimized dc-link capacitance value given by the following [26]:

$$C_{\rm DC,min} = \frac{\eta_S^{-1}\eta_G^{-1}P_L}{\omega_G V_{\rm DC,rms}^{*}}\frac{1}{\sqrt{\left(V_{\rm DC,rms}^{*}\right)^2 - V_{GM,\max}^2}} \tag{13}$$

with $V_{GM,\max}$ denoting maximum expectable value of grid voltage magnitude. Unfortunately, if substantial load transients are projected, minimum required dc-link capacitance value would be significantly underestimated by (13) [27]. DC-link voltage expression (10) may be further approximated as follows [29]:

$$\begin{aligned} v_{\rm DC}(t) &\approx V_{\rm DC}^{*} - \underbrace{\frac{\eta_S^{-1}\eta_G^{-1}P_L}{2\omega_G V_{\rm DC}^{*}C_{\rm DC}}\sin\left(2\omega_G t\right)}_{\Delta V_{\rm DC}} \\ &= V_{\rm DC}^{*}\underbrace{-\Delta V_{\rm DC}\sin\left(2\omega_G t\right)}_{\Delta v_{\rm DC}(t)} = V_{\rm DC}^{*} + \Delta v_{\rm DC}(t) \end{aligned} \tag{14}$$

since dc-link ripple magnitude $\Delta V_{\rm DC}$ is much lower than the set point $V_{\rm DC}^{*}$ in practice. Taking into account (1), (3), and (14) with Fig. 1(b), there is

$$i_{GM}(t) = I_{GM} + \Delta i_{GM}(t) = I_{GM}\underbrace{-\Delta I_{GM}\sin\left(2\omega_G t+\theta\right)}_{\Delta i_{GM}(t)} \tag{15}$$

with I_{GM} defined in (9) and

$$\Delta I_{GM} = \Delta V_{\rm DC}|C_V(2\omega_G)|, \theta = \measuredangle C_V(2\omega_G) \tag{16}$$

so that $\Delta I_{GM} << I_{GM}$ [9]. Steady-state grid-side current is hence given by the following [cf. Fig. 1(b)]:

$$\begin{aligned} i_G(t) &= i_{GM}(t)\sin\left(\omega_G t\right) \\ &\cong I_{GM}\sin\left(\omega_G t\right) + \frac{\Delta I_{GM}}{2}\cos\left(3\omega_G t+\theta\right) \end{aligned} \tag{17}$$

i.e., most of the THD is caused by the third harmonic (which is the one that usually has the highest limits from the standards). Grid-side current THD is then obtained as [cf. (13), (16)]

$$\text{THD} \cong \frac{1}{2}\frac{\Delta I_{GM}}{I_{GM}} = \frac{V_{GM}}{8\omega_G V_{\rm DC}^{*}C_{\rm DC}}\left|C_V(2\omega_G)\right|. \tag{18}$$

It is well-evident that THD may be suppressed by minimizing the gain of voltage regulator $C_V(s)$ at double-grid frequency by e.g., combining a notch filter centered on $\omega_f = 2\omega_G$ in series with the commonly used PI compensator, i.e.

$$C_V(s) = \underbrace{K\frac{\tau s+1}{s}}_{C_V^{PI}(s)}\underbrace{\frac{s^2+\omega_f^2}{s^2+2\xi_f\omega_f s+\omega_f^2}}_{C_V^{NF}(s)}. \tag{19}$$

Unfortunately, mains frequency ω_G seldom remains constant, varying within predetermined limits [30] so that notch and double-grid frequency are related as follows:

$$\omega_f = 2\alpha\omega_G \tag{20}$$

with $\alpha \in [\alpha_{\min} < 1, \alpha_{\max} > 1]$ denoting the deviation of the notch frequency from double-grid frequency with $\alpha = 1$ referred to as "nominal case." Considering (19) and (20), grid-side current THD in (18) becomes

$$\text{THD} \cong \frac{V_{GM}K\sqrt{\left(2\omega_G\tau\right)^2+1}}{16\omega_G^2 V_{\rm DC}^{*}C_{\rm DC}}\left(1+4\xi_f^2\frac{\alpha^2}{\left(\alpha^2-1\right)^2}\right)^{-0.5} \tag{21}$$

with

$$\alpha = \begin{cases} \alpha_{\min}, & \frac{\alpha_{\min}^2}{\left(\alpha_{\min}^2-1\right)^2} < \frac{\alpha_{\max}^2}{\left(\alpha_{\max}^2-1\right)^2} \\ \alpha_{\max}, & \frac{\alpha_{\min}^2}{\left(\alpha_{\min}^2-1\right)^2} > \frac{\alpha_{\max}^2}{\left(\alpha_{\max}^2-1\right)^2} \end{cases}. \tag{22}$$

According to (21), THD reduces (theoretically) to zero in the "nominal case" and increases when $\alpha \to \alpha_{\min}$ or $\alpha \to \alpha_{\max}$. On the other hand, the worst-case value of THD corresponds to one of the two boundary values of α as per (22).

IV. Worst-Case Transient Response

DC-link voltage dynamics (8) may be reformulated as follows:

$$\begin{aligned} C_{\rm DC}\dot{v}_{\rm DC}(t)v_{\rm DC}(t) \approx \\ 0.5\eta_G v_{GM}(t)i_{GM}(t) + \eta_L p_L(t) + \eta_G\Delta p_G(t). \end{aligned} \tag{23}$$

Linearizing (23) around operation point (9), assuming unity converters efficiencies for brevity and neglecting relatively small and non-frequent grid voltage magnitude variations results in

$$\begin{aligned} \frac{d\tilde{v}_{DC}(t)}{dt} &= \frac{1}{C_{DC}V_{DC}^{*}}\times \\ &\left(\frac{V_{GM}\tilde{i}_{GM}(t)+I_{GM}\tilde{v}_{GM}(t)}{2} - \tilde{p}_L(t) - \underbrace{\tilde{p}_{GM}(t)\cos\left(2\omega_G t\right)}_{\tilde{p}_{GM2}(t)}\right). \end{aligned} \tag{24}$$

The structure of linearized voltage loop is shown in Fig. 2.

Load power—to—dc-link voltage transfer function may be obtained from Fig. 2 as follows:

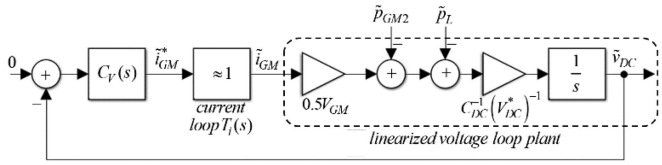

Fig. 2. Linearized dc-link voltage loop.

$$\left.\frac{\tilde{v}_{\rm DC}(s)}{\tilde{p}_L(s)}\right|_{\tilde{p}_{GM2}(s)=0} = \frac{G_n s\left(s^2+2\xi_f\omega_f s+\omega_f^2\right)}{s^4+\left(2\xi_f\omega_f+2\xi_n\omega_n\right)s^3+\left(\omega_f^2+\omega_n^2\right)s^2+2\xi_n\omega_n\omega_f^2 s+\omega_f^2\omega_n^2} \tag{25a}$$

with

$$G_n=\left(C_{\rm DC}V^*_{\rm DC}\right)^{-1},\ \omega_n=\sqrt{\frac{0.5KV_{GM}}{C_{\rm DC}V^*_{\rm DC}}},\ \xi_n=\omega_n\frac{\tau}{2}. \tag{25b}$$

In case damping factor of the Notch filter is small enough to satisfy

$$\xi_f << \min\left(\frac{1}{4\xi_n}\left(\frac{\omega_f}{\omega_n}+\frac{\omega_n}{\omega_f}\right),\xi_n\frac{\omega_f}{\omega_n}\right) \tag{26}$$

(25a) reduces to

$$\left.\frac{\tilde{v}_{\rm DC}(s)}{\tilde{p}_L(s)}\right|_{\tilde{p}_{GM2}(s)=0} \approx G_n\frac{s}{s^2+2\xi_n\omega_n s+\omega_n^2}. \tag{27}$$

Thus, load power step ΔP_L would impose dc-link voltage perturbation given by

$$\left|\tilde{v}_{\rm DC}(s)|_{\tilde{p}_{GM2}(s)=0}\right| = \Delta P_L\frac{G_n}{s^2+2\xi_n\omega_n s+\omega_n^2} \Rightarrow$$

$$\left|\tilde{v}_{\rm DC}(t)|_{\tilde{p}_{GM2}(t)=0}\right| = \frac{G_n\Delta P_L}{\omega_n\sqrt{1-\xi_n^2}}e^{-\xi_n\omega_n t}\sin\left(\omega_n\sqrt{1-\xi_n^2}t\right) \tag{28}$$

maximized at

$$t_p=\frac{1}{\omega_n\sqrt{1-\xi_n^2}}\tan^{-1}\left(\frac{\sqrt{1-\xi_n^2}}{\xi_n}\right) \tag{29}$$

as

$$\max\left|\tilde{v}_{\rm DC}(t)|_{\tilde{p}_{GM2}=0}\right| = \frac{G_n\Delta P_L}{\omega_n}e^{-\frac{\xi_n\cos^{-1}\xi_n}{\sqrt{1-\xi_n^2}}}. \tag{30}$$

Pulsating power component—to—dc-link voltage transfer function may be attained from Fig. 2 as follows:

$$\left.\frac{\tilde{v}_{\rm DC}(s)}{\tilde{p}_{GM2}(s)}\right|_{\tilde{p}_L(s)=0} = \left.\frac{\tilde{v}_{\rm DC}(s)}{\tilde{p}_L(s)}\right|_{\tilde{p}_{GM2}(s)=0}. \tag{31}$$

Due to the fact that $|C_V(2\omega_G)| << 1$, response to ripple component remains nearly unaffected by closed loop, i.e.

$$\left.\frac{\tilde{v}_{\rm DC}(s)}{\tilde{p}_{GM2}(s)}\right|_{\tilde{p}_L(s)=0} \approx \frac{G_n}{s} \Rightarrow \tag{32a}$$

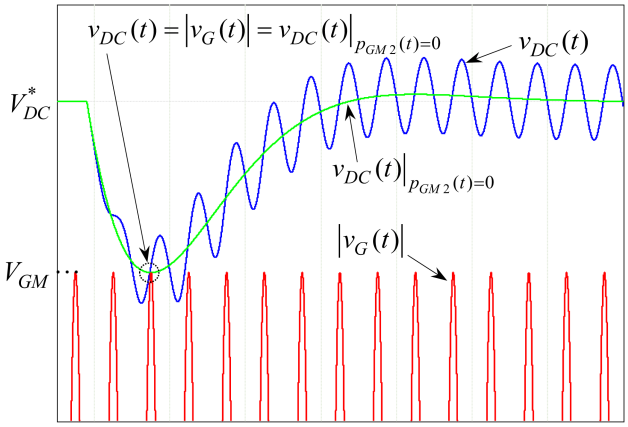

Fig. 3. Worst-case dc-link voltage response to a load power step.

$$\tilde{v}_{\rm DC}(t)|_{\tilde{p}_L(t)=0} \approx p_{GM}(t)\frac{G_n}{2\omega_G}\sin\left(2\omega_G t\right). \tag{32b}$$

Combining (30) and (32), overall dc-link voltage deviation is obtained as follows:

$$\begin{aligned}\tilde{v}_{\rm DC}(t) &\approx \tilde{v}_{\rm DC}(t)|_{\tilde{p}_{GM2}(t)=0}+\tilde{v}_{DC}(t)|_{\tilde{p}_L(t)=0}\\ &\approx \frac{\Delta P_L}{\omega_n V^*_{\rm DC}C_{\rm DC}\sqrt{1-\xi_n^2}}e^{-\xi_n\omega_n t}\sin\left(\omega_n\sqrt{1-\xi_n^2}t\right)\\ &\quad+\frac{p_{GM}(t)}{2\omega_G V^*_{\rm DC}C_{\rm DC}}\sin\left(2\omega_G t\right).\end{aligned} \tag{33}$$

DC-link voltage response to a zero-to-ΔP_L load power step is then given by the following:

$$v_{\rm DC}(t)=V^*_{\rm DC}-\tilde{v}_{\rm DC}(t). \tag{34}$$

On the other hand, recalling that (5) must hold while noticing that $p_{GM}(t_p)=\Delta P_L$, the worst case of (5) is given by the following [cf. (30)]:

$$\begin{aligned}V_{GM}&\left|\sin\left(\omega_G t\right)\right|\\ &= V^*_{\rm DC}-\frac{G_n\Delta P_L}{\omega_n}e^{-\frac{\xi_n\cos^{-1}\xi_n}{\sqrt{1-\xi_n^2}}}-\frac{\Delta P_L}{2\omega_G V^*_{\rm DC}C_{\rm DC}}\sin\left(2\omega_G t\right).\end{aligned} \tag{35}$$

Furthermore, rectified mains voltage is maximized when $\omega_G t$ is an integer multiple of $\pi/2$. At the same instant, $2\omega_G t$ is an integer multiple of π. Therefore

$$\left|\sin\left(\omega_G t=k\frac{\pi}{2}\right)\right|=1,\ \sin\left(2\omega_G t=k\pi\right)=0 \tag{36}$$

and (35) reduces to

$$V^*_{DC}-V_{GM}\le\frac{G_n\eta_S^{-1}\eta_G^{-1}\Delta P_L}{\omega_n}e^{-\frac{\xi_n\cos^{-1}\xi_n}{\sqrt{1-\xi_n^2}}}. \tag{37}$$

It may then be concluded that pulsating power component does not contribute to the worst-case scenario, as shown in Fig. 3.

V. Derivation of Minimum DC-Link Capacitance Value

Denoting the maximum allowed value of grid current THD as THD* while taking the boundary case of transient response

into account, two design equations are given by [cf. (21), (37)]

$$\frac{V_{GM}K\sqrt{(2\omega_G\tau)^2+1}}{16\omega_G^2 V_{\rm DC}^* C_{\rm DC}}\left(1+4\xi_f^2\frac{\alpha^2}{(\alpha^2-1)^2}\right)^{-0.5}={\rm THD}^*, \tag{38}$$

$$V_{\rm DC}^*-V_{GM}=\frac{G_n\eta_S^{-1}\eta_G^{-1}\Delta P_L}{\omega_n}e^{-\frac{\xi_n\cos^{-1}\xi_n}{\sqrt{1-\xi_n^2}}}. \tag{39}$$

According to Fig. 2, dc-link voltage loop gain is obtained as follows:

$$L(s)=\omega_n^2\frac{2\frac{\xi_n}{\omega_n}s+1}{s^2}\underbrace{\frac{s^2+(2\alpha\omega_G)^2}{s^2+4\xi_f\alpha\omega_G s+(2\alpha\omega_G)^2}}_{C_V^{NF}(s)}. \tag{40}$$

Signifying the crossover frequency of $L(s)$ as ω_c, phase and gain contribution of $C_V^{NF}(s)$ at ω_c are

$$\begin{aligned}\angle G_V^{NF}(\omega_c)&=-\tan^{-1}\left(2\xi_f\frac{\omega_f\omega_c}{\omega_f^2-\omega_c^2}\right)\\ \left|G_V^{NF}(\omega_c)\right|&=\sqrt{\frac{\left(\omega_f^2-\omega_c^2\right)^2}{\left(\omega_f^2-\omega_c^2\right)^2+(2\xi_f\omega_f\omega_c)^2}}\end{aligned} \tag{41}$$

respectively. Hence, in order to minimize the above contributions by keeping

$$\left|C_V^{NF}(\omega_c)\right|\approx 1, \angle C_V^{NF}(\omega_c)\approx 0. \tag{42}$$

ξ_f must obey

$$\xi_f << \frac{1}{2}\left(\frac{\omega_f}{\omega_c}-\frac{\omega_c}{\omega_f}\right). \tag{43}$$

Rewriting (43) as

$$\xi_f=\frac{1}{2}\beta\left(\frac{\omega_f}{\omega_c}-\frac{\omega_c}{\omega_f}\right) \tag{44}$$

and substituting into (41), there is

$$\begin{aligned}\angle G_V^{NF}(\omega_c)&=-\tan^{-1}(\beta)\approx-\beta,\quad \beta\ll 1\\ \left|G_V^{NF}(\omega_c)\right|&=\sqrt{\frac{1}{1+\beta^2}}\approx 1-\frac{\beta^2}{2},\ \beta\ll 1.\end{aligned} \tag{45}$$

For the value of $\beta=0.1$, phase and gain contributions of the Notch filter would be approximately –5° and 0.995, respectively. While gain contribution is minor and may be neglected, phase contribution may (if necessary) be offset by biasing the desired value of voltage loop phase margin. Denoting the latter as *PM* while analyzing (40) with (45) yields

$$\begin{aligned}|L(\omega_c)|&\cong\frac{\omega_n^2}{\omega_c^2}\sqrt{\left(2\xi_n\frac{\omega_c}{\omega_n}\right)^2+1}=1\\ \Rightarrow\omega_c&=\xi_n\omega_n\sqrt{2+2\sqrt{1+\frac{1}{4\xi_n^4}}},\\ \angle L(\omega_c)&\cong tg^{-1}\left(2\omega_c\frac{\xi_n}{\omega_n}\right)-\pi=-\pi+PM\end{aligned} \tag{46}$$

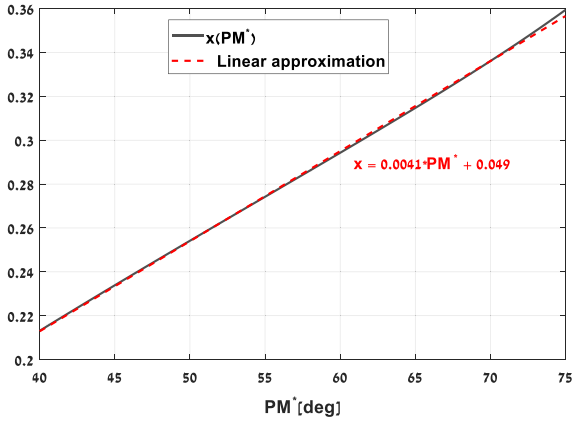

Fig. 4. Analytical relation of x in (51) versus PM* and linear approximation (52).

$$\Rightarrow\xi_n=\left(\frac{\left(\frac{tg(PM)}{2\sqrt{2}}\right)^4}{2\left(\frac{tg(PM)}{2\sqrt{2}}\right)^2+\frac{1}{4}}\right)^{\frac{1}{4}}. \tag{47}$$

In practical systems, desired values of phase margin are typically PM* $\geq 40°$ [28], hence the range $\xi_n\geq 0.327$ is of interest. Substituting (25b) into (38) and rearranging yields the following:

$$\omega_n=\sqrt{8}\omega_G\xi_n \times\left(\sqrt{1+\frac{1}{\xi_n^4}\left(1+4\xi_f^2\frac{\alpha^2}{(\alpha^2-1)^2}\right)({\rm THD}^*)^2}-1\right)^{0.5} \tag{48}$$

which may be further simplified considering practical parameter ranges of THD* <0.1, $0.98<\alpha<1.02$, $\xi_f<0.1$ as

$$\omega_n\cong 2\frac{\omega_G}{\xi_n}{\rm THD}^*\sqrt{1+4\xi_f^2\frac{\alpha^2}{(\alpha^2-1)^2}}. \tag{49}$$

Combining (49) with (39) yields the minimum dc-link capacitance value

$$C_{\rm DC,min}=\frac{\eta_S^{-1}\eta_G^{-1}\Delta P_L\left(1+\xi_f^2\frac{4\alpha^2}{(\alpha^2-1)^2}\right)^{-0.5}}{2\omega_G{\rm THD}^*V_{\rm DC}^*\left(V_{\rm DC}^*-V_{GM,\max}\right)}\xi_n e^{-\frac{\xi_n\cos^{-1}\xi_n}{\sqrt{1-\xi_n^2}}}. \tag{50}$$

Further denoting

$$x=\xi_n e^{-\frac{\xi_n\cos^{-1}\xi_n}{\sqrt{1-\xi_n^2}}} \tag{51}$$

combining with (47) and plotting versus PM* reveals the following linear approximation (cf. Fig. 4):

$$x\cong 0.0041\cdot{\rm PM}^*+0.049,\quad 40°\leq{\rm PM}^*\leq 75°. \tag{52}$$

Hence, (50) may be further simplified as follows:

$$C_{\rm DC,min}=\frac{0.5\eta_S^{-1}\eta_G^{-1}\Delta P_L(0.0041\cdot{\rm PM}^*+0.049)}{\omega_G{\rm THD}^*V_{\rm DC}^*\left(V_{\rm DC}^*-V_{GM,\max}\right)\sqrt{1+\xi_f^2\frac{4\alpha^2}{(\alpha^2-1)^2}}}. \tag{53}$$

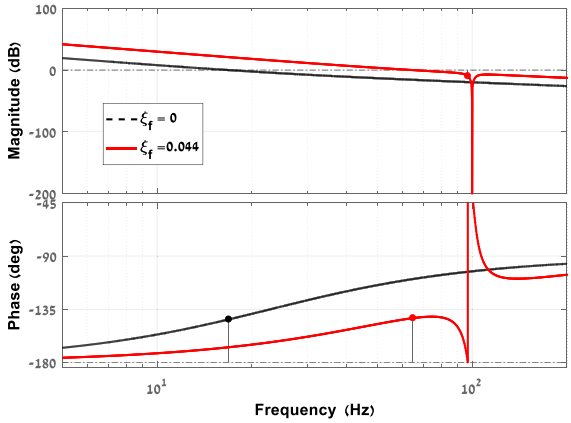

Fig. 5. Bode diagrams of the voltage loop gain.

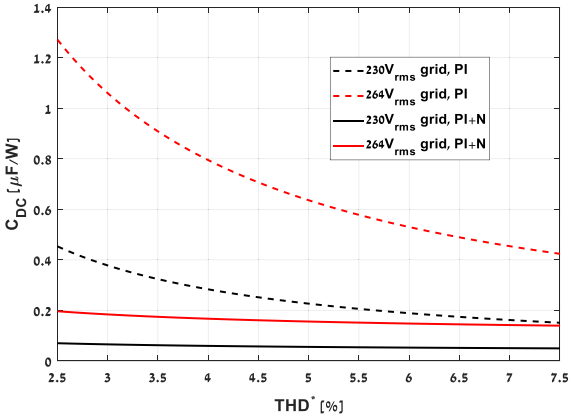

Fig. 6. Required amount of dc-link capacitance per watt loading versus THD* for two different values of grid voltage.

VI. Remarks

A. Controller Coefficients Tuning

It is interesting to emphasize that the minimum capacitance value (53) is independent of $C_V^{\mathrm{PI}}(s)$ coefficients, while the latter do depend on the dc-link capacitance value. Note that increasing ξ_f leads to minimum capacitance value reduction. However, it would also lead to increased phase and gain contribution of $C_V^{NF}(s)$ to $L(s)$ at ω_c. Hence, ξ_f must be determined first (using $\beta \approx 0.1$ in (44) seems a fair tradeoff), followed by obtaining K and τ. Combining (46) with (49) yields

$$\omega_c = \omega_y \sqrt{1 + z\xi_f^2} \tag{54}$$

with

$$\omega_y = 2\omega_G \mathrm{THD}^* \sqrt{2 + 2\sqrt{1 + \frac{1}{4\xi_n^4}}}, z = \frac{4\alpha^2}{(\alpha^2 - 1)^2}. \tag{55}$$

Merging (44) with (54) gives

$$\xi_f^4 + \frac{\frac{4}{\beta^2}\omega_f^2 + 2z\left(\omega_f^2 - \omega_y^2\right)}{z\left(\frac{4}{\beta^2}\omega_f^2 - z\omega_y^2\right)}\xi_f^2 - \frac{\left(\omega_f^2 - \omega_y^2\right)^2}{z\omega_y^2\left(\frac{4}{\beta^2}\omega_f^2 - z\omega_y^2\right)} = 0 \tag{56}$$

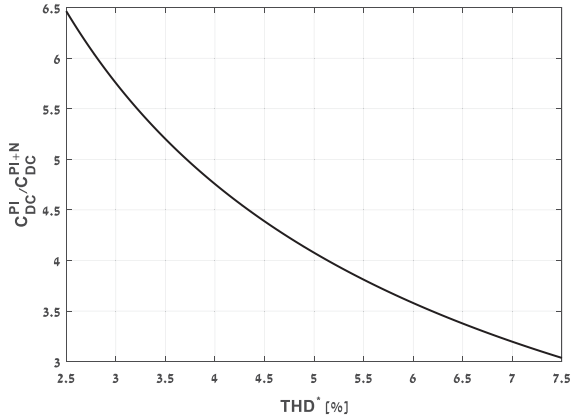

Fig. 7. DC-link capacitance reduction ratio versus THD*.

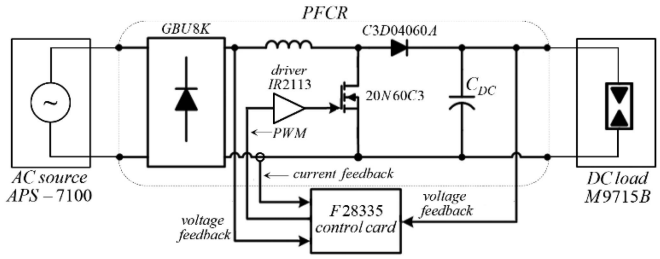

Fig. 8. Experimental setup schematic.

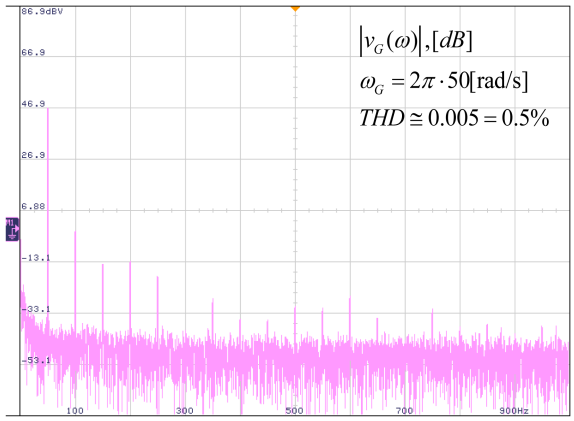

Fig. 9. Measured spectra and corresponding THD of ac source voltage.

i.e.

$$\xi_f = \sqrt{\frac{\sqrt{b^2 + 4c} - b}{2}} \tag{57}$$

with

$$b = \frac{\frac{4}{\beta^2}\omega_f^2 + 2z\left(\omega_f^2 - \omega_y^2\right)}{z\left(\frac{4}{\beta^2}\omega_f^2 - z\omega_y^2\right)}, c = \frac{\left(\omega_f^2 - \omega_y^2\right)^2}{z\omega_y^2\left(\frac{4}{\beta^2}\omega_f^2 - z\omega_y^2\right)}. \tag{58}$$

Hence, the proposed process of minimum capacitance value selection and coefficients tuning is as follows:

1) Initialize ω_G, $V_{GM,\max}$, a, THD* and V_{DC}^*.
2) Select β and set PM* taking into account (45).
3) Obtain ξ_n using (47).

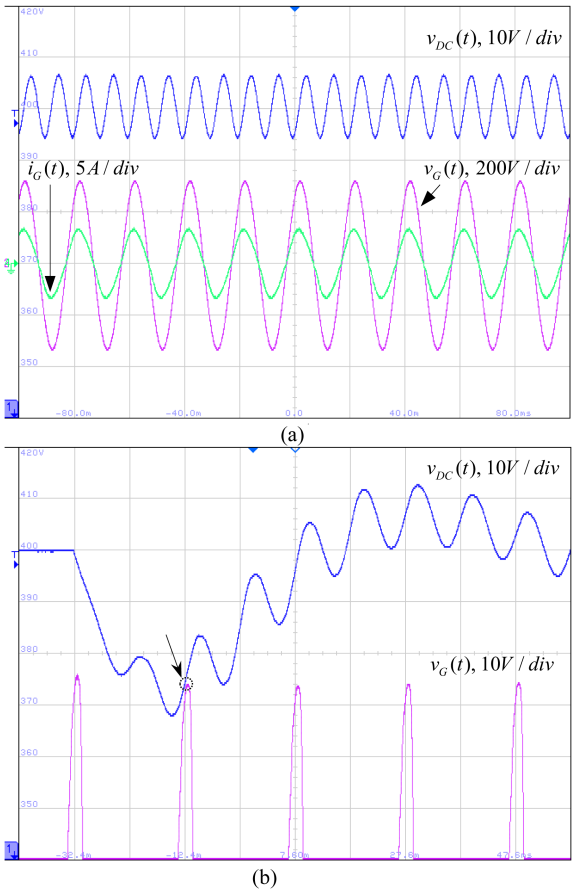

Fig. 10. Experimental results, PI controller, $\text{THD}^* = 5\%$. (a) Steady-state regime, $\text{THD}^* = 5\%$, $\text{THD} = 5.2\%$. (b) Transient regime.

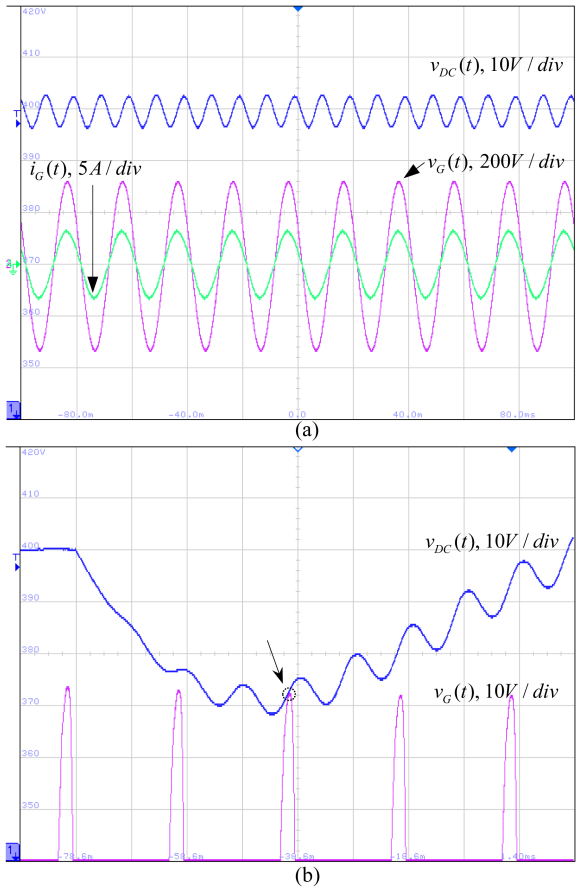

Fig. 11. Experimental results. PI controller, $\text{THD}^* = 2.5\%$. (a) Steady-state regime, $\text{THD}^* = 2.5\%$, $\text{THD} = 2.8\%$. (b) Transient regime.

TABLE I
MINIMUM DC-LINK CAPACITANCE VALUES

THD^*	C_{DC} [μF/W] - analytical		C_{DC} [μF] – 500 W prototype	
	PI	PI+N	PI	PI+N
0.05	0.64	0.16	340	85
0.025	1.28	0.21	660	108

4) Evaluate ω_y and z employing (55).
5) Set $\omega_f = 2\omega_G$. Calculate ξ_f from (57).
6) Determine $C_{\text{DC,min}}$ value using (53).
7) Determine K and τ by [cf. (25b)]

$$K = \frac{2C_{\text{DC}}V_{\text{DC}}^*}{V_{GM}}\omega_n^2, \tau = \frac{2\xi_n}{\omega_n}. \quad (59)$$

B. Notch Filter Realization

It is important to emphasize that in case of digital implementation, finite word length and quantization effects typically cause shift of the notch center frequency, which in turn implies gain reduction at one of the frequency range of interest bounds [30]. Similar effect is expected also in case of analog implementation [31] due to component tolerances. Therefore, the value of a may have to be adjusted to cope with the above.

TABLE II
DC-LINK VOLTAGE CONTROLLER COEFFICIENTS

THD^*	Controller	ξ_f	ω_f	K	τ
0.05	PI	0	--	6	0.069
	PI+N	0.05	100π	19.9	0.002
0.025	PI	0	--	3	0.014
	PI+N	0.08	100π	15.7	0.003

TABLE III
GRID-SIDE CURRENT THD

	PI	PI+N		
ω_G, rad/s	2π·50	2π·49.5	2π·50	2π·50.5
$\text{THD}^* = 0.05$	0.052	0.051	0.031	0.053
$\text{THD}^* = 0.025$	0.028	0.028	0.021	0.027

VII. EXAMPLE

Consider a P_R [W]-rated PFCR operating from 230 V, 50 ± 0.5 [Hz] mains (i.e., $\alpha \in [0.99, 1.01]$) with 5% allowed grid-side current THD. According to (22), $\alpha = 0.99$ is the worst case to be considered. Moreover, grid magnitude is typically allowed to vary within ±10% region around the nominal value [32]. In order to establish a baseline, consider first a voltage loop compensated by pure PI controller [i.e., $\xi_f = 0$ in (1) or $\beta = 0$ in (44)]. Following the design process proposed in the previous section, there is the following.

1) $\omega_G = 100\pi$, $V_{GM,\max} = 1.1{\cdot}\sqrt{2}{\cdot}230$, α is irrelevant, $V_{\mathrm{DC}}^{*} = 400$ and $\mathrm{THD}^{*} = 0.05$.
2) $\beta = 0$, $\mathrm{PM}^{*} = 40°$.
3) $\xi_n = 0.327$.
4) $\omega_y = 106.6$, z is irrelevant.
5) ω_f is irrelevant, $\xi_f = 0$.
6) $\frac{C_{\mathrm{DC,min}}}{P_R} \approx 0.4\ \mu$F/W.

Corresponding loop gain Bode diagram [cf. (40)] is depicted in Fig. 5. The resulting crossover frequency and phase margin are $2\pi{\cdot}16.9$ rad/s and 39.5°, accurately following theoretical prediction of $\omega_c = 2\pi{\cdot}16.8$ rad/s [cf. (54)] and the desired value of phase margin. Next, consider a voltage loop compensated by PI+N controller. Applying the design process above yields the following:

1) $\omega_G = 100\pi$, $V_{GM,\max} = 1.1{\cdot}\sqrt{2}{\cdot}230$, $\alpha = 0.99$, $V_{\mathrm{DC}}^{*} = 400$ and $\mathrm{THD}^{*} = 0.05$.
2) $\beta = 0.1$, $\mathrm{PM}^{*} = 40° + 5° = 45°$ (to get 40° phase margin).
3) $\xi_n = 0.4$.
4) $\omega_y = 92$, $z = 9899.8$.
5) $\omega_f = 200\pi$, $\xi_f = 0.044$.
6) $\frac{C_{\mathrm{DC,min}}}{P_R} \approx 0.098\ \mu$F/W.

Corresponding loop gain Bode diagram [cf. (40)] is shown in Fig. 5. The resulting crossover frequency and phase margin are $2\pi{\cdot}63.5$ rad/s and 39.5°, closely following theoretical prediction of $\omega_c = 2\pi{\cdot}64.5$ rad/s [cf. (54)] and the desired value of phase margin. Comparing the outcomes of Step 6, it is evident that employing a PI+N controller instead of pure PI compensator leads to ∼fourfold reduction of the minimum dc-link capacitance.

In order to generalize the results, Fig. 6 presents the relation between minimum capacitance values and THD^{*} for two different values of grid voltage, namely 230 Vrms (typical nominal value) and 264Vrms (maximum value supported by power supplies with universal input), employing a PI+N controller. It may be concluded that PI+N controller influence increases if THD^{*} is reduced. For example, for 5% allowed grid-side current THD employing PI+N controller instead of pure PI one yields more than 4rfold reduction of dc-link capacitance, while in case of 2.5% allowed grid-side current THD circa 6.5-fold reduction is achieved, irrespectively of grid voltage magnitude value. DC-link capacitance reduction ratio versus THD^{*} is depicted in Fig. 7.

VIII. Experimental Validation

In order to experimentally validate the proposed design methodology, a 500 W diode bridge + boost converter-based PFC rectifier prototype shown in Fig. 8 was employed. The control system was implemented digitally using TMS320F28335 DSP-based control card. Average current control at a fixed switching frequency of 150 kHz was adopted in the inner loop. The PFCR was operated from APS-7100 Gwinstek programmable ac power source functioning as 50 Hz, 264 Vrms mains and loaded by M9715B Maynuo dc electronic load functioning in constant power mode. Prior to methodology verification, voltage spectra of APS-7100 power source was

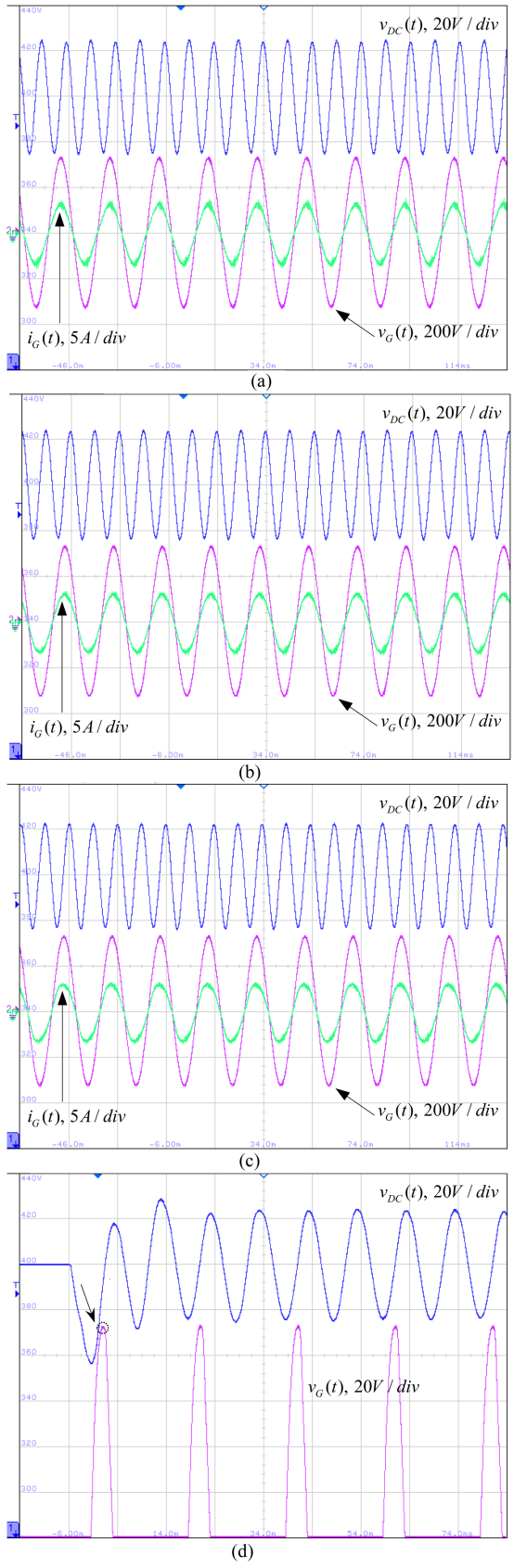

Fig. 12. Experimental results. PI+N controller, $\mathrm{THD}^{*} = 5\%$. (a) Steady-state regime, 49.5 Hz mains, $\mathrm{THD}^{*} = 5\%$, $\mathrm{THD} = 5.1\%$. (b) Steady-state regime, 50 Hz mains, $\mathrm{THD}^{*} = 5\%$, $\mathrm{THD} = 3.1\%$. (c) Steady-state regime, 50.5 Hz mains, $\mathrm{THD}^{*} = 5\%$, $\mathrm{THD} = 5.3\%$. (d) Transient regime.

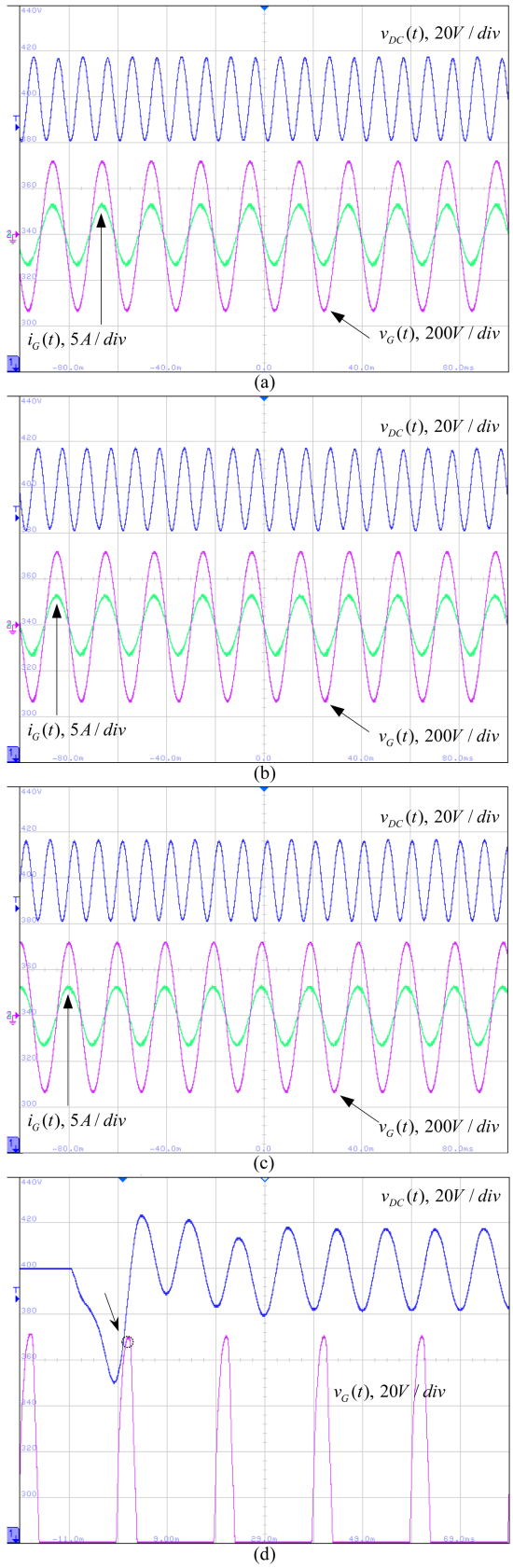

Fig. 13. Experimental results. PI+N controller, THD* = 2.5%. (a) Steady-state regime, 49.5 Hz mains, THD* = 2.5%, THD = 2.8%. (b) Steady-state regime, 50 Hz mains, THD* = 2.5%, THD = 2.1%. (c) Steady-state regime, 50.5 Hz mains, THD* = 2.5%, THD = 2.7%. (d) Transient regime.

measured and corresponding THD was found to be 0.5%, as shown in Fig. 9. Hence, measured values of grid-side current THD should be scaled accordingly.

The proposed process of minimum capacitance value selection and coefficients tuning was applied for both PI and PI+N controllers for two different desired THD values (2.5% and 5%) and $V_{GM,\max} = \sqrt{2}\cdot 264$ V (the rest of design parameters were similar to examples in Section VII). Resulting minimum attainable dc-link capacitance values (both analytical and experimental) as well as corresponding controller coefficients are summarized in Tables I and II, respectively.

Figs. 10 and 11 depict experimental results of steady-state PFCR operation under rated load and of transient response to zero-to-rated load power step (shown for 50 Hz mains frequency only since variations of the latter has a negligible influence on both steady-state and transient PFCR performance under PI compensation), utilizing a pure PI controller for both 5% and 2.5% desired THD values, respectively. On the other hand, Figs. 12 and 13 demonstrate experimental results of steady-state PFCR operation under rated load for 49.5, 50, and 50.5 Hz mains frequency and of transient response to zero-to-rated load power step (for 50 Hz mains frequency only for brevity since variations of the latter has a negligible influence on transient PFCR performance under PI+N compensation), utilizing PI+N controller for both 5 and 2.5% desired THD values, respectively. It may be concluded that experimental outcomes accurately verify corresponding analytical predictions regarding both minimum dc-link capacitance and grid-side current THD (taking into account Fig. 9). As expected, in case PI+N controller is utilized the lowest THD is attained under nominal grid frequency. However, due to finite word length and component values tolerances, zero THD may not be achieved in practice. Table III summarizes desired versus measured THD values for all cases.

IX. Conclusion

The article proposed to minimize the value of dc-link capacitance required in practical PFCR by employing PI + Notch voltage controller at the expense of increased dc-link voltage swing/ripple. Analytical expression for minimal value of dc-link capacitance was developed, based on desired values of grid-side THD and voltage loop phase margin, range of possible grid frequency values, maximum expected mains voltage magnitude, and worst-case load power step-like increase. Analytic guidelines for tuning the controller parameters were also provided. The proposed methodology was successfully validated by experiments.

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