Compact-Interleaved Packaging Method of Power Module With Dynamic Characterization of 4H-SiC MOSFET and Development of Power Electronic Converter at Extremely High Junction Temperature

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***Abstract*—Due to the outstanding material properties, silicon carbide (SiC) power device is the most promising alternative to silicon devices and can work at higher junction temperature. However, existing packaging technologies obstruct the use of SiC devices at high temperature and impede the continued exploration of SiC devices in high-temperature applications. This article proposes a novel hermetic metal packaging method called compact-interleaved package. The compact-interleaved power module handles the mentioned problems from three key considerations: packaging parasitic parameters, direct electrode measurement structure, and packaging materials. Based on the elaborate high-temperature double pulse test platform, dynamic characteristics of 1.2-kV/13-mΩ 4H-SiC power MOSFET are studied under the condition of extremely high junction temperature (up to 550 °C) and extremely high switching speed (about 3 kA/μs). The dynamic characteristics of SiC MOSFET are theoretically analyzed and verified by experimental measurements. Compared with other SiC bipolar devices, SiC MOSFET maintains outstanding dynamic characteristics at extremely high temperatures and has an optimal operating high-temperature range. Finally, this article demonstrates an extreme-high-temperature power electronic converter to verify the superiority of the packaging method, and also proves the extreme-high-temperature power converting capability of SiC MOSFET.**

***Index Terms*—Dynamic characteristics, high-temperature applications, packaging and integration, power module, silicon carbide (SiC) MOSFET, thermal runaway, wide bandgap (WBG) power device.**

I. Introduction

WIDE bandgap (WBG) power device provides the primary impetus to power electronics development progress. Due to high operating temperature, high blocking voltage, fast switching speed, and low ON-resistance, silicon carbide (SiC) power device is gradually taking over silicon (Si) device in various application fields [1], [2]. The development of electric vehicles and renewable energy grids promotes the application of SiC MOSFET in high frequency, high voltage, and high power density. However, there is a lack of sufficient research in high-temperature SiC applications.

The package of power devices is most noteworthy and has become the key in developing high-temperature applications. On the one hand, existing packaging methods hinder high-temperature applications of SiC devices for redundant parasitic parameters, large thermo-mechanical stresses, and low high-temperature tolerance. Specifically, parasitic parameters can distort the switching characteristics. The wire-bonding structure is typical and features redundant parasitic inductances due to the bond wires. Given that the SiC MOSFET's sensitivity of parasitic parameters is high, redundant parasitic parameters limit the switching speed and cause voltage breakdown. Large thermo-mechanical stresses and low high-temperature tolerance reduce the reliability of the power module at high temperature.

On the other hand, the inappropriate packaging methods affect the accuracy of the SiC device's characterizations and cannot perform accurate condition monitoring. Dynamic characterization is critical to the use of SiC devices, and can evaluate possible problems during power electronic converter operation, such as turn-OFF overshooting, electromagnetic interference (EMI) noise, false-ON crosstalk, temperature-sensitive electrical parameters (TSEPs), switching energy, and reliability [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13]. Therefore, studying the high-temperature switching characteristics can make theoretical guidance and evaluate the potential of SiC devices or converters at the extremely high junction temperature. SiC unipolar and bipolar power devices have different sensitivities to temperature. Previous literatures have studied the effects of temperature on the characteristics of SiC bipolar power devices, such as IGBT [14], [15], [16], [17], [18], [19], GTO/ETO [20], [21], [22], [25], BJT [23], [24], [25] and P-i-N diode [14], [15], [26],

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TABLE I
SUMMARY OF SiC mosfet DYNAMIC CHARACTERISTICS TEST UNDER HIGH TEMPERATURE

Reference	Maximum Temperature	Measure Fixture	Package of Device	Test Information
[28]	240°C	Curve tracer	Wire-bonding (ribbon) power module	Both the device under test (DUT) heated; only static characteristic; low current value
[29]	below 240°C	Double pulse tester	Wire-bonding power module	Both the DUT heated; high current value
[30]	250°C	Double pulse tester	Wire-bonding power module	Both the DUT heated; low current value
[31]	200°C	Double pulse tester	Wire-bonding power module	Only the DUT heated; low current value
[32] [33]	220°C	Double pulse tester	Commercial TO package	Only the DUT heated; low current value
[34]	330°C	Double pulse tester	Commercial TO package	Only the DUT heated; only SiC MOSFET body diode; low current value
[35]	200°C	Double pulse tester	Double-sided module	Both the DUT heated; high current value

by experiments or finite-element analysis (FEA) simulation. Even in the temperature range not higher than 200 °C, the temperature variability of bipolar devices is not negligible, while much smaller than that of silicon bipolar devices. Therefore, SiC unipolar power devices appear more promising at high temperatures.

Due to the packaging technology, the existing research on the temperature range is still not too high and is disturbed by large packaging parasitic parameters. It hinders the continuous exploration of the SiC device's potential at high temperature and high switching speed. In [27], a multilayer three-dimensional packaging technology is adopted. This packaging method features high power density and good cooling capability. But only static characteristics are measured at up to 279 °C, and the manufacturing process is complex. The high-temperature wire-bonding power modules are studied and fabricated [28], [29], [30], [31]. Because they use the mature package structure, their fabrication process is simple and reliable. The maximum measurement temperature for those power modules exceeds 175 °C, but not higher than 250 °C. Bond wires introduce unsatisfactory packaging parasitic parameters. For the studies of SiC power devices' dynamic characteristics under high temperature, related studies are given in Table I. Most previous studies are based on discrete devices or power modules packaged with bond wires and traditional materials that cannot stand higher operating temperatures.

In summary, a reasonable packaging method is required to overcome the obstacles of giving full play to SiC devices. None of SiC MOSFET's dynamic performance, which features extremely high temperature, high switching speed, and parasitic-inductances-unaffected, is characterized and analyzed in previous research. Thus, this article proposes a novel hermetic metal half-bridge (HB) power module with low inductances, low thermal resistance, and extreme-high-temperature tolerance. In addition, the SiC MOSFET switching waveforms under extremely high-temperature (up to 550 °C) and extremely high switching speeds (about 3 kA/μs) are characterized and analyzed to provide a theoretical basis to promote the SiC device's high-temperature applications. Futhermore, an extreme-high-temperature power electronic converter prototype is developed and operates at the ambient temperature of 250 °C and estimated junction temperature of 400 °C for 30 min.

The article is structured as follows. Section II discusses the proposed packaging method, including packaging structure, materials, and fabrication process. Section III introduces the details

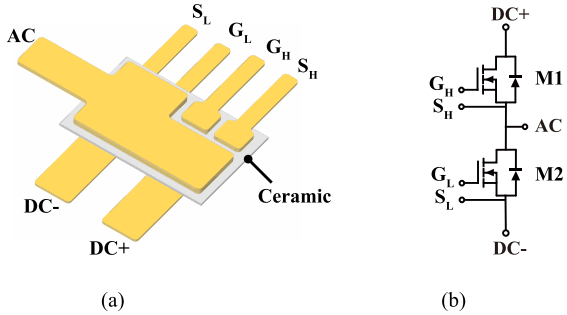

Fig. 1. General view of the power module based on the proposed packaging method. (a) Power module. (b) Equivalent circuit.

of high-temperature double pulse test (DPT) and the dynamic parameters to be measured. In Section IV, the SiC device's dynamic performances are characterized and analyzed. In Section V, the extreme-high-temperature power electronic converter prototype is developed and tested. Finally, the conclusions drawn from the analysis are provided in Section VI.

II. COMPACT-INTERLEAVED PACKAGING METHOD

This section introduces the novel compact-interleaved packaging method. At first, the profile of the proposed method is presented. Then, three keys for high-temperature use and its countermeasure are severally discussed. In detail, three key considerations include the low packaging parameters based on the small current commutation loop (CCL), the direct electrode measurement structure, and the packaging materials. The proposed packaging structure not only makes full use of the SiC device's remarkable performances but facilitates the measurement of its dynamic characteristics at the extreme-high-temperature junction and high switching speed.

A. Profile of Compact-Interleaved Packaging Method

For the compact-interleaved packaging method, the power module integrates two SiC MOSFETs bare dies to form a HB which is the basic structure of most power electronic converters (see Fig. 1). The module eliminates wire bonds inside and uses the busbar-like form called planar interconnection (see Fig. 2). Two SiC MOSFET bare dies are attached on both sides of the direct bonding copper (DBC) substrate to perform the interleaved position. Some copper-filled via-holes connect both sides of

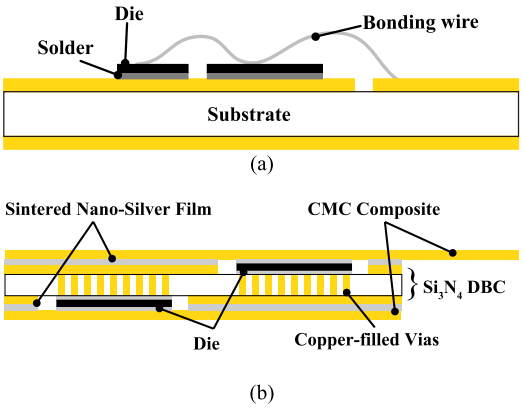

Fig. 2. Lateral view of the power module. (a) Traditional wire-bonding structure. (b) Compact-interleaved structure.

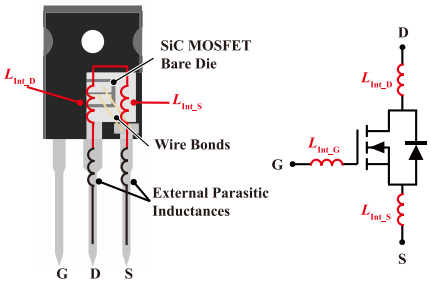

Fig. 3. Packaging parasitic inductances of transistor out-line package. (a) Internal distribution. (b) Equivalent diagram.

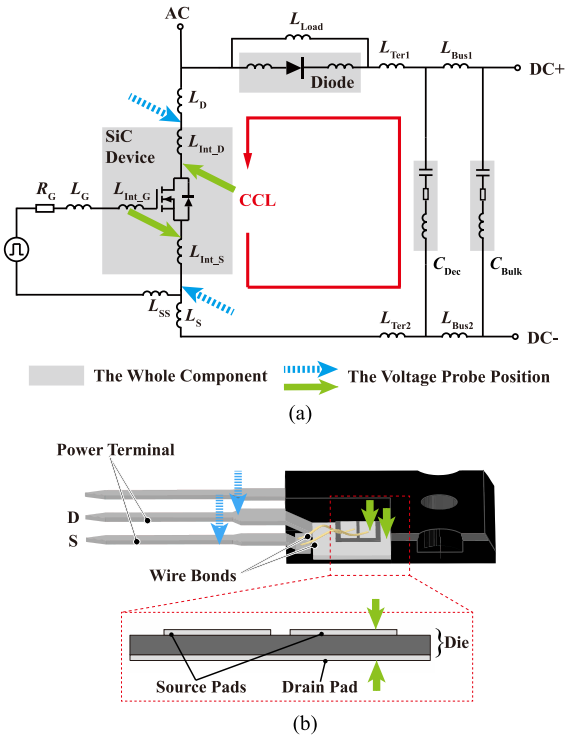

Fig. 4. DPT circuit and different probing positions for DUT. (a) Equivalent circuit of DPT. (b) Different probing positions taking TO package as example.

DBC copper to obtain the specific electrical connections. The insulation inside the module can be vacuum or filled with insulation materials. This article adopts the hermetic vacuum/inert gas. This module has three power terminals (DC+, DC-, AC) and four signal terminals (high-side $G_{\rm H}$, $S_{\rm H}$; low-side $G_{\rm L}$, $S_{\rm L}$) for the gate drive function constructed by Kelvin source connection to increase the stability of the gate driving signal [36]. The equivalent circuit is shown in Fig. 1(b). The double-sided cooling (DSC) method can theoretically decrease the junction-to-case thermal resistance by 50% compared with the single-sided cooling (SSC) method. In the high-temperature dynamic characterization of SiC MOSFET, the compact-interleaved hermetic power module can deal with the three key considerations well. The details are presented as follows.

B. Low Packaging Parameters

The first consideration comes from parasitic parameters of the bare die's package and test fixture. In practical applications, the extra inductances may damage the DUTs by transmuting the SiC device's dynamic characteristics. The DUT usually is a transistor out-line package (TO package) or wire-bonding power module, which features considerable parasitic inductances. The parasitic inductances mainly exist in the bond wires and power terminals (see Fig. 3). $L_{\rm Int\_D}$, $L_{\rm Int\_S}$, and $L_{\rm Int\_G}$ represent the internal parasitic inductances named after their locations. Besides, quite a few parasitic inductances come from the test fixture, which belongs to the CCLs. The DPT is usually conducted to obtain the dynamic characteristics. The test scheme is half bridge [see Fig. 4(a)]. The high-frequency current conducts the CCL at the SiC device switching transients [indicted by the red line in Fig. 4(a)]. For clarity, the upper switch is represented by its body diode. The Darin-source overshoot voltage can be written as

$$V_{\rm overshoot} = (L_{\rm DPT} + L_{\rm package})\frac{di_{\rm D}}{dt} \tag{1}$$

where $L_{\rm DPT}$ is the DPT fixture's parasitic inductances consisting of $L_{\rm Bus1}$, $L_{\rm Bus2}$, $L_{\rm Ter1}$, $L_{\rm Ter2}$, $L_{\rm D}$, and $L_{\rm S}$, $L_{\rm package}$ is packaging parasitic inductances of SiC device, diode, and decoupling capacitors which are marked in the respective gray shadow shown in Fig. 4(a). Due to the high switching speed, SiC device features high sensitivity to parasitic inductance. Even low inductances would induce high voltage overshoot and noise, and cause deviation in dynamic characteristics [36]. For example, SiC MOSFET turn-OFF switching speed can reach a few amperes per nanosecond. Therefore, even a tiny parasitic inductance (dozens of nano-henrys) will induce a significant voltage overshoot. As Fig. 5 shows, the extra inductances will transmute the switching waveforms (indicated by the green line), and the unreasonable probing position deviates from measured voltage waveforms (indicated by the red line).

This packaging method makes the module features a tiny CCL area that is proportional to the parasitic inductances. This means the distances at which the current conduct is shortened, and there is a strong electromagnetic cancellation effect in the CCL. As shown in Fig. 6, the CCL includes the main part, the terminals and the capacitor part. The main CCL features

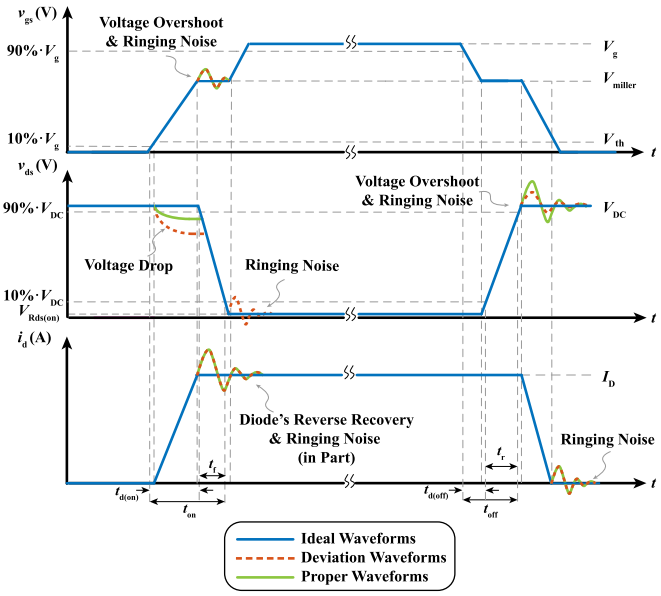

Fig. 5. Switching waveforms of SiC MOSFET considering parasitic parameter and probing position.

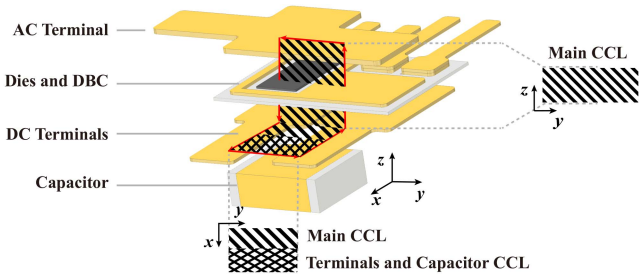

Fig. 6. CCL in the compact-interleaved power module with decoupling capacitor.

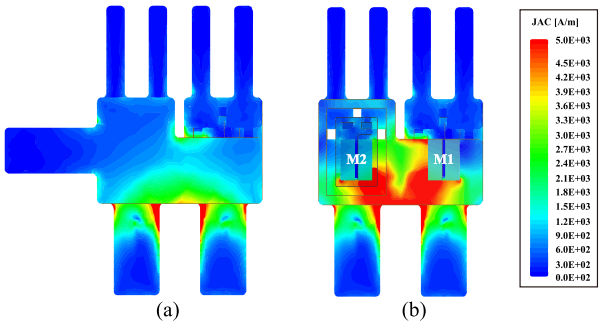

Fig. 7. illustrations of the power module's current density. (a) Top view. (b) Top view omitting ac terminal.

a small area of about 9.75 mm × 1.70 mm, determined by the module structure. The terminals and capacitor CCL are mainly determined by the decoupling capacitor's installable location and feature a relatively small area of 9.5 mm × 9.5 mm. Fig. 7 shows current density distributions (the current source value is 50 A in the simulation). It can be concluded that the CCL in this power module is very small. In other words, the main body of this module has very low packaging inductances. The power module is divided into several parts to extract the respective

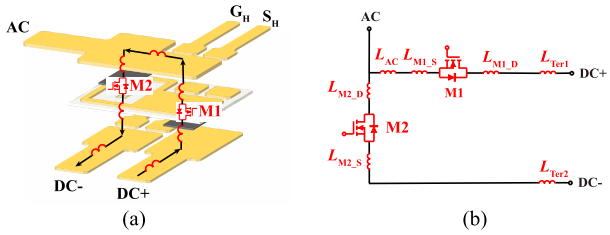

Fig. 8. Exploded view of the compact-interleaved power module with the distinctions of packaging parameters. (a) Power module. (b) Equivalent circuit.

TABLE II
SIMULATION RESULTS OF PARASITIC INDUCTANCES

	Results (nH)		Results (nH)
L_{M1_D}	0.00462	L_{AC}	0.3019
L_{M1_S}	0.01424	L_{Ter1}	3.4292
L_{M2_D}	0.00476	L_{Ter2}	3.4065
L_{M2_S}	0.01149		
Main CCL		0.3370nH	

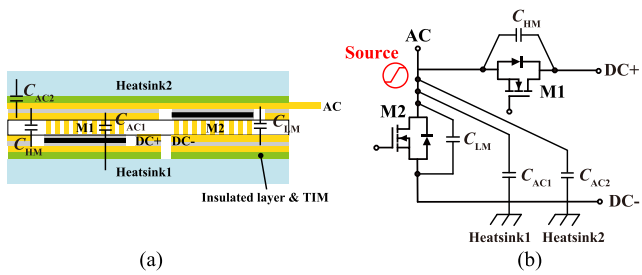

Fig. 9. Distributions of packaging parasitic capacitors in the compact-interleaved power module. (a) Power module. (b) Equivalent circuit.

parasitic inductance (see Fig. 8). The extracted inductances by ANSYS Q3D are given in Table II. The solution frequency is set as 100 MHz. The inductances of every part in this module are less than 0.5 nH. An easy-to-install location for decoupling capacitors is designed to eliminate the redundant inductances (L_{Ter1} and L_{Ter2}). Because the decoupling capacitors provide a high-frequency current path to decouple the DUTs from other components in the DPT fixture. These can reduce the "L_{DPT}," but not all. The reasons are the parasitic parameters of the capacitor and the limitation of physical positions. Due to the compact-interleaved structure, the power module has only 0.3370 nH compared to the TO package inductances of 10–15 nH [37], [38].

As for the packaging parasitic capacitance, the simulations used by ANSYS Q3D also are conducted. The solution frequency is still set as 100 MHz. The sum of the thickness of thermal interface material (TIM) and insulated layer is set as 0.7 mm. The primary influence which causes the distortion of switching waveforms and common-mode EMI are marked in Fig. 9. These capacitance values (see Table III) are rational and do not cause significant side effects. Other values of parasitic capacitors are obviously small and not discussed.

TABLE III
SIMULATION RESULTS OF PARASITIC CAPACITANCES

	Results (pF)		Results (pF)
C_{HM}	17.85	C_{AC1}	0.3246
C_{LM}	12.14	C_{AC2}	28.11

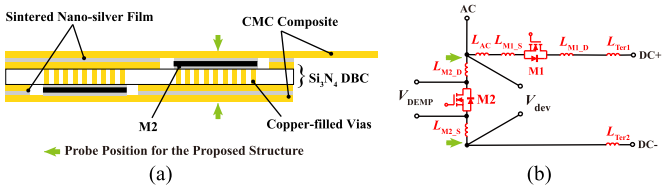

Fig. 10. DEMP in the compact-interleaved power module. (a) Power module with DEMP. (b) Equivalent circuit (only CCL's packaging inductances shown).

C. Direct Electrode Measurement Position (DEMP)

The second consideration is the voltage probing position. Take the TO package as an example, Fig. 4 shows the two different probing positions. The green arrow is the proper probing position. Limited to the encapsulation and packaging structure, the measurable position is indicated by the blue dotted arrow and contains extra parasitic inductances. As shown in Fig. 5, the inappropriate probing position causes switching waveforms' deviations, mainly reflected in drain-source switching voltage of overshoot, drop, and turn-OFF noise (inducted by the red dashed lines). The detailed analyses are presented in Appendix. This phenomenon will worsen when the switching speed becomes faster or the packaging parasitic inductance are more considerable. Probing position has a tremendous influence on SiC MOSFET switching waveforms. The characterization with deviations for overshoot (smaller)/drop (bigger) voltage may cause the reliability problem and inappropriate thermal management design [36], [46]. The turn-ON voltage noise can bring the design problem of electromagnetic compatibility and protection, such as DESAT blanking time.

Due to the proposed structure, the switching voltage of the SiC MOSFET'S electron pads is easily measured. As Fig. 10 shows, the green arrows point to the voltage probing position for low-side switches "M2" while the included parasitic inductances are only 0.01625 nH ($= L_{M2\_D} + L_{M2\_S}$). The parasitic inductance is too small that it can be ignored. This can be considered a direct measurement of the die's electrode surface. Thus, these measurement positions based on the compact-interleaved packaging method can be called the DEMP. The simulation results by LTSpice are shown in Fig. 11. The simulation circuit is built according to Fig. 4(a). The deviations mainly come from the packaging inductances. For example, the deviated voltage is equal to (V_{dev}-V_{DEMP}) which is induced from L_{M2_D} and L_{M2_S} in Fig. 10. Thanks to the DEMP, the voltage deviations and noise can be almost eliminated.

D. High-Temperature Packaging Materials System

The third consideration is the traditional packaging material of the power module cannot stand high-temperature junction

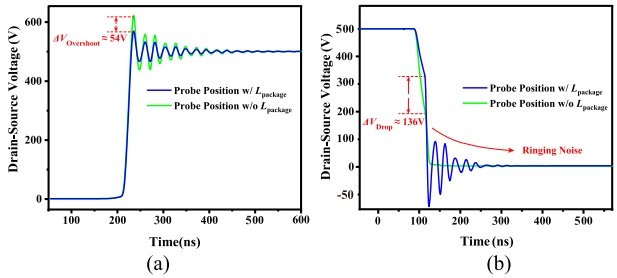

Fig. 11. Simulation results about deviations and optimized waveforms. The sum of L_{Int_D}, L_{Int_S} is 15 nH, other parasitic inductances are totally 20 nH. (a) Turn-OFF overshoot voltage. (b) Turn-ON drop and voltage noise.

TABLE IV
LIST MATERIALS FOR THE PROPOSED POWER MODULE

Part	Material	Specifications
Device	Cree SiC MOSFET bare die	QPM3-1200-0013D, 1200V/13mΩ Die size: 4.36 × 7.26 mm^2 Top side metallization: Au Bottom side metallization: Au
Die-attach material	Nano-silver	Pressure sinter nano-sliver paste Sintering temperature: 210°C
Substrate	Si_3N_4 DBC	Cu/ Si_3N_4/Cu: 0.1mm/0.32mm/0.1mm Coated with the Ni/Au layer
Metal part	Cu/Mo/Cu sandwich composite	Cu/Mo/Cu: 13/74/13 Total thickness: 0.5mm Thru-thickness thermal conductivity: 170 W/(m·K) @25°C In-plane thermal conductivity: 200 W/(m·K) @25°C Coefficient of thermal expansion: 5.6 ppm/K @25°C
Insulation	Hermetic package	-

operation. Khazaka et al. [39] shows the commercially available polymeric encapsulation (silicone gels) exhibits a maximum temperature limit for continuous service of less than 250 °C. Rigid materials such as epoxy present reliability problems under thermal cycles where cracks appear and also are less than 250 °C [40]. As for reliability, die-attach and interconnection materials are the most focused objective. The common die-attach materials cannot operate above 250 °C. Even for Pb-rich and eutectic solders such as Pb95-Sn5 and Au88-Ge12 (mass%), the safe operating temperature shall not exceed 300 °C. Most commercial devices and power modules are limited to the maximum temperature of 150 °C or 175 °C. As for the interconnection material, the bond wires are the most common technology. However, apart from the large packaging inductances and the poor ability to dissipate heat, the main problem is that its reliability of fatigue caused by thermomechanical stress can face significant challenges in high-temperature applications.

The packaging materials are given in Table IV. Some considerations are as follows.

1) The essential parts are die-attach and interconnection materials. In the proposed packaging method, the two materials are nano-silver film. After the sintering with the special process (pre-dried, time-extending, and time-variant pressure sintering process), the nano-silver paste becomes film and features up to the melting point of 962°C

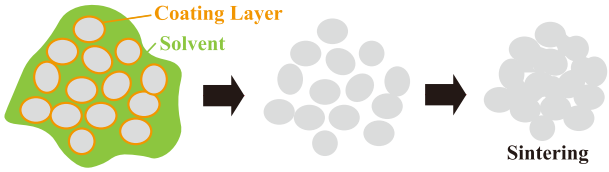

Fig. 12. Profile of the sintering nanosilver paste and the sintering processes.

theoretically, very low coefficient of thermal expansion (CTE), high shear strength which is many times high than the criterion (6.1MPa) [41], and higher long-term reliability.

2) The ceramic substrate is the body structure of the power module. The selection of ceramic types is essential for the thermal management and reliability of the entire power module. The widely used alumina is discarded due to the too large CTE of 6.8–8 ppm/K [42]. There are two choices: aluminum nitride and silicon nitride (Si_3N_4). This article chooses the Si_3N_4 for the low CTE (3.2–3.5 ppm/K) close to the SiC (3.7–4.4 ppm/K) [42] and high fracture toughness.
3) The metal part is the Cu/Mo/Cu (CMC) sandwich composite consisting of a molybdenum core layer and two copper-clad layers. It has tailorable CTE (5.6 ppm/K) and high thermal conductivity (170 W/(m·K) of thru-thickness). The two excellent features guarantee the module's high-temperature reliability because the metal parts assume the primary current carrier and the cooling path's central part.

As mentioned before, the essential parts for the high-temperature operation are die-attach and interconnection materials. In this high-temperature packaging system, the nanosilver paste is chosen. The nanosilver particles are encased in an organic coat and stored in organic solvents. As Fig. 12 shows, as the temperature rises, organic matter evaporates. Then, the temperature reaches the sintering temperature (usually 180 °C–250 °C). The sintering nanosilver particles remain in the solid-state during the whole sintering progress. According to the microscopic properties of nanosilver particles after sintering, the nanosilver film exhibits excellent properties compared to the traditional solder. Some literature has been studied to enhance the strength of nanosilver layer [43], [44], [45]. However, the application temperature of most studies is less than 200 °C. For the high-temperature usage, using an unoptimized sintering process causes nanosilver layers to be unreliable in the connect strength. This power module adopts the time-extending and time-variant pressure sintering processes. The results of the die-shear test show that the nano-silver film still has good connection strength (see Fig. 13) after high-temperature aging (300 °C).

The thermal performance of the compacted-interleaved power module is conducted. Fig. 14 shows the thermal model of compacted-interleaved power module with self-heating and thermal coupling resistances. For clarity, switch M2 is analyzed as the primary heat source. As for the self-heating resistances, the thermal resistances of the heatsink, insulation layer, and TIM

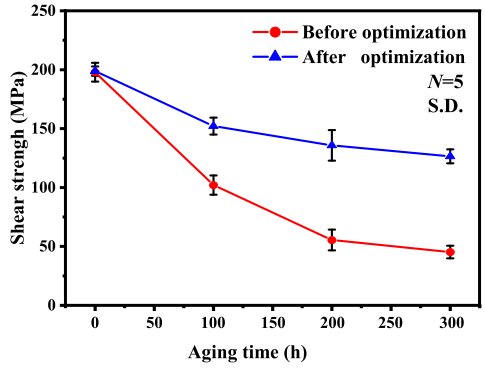

Fig. 13. Shear strength with aging time.

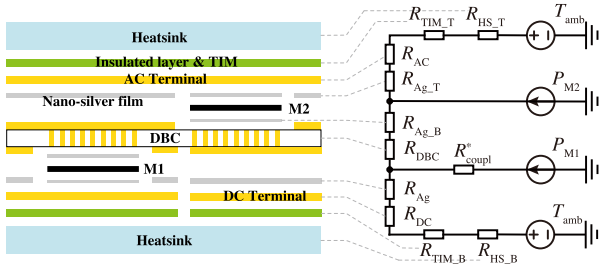

Fig. 14. Thermal model of compacted-interleaved power module (use *M*2 as an example).

are determined by the user's choice and setup. The self-heating thermal resistance can be written as

$$R_{\text{self}} = R_{\text{TOP}} // R_{\text{BOT}} \tag{2}$$

where the R_{TOP} and R_{BOT} is represented as

$$R_{\text{TOP}} = R_{\text{Ag\_T}} + R_{\text{AC}} + R_{\text{TIM\_T}} + R_{\text{HS\_T}} \tag{3}$$

$$R_{\text{BOT}} = R_{\text{Ag\_B}} + R_{\text{DBC}} + R_{\text{Ag}} + R_{\text{DC}} + R_{\text{TIM\_V}} + R_{\text{HS\_B}}. \tag{4}$$

As for the thermal coupling resistances, the total equivalent thermal coupling resistances ξ_{coupl} can be written as

$$\xi_{\text{coupl}} = \beta \cdot (R^*_{\text{coupl}} + R_{\text{Ag\_B}} + R_{\text{DBC}}) \tag{5}$$

where the R^*_{coupl} is the compensatory thermal coupling resistance. β represents the proportion of the coupling power dissipation (transfers from M1 to M2) to M1's total power dissipation P_{M1}. Considering the low thermal resistance of this power module and the insensitivity of the SiC device to temperature compared with the Si device, the predictable experimental measurement errors cannot be ignored. Thus, the simulation results conducted by ANSYS Workbench mechanical are given here. The thermal resistance from junction to case is simulated as 0.01831 °C/W of M1 and 0.01823 °C/W of M2. These values are much smaller than the thermal resistance of the TO package (typically more than 0.2 °C/W). The comparisons between self-heating and thermal coupling temperature rise are also introduced. The cooling capability of the heatsink, insulation layer, and TIM is represented by the equivalent convection heat transfer coefficient (HTC). The sweep range is 200–10000 W/m^{2}K. The improvement of thermal performance is quantified

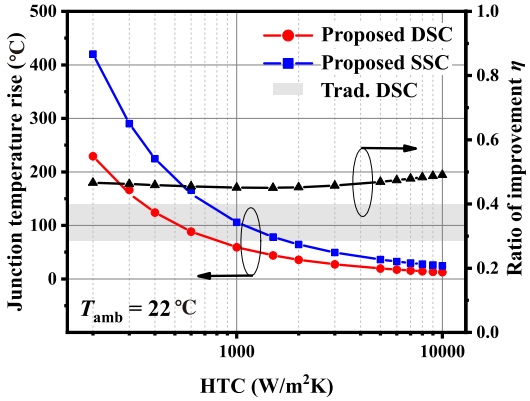

Fig. 15. Comparison of self-heating temperature rises between compact-interleaved DSC and SSC.

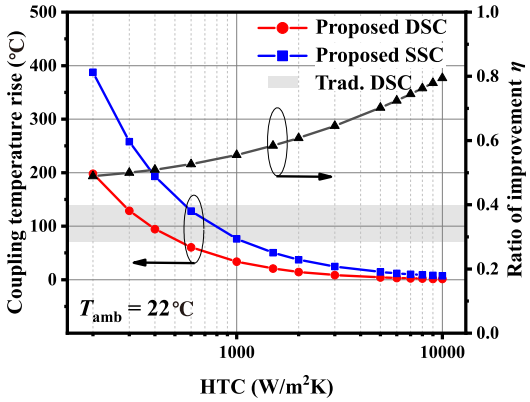

Fig. 16. Comparison of thermal coupling temperature rises between compact-interleaved DSC and SSC.

as η, calculated as one minus the ratio as the DSC's temperature rise to the SSC's temperature rise. Fig. 15 shows the ratio is close to 0.5 from below. The reason is that solid vias in DBC slightly reduce cooling capacity. Noted that, for the traditional DSC power module, because the SiC die area is small, the thermal resistance of metal spacer is correspondingly large, resulting in an about 29%–40% decrease in junction-to-case thermal resistance compared to the SSC power module [35], [51], [52]. For the improvement in the thermal coupling, Fig. 16 shows that the thermal coupling effect between bare dies is greatly optimized as HTC increases. The junction-to-case thermal resistance of the compact-interleaved DSC method decrease by nearly 50% than the SSC method.

E. HB Power Module for Extreme-High-Temperature Applications

As Fig. 17 shown, the HB power module based on the compact-interleaved packaging method is suitable for high-temperature applications. Its packaging materials are carefully selected for high-temperature reliability, especially the nanosilver time-extending sinter process and the matching CTE among the different packaging materials. This packaging method can provide sufficient tolerance capability, low thermal resistance and low packaging parameters for high switching speed in extreme-high-temperature (more than 300 °C).

Fig. 17. Fabricated compact-interleaved SiC power module. (a) Power module with the fixing fixture of graphite boat. (b) Overall illustration of power module.

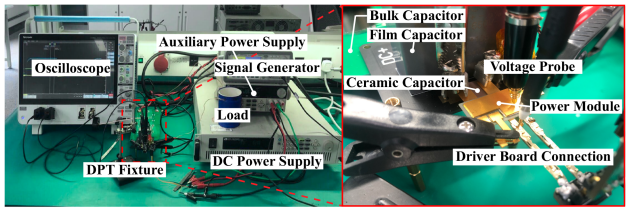

Fig. 18. High-temperature and low-inductance fixture of DPT. (a) Overview. (b) Detailed view.

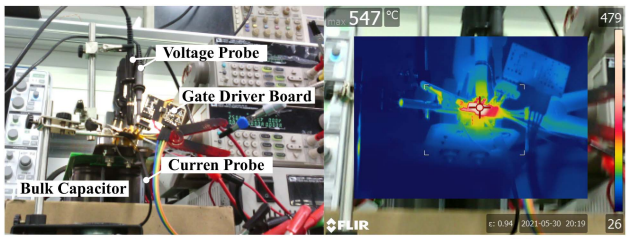

Fig. 19. Diagram of DPT fixture from the perspective of temperature measurement. (a) DPT fixture obtained by thermal camera. (b) Junction temperature of about 550 °C.

III. SiC MOSFET Switching Measurement Under Extremely High Junction Temperature

This section introduces the detailed switching measurement of SiC devices under high-temperature junction, including the DPT fixture setup with design considerations and the definition of measurement objects.

A. Setup Principle of High-Temperature DPT

The DPT can concisely and accurately characterize the switching performance of the power switches, such as the IGBT and MOSFET. Fig. 4(a) shows the equivalent circuit diagram. During the test, the low-side switch is usually tested for safety consideration, and the high-side switch remains turn-OFF to perform as a freewheel diode. Two square pulses generated by pulse function arbitrary generator are launched to the low-side switch. Switching waveforms that belong to the end of the first pulse and the beginning of the second pulse are demanded. To obtain the actual dynamic performance and changing trend with temperature, the high-temperature DPT was constructed (see Fig. 18) and the setup principles are shown below.

1) Low Parasitic Inductances: Considering the SiC MOSFET's sensitivity to parasitic parameters, the fixture should be designed carefully to prevent extra parasitic inductances. As mentioned before, the parasitic parameters mainly come from

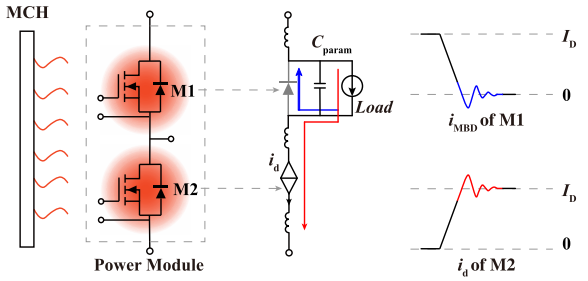

Fig. 20. Heating object and their effect on turn-ON switching current waveform. The load is equivalent to a current source and M2 is equivalent to a controlled current source in the saturation region.

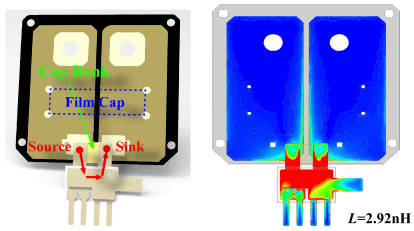

Fig. 21. Illustration for the position of capacitor bank (left) and the current distributions (right). The fixture with capacitor bank close to the power module. The simulated current density is the highest in red, lower in green and the lowest in blue.

the package and test fixture. The inappreciable parasitic parameters are introduced attributed to the compact-interleaved structure. As for the test fixture, countermeasures to reduce parasitic inductance are presented in the following section.

2) Heated Object: As for the temperature setting, some previous studies often lacked simultaneous heating of the upper and lower switches. Given the dynamic characteristics of the SiC switch will be affected by the complementary switch in HB, the complementary switch must be considered in the estimation of switching energy and EMI. As Figs. 19 and 20 shows, the current overshoot of M2 is mainly determined by the body diode or anti-parallel diode of complementary switch M1 in HB. Current overshoot usually comes from reverse recovery charge, which consists of three sources: reverse recovery process of body diode or antiparallel diode; packaging parasitic capacitance discharge process; and quasi-turn-ON conduction. Even if the parasitic capacitances are alleviated by the packaging method, and the quasi-turn-ON conduction is eliminated by using the turn-OFF drive resistor of zero ohm, the current overshoot caused by the change of the body diode's reverse recovery characteristics at extremely high temperature cannot be ignored. If only a single device in the HB module is heated, the experimental switching waveforms and the actual switching waveforms differ widely in the turn-on current switching waveforms. In this DPT, the two SiC devices are heated easily attributed to the packaging method.

3) Other Interference Factors: Before the packaging process, the SiC bare dies are evaluated by consistency detection to prevent the deviation of electrical parameters due to the manufacturing process. All the DPTs were completed in a short time to minimize the impact of self-heated.

B. Fixture Setup of High-Temperature DPT

The extra parasitic inductances partly come from the test fixture. The accuracy of measuring waveform largely depends on setting the board reasonably. This article makes improved arrangements in the following aspects.

1) C *Snubber Board*: To decouple the large parasitic inductances from the bulk capacitors and its board, a compact *C* snubber board with one low-inductance film capacitor is introduced. The film capacitor can effectively alleviate the ringing phenomenon in the middle and low frequency.
2) *High-Temperature Ceramic Capacitor Bank*: to decouple the extra parasitic inductances from the C snubber board and the module's power terminals which could result in the ringing in the high and middle frequency, the ceramic capacitor bank is utilized and fixed very close to the main body of the power module (see Fig. 21). The whole parasitic inductance is only 2.92 nH obtained by simulation. The extra introduction of the parasitic inductances reduced by 6.5 times theoretically compared to the unoptimized fixture (see Fig. 33). See the Appendix for further detailed explanations.
3) *Connection*: Crimp terminals are used for electrical connection where the temperature may exceed the melting point of the solder. The reasonable connection strength will be guaranteed to minimize the contact resistances at the connection joint. As for the signal's connection and measurement instrument, the cable is as short as possible to reduce propagation delay.
4) *Considerations for Measurement Instrument*: The instrument with high bandwidth and low propagation delay are utilized. The measurement error can be considered that has been eliminated for the voltage measurement. As for the current measurement, utilizing a current high-performance probe inevitably introduces large extra parasitic parameters duo to these physical shapes and installation methods. Thus, the Rogowski coil current probe (50 MHz-bandwidth) is utilized. As for the errors caused by current probes, the propagation delay time is corrected in the postprocessing. Other deviations do not affect the trend of electrical characteristics changing with temperature.

Table V gives the details of the high-temperature DPT fixture. In the CCL of the high-temperature DPT fixture, the extra parasitic inductances are significantly reduced because of two main aspects: a compact-interleaved power module with ultralow parasitic inductance, and the other is the location where the decoupling capacitor can be fixed closely to almost decouple the power terminal. Common commercial power devices/modules are not achievable. From the perspective of reducing the influence of parasitic parameters and ensuring reliable operation at high temperatures, DPT is more suitable for characterizing the dynamic characteristics of SiC devices at extremely high temperatures and high switching speed.

C. Type of Measured Dynamic Characteristics

Several SiC MOSFET'S dynamic characteristics are measured and analyzed. Fig. 5 illustrates the partial definition of these characteristics. Some dynamic characteristics vary with temperature

TABLE V
DETAILS OF EXPERIMENTAL EQUIPMENTS

Objective	Details
Gate Driver	Texas Instruments UCC5350SCD, typical peak source/sink current: 10A/10A External gate resistances: zero Ohm
Ceramic capacitor	C3640H473KGGWCT050, 47nF For high temperature use, three in parallel
Oscilloscope	Tektronix MDO4054C, 500MHz, 2.5GS/s
Signal Generator	Keysight 33500B
DC power supply	ITECH IT6726V 1200V/5A/3000W
Auxiliary power supply	ITECH IT6302 0~30V, 3Ax2CH/0-5V,3A
Voltage probe	Tektronix TPP0500B 300V/500MHz; TPP0850 1000V/800MHz
Rogowski coil current probe	CWT Mini50HF: 50MHz bandwidth, 120A;
Thermal camera	FLIR T630sc; precision ±1°C
Heating equipment	Metal Ceramics Heater (MCH); Heating core: Tungsten, lead: nickel wire

and can be called TSEP. TSEPs are preferred to be selected for the large temperature correlation. It facilitates the analysis of temperature-relevant electrical parameter changes in SiC MOSFET and estimates its feasibility for extremely high-temperature applications.

1) Switching Delay Time: As Fig. 5 shows, the turn-ON delay time is defined as the interval between the time when the gate-source voltage increases to 10% of V_g and the drain-source voltage decreases to 90% of V_{DC}. The turn-OFF delay time is defined as the interval between the time when the gate-source voltage decreases to 90% of V_g and the drain-source voltage increases to 10% of V_{DC}. The switching delay time is highly correlated with the parasitic capacitors of the switches, and the deviation details are presented in the Appendix. The turn-ON and turn-OFF delay times are

$$t_{d(\text{on})} = \tau \ln\left(\frac{0.9V_g}{V_g - V_{\text{Miller}}}\right) + \frac{0.1V_{DC}R_G C_{GD\_av}}{V_g - V_{\text{Miller}}} \tag{6}$$

$$t_{d(\text{off})} = \tau \ln\left(\frac{0.9V_g}{V_{\text{Miller}}}\right) + \frac{(0.1V_{DC} - V_{\text{Rds(on)}})R_G C_{GD\_av}}{V_{\text{Miller}}}. \tag{7}$$

As for the turn-ON delay time, the TSEPs are mainly R_G (partly from the charging time constant τ) and V_{Miller}, which is also load and V_{DC} dependence [34]. The two parameters exhibit negative temperature dependence. Thus, the $t_{d(\text{on})}$ decreases with the temperature rising theoretically.

As for the turn-OFF delay time, the TSEPs are also R_G and V_{Miller}. According to (7), the $t_{d(\text{off})}$ features different change directions as temperature increases. The existing research indicates that the Miller plateau (MP) voltage is dominant [29] below the 225 °C. On the broader temperature range, the dependence is not clear.

2) Switching Speed Time: The rise time of voltage is defined as the interval between the time when the drain-source voltage increases to 10% of V_{DC} and then increases to 90% of V_{DC}; the fall time of voltage is defined as the interval between the time when the drain-source voltage decreases to 90% of V_{DC} and then decreases to 10% of V_{DC}. The expression can be written as (D4) and (D9) in the Appendix. It can be concluded that two parameters are temperature dependent, partly determined with R_G and V_{Miller}. As mentioned before, the two parameters exhibit negative temperature dependence. The temperature dependence is unclear for the voltage rise time because of the contradiction between the two TSEPs with temperature changing. The temperature dependence is also unclear for the voltage fall time because of the contradiction between the two terms in the (D4) with temperature changing.

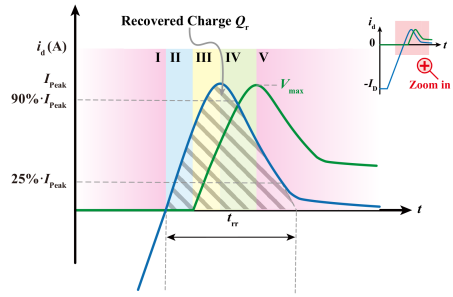

Fig. 22. Typical diode reverse-recovery characteristics divided by five different stages (blue line represents current waveform and green line represents voltage waveform).

3) Diode's Reverse Recovery: To switch the body diode of SiC MOSFET from its ON-state mode to the reverse block mode, it is necessary to remove the free carriers in the drift region to form a depletion region that can support a high electric field. It is summed up as the charge storage effect or capacitive effect, consisting of two different mechanisms [48], especially in the stages III and V shown in Fig. 22. Both of these mechanisms show different weight contributions. The first is related to the depletion layer charge. When the voltage across the diode increase, the charge of depletion increases to balance the change in the junction voltage. The equivalent capacitor is named junction capacitance. Another is drift capacitance because of the formation of drift layer charge when the large field builds up inside the body diode. The total recovery current is equal to the sum of junction capacitance's current $i_j(t)$ and drift capacitance's current $i_d(t)$ written as

$$\begin{aligned} i_r(t) &= i_j(t) + i_d(t) \\ &= C_{j\_av}\frac{du(t)}{dt} + C_D(t)\frac{du(t)}{dt} + \frac{dC_D(t)}{dt}u(t) \end{aligned} \tag{8}$$

where C_{j_av} is the average junction capacitance that consists of the MOSFET'S output capacitances and inductive load's parasitic capacitances, $C_D(t)$ is drift capacitance which is equivalent to the charge aggregation effect, and $u(t)$ is the voltage drop across the body diode. The two equivalent capacitor features a high correlation with temperature because the carrier concentrations determine them. In the subsequent measurement, the recovered charge Q_r is focused on and defined as the current integral over t_{rr}, which is the interval between the time when the drain current passes through zero and the time when, for decreasing value of i_d, a line through the points for 90%I_{peak} and 25%I_{peak}

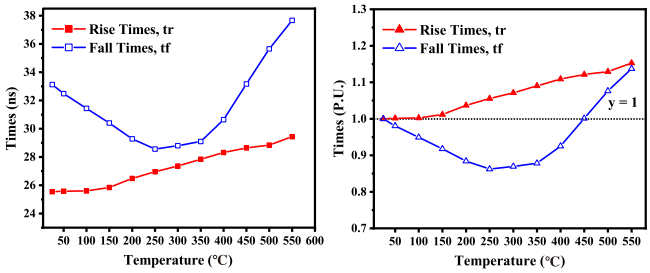

Fig. 23. SiC MOSFET waveforms of the rise time and fall time of the drain-source voltage. (a) Rise time and fall time at different temperatures. (b) Normalized rise time and fall time at different temperatures.

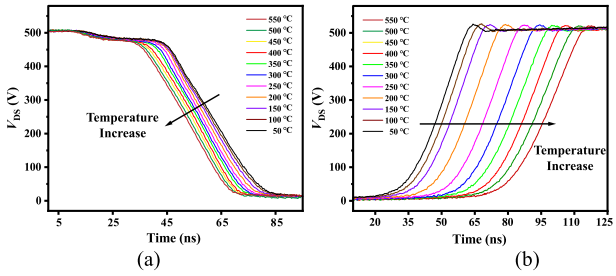

Fig. 24. SiC MOSFET switching waveforms of the drain-source voltage at different temperatures. (a) Turn-ON transients. (b) Turn-OFF transients.

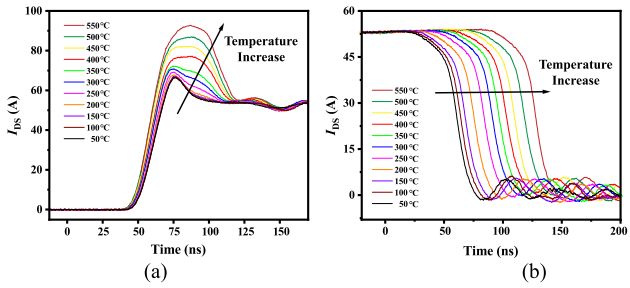

Fig. 25. SiC MOSFET switching waveforms of the drain-source current at different temperatures. (a) Turn-ON transients. (b) Turn-OFF transients.

crosses the zero current axis. The measurement method follows the relevant standards [49].

IV. Experimental Characteristic Results

In this section, the switching waveforms of SiC MOSFET are presented first, and the dynamic characteristics which are temperature dependence will be introduced and discussed. All dynamic characteristics are obtained at high-fast switching speeds.

A. Overview of the Switching Waveforms

Figs. 24 and 25 show the switching waveforms at different temperatures. The high switching speed is gained that the current rise time is about 22 ns from $10\%I_{\text{peak}}$ to $90\%I_{\text{peak}}$ at the steady-state current of 50 A, and the voltage rise time is about 27 ns from $10\%V_{\text{DC}}$ to $90\%V_{\text{DC}}$ at the bus voltage of 500 V. The SiC MOSFET switching speed is high enough compared to the existing literature. It can be evident that, with the external factors unchanged, the SiC MOSFET still remains the characteristic of

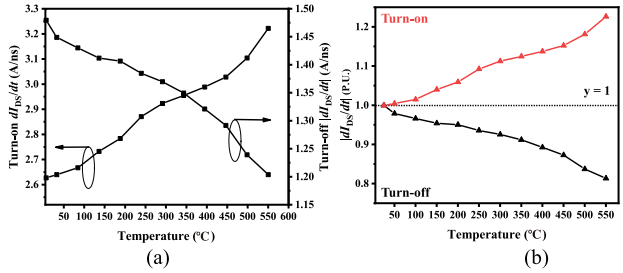

Fig. 26. The SiC MOSFET waveforms of the current change rate. (a) The turn-ON and turn-OFF current change rate at different temperatures. (b) The normalized turn-ON and the turn-OFF current change rate at different temperatures.

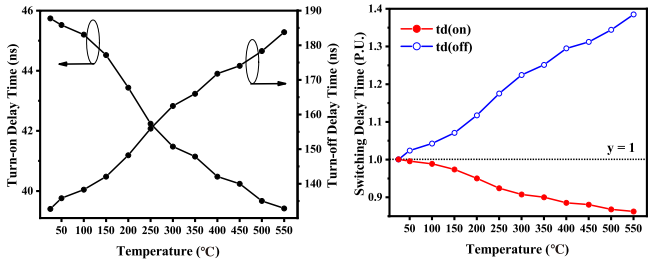

Fig. 27. The SiC MOSFET waveforms of switching delay time. (a) The turn-ON and turn-OFF delay time at different temperatures. (b) The normalized turn-ON and turn-OFF delay time at different temperatures.

high switching speed at the wide high-temperature range. This article does not calculate the module's parasitic inductances because the relevant characteristics caused by the parasitic inductance are too inconspicuous in the waveform. Small reading errors will cause large result errors. In addition, as Fig. 24(a) shows, there is no turn-ON voltage oscillation noise. Because the probing position is DEMP.

For the turn-OFF transients, the voltage overshoot is about 25V (only 5% of the bus voltage V_{DC}). As the junction temperature increase, the voltage overshoot decreases due to the decline of the rate of current change (see Fig. 26). It implies that the voltage breakdown caused by parasitic parameters will be alleviated to a limited extent in high-temperature applications.

For the turn-ON transients, the current overshoot presents a huge deviation with the temperature rising. The reason is caused by the reverse recovery of the complementary MOSFET'S body diode in the HB module. In this measurement, benefited from the compact-interleaved power module, the two complementary SiC MOSFET can be tested at the same temperature to study the electrical characteristics of actual high-temperature conditions. The following subsection will give the relevant details.

B. Switching Times and Speed

The switching delay time presents large deviations with the temperature changing. Fig. 27 shows the turn-ON and turn-OFF delay times. According to (6) and (7), the main temperature parameters are R_{G} and V_{Miller}. Both parameters are negatively correlated with temperature. So, the turn-ON delay time presents a negative temperature coefficient. As for the turn-OFF delay time, the two factors contradict each other. The measurement

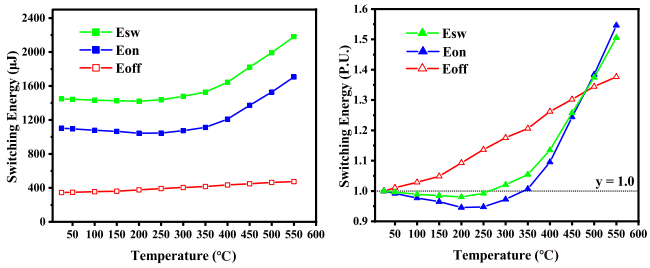

Fig. 28. The SiC MOSFET waveforms of the total switching energy, the turn-ON and turn-OFF switching energy. (a) The switching energy at different temperatures. (b) The normalized switching energy at different temperatures.

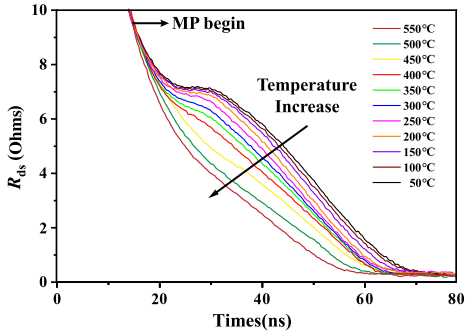

Fig. 29. Measured waveforms of the SiC MOSFET's drain-source resistance. The time difference of these waveforms at different temperatures are compensated based on the MP beginnings.

results demonstrate that the V_{Miller} sustains its predominant effect from 25 °C to 550 °C. Thus, the turn-OFF delay time presents a positive temperature coefficient.

The two electrical parameters have a good linear relationship with temperature. The normalized switching delay time [see Fig. 27(b)] shows the turn-OFF delay time features more temperature-sensitive than the turn-ON delay time. The absolute temperature coefficients are about 99.18 ps/°C and 13.26 ps/°C, respectively. The turn-OFF delay time presents higher sensitivity to the temperature in this switching speed and current class. So, it shows great potential in the online temperature measurement in SiC high-temperature applications.

The voltage rise time features quite an excellent positive linear relationship. It can be concluded that the V_{Miller} is dominated by temperature rise. The temperature sensitivity is about 8.87 ps/°C. As for the fall time, the measurement results show a nonlinear relationship that has not been reported by existing research. The fall time can be expressed as

$$t_{\mathrm{f}} = \frac{R_{\mathrm{G}} C_{\mathrm{GD\_av}}}{V_{\mathrm{g}} - V_{\mathrm{Miller}}} [V_{\mathrm{DC}} - I_{\mathrm{D}} R_{\mathrm{ds\_on}}(V_{\mathrm{Miller}})]. \tag{9}$$

Its detailed derivation can be found in the Appendix. Considering that R_{G} and V_{Miller} are negatively correlated with temperature, it is easy to conclude that the first term is negative temperature dependence. As for the second term, $R_{\mathrm{ds\_on}}(V_{\mathrm{Miller}})$ is the ON-resistance when the gate-source voltage equals the MP voltage at the end of the MP. Fig. 29 shows the drain-source resistance with different junction temperatures. In the whole MP, the R_{ds} decrease with junction temperature rising. It can be concluded that $R_{\mathrm{ds\_on}}(V_{\mathrm{Miller}})$ has a negative temperature

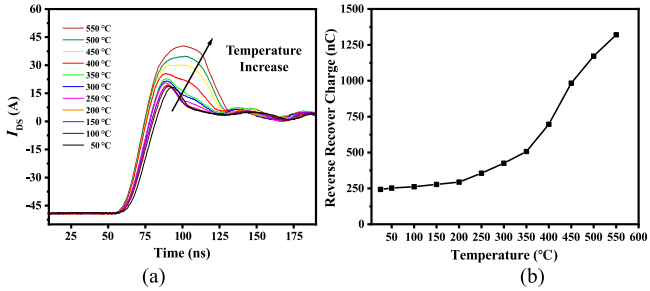

Fig. 30. The SiC MOSFET's body diode waveforms of the recovery current at different temperatures. (a) The transient current. (b) The reverse recovery charges.

correlation. Therefore, the temperature correlation of the fall time depends on which of the two terms dominates. In this DPT, the fall time increases first and then decreases with the junction temperature rising at the load current of 50 A. The absolute temperature coefficients are about 21.96 ps/°C at descending stage and 46.87 ps/°C at increasing stage. Noted that, the I_{D} in the second term affects the temperature coefficients. This finding reveals that using the fall time for junction temperature prediction is complicated.

C. Current Overshoot and Body Diode's Soft Recovery

Another apparent noticeable change is the current overshoot at the turn-ON transients. Because both the two SiC MOSFETs are heated together in the compact-interleaved HB power module, the reverse recovery effect of the upper switch's body diode affects the focused lower switch's turn-ON switching characteristics. The results show that the waveform is mutated after the junction temperature reaches 350 °C (see Fig. 30). The increase in reverse recovery time at stage V is most apparent. This phenomenon is usually called soft recovery. The main reason is that, the drift capacitance C_{D} dominates the recovery characteristics due to a lot of carriers in the drift region, thus the C_{D} becomes considerable with junction temperature rising. As for the soft recovery, the average damping ratio ξ^* can be given as [48]

$$\xi^* = \frac{1}{2}\sqrt{\frac{C_{\mathrm{D}}}{L}} \tag{10}$$

where the L is the packaging parasitic inductances. Thus, the reverse recovery process is over-damped, and the current decays with a low *di/dt* are produced. The large reverse recovery charge will contribute to the excessive power dissipation of the complementary switch. The long reverse recovery time will bring trouble in the high-frequency electronic applications.

D. Switching Energy

The turn-ON switching energy is predominant in the total energy loss (see Figs. 31 and 28). According to the following section, the reverse recovery of the complementary MOSFET'S body diode in a HB contributes to the main proportions in the total loss increase caused by rising junction temperature. Besides, the voltage fall time increase is also a contributing factor. In detail, Fig. 28(b) shows the growth rate of turn-ON

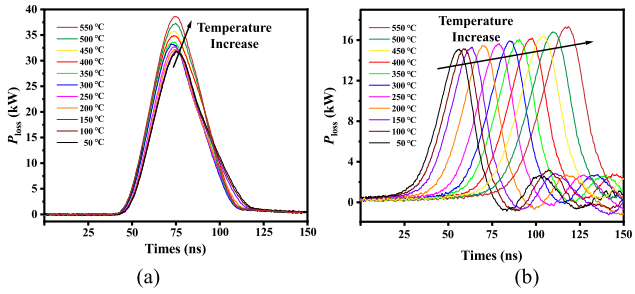

Fig. 31. The SiC MOSFET switching power waveforms. (a) The turn-ON transients. (b) The turn-OFF transients.

switching energy becomes more significant after 350°C (from 0.6574 μJ/°C to 3.296 μJ/°C). This is approximately consistent with the knee point in the increase of reverse recovery charge. Below the 350 °C, the trend of turn-ON switching energy is to fall first (about -0.3331 μJ/°C) and then rise. This is primarily related to the change of voltage fall time with junction temperature increasing (see Fig. 23).

As for the turn-OFF switching energy, it is weakly correlated with the temperature change (about 0.2588 μJ/°C). Thus, the total switching energy loss presents a trend consistent with the turn-OFF loss—it first drops, then rises, and then increases faster. The trend of switching energy is related to the silicon carbide materials with temperature changing. Under other operating conditions, the proportion of turn-ON and turn-OFF switching energy may change. But the trend will not diverge. It means that, there is an optimum point of switching energy during the high-temperature range from about 175 °C to 350 °C. As for the extreme high-temperature range (above 350 °C), the temperature variation characteristics of the body diode dominate the total switching energy.

In summary, the SiC device's total switching energy has an optimal temperature operating point over the test temperature range. The reason for the optimal "knee point" is the sharp increment in the reverse recovery charge of the body diode at extremely high temperatures and the nonmonotonic changes in the voltage fall time. For SiC high-temperature applications, especially in high-frequency operating conditions where switching energies dominate, this finding means a temperature range of 200 °C–300 °C will be the best operating temperature. If the junction temperature maintains an extremely high temperature (greater than 350 °C), the power electronic converter may have a thermal runaway due to the increasing switching energy with the temperature rising.

V. Power Electronic Converter Prototype

This section introduces the extreme-high-temperature electronic converter consisting of the compact-interleaved SiC power module, heatsinks [see Fig. 32(a)], high-temperature gate driver, and passive components [see Fig. 32(b)]. To evaluate the capability of power conversion at extremely high temperature, the converter prototype is tested under 250 °C ambient temperature and the SiC MOSFET's junction temperature is estimated to be approximately 400 °C.

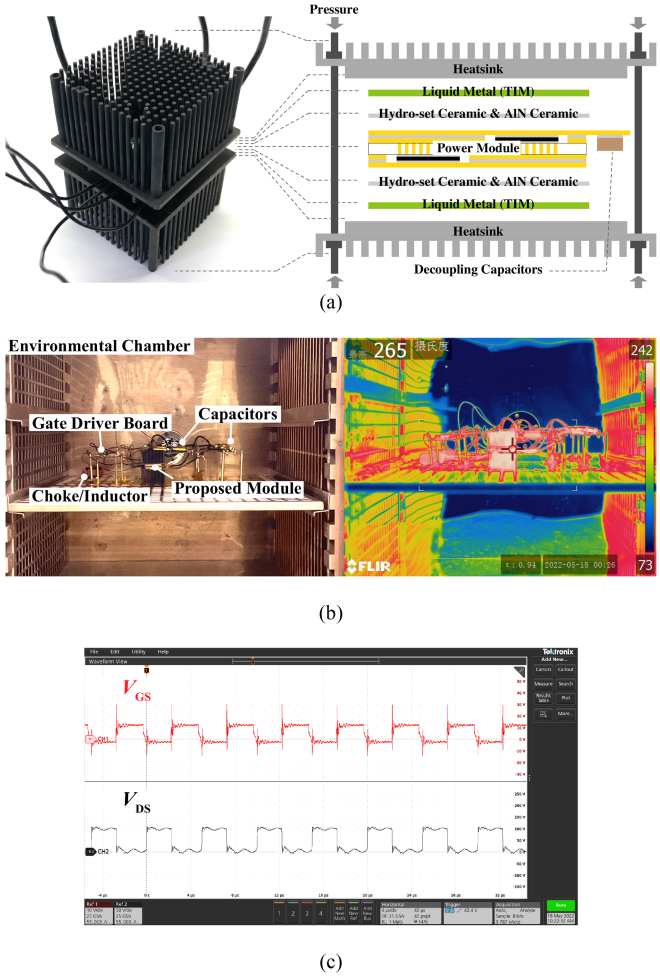

Fig. 32. The details of the high temperature SiC power electronic converter. (a) The compact-interleaved SiC power module with two heatsinks. (b) The converter prototype with the temperature distributions. (c) The recorded converter waveforms at extremely high junction temperature.

A. Development of the Converter Prototype

The compact-interleaved SiC power module is utilized in the buck converter. All components are selected after the evaluation of high-temperature characteristics. In detail, the choke/inductor is designed using the MPP (Fe-Ni-Mo) core with a relative permeability of 60 and a Curie temperature of 460 °C. The C0G ceramic and wet tantalum capacitor are chosen for decoupling, filtering, and energy storage. The core of the gate drive board adopts commercial high-temperature chips. We have tested and improved the entire driver board in a wide temperature range to ensure its driving stability.

Since there is very little research literature on SiC converters for extreme-high-temperature applications, we have carefully and conservatively designed the power ratings of the converters to prevent junction temperatures from exceeding our expectations. There are some reasons.

1) *Difficult to Directly Measure Junction Temperature*: The converter fixture is settled in an environmental chamber to replicate an extreme-high-temperature environment. Thermocouples (the contact-type measurement) must not be placed too close to

the power module to prevent the risk of insulation. The Infrared camera method requires opening the chamber's door and taking the measurement at a safe distance to prevent personnel from contacting the hot air.

2) *Lack of Effective Cooling Method at Extremely High Temperature*: The conventional forced cooling methods are unavailable, and there is no effective cooling method under extremely high temperature. This causes the junction temperature to easily exceed the limit.

3) Even though the components of the converter are elaborately designed, there is still no experience in operation at extremely high temperature.

4) There is predictable descent in the current capability of SiC power modules at extremely high temperature and low HTC. For the above reasons, we derate the converter.

We first conduct power experiments at room temperature to determine the temperature rise under specific losses. According to the approximately linear relationship between the ambient temperature and the junction temperature when the other cooling conditions remain unchanged, we can infer the approximate junction temperature under extremely high ambient temperature (we also conduct auxiliary inference through FEA simulations of ANSYS ICEPAK).

B. Experimental Results and Analysis of the Prototype

The buck converter prototype operates at 100 V input voltage, 50% duty ratio, 200 kHz switching frequency, and hard-switching mode. The gate ON and OFF resistances is 2.8 Ω and 5 Ω. The operating point is settled according to total losses of 50 W. The prototype first reaches the operating point at room temperature and is recorded the heat-sink temperature rise to provide data for junction temperature prediction. The surface of the heat-sink is sprayed with blackbody material to improve measurement accuracy. Then, the ambient temperature is raised (temperature rise stage) and the prototype continuously operates for 30 minutes at an ambient temperature of 250 °C (extreme-high-temperature operating stage). In the two stages mentioned, losses are strictly monitored.

Fig. 32(b) shows the converter prototype and the temperature distributions at the extreme-high-temperature operating stage. The temperature distribution shows that the maximum temperature of the converter is on the side surface of the power module, but it is only 265 °C. This is because the temperature distributions are measured at a long distance while the environmental chamber's door is opened. The convection of hot and cold air when the door is opened makes the temperature distributions of the converter prototype change drastically and the long-distance measurement position makes the non-negligible measurement errors. Therefore, we estimate by the linear relationship method mentioned before and FEA simulations. The estimated result is that the junction temperature is around 400 °C.

Fig. 32(c) shows the recorded converter waveforms at extremely high junction temperature, including the gate-source and drain-source voltage of the upper SiC switch in the HB. The compact-interleaved power module features DEMP, and the reliability and accuracy in protection and DESAT blanking time are guaranteed. However, since the probes cannot endure 250 °C, the voltage of the SiC chip can only be measured outside the chamber. Thus, we equate the potentials out of the chamber via wires. The length of these wires is about half a meter, so the obtained waveforms have non-negligible distortions. Even so, we can conclude from the recorded waveforms that the extreme-high-temperature converter can operate stably.

There are two points to note about converter losses. One is that the converter losses maintain unchanged at the extreme-high-temperature operating stage. This means that no thermal runaway occurs when the junction temperature is as high as 400 °C and the cooling conditions are poor. This conclusion is only valid under this operating condition. Part of the reason should be attributed to the high-temperature stability of SiC MOSFET and the lower current rating of this converter prototype. The other is that the converter losses are reduced by approximately 1 W at the temperature rise stage. Although the reduction is particularly small, it is unexpected. We think this is partly due to reduced switching losses in the proposed power module. Given the lower current rating and higher switching frequency of the converter prototype, switching energy dominate in the total power module losses. As the temperature increases, the total switching energy shows a trend of first decreasing and then increasing (see Section IV-D. The knee point will change under different operating conditions). Thus, the converter losses are slightly reduced.

In conclusion, the converter prototype, based on the compact-interleaved power module which is the key component, exhibits excellent extreme-high-temperature operation capability under these operating conditions. This validates the superiority of the packaging method.

VI. Conclusion

This article proposes a high-temperature packaging method called the compact-interleaved package for power modules. For dealing with the problems in the high-temperature applications, three considerations are presented, including the low packaging parameter design, DEMP, and high-temperature packaging material system. For the packaging parameters, it is necessary to make the SiC device feature low parasitic parameters to give full play to its superior characteristics. The simulated parasitic inductance is only 0.3370 nH of the main CCL and the capacitances are small enough. For the voltage measurement, the DEMP of the compact-interleaved power module effectively deals with an extra drain-source switching voltage of overshoot, drop, and turn-OFF noise. For the packaging material system, the optimized nanosilver sintered process for high-temperature applications is introduced. The shear strength after the aging test increases by three times. It means that the stability and reliability of nanosilver film have been greatly improved. The packaging materials also feature lower and similar CTE. In addition, the thermal performance analysis of the power module is also performed. Compered to SSC, The junction-to-case thermal resistance of the compact-interleaved DSC method decreases by nearly 50%, while the traditional double-sided modules are 29%–40%.

Based on the high-temperature compact-interleaved SiC power module, the dynamic characterization of 4H-SiC MOSFET at 50 °C–550 °C junction temperature and high switching speed is conducted. For the dynamic characterization via DPT, the extra inductances of the DPT fixture are reduced to 2.92 nH through the near decoupling method. By means of the superiority of the compact-interleaved power module and the high-temperature low-inductance fixture, the DUT is conducted to explore the extreme switching characteristics of SiC devices at 50 °C–550 °C and high switching speeds. From the experimental results, SiC MOSFET still maintains outstanding dynamic characteristics at extremely high temperatures. This shows the potential for future applications of SiC devices at extremely high temperatures. However, if we choose the body diode of the SiC MOSFET as a freewheeling diode in a HB module, this may be causing some problems at extremely high temperatures. For example, the reverse recovery currents' mutant at an extremely high temperature may cause positive feedback between switching energy and junction temperature, resulting in thermal runaway.

An extreme-high-temperature power electronic converter prototype is established at a low power level due to the cooling limitation. The prototype, including the proposed power module, gate driver board and passive devices, continuously operates at the ambient temperature of 250 °C for 30 min. And the estimated junction temperature of SiC dies is approximately 400 °C. Although there are still many unsolved problems in the SiC power device at extremely high temperature, the experimental results validate the superiority of the compact-interleaved packaging method and raised the potential application temperature range in the field of SiC power semiconductors.

APPENDIX

A. Effect of Kelvin Source Connection

Kelvin source connection improves the stability of the driving signal. Fig. 33(a) shows the turn-on switching transients without Kelvin source connection. When the device turns on, the $L_{\mathrm{Int\_S}}$ induces the voltage $V_{\mathrm{L}} = L_{\mathrm{Int\_S}} \cdot di_{\mathrm{D}}/dt$ to oppose current changes di_{D}/dt in the power loop. Meanwhile, the induced voltage V_{L} also exists in the gate driver loop. Thus, the gate-source voltage is

$$V_{\mathrm{GS}} = V_{\mathrm{P}} - R_{\mathrm{G}} I_{\mathrm{G}} - (L_{\mathrm{G}} + L_{\mathrm{Int\_G}} + L_{\mathrm{Int\_S}}) \cdot \frac{di_{\mathrm{G}}}{dt} - L_{\mathrm{Int\_S}} \cdot \frac{di_{\mathrm{D}}}{dt}. \tag{A1}$$

As shown in Fig. 33(b), $L_{\mathrm{Int\_S}}$ with Kelvin connection exists only in the power loop. The gate-source voltage is

$$V_{\mathrm{GS}} = V_{\mathrm{P}} - R_{\mathrm{G}} I_{\mathrm{G}} - (L_{\mathrm{G}} + L_{\mathrm{Int\_G}} + L_{\mathrm{S}}) \cdot \frac{di_{\mathrm{G}}}{dt}. \tag{A2}$$

Compared to (A1), the omitted term "$V_{\mathrm{L}} = L_{\mathrm{Int\_S}} \cdot di_{\mathrm{D}}/dt$" indicates there is no power-signal coupling effect that L_{S} couples "di_{D}/dt" of the power loop to the gate driver loop. Therefore, the stability of the drive signal is enhanced. The analysis process of the turn-off switching transients is similar.

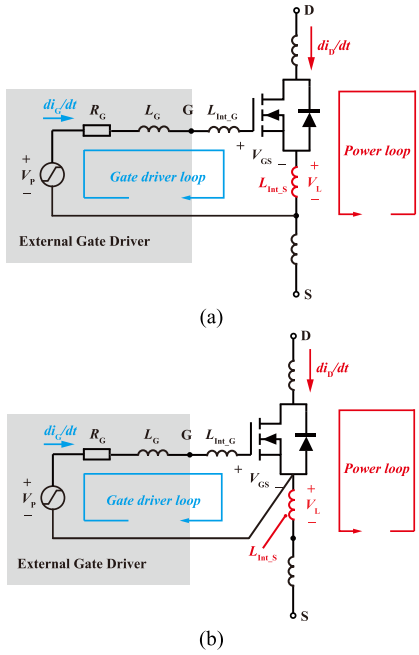

Fig. 33. The effect of Kelvin source connection. (a) The $L_{\mathrm{Int\_S}}$ couples the power and gate driver loop. (b) $L_{\mathrm{Int\_S}}$ exists only in the power loop utilizing Kelvin source connection.

B. Details of Waveform Deviations

1) Turn-off Voltage Overshoot: Fig. 34(a) shows the distributions of parasitic parameters where the C_H^* is the sum of junction and packaging capacitances paralleled with high-sided switches, the C_L^* is the sum of junction and packaging capacitances paralleled with low-sided switches, L_{A} and L_{C} are the parasitic inductances located at the diode's anode and cathode, respectively. For simplicity, the parasitic resistances are not shown. The following analysis object is the lower device that is being turned OFF. In the CCL, the equivalent frequency is very high at the turn-OFF transients, and the inductive reactance is much larger than the capacitive reactance. So, the parasitic capacitors in CCL can be considered a short-circuit. The frequency-domain equivalent circuit during the turn-OFF transients is shown in Fig. 34(b). The *di/dt* in CCL is clockwise because the current in the lower device is decreasing while the freewheeling current in the upper device is increasing at the same rate. According to Lenz's law, parasitic inductances induce voltage that hinders the current change. Note that the overshoot voltage is different from the deviation voltage obtained by the usual voltage measurement method. The difference can be written as

$$V_{\mathrm{DS}} - V_{\mathrm{Dev}} = V_{\mathrm{L1}} + V_{\mathrm{L2}}. \tag{B1}$$

This indicates that the actual voltage stress/overshoot on the bare die is bigger than the usual measurement results. The deviation degree depends on the proportion of the parasitic inductance from the measurement (usually includes packaging and fixture parasitic inductances) in the CCL's total parasitic inductances.

2) Turn-on Voltage Overshoot: Analysis of turn-ON transients is similar to turn-OFF transients. The di_{D}/dt in CCL is

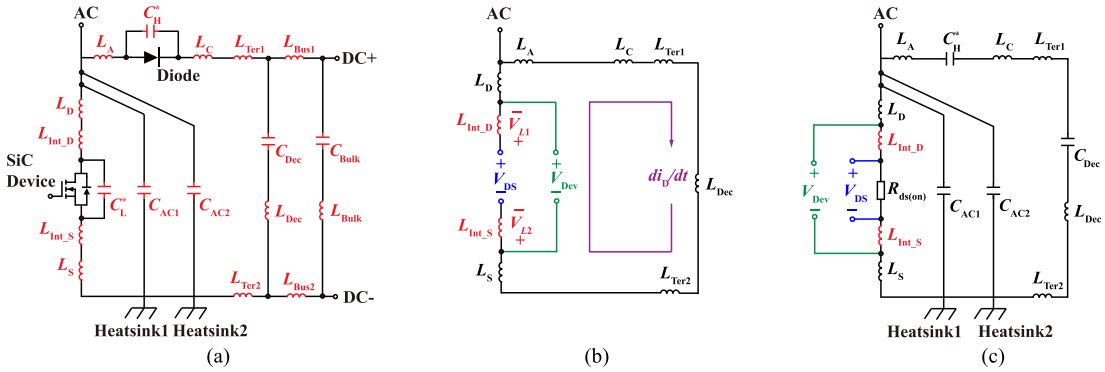

Fig. 34. The illustration for the waveform deviations. (a) The distributions of parasitic parameters in the half bridge (the parasitic resistances are not shown for simplicity). (b) The frequency-domain equivalent circuit during the turn-off transients (current change stage) of SiC device. (c) The frequency-domain equivalent circuit after the turn-on transients (ringing stage) of SiC device.

counter-clockwise. Thus, the difference can be written as

$$V_{\mathrm{DS}} - V_{\mathrm{Dev}} = -(V_{\mathrm{L1}} + V_{\mathrm{L2}}). \tag{B2}$$

This indicates that the actual voltage drop on the bare die is bigger than the usual measurement results at the turn-ON transients.

3) Ringing Noise: This deviation occurs after the turn-ON transients. Fig. 34(c) shows the frequency-domain equivalent circuit at the ringing stage. The device is equivalent to a resistor $R_{\mathrm{ds(on)}}$ because it is already conducting. The ringing frequency is generally tens of MHz, which is much less than the equivalent frequency of switching transients. The resonant loop consists of parasitic inductances, capacitances, and resistances (not shown). Ideally, the drain-source voltage at this stage is a constant value, that is $V_{\mathrm{DS}} = I_{\mathrm{D}} \cdot R_{\mathrm{ds(on)}}$. The deviations between V_{DS} and V_{Dev} can be obtained as

$$V_{\mathrm{DS}} - V_{\mathrm{Dev}} = V'_{\mathrm{L1}} + V'_{\mathrm{L2}} \tag{B3}$$

where V'_{L1} and V'_{L2} are the resonant voltages induced on the parasitic inductance L_1 and L_2. Therefore, the measured voltage often features redundant ringing noise.

C. High-Temperature Ceramic Capacitor Bank

Considering the ultralow parasitic inductances of the compact-interleaved power module, the DPT fixture and the module's power terminals that contribute most of the parasitic inductances in CCL can be decoupled by the bank. In the capacitor bank, three ceramic capacitors in the C0G dielectric are paralleled to reduce their inductances. The decoupling effect is verified by the FEA software named ANSYS Q3D. The compared setups are shown in Figs. 21 and 35. The parasitic inductances are reduced from 19.09 nH to 2.92 nH (about 6.5 times), consisting of the fixture's current conduction path, power module, and power terminals. A significant reduction in parasitic inductances facilitates the measurement of correct waveforms.

D. Derivation of Switching Time

The amplitude of the Drain voltage of SiC MOSFET remains at V_{g}, and the gate-drain capacitor also remains constant until the gate voltage reaches the amplitude of Miller voltage V_{Miller}. The

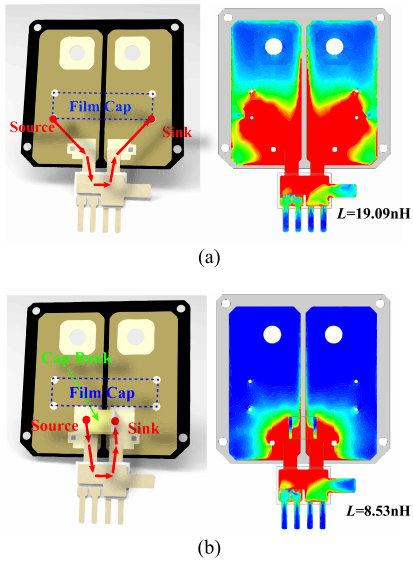

Fig. 35. The illustration for the position of capacitor bank (left) and the current distributions (right). The current density is the highest in red, lower in green and the lowest in blue. (a) The fixture without capacitor bank. (b) The fixture with capacitor bank.

gate voltage can be written as follows according to the capacitor charging law

$$V_{\mathrm{gs}}(t) = \left(V_{\mathrm{g}} - L_D^* \cdot \frac{di_{\mathrm{DS}}}{dt}\right) \cdot (1 - e^{-t/\tau}) \tag{D1}$$

where the $\tau = R_{\mathrm{G}}(C_{\mathrm{GS}} + C_{\mathrm{GD}})$ is the charging time constant, the $L_D^*$is the parasitic inductances of the SiC MOSFET drain. Because the ultralow parasitic inductances of the compact-interleaved power module and the reasonable setup of DPT, L_{D}^* can be ignored. Thus, (D1) can be rewritten as

$$t = -\tau \cdot \ln\left[\frac{V_{\mathrm{g}} - V_{\mathrm{gs}}(t)}{V_{\mathrm{g}}}\right]. \tag{D2}$$

The gate-source voltage remains at Miller voltage during the drain voltage decreasing interval. Thus, the rate of drain voltage decreasing is equal to the gate-drain voltage decreasing. Then,

the expression of the drain voltage over time $[t - t_{V_{\mathrm{DC(on)}}}]$ is

$$V_{\mathrm{ds}}[t - t_{V_{\mathrm{DC(on)}}}] = V_{\mathrm{DC}} - \frac{(V_{\mathrm{g}} - V_{\mathrm{Miller}}) \cdot [t - t_{V_{\mathrm{DC(on)}}}]}{R_{\mathrm{G}} C_{\mathrm{GD\_av}}} \quad \text{(D3)}$$

where the $C_{\mathrm{GD\_av}}$ is the constant average of the drain voltage decreasing interval; $t_{V_{\mathrm{DC(OFF)}}}$ is the moment when the drain voltage begins to fall or the gate voltage reaches the Miller voltage in the turn-ON transients; and R_{G} is the sum of external and internal resistances.

The voltage of fall time can be obtained as follows:

$$t_{\mathrm{f}} = \frac{R_{\mathrm{G}} C_{\mathrm{GD\_av}}}{V_{\mathrm{g}} - V_{\mathrm{Miller}}} [V_{\mathrm{DC}} - I_{\mathrm{D}} R_{\mathrm{ds\_on}}(V_{\mathrm{Miller}})] \quad \text{(D4)}$$

where the $R_{\mathrm{ds\_on}}(V_{\mathrm{Miller}})$ is the ON-resistance when the gate-source voltage is equal to the MP voltage. According to (D2), the moment when the drain voltage decreases from V_{DC} to $90\%V_{\mathrm{DC}}$ is

$$t_{90\%V_{\mathrm{DC}}} - t_{V_{\mathrm{DC}}} = \frac{0.1 V_{\mathrm{DC}} R_{\mathrm{G}} C_{\mathrm{GD\_av}}}{V_{\mathrm{g}} - V_{\mathrm{Miller}}} \quad \text{(D5)}$$

where $t_{V_{\mathrm{DC}}} = t_{V_{\mathrm{Miller}}}$ can be obtained by (D1).

The turn-ON delay time can be written as

$$\begin{aligned} t_{d(\mathrm{on})} &= t_{90\%V_{\mathrm{DC}}} - t_{10\%V_{\mathrm{g}}} \\ &= \tau \ln\left(\frac{0.9 V_{\mathrm{g}}}{V_{\mathrm{g}} - V_{\mathrm{Miller}}}\right) + \frac{0.1 V_{\mathrm{DC}} R_{\mathrm{G}} C_{\mathrm{GD\_av}}}{V_{\mathrm{g}} - V_{\mathrm{Miller}}}. \end{aligned} \quad \text{(D6)}$$

The derivation of the turn-OFF delay time is similar to the turn-OFF delay time. The following analyses are in the turn-OFF transients of SiC MOSFET. During the internal of descent from V_{g} to V_{Miller}, the gate voltage can be expressed as follows with the simplification

$$t = -\tau \cdot \ln\left[\frac{V_{\mathrm{gs}}(t)}{V_{\mathrm{g}}}\right]. \quad \text{(D7)}$$

Thus, the moments when the gate voltage decreases to 90% of V_{g} and reaches the Miller voltage can be obtained. During the drain voltage increasing interval, the gate-source voltage remains at Miller voltage, and all the gate current discharges the gate-drain capacitor with the unchanged charge of the gate-source. Thus, the rate of drain voltage increasing is equal to the gate-drain voltage increasing. Then, the expression of the drain voltage over time $[t - t_{V_{\mathrm{DC(off)}}}]$ is

$$V_{\mathrm{ds}}[t - t_{V_{\mathrm{DC(off)}}}] = V_{\mathrm{Rds(on)}} + \frac{V_{\mathrm{Miller}} \cdot [t - t_{V_{\mathrm{DC(off)}}}]}{R_{\mathrm{G}} C_{\mathrm{GD\_av}}} \quad \text{(D8)}$$

where $t_{V_{\mathrm{DC(OFF)}}}$ is the moment when the drain voltage begins to increase or the gate voltage reaches the Miller voltage in the turn-OFF transients. The voltage of rise time can be obtained as follows:

$$t_{\mathrm{V}} = R_{\mathrm{G}} C_{\mathrm{GD\_av}} \frac{V_{\mathrm{DC}} + V_{\mathrm{FD}} - V_{\mathrm{Rds(on)}}}{V_{\mathrm{Miller}}} \quad \text{(D9)}$$

where the V_{FD} is a voltage drop of the complementary MOSFET'S body diode.

According to the linear variation of drain voltage, the moment when the drain voltage increases form $V_{\mathrm{Rds(on)}}$ to $10\%V_{\mathrm{DC}}$ is

$$t_{10\%V_{\mathrm{DC}}} - t_{V_{\mathrm{Rds(on)}}} = \frac{[0.1 V_{\mathrm{DC}} - V_{\mathrm{Rds(on)}}] R_{\mathrm{G}} C_{\mathrm{GD\_av}}}{V_{\mathrm{Miller}}} \quad \text{(D10)}$$

where $t_{V_{\mathrm{Rds(on)}}} = t_{V_{\mathrm{Miller}}}$ is the moment when the drain voltage begins to increase from $V_{\mathrm{Rds(on)}}$ or the gate voltage reaches the Miller voltage in the turn-OFF transients

$$\begin{aligned} t_{d(\mathrm{off})} &= t_{10\%V_{\mathrm{DC}}} - t_{90\%V_{\mathrm{g}}} \\ &= \tau \ln\left(\frac{0.9 V_{\mathrm{g}}}{V_{\mathrm{Miller}}}\right) + \frac{(0.1 V_{\mathrm{DC}} - V_{\mathrm{Rds(on)}}) R_{\mathrm{G}} C_{\mathrm{GD\_av}}}{V_{\mathrm{Miller}}}. \end{aligned} \quad \text{(D11)}$$

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