Bidirectional Buck-Boost Converter Using Cascaded Energy Storage Modules Based on Cell Voltage Equalizers

Masatoshi Uno, *Member, IEEE*, Dexiao Cheng, Satoru Onodera, and Yuta Sasama

***Abstract*—Ordinary modular energy storage systems require cell- and module-level equalizers, in addition to a main bidirectional converter, increasing the system complexity and cost. This article proposes a bidirectional buck-boost converter using cascaded energy storage modules. Each module contains a cell-level equalizer with a half-bridge cell. The half-bridge cell in each module is utilized not only for the cell-level equalizer but also for the cascaded buck-boost converter. Module voltages are equalized by adjusting duty cycles of the half-bridge cells, allowing the elimination of dedicated module-level equalizers. Furthermore, the cascaded structure equivalently increases the switching frequency and reduces the inductor current ripple. An experimental charge-discharge cycling test using the prototype was performed for three electric double-layer capacitor modules. Cell and module voltages were gradually equalized during cycling, demonstrating the bidirectional power conversion and cell- and module-voltage equalization capabilities of the proposed converter.**

***Index Terms*—Buck-boost converter, cascaded converter, electric double-layer capacitor (EDLC), voltage equalizer, voltage imbalance.**

I. Introduction

VOLTAGES of series-connected energy storage cells, such as electric double-layer capacitors (EDLCs) and lithium-ion batteries, are gradually imbalanced due to component tolerance, uneven aging, nonuniform temperature conditions, etc. In voltage-imbalanced energy storage modules/systems, some cells might be over-charged or -discharged, which translates into premature deterioration and hazardous consequences of fire and, in the worst case, explosion [1], [2]. Hence, cell voltage equalization is indispensable to ensure years of safe operation of energy storage cells.

Various kinds of cell equalizers have been proposed and developed. Three representative cell equalization architectures are listed in Fig. 1. The most typical architecture is the adjacent cell-to-cell equalizers [see Fig. 1(a)] that are essentially nonisolated bidirectional converters, such as pulsewidth modulation converter [3], [4], [5] and switched capacitor converter (SCC) [6], [7], [8], [9], [10], [11]. The adjacent equalizers offer good modularity as the system can flexibly be scalded up by adding cells and equalizers. However, the number of equalizers is proportional to the cell count, and hence the system complexity tends to soar as the system scales up.

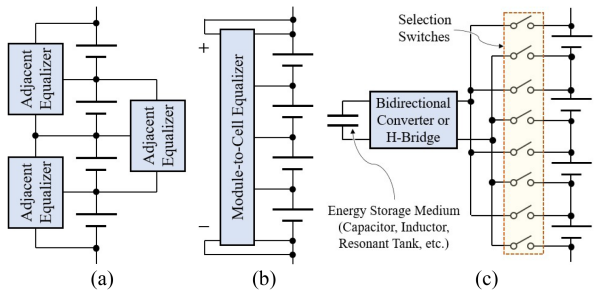

Fig. 1. Cell equalization architectures based on (a) adjacent cell-to-cell equalizer, (b) module-to-cell equalizer, and (c) selection switches.

Meanwhile, the module-to-cell equalizers [see Fig. 1(b)], which are based on a single-input–multi-output converter [12], [13], [14], [15], [16], [17], [18], can reduce the number of equalizers as each equalizer handles multiple cells. However, the modularity (or scalability) of module-to-cell equalizers is generally poor as the equalizers' design depends on the number of series-connected cells—equalizers must be redesigned every time the cell count changes.

The equalizers with selection switches [19], [20], [21], [22], [23], [24], also known as multicell to multicell equalizers, equalize cell voltages by transferring energies from the most charged cells to the least charged ones via the energy storage medium and bidirectional converter or H-bridge circuit [see Fig. 1(c)]. This architecture excels others in terms of volume thanks to the reduced passive component counts. However, the voltage stresses of selection switches are dependent on the module voltage or the number of cells connected in series, and therefore this architecture cannot flexibly be scaled up to large-scale systems.

SCC-based multicell to multicell equalizers without selection switches have also been proposed [25], [26]. Switch voltage stresses can be as low as cell voltages. However, voltage stresses of capacitors soar with the module voltage or the number of cells connected in series. Multicell to multicell equalizers using multiwinding transformers [27] do not suffer from the issues

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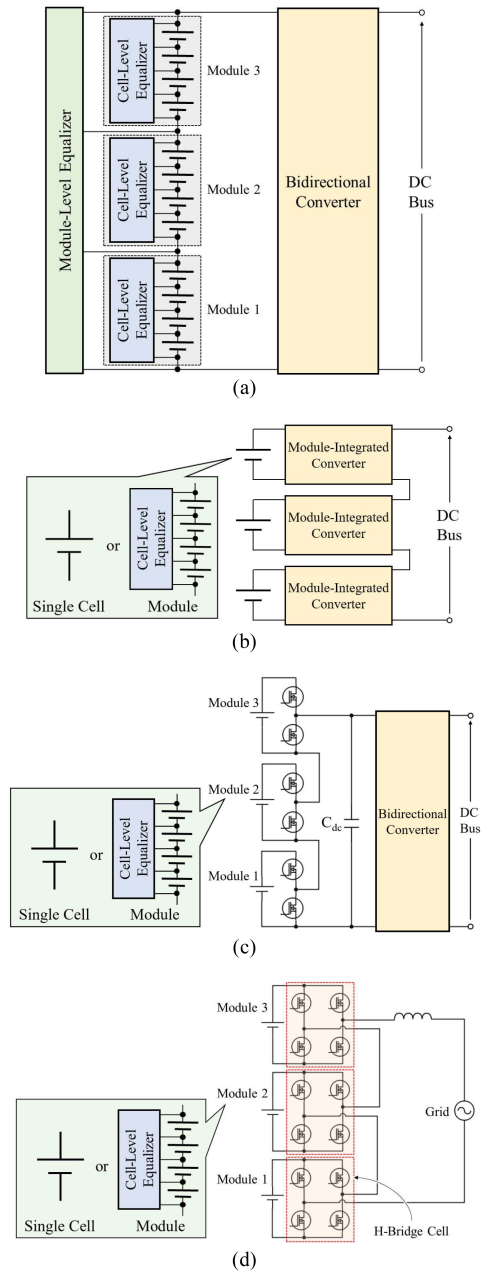

Fig. 2. Conventional energy storage systems using (a) cell- and module-level equalizers and bidirectional converter, (b) module-integrated converters, (c) reconfiguration circuit, and (d) cascaded multilevel converter.

of voltage stresses of switches and capacitors. The existence of a multi-winding transformer, however, is often cited as a top concern due to its design difficulty and poor modularity.

Modular energy storage systems with modular equalizers have also been proposed and developed [28], [29], [30], [31], [32], as shown in Fig. 2(a). The system comprises multiple modules, each consisting of series-connected cells and a cell-level equalizer. Cell voltages in each module are equalized by cell-level equalizers while module-level equalizers eliminate module voltage imbalance. This system allows different types of equalization architectures to be employed as cell- and module-level equalizers. For example, the module-to-cell equalizer [see Fig. 1(b)] is employed as the cell-level equalizer to simplify the

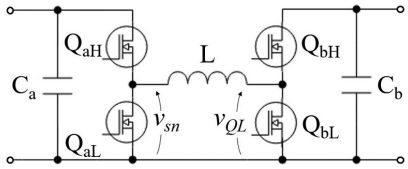

Fig. 3. Bidirectional noninverting buck-boost converter.

module design, while the adjacent module-to-module equalizers [see Fig. 1(a)] are used as module-level equalizers to realize good modularity. Although the modular system offers flexible system design and equalizer selections, a main bidirectional converter is necessary for charge-discharge regulation of the energy storage modules, in addition to cell- and module-level equalizers. The existence of three kinds of converters increases the system complexity and cost.

Distributed systems with module-integrated converters [33], [34], [35], [36] have also been proposed as a modular energy storage system, as shown in Fig. 2(b). Module-integrated converters perform charge-discharge regulation for modules (or cells) and voltage equalization. Although module-level equalizers are no longer necessary, the distributed system requires numerous module-integrated converters containing a bulky magnetic component (inductor or transformer) and a feedback control loop.

Reconfiguration circuits, shown in Fig. 2(c), are fully modular and can perform module-level equalization [37], [38]. The most charged modules are bypassed during charging, and so are the least charged modules during discharging. This system allows for reducing the converter count in comparison with Fig. 2(b). However, since the number of series-connected modules varies as some modules are bypassed during the equalization process, a bidirectional converter with a wide voltage range is necessary for this system.

Modular cascaded multilevel converters for grid-connected energy storage systems have been developed, as shown in Fig. 2(d) [39], [40], [41]. Energy storage modules, each with an H-bridge cell, are cascaded, and module voltages (or state of charges) are equalized by adjusting the duty cycles of H-bridge cells. This system is fully modular and suitable for circuit downsizing, as each H-bridge cell is inductor-less. However, this system is basically for ac systems, not for dc systems, and cell-level equalizers are still necessary because each H-bridge cell lacks cell-level equalization capability.

Meanwhile, a bidirectional converter is necessary for charge-discharge regulation in dc systems, as illustrated in Fig. 2(a)–(c). A noninverting buck-boost converter (see Fig. 3) is a suitable topology for energy storage modules with wide voltage variations, such as EDLCs. An inductor current ripple is proportional to the applied voltage amplitude and inverse of switching frequency. The inductor in the conventional buck-boost converters in Fig. 2(a) and (c) tends to be bulky as a sum of module voltages is applied to the inductor.

This article proposes a bidirectional buck-boost converter based on cascaded energy storage modules. Each module consists of series-connected cells and a module-to-cell equalizer with a half-bridge cell [18]. The half-bridge cell in each module is utilized not only for the module-to-cell equalizer but also

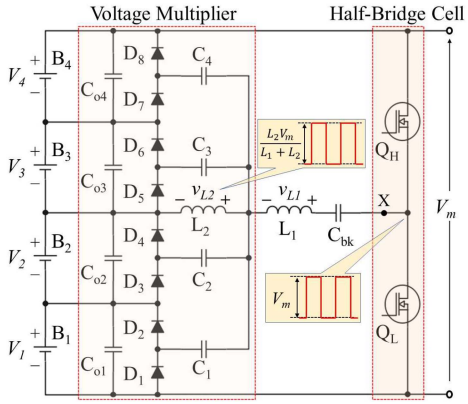

Fig. 4. Conventional transformerless module-to-cell equalizer (cell-level equalizer) for four cells connected in series [18].

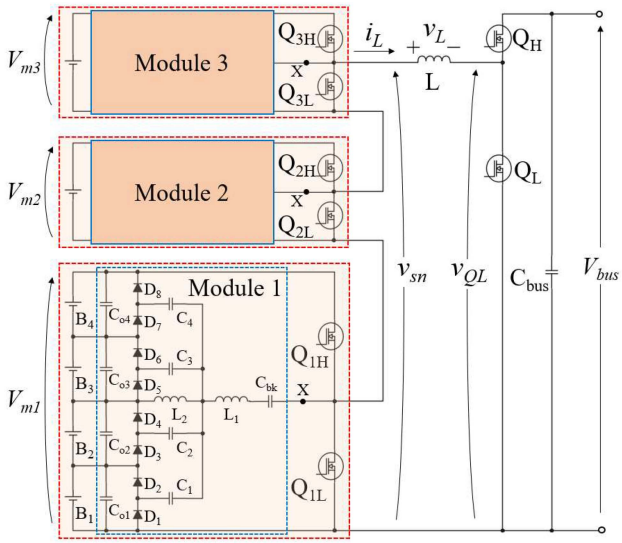

Fig. 5. Proposed bidirectional interleaved buck-boost converter using cascaded energy storage modules based on module-to-cell equalizers.

for the cascaded buck-boost converter. Module voltages are equalized by adjusting duty cycles of half-bridge cells, while module-to-cell equalizer automatically eliminates cell voltage imbalance. The cascaded structure allows for downsizing the inductor volume as it increases the driving frequency and decreases applied voltage amplitude.

The remainder of this article is organized as follows. Section II introduces and explains the proposed cascaded converter and its major features. Section III performs the operation analysis, followed by the discussion about the control system in Section IV. Experimental results of three EDLC modules are presented in Section V. Section IV discusses the comparison with converters in conventional systems.

II. Proposed Interleaved Bidirectional Converter

A. Module-to-Cell Equalizer (Cell-Level Equalizer)

The module-to-cell equalizer is the foundation of the proposed cascaded converter. Fig. 4 shows the transformerless module-to-cell equalizer for four cells [18]. This equalizer comprises a half-bridge cell and a voltage multiplier. The half-bridge cell generates a square wave voltage with an amplitude equal to the module voltage V_m. The voltage amplitude is divided to $V_m \times L_2/(L_1+L_2)$, by which the voltage multiplier is driven.

Driving the half-bridge cell automatically equalizes all the cell voltages without feedback control. An equalization current automatically flows toward the least charged cell(s) with the lowest voltage. The equalization current is dependent on the magnitude of $V_m \times L_2/(L_1+L_2)$. The cell-level equalization relies on diodes and capacitors in the voltage multiplier, and therefore component tolerance influences cell-level equalization performance to some extent. However, the previous work [18] as well as experimental results in this article (see Fig. 15) report that cell voltages can be adequately unified with a residual voltage imbalance less than a few ten millivolts.

The efficiency of the module-to-cell equalizer is low (reportedly around 60% [18]) chiefly because diode forward voltage drops take a significant portion of output voltages. However, such poor efficiency performance would not impair a system efficiency in practical use because cell equalizers handle negligibly small power compared to a main charge-discharge converter. A cell equalization current or power equivalent to one-hundreds of the main charge-discharge converter is generally considered sufficient to preclude cell voltage imbalance [42], [43].

The previous work reported the detailed operation analysis and equalization mechanism [18], and therefore, the remainder of this article does not deal with the module-to-cell equalizer.

B. Interleaved Buck-Boost Converter Using Cascaded Energy Storage Modules

Fig. 5 shows the proposed bidirectional buck-boost converter using cascaded energy storage modules. Three modules, each having a half-bridge cell, are cascaded. An inductor L is sandwiched by the top module (module 3) and right-hand half-bridge cell (Q_H-Q_L).

A dual interleaving operation is employed to drive half-bridge cells in the proposed converter. Half-bridge cells in the modules are driven in the interleaving manner with 360°/n out of phase where n being the module count. Hence, modules 1–3 (n = 3 in the case of Fig. 5) are driven 120° out of phase. The frequency of the square wave voltage v_{sn} at the node Q_{3H}-Q_{3L} is three times higher than the switching frequency of the modules. Accordingly, the right-hand half-bridge cell is driven at f_s, whereas the switching frequencies of the modules are f_s/3 so that the frequency of v_{sn} can be f_s. Furthermore, v_{sn} and v_{QL} are interleaved 180° out of phase to reduce the inductor current ripple. Thus, the dual interleaving operation shifts not only the phase among cascaded cells but also the phase between v_{sn} and v_{QL}.

Cell voltages in each module are automatically equalized by driving the respective half-bridge cell, as mentioned in Section II-A. Meanwhile, the module equalization is performed by actively adjusting the duty cycles of half-bridge cells. In other words, half-bridge cells in energy storage modules are utilized for cell- and module-level equalization, in addition to the

bidirectional buck-boost converter. Module voltages are actively equalized based on feedback control and individual module voltage measurement (see Fig. 11), achieving the module-level equalization unaffectedly by component tolerance. Detailed analysis and control strategy for the module voltage equalization will be discussed in Sections III and IV.

The fundamental structure of the proposed converter, except for module-to-cell equalizers, is equivalently the same as that of the conventional buck-boost converter (see Fig. 3)—L is sandwiched by two square waves of v_{sn} and v_{QL}. Hence, the dynamic characteristics of the proposed converter are expected to be similar to that of the conventional converter (see Appendix).

C. Features

The lack of module-level equalizers is the top benefit of the proposed converter. Adjusting the duty cycles of half-bridge cells achieve module-level equalization, and therefore, dedicated module-level equalizers is no longer necessary.

In addition to the elimination of the module-level equalizer, the reduced total switch count is also an appealing feature. The half-bridge cell in each module-to-cell equalizer is utilized not only for cell voltage equalization, but also for the bidirectional buck-boost converter. Hence, the total switch count can be reduced in comparison with the conventional system using bidirectional converter and equalizers separately (see Fig. 2).

The proposed converter also achieves inductor current ripple reduction. Driving modules in the interleaving manner (120° out of phase for three modules) equivalently increases the operating frequency of the inductor. In addition, the left-hand cascaded half-bridge cell and the right-hand half-bridge cell are also driven in the interleaving manner with 180° out of phase. The dual interleaving operation realizes a lower inductor current ripple than conventional buck-boost converters in a wide range of voltage conversion ratios. Although the cascaded structure may look identical to the reconfiguration circuit [see Fig. 2(c)], the operation principle totally differs. Cascaded half-bridge cells operate at high frequencies, and their duty cycles are adjusted to equalize module voltages (see Section IV-A for details), whereas the reconfiguration circuit bypasses some modules to equalize module voltages. The reconfiguration circuit does not contribute to inductor current ripple reduction because it is directly connected to a dc bus [see $C_{\rm dc}$ in Fig. 2(c)].

Switches are essentially driven in a hard switching manner, similar to those in the conventional systems in Fig. 2. However, voltage stresses of MOSFETs in the left-hand cascaded half-bridge cell are theoretically as low as module voltages. Hence, in comparison with a bidirectional converter in Fig. 2(a) and (c), the cascaded structure allows for reducing switching losses—the reduced switching losses can also be achieved by the conventional module-integrated and cascaded converters in Fig. 2(b) and (d). MOSFETs in the right-hand half-bridge cell, on the other hand, are exposed to as high as the bus voltage, and their voltage stresses cannot be reduced.

Switches in all modules must be driven at the same frequency with proper phase differences in order to achieve the interleaving operations. To this end, a central controller is necessary to generate gating signals for all modules. In other words, the proposed converter is considered not suitable for large-scale systems where distributed controllers are generally employed. The proposed converter would find applications in relatively small-scale energy storage systems where a central controller can handle all modules.

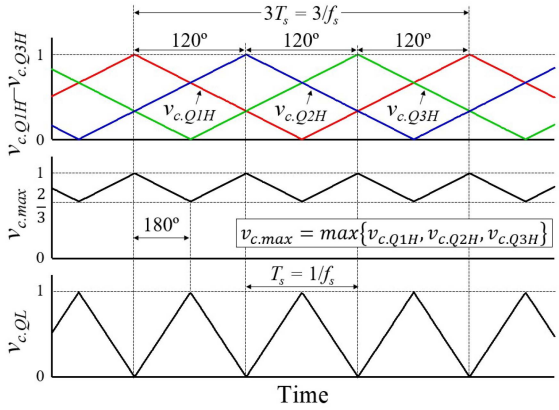

Fig. 6. Triangular carrier waves for Q_{1H}–Q_{3H} and Q_L.

III. Operation Analysis

Duty cycles of high-side switches Q_{1H}, Q_{2H}, and Q_{3H} are defined as d_{1H}, d_{2H}, and d_{3H}. The duty cycle of Q_L is d_L. In practical use, d_{1H}–d_{3H} are individually adjusted to equalize module voltages, and d_L is set equal to the average of d_{1H}–d_{3H} (see Section IV for details). However, this section performs operation analysis for the case that all module voltages are balanced and that modules discharge to the dc bus. Under the voltage-balanced conditions, $d = d_{1H} = d_{2H} = d_{3H} = d_L$ can be assumed, and all the module voltages are equalized as $V_{m1} = V_{m2} = V_{m3} = V_m$.

A. Carrier Waves for Dual Interleaving Operation

As briefly mentioned in Section II-B, three energy storage modules are driven 120° out of phase at $f_s/3$ so that the frequency of v_{sn} can be f_s. The right-hand half-bridge cell, on the other hand, is driven at f_s and 180° out of phase with v_{sn}.

Carrier waves for Q_{1H}–Q_{3H} and Q_L are illustrated in Fig. 6. Triangular carrier waves for Q_{1H}–Q_{3H}, $v_{c.Q1H}$–$v_{c.Q3H}$, are 120° out of phase. $v_{c.\max}$ is the maximum of $v_{c.Q1H}$–$v_{c.Q3H}$, which is defined as $v_{c.\max} = \max\{v_{c.Q1H}, v_{c.Q2H}, v_{c.Q3H}\}$, and its frequency is equal to f_s. It should be noted that $v_{c.\max}$ is a virtual carrier wave and is not used to generate gating signals. The triangular carrier wave for Q_L, $v_{c.QL}$, is 180° out of phase with $v_{c.\max}$. The frequency of $v_{c.QL}$ must be equal to that of $v_{c.\max}$ so that the left-hand cascaded half-bridge cell and right-hand half-bridge cell are driven in the interleaving manner.

B. Operation Conditions

The proposed converter operates either in six cases depending on duty cycle conditions. The boundary duty cycles are $d =$

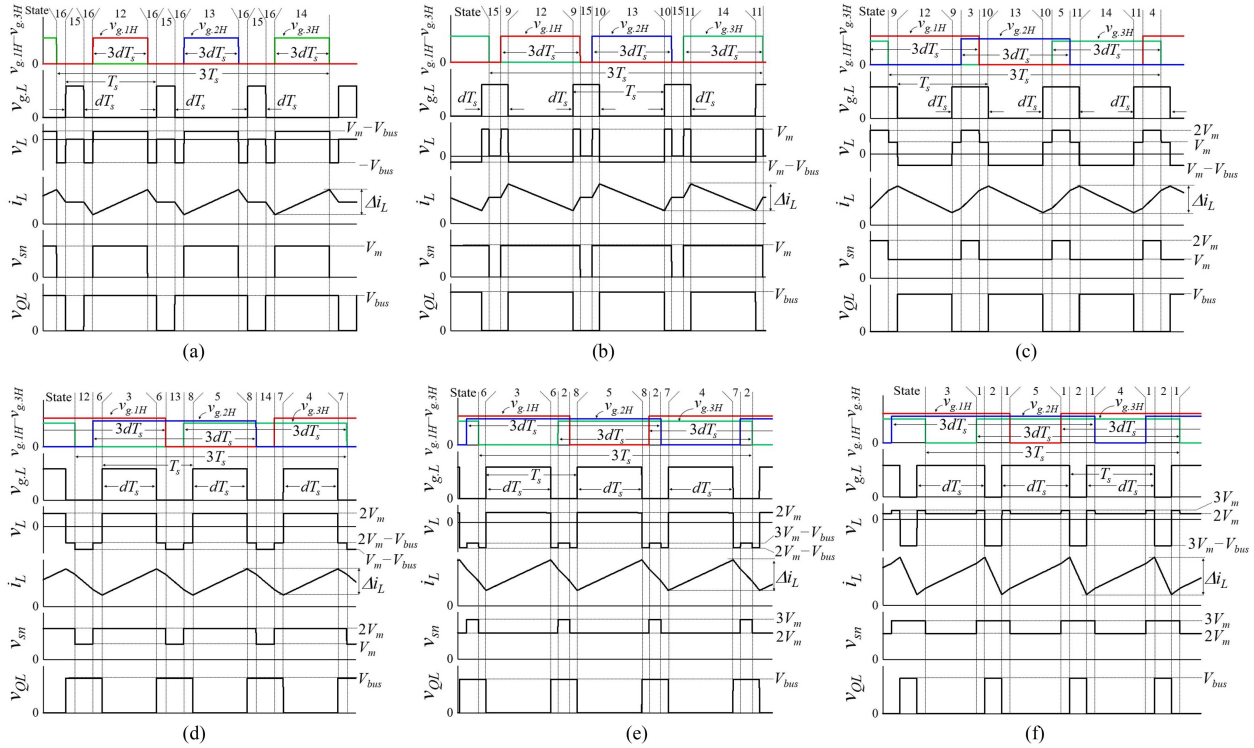

Fig. 7. Theoretical key operation waveforms in the case of (a) $0 < d < 0.25$, (b) $0.25 \le d < 0.33$, (c) $0.33 \le d < 0.5$, (d) $0.5 \le d < 0.67$, (e) $0.67 \le d < 0.75$, and (f) $0.75 \le d < 1$.

TABLE I
SWITCHING STATES, VOLTAGES, AND STATE LENGTH

State	Switch Status				Voltage			State Length					
	Q_{1H}	Q_{2H}	Q_{3H}	Q_L	v_{sn}	v_{QL}	v_L	$0<d<0.25$	$0.25<d<0.33$	$0.33<d<0.5$	$0.5<d<0.67$	$0.67<d<0.75$	$0.75<d<1.0$
1	1	1	1	1	$3V_m$	0	$3V_m$	-	-	-	-	-	$2d-3/2$
2	1	1	1	0	$3V_m$	V_{bus}	$3V_m-V_{bus}$	-	-	-	-	$3d-2$	$1-d$
3	1	1	0	1	$2V_m$	0	$2V_m$	-	-	$3d-1$	d	d	$3(1-d)$
4	1	0	1	1	$2V_m$	0	$2V_m$	-	-	$3d-1$	d	d	$3(1-d)$
5	0	1	1	1	$2V_m$	0	$2V_m$	-	-	$3d-1$	d	d	$3(1-d)$
6	1	1	0	0	$2V_m$	V_{bus}	$2V_m-V_{bus}$	-	-	-	$d-1/2$	$3/2-2d$	-
7	1	0	1	0	$2V_m$	V_{bus}	$2V_m-V_{bus}$	-	-	-	$d-1/2$	$3/2-2d$	-
8	0	1	1	0	$2V_m$	V_{bus}	$2V_m-V_{bus}$	-	-	-	$d-1/2$	$3/2-2d$	-
9	1	0	0	1	V_m	0	V_m	-	$2d/3-1/2$	$1/2-d$	-	-	-
10	0	1	0	1	V_m	0	V_m	-	$2d/3-1/2$	$1/2-d$	-	-	-
11	0	0	1	1	V_m	0	V_m	-	$2d/3-1/2$	$1/2-d$	-	-	-
12	1	0	0	0	V_m	V_{bus}	V_m-V_{bus}	$3d$	$1-d$	$1-d$	$2-3d$	-	-
13	0	1	0	0	V_m	V_{bus}	V_m-V_{bus}	$3d$	$1-d$	$1-d$	$2-3d$	-	-
14	0	0	1	0	V_m	V_{bus}	V_m-V_{bus}	$3d$	$1-d$	$1-d$	$2-3d$	-	-
15	0	0	0	1	0	0	0	d	$1-d/3$	-	-	-	-
16	0	0	0	0	0	V_{bus}	$-V_{bus}$	$1/2-2d$	-	-	-	-	-

0.25, 0.33, 0.5, 0.67, and 0.75. Theoretical operation waveforms are shown in Fig. 7, where $v_{g.1H}$–$v_{g.3H}$ and $v_{g.L}$ are the gating signals of Q_{1H}–Q_{3H} and Q_L. The boundary duty cycles are determined by whether gating signals are overlapped. The boundaries of 0.33 and 0.67 originate from the overlapping of $v_{g.1H}$–$v_{g.3H}$. The boundaries of 0.25, 0.5, and 0.75 are relevant to the overlapping between $v_{g.1H}$–$v_{g.3H}$ and $v_{g.L}$.

Switching states, voltages, and state lengths are given in Table I, in which 1 and 0 stand for ON and OFF states. Current flow directions in each state are illustrated in Fig. 8. This subsection focuses only on the operation in $0.5 < d \le 0.67$ as a representative case [see Fig. 7(d)].

1) *States 3–5:* Two out of three modules are connected to L, and v_{sn} equals to $2V_m$. In State 3, for example, Q_{1H} and Q_{2H} are on, and modules 1 and 2 are discharging in series. At the same time, v_{QL} is 0 as Q_L is on. Hence, the inductor voltage v_L is $2V_m$ ($= v_{sn} - v_{QL}$), and the inductor current i_L linearly increases.

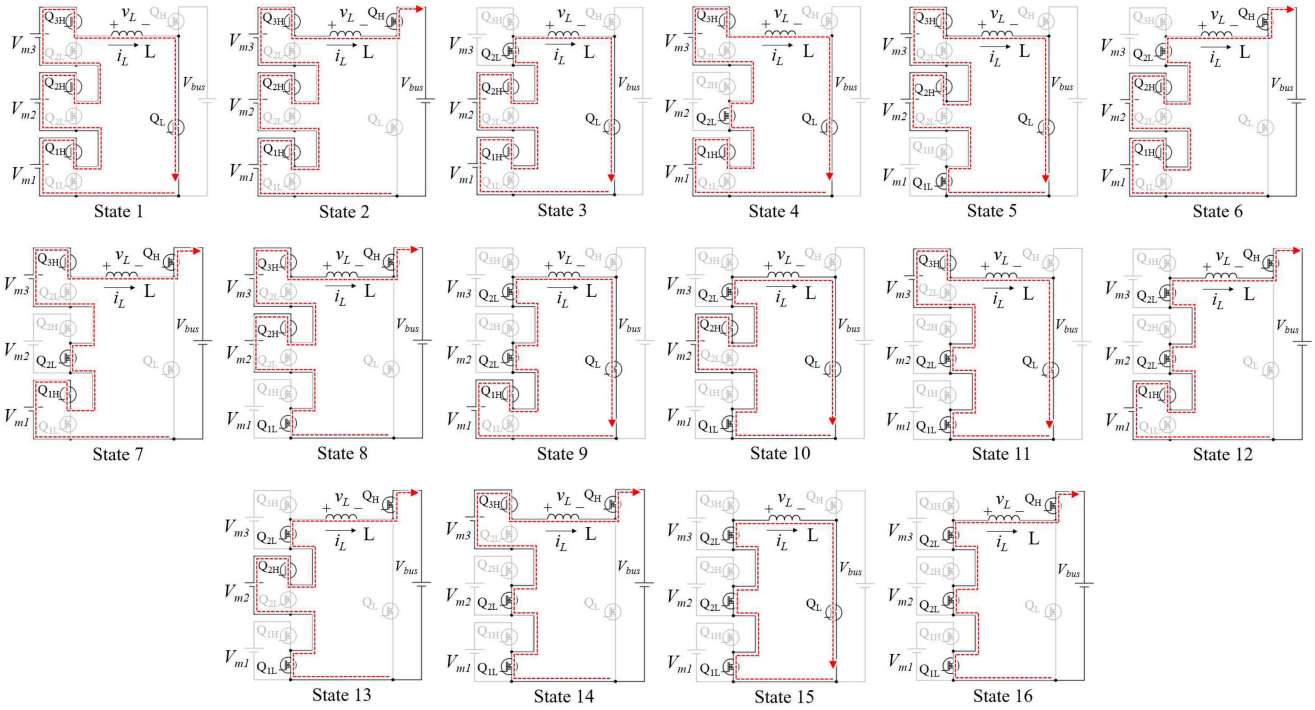

Fig. 8. Current flow directions in states 1–16.

2) *States 6–8:* Q_L and Q_H are turned off and on, respectively, and two out of three modules are discharging to the dc bus through L. As L is connected to the dc bus, v_{QL} is equal to the dc bus voltage $V_{\rm bus}$. Hence, v_L equals to $2V_m - V_{\rm bus}$, and i_L decreases.
3) *States 12–14:* Q_L and Q_H are off and on, respectively, and one out of three modules is discharging to the dc bus through L. v_{sn} decreased as low as V_m, and v_L becomes $V_m - V_{\rm bus}$.

C. Voltage Conversion Ratio

The average of v_L must be zero under steady-state conditions. From Table I, the volt-sec balance on L yields the following equation:

$$\overbrace{2V_m 3d}^{\text{State 3, 4,5}} + \overbrace{(2V_m - V_{\rm bus})\left(d - \frac{1}{2}\right)6}^{\text{State 6,7,8}} + \overbrace{(V_m - V_{\rm bus})(2-3d)3}^{\text{State 12,13,14}} = 0. \tag{1}$$

Rearrangement of (1) produces

$$\frac{V_{\rm bus}}{3V_m} = \frac{d}{1-d}. \tag{2}$$

This equation is identical to the voltage conversion ratio of the conventional buck-boost converter with an input voltage of $3V_m$.

This section has analyzed the case of $0.5 < d \leq 0.67$ only. Although other cases contain different operation modes, conversation ratios in other cases are identical to (2) because the same triangular carrier waves are used in all cases to generate gating signals, similar to traditional interleaving buck-boost converters [44].

D. Inductor Current Ripple

This subsection derives theoretical inductor current ripple Δi_L and compares it with the conventional buck-boost converter.

The longest state length in each case in Fig. 7 determines Δi_L. In the case of $0 < d \leq 0.25$ and $0.25 < d \leq 0.33$, for example, states 12–14 dictate Δi_L. From state lengths and v_L in each case (see Table I), Δi_L of the proposed converter can be derived as

$$\Delta i_L = \begin{cases} \frac{(V_m - V_{\rm bus})3dT_s}{L} & (0 < d \leq 0.25) \\ \frac{(V_{\rm bus} - V_m)(1-d)T_s}{L} & (0.25 < d \leq 0.5) \\ \frac{2V_m dT_s}{L} & (0.5 < d \leq 0.75) \\ \frac{(V_{\rm bus} - 3V_m)(1-d)T_s}{L} & (0.75 < d \leq 1) \end{cases}. \tag{3}$$

This set of equations assumes all module voltages are uniform. If module voltages are imbalanced, Δi_L deviates from (3) as d of each module is adjusted depending on the degree of module voltage imbalance, as will be detailed in Section IV-A—according to (7) and (8), $\pm$ 10% voltage imbalance, for example, corresponds to $d \pm 10\%$. Hence, applying $V_m \pm 10\%$ and $d \pm 10\%$ would roughly determine Δi_L under such voltage imbalance conditions.

In order to compare with conventional buck-boost converters in different operation conditions, Δi_L is normalized by

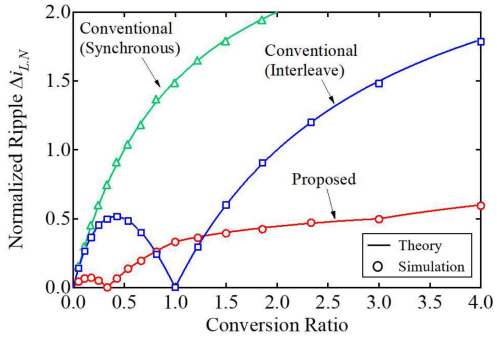

Fig. 9. Normalized inductor current ripples of proposed and conventional buck-boost converters.

$3V_mT_s/L$—the total input voltage of the proposed converter is $3V_m$. Substituting (2) into (3) yields the normalized inductor current ripple, $\Delta i_{L.N}$, as

$$\Delta i_{L.N} = \begin{cases} \frac{d(1-4d)}{1-d} & (0 < d \le 0.25) \\ \frac{4d-1}{3} & (0.25 < d \le 0.5) \\ \frac{2d}{3} & (0.5 < d \le 0.75) \\ 2d-1 & (0.75 < d \le 1) \end{cases}. \quad (4)$$

The conventional buck-boost converter (see Fig. 3) operates either in synchronous or interleaving modes [44]. Q_{aH} and Q_{bL} are synchronized in the synchronous mode. In the interleaving mode, on the other hand, Q_{aH} and Q_{bL} are driven 180° out of phase. Normalized inductor current ripples of the conventional converter in the synchronous and interleaving modes, $\Delta i_{L.\mathrm{sync}.N}$ and $\Delta i_{L.\mathrm{int}.N}$, are expressed as

$$\Delta i_{L.\mathrm{sync}.N} = 3d \quad (5)$$

$$\Delta i_{L.\mathrm{int}.N} = \begin{cases} \frac{3d(1-2d)}{1-d} & (0 < d \le 0.5) \\ 3(2d-1) & (0.5 < d \le 1) \end{cases}. \quad (6)$$

The coefficient 3 originates from that the conventional converters operate at $f_s/3$, which is equal to the frequency of cascaded modules in the proposed converter.

Fig. 9 compares the derived normalized inductor current ripples $\Delta i_{L.N}$ as a function of voltage conversion ratio. Theoretical models [see (4)–(6)] agreed well with the simulation results. $\Delta i_{L.N}$ of the proposed and conventional interleaved converters become zero at the conversion ratios of 0.33 and 1.0, respectively, thanks to the interleaving manner between the left- and right-hand half-bridge cells. The proposed converter achieves a lower ripple current in a wide range of conversion ratios.

E. System Extension

The proposed converter for the case of $n = 3$ (where n is the number of modules) has been analyzed in Section III. The system can be arbitrarily extended by adding modules with introducing n carrier waves that are 360°/n out of phase.

The proposed converter for $n = 4$ and its triangular carrier waves are shown in Fig. 10(a) and (b), respectively. The frequency of $v_{c.Q1H}$–$v_{c.Q4H}$ are one-fourth that of $v_{c.QL}$.

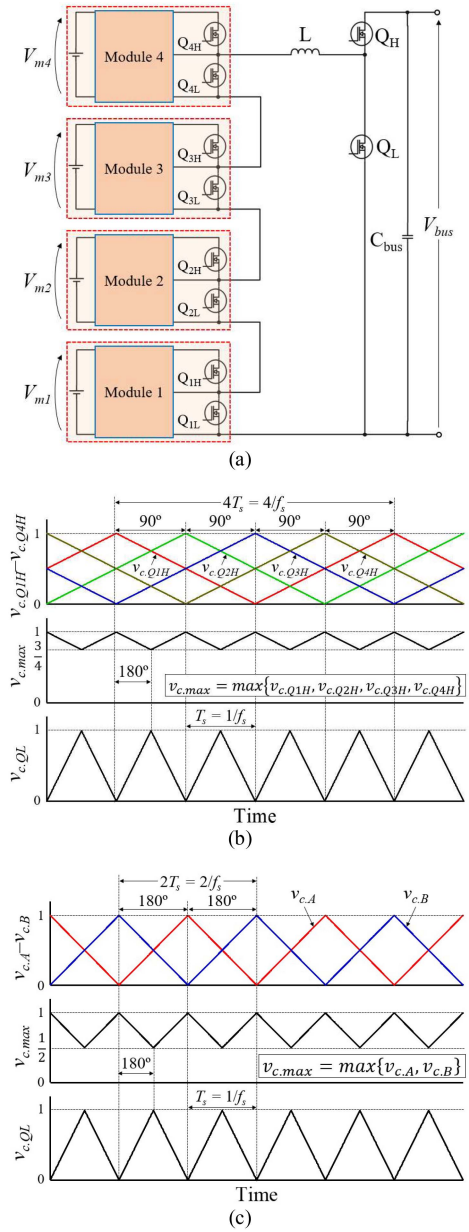

Fig. 10. (a) Proposed converter for four modules. (b) Carrier waves for ungrouped modules. (c) Carrier waves for grouped modules.

The inductor current ripple tends to decrease as n increases. However, the switching frequency of each module is f_s/n and, therefore, is prone to decrease. The lower the frequency, the larger will be the passive component volume in each module-to-cell equalizer. This tendency implies that passive components in module-to-cell equalizers would be bulky as the system extends.

To avoid the decrease in the modules' switching frequency, multiple modules can be grouped and synchronized. In the case of $n = 4$, two modules are grouped (e.g., modules 1 and 2 belong to group A, and modules 3 and 4 belong to group B) and are synchronized. Carrier waves for grouped modules are exemplified in Fig. 10(c). Carrier waves for groups A and B are $v_{c.A}$ and $v_{c.B}$. Modules in group A are synchronized, and so

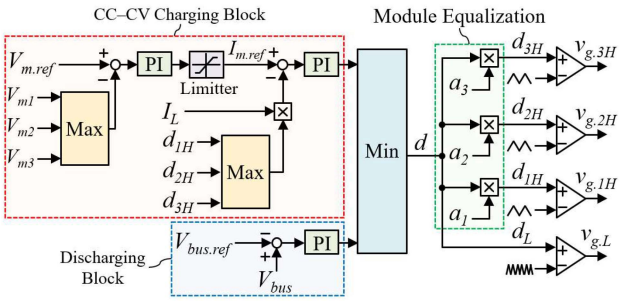

Fig. 11. Control block diagram.

are modules in group B. Frequencies of $v_{c.A}$ and $v_{c.B}$ are $f_s/2$, thus avoiding the frequency decrease.

This grouping technique is feasible if n is divisible. However, systems with a prime number of n (= 2, 3, 5, 7 …) cannot be divided into groups.

IV. Control System

The control block diagram for the proposed converter is shown in Fig. 11. It should be noted that this control system regulates either a module voltage, module current, or bus voltage, and that cell equalization is independently performed by each module-to-cell equalizer without feedback control. The control system consists of the constant-current–constant-voltage (CC–CV) charging block, discharging block, and module equalization block. The minimum function (Min) selects either the CC–CV charging or discharging blocks, depending on the conditions of V_{m1}–V_{m3} and $V_{\rm bus}$. The minimum function outputs the duty cycle d to the module equalization block. Module voltages are equalized by adjusting d_{1H}–d_{3H}. The imbalance coefficients a_1–a_3, which reflect the degree of module voltage imbalance, are introduced and multiplied by d to generate d_{1H}–d_{3H}.

A. Module Equalization

The module-level equalization is performed by adjusting the duty cycles of Q_{1H}–Q_{3H}, d_{1H}–d_{3H}. To this end, the imbalance coefficients, a_1–a_3, which are proportional to the degree of module voltage imbalance, are introduced. a_1–a_3 are defined as the ratio of the module voltage V_{mj} ($j = 1 \ldots 3$) to the average module voltage $V_{m.\rm ave}$, as

$$a_j = \begin{cases} 1 - \frac{V_{mj} - V_{m.\rm ave}}{V_{m.\rm ave}} & \text{(Charging)} \\ 1 + \frac{V_{mj} - V_{m.\rm ave}}{V_{m.ave}} & \text{(Discharging)} \end{cases}. \tag{7}$$

For example, for high-voltage modules with $V_{mj} > V_{\rm ave}$, $a_j < 1.0$ during charging mode, and $a_j > 1.0$ during discharging mode. Similarly, for low-voltage modules with $V_{mj} < V_{\rm ave}$, $a_j > 1.0$ and $a_j < 1.0$ during charging and discharging modes, respectively.

The duty cycle d, which is outputted by either the CC–CV charging or discharging blocks, is multiplied by a_j to generate the duty cycle of the high-side switch for the jth module, d_{jH}, as

$$d_{jH} = a_j d. \tag{8}$$

The average current of the jth module, $I_{m.j}$, is expressed by

$$I_{mj} = d_{jH} I_L = a_j d I_L \tag{9}$$

where I_L is the average inductor current. This equation indicates that module current I_{mj} can be adjusted depending on module voltage imbalance, which is expressed in the form of the imbalance coefficient a_j.

High-voltage modules ($V_{mj} > V_{\rm ave}$) operate with $a_j < 1.0$ during charging mode and $a_j < 1.0$ during discharging modes, which translates into less charging current and more discharging current. On the other hand, low-voltage modules ($V_{mj} < V_{\rm ave}$) operate with more charging current ($a_j > 1.0$) and less discharging current ($a_j < 1.0$). Such charging and discharging current adjustment eventually equalizes module voltages.

B. Control for CC–CV Charging and Discharging

The CC–CV charging block consists of the outer voltage control loop and inner current control loop. This charging block regulates either the voltage of the most charged module or the charging current of the least charged module.

The outer voltage control loop plays the role of regulating the voltage of the most charged module. Since the most charged module is most likely to be over-charged, the outer voltage control loop should regulate the most charged module to avoid overcharging. The voltage of the most charged module is higher than the others, and therefore the maximum function (Max) selects the highest voltage among V_{m1}–V_{m3} as a control target. The voltage reference $V_{m.\rm ref}$ corresponds to the CV charging voltage. The controller regulates only the highest voltage module, and therefore other module voltages do not reach the voltage level of $V_{m.\rm ref}$, especially when the voltage imbalance is severe. Regulating module voltages individually using separate voltage control loops would solve this issue, and it will be a part of our future works.

Meanwhile, the inner current control loop regulates the charging current of the least charged module. The charging current of the least charged module is the largest among all modules because of the imbalance coefficients a_j in the module equalization block, as explained in the following section. Since a module current I_{mj} is the product of I_L and d_{jH} [see (9)], the current of the least charged module can be calculated from the I_L and the highest duty cycle among d_{1H}–d_{3H}. The upper limit of the limiter generates a current reference $I_{m.\rm ref}$ that corresponds to the CC charging current of the least charged module. Module currents during the charging process are individually adjusted by the module equalization block using a_j, depending on the degree of module voltage imbalance. In other words, the charging current of the least charged module is regulated to be $I_{m.\rm ref}$, whereas other modules' currents are less due to a_j in the module equalization block.

The discharging block is a typical voltage control loop. The reference of $V_{\rm bus.ref}$ is set slightly lower than the nominal value of $V_{\rm bus}$. As long as the energy in the dc bus is sufficient for charging modules, $V_{\rm bus}$ is higher than $V_{\rm bus.ref}$. In such a case, the output signal from the discharging block is higher than that of the CC–CV charging block, and the minimum function (Min)

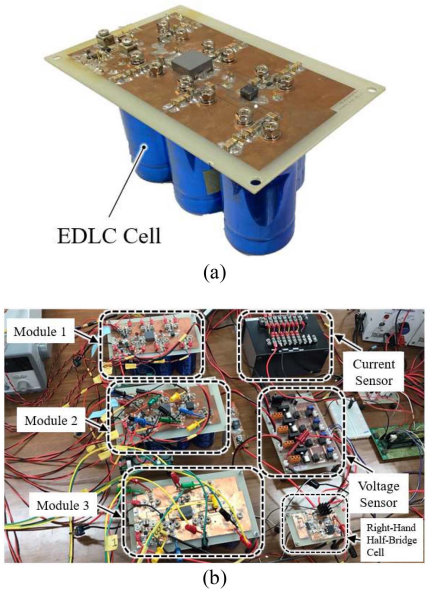

Fig. 12. (a) EDLC module with module-to-cell equalizer. (b) Experimental setup for three modules.

selects the charging block. In the case of insufficient energy in the dc bus, on the other hand, $V_{\rm bus}$ decreases. When $V_{\rm bus}$ decreases as low as $V_{\rm bus.ref}$, Min selects the discharging block to regulate $V_{\rm bus}$. In other words, the discharging block functions as an under-voltage protection for $V_{\rm bus}$. Even during discharging process, the module equalization block adjusts discharging currents of modules, depending on the degree of module voltage imbalance.

C. Control for Extended System

Sections IV-A and B dealt with the three-module system. The control system in Fig. 11 can be applied to an extended system consisting of more modules. For the four-module system [see Fig. 10(a)], for example, all the module voltages of V_{m1}–V_{m4} are individually measured, regardless of whether the ungrouped or grouped strategy is employed (see Section III-E). Duty cycles d_{1H}–d_{4H} are individually generated based on the calculated values of a_1–a_4, and therefore module voltages can be equalized. The ungrouped strategy uses four carrier waves ($v_{c.Q1H}$–$v_{c.Q4H}$) with 90° out of phase. The grouped strategy also uses four carrier waves, but they are grouped into two ($v_{c.A}$ and $v_{c.B}$) and are 180° out of phase.

V. Experimental Results

A. Prototype

The prototype of the module-to-cell equalizer for six EDLC cells is shown in Fig. 12(a). The experimental setup using three EDLC modules is shown in Fig. 12(b). Three EDLC modules and the right-hand half-bridge cell with L were connected using cables. Component values are given in Table II. 400-F cells with a rated charging voltage of 2.5 V were used for experiments. The prototype was operated at $f_s = 150$ kHz.

TABLE II
Component Values of Prototype

	Component	Value
Module	Q_{1H}, Q_{1L}	IRFP7341, R_{on} = 50 mΩ
	L_1	4.7 μH
	L_2	8.2 μH
	C_1–C_6	Ceramic capacitor, 94 μF
	D_1–D_{12}	Schottky Barrier Diode, V_f = 0.3 V
	C_{o1}–C_{o6}	Ceramic capacitor, 720 μF, 10 mΩ
	Gate Driver	IRS2184S
Right-Hand Half-Bridge Cell	L	47 μH, 160 mΩ
	Q_H, Q_L	FQD13N10, R_{on} = 180 mΩ
	$C_{\rm bus}$	Ceramic capacitor, 720 μF, 50 mΩ

B. Waveforms and Power Conversion Efficiency

Key waveforms and power conversion efficiency of the prototype were measured using 12-V regulated power supplies instead of EDLC modules. Module-to-cell equalizers were disabled by breaking the points X (see Figs. 4 and 5) to measure the characteristics of the cascaded buck-boost converter alone—the past work performed the detailed evaluation for the module-to-cell equalizer [18].

Measured key waveforms are shown in Fig. 13. Switching surge voltages were observed, especially in v_{sn}, because of the cables for connecting modules. However, the experimental results agreed well with the theoretical ones (see Fig. 7). Measured ripple currents Δi_L (see Fig. 13) also agreed satisfactorily with theoretical values of 0.26, 0.34, 1.02, 2.04, 2.38, and 3.06 A at $d = 0.2$, 0.3, 0.4, 0.6, 0.7, and 0.8, respectively, verifying the ripple current (3).

The measured and calculated power conversion efficiencies are shown in Fig. 14(a)—details of the theoretical loss model are not discussed in this article for the sake of page length. The peak efficiency was as high as 92% at 15 W, and the full load efficiency was 90%. The measured efficiency satisfactorily matched the calculated one.

The calculated loss breakdown at the output powers of 30 and 60 W are shown in Fig. 14(b). Conduction losses (Joule losses) were calculated based on the instantaneous current of i_L and component resistances (see Table II). i_L at 30 and 60 W were 1.46 and 2.92 A, respectively. Switching losses were determined from voltages and currents at the instant of switching—voltages of switches in the left- and right-hand bridge cells were 12 and 48 V, respectively, and instantaneous switch currents were equal to i_L. The fixed loss was experimentally measured and was equal to the no-load loss that includes the iron loss and parasitic capacitance loss. The major loss contributors were switches in the right-hand half-bridge cell (i.e., Q_L and Q_H) because these switches are exposed to relatively high voltage of 48 V. Meanwhile, losses of switches in modules (Q_{1L}–Q_{3L} and Q_{1H}–Q_{3H}) were minor as their voltage stresses are rather low due to the cascaded structure.

C. Charge-Discharge Cycling Test

The charge-discharge cycling test was performed from the initial condition that all module voltages as well as cell voltages

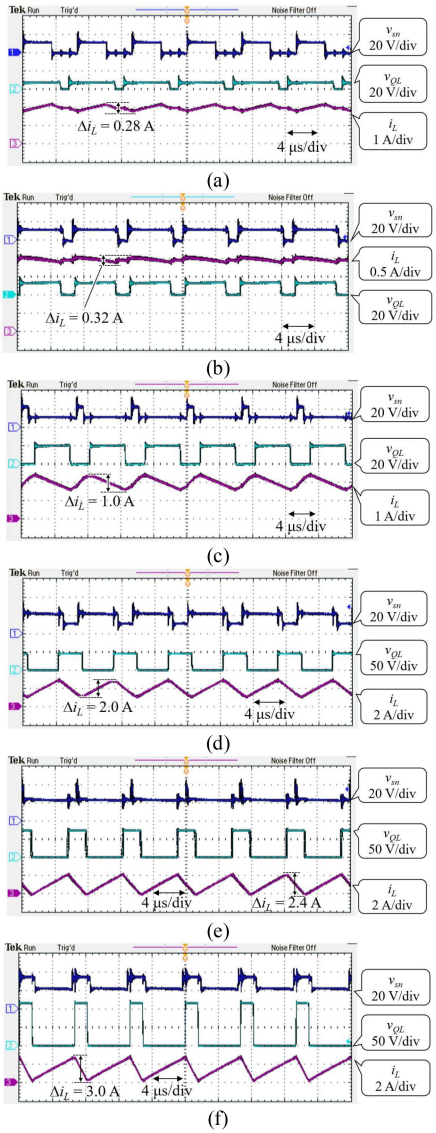

Fig. 13. Measured waveforms at (a) $d = 0.2$, (b) $d = 0.3$, (c) $d = 0.4$, (d) $d = 0.6$, (e) $d = 0.7$, and (f) $d = 0.8$.

in each module were severely imbalanced. The points X were closed to enable module-to-cell equalizers. A 34-V regulated power supply and a resistor were connected to the dc bus. During charging, the power supply was enabled, and the modules were charged with the CC–CV charging of 1.0 A–14 V ($I_{m.\mathrm{ref}} =$ 1.0 A and$V_{m.\mathrm{ref}} =$ 14 V). During discharging, on the other hand, the power supply was disabled, and the modules were discharged to the bus resistor with $V_{\mathrm{bus.ref}} = 33.8$ V. In general, the lower the cut-off voltage of EDLCs, the higher will be the energy utilization ratio—cut-off voltages equal to 0.5 and 0.32 of charging voltages correspond to 75% and 90% energy utilization ratios, respectively [45]. However, the converter may operate with an extreme duty cycle if the cut-off voltage is too low, as (2) indicates. Hence, the EDLC modules were discharged to as low as 7.0 V, half the charging voltage of 14 V. This cycling condition corresponds to 75% energy utilization ratio or 1.36 Wh variation per module (or 0.13 Ah variation per module).

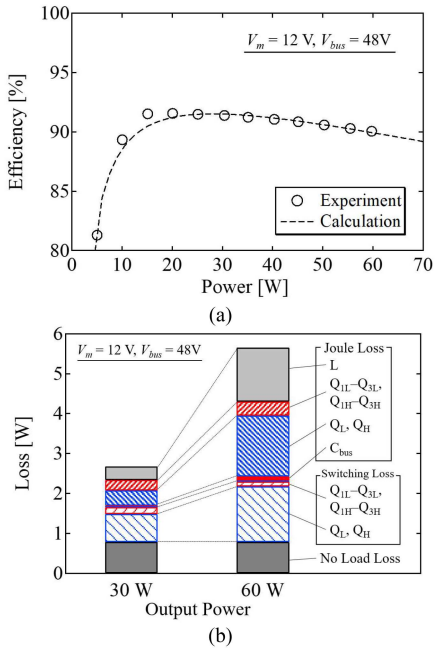

Fig. 14. (a) Measured power conversion efficiencies. (b) Calculated loss breakdown.

The resultant charge-discharge cycling profiles are shown in Fig. 15(a). Cell and module voltages in the results include impedance voltage drops due to equalization currents. Since an impedance of EDLCs is generally rather lower than that of lithium-ion batteries, EDLCs can be satisfactorily equalized even without compensating voltage drops. The highest module voltage was regulated to be 14 V during CV charging periods. Meanwhile, V_{bus} was regulated to be approximately 33.8 V during discharging, verifying the charge-discharge regulation of the proposed converter. Module voltage imbalance was gradually eliminated as cycling progressed. At the same time, cell voltages in each module were automatically equalized. The standard deviation of cell voltages decreased in the first few cycles but fluctuated in the range of 20–50 mV due to innate mismatch in EDLC capacitance—capacitance mismatch generates cell voltage imbalance during charge-discharge cycling.

Zoom-in charging profiles in the first cycle and discharging profiles in the last (fifth) cycle are shown in Fig. 15(b). The maximum cell voltage mismatch in the last cycle was reduced to less than 50 mV. Although a slight residual voltage mismatch was observed due to the capacitance mismatch, cell and module voltages were satisfactorily equalized while cycling, demonstrating the efficacy of the proposed converter.

VI. Comparison With Conventional Systems

This section compares the proposed converter with conventional ones in Fig. 2(a) and (b). It should be noted that cell- and module-level equalizers are excluded from the comparison as equalizers handle negligibly small power compared to main converters [42], [43]. All converters in the conventional systems are assumed to be based on the bidirectional buck-boost converter in Fig. 3.

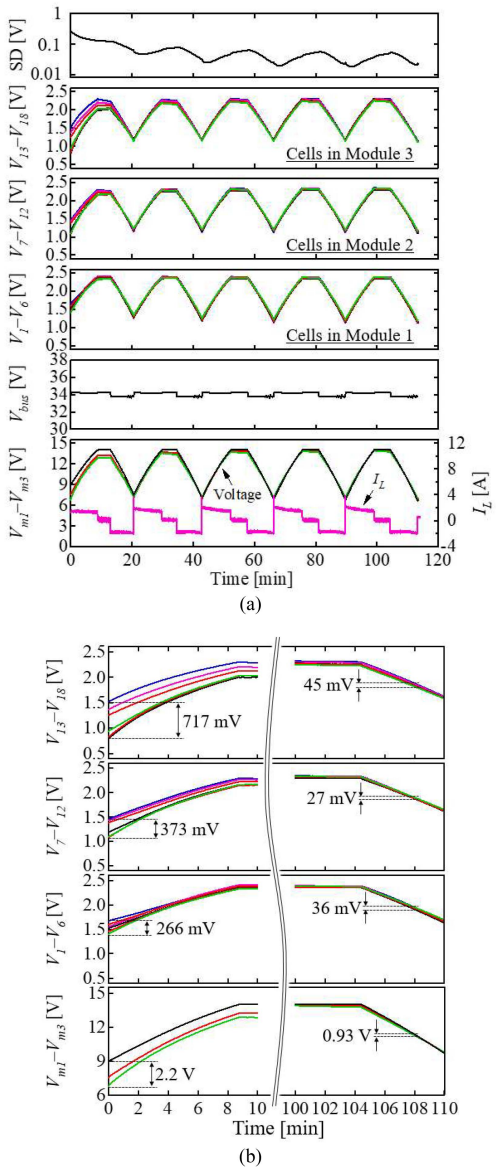

Fig. 15. (a) Experimental result of charge-discharge cycling test for three EDLC modules. (b) Zoomed-in charging profiles in the first cycle and discharging profiles in the last (fifth) cycle.

TABLE III
COMPARISON IN TERMS OF SWITCH COUNT, VOLTAGE AND CURRENT STRESSES, AND TDPR

System	Switch Count	Voltage Stress		Current Stress		TDPR
		Left-Hand	Right-Hand	Left-Hand	Right-Hand	
Fig. 2(a)	4	nV_m	V_{bus}	I_m/d	$I_{bus}/(1-d)$	$2P/\{d(1-d)\}$
Fig. 2(b)	$4n$	V_m	V_{bus}/n	I_m/d	$I_{bus}/(1-d)$	$2P/\{d(1-d)\}$
Proposed	$2n+2$	V_m	V_{bus}	I_m/d	$I_{bus}/(1-d)$	$2P/\{d(1-d)\}$

A. Switches

Table III compares the proposed and conventional converters for systems comprising n modules, from the viewpoints of the switch count, voltage and current stresses of switches. I_m and $I_{\rm bus}$ are the current of a module and bus, respectively. The converter in Fig. 2(a) can minimize the switch count as it consists of only four switches, regardless of n. However, switches must be rated for the total module voltage of nV_m or the full bus voltage $V_{\rm bus}$. The converter in Fig. 2(b) and the proposed converter can reduce voltage stresses, though the switch count increases. Meanwhile, the current stresses of all converters are identical.

The total device power rating (TDPR) is often introduced to quantitatively compare various topologies containing a different number of switches with different stresses [46], [47]. TDPR is defined as the total of voltage-current stresses of all semiconductor devices, as

$$\text{TDPR} = \sum_{\text{All Switches}} V_Q I_Q \tag{10}$$

where V_Q and I_Q are the voltage and current stresses, respectively. The lower the value of TDPR, the less amount of silicon will be used in a converter at a given power rating. TDPR values of all converters are the same, as given in Table III where P ($= nV_mI_m = V_{\rm bus}I_{\rm bus}$) is the input or output power of the converter. Despite the different switch count and voltage stresses, all converters are quantitatively comparable in terms of TDPR because all converters are based on the buck-boost converter in Fig. 3.

B. Inductors

The prototype of the proposed converter employed 47-μH inductor (see Table II) for the three-module system with $V_{\rm bus}$ = 34 V and V_m varying between 7.0 and 14 V. This condition was equivalent to the voltage conversion ratio between 0.81 and 1.62. Inductances of the conventional converters in the same condition were calculated. An 83-μH inductor is necessary for the converter in Fig. 2(a) to achieve the same ripple current Δi_L. The converter in Fig. 2(b) can reduce the inductance as low as 27.5 μH, though it necessitates three inductors in total as each converter contains one inductor.

In general, an inductor volume is proportional to stored energy in the form of $0.5LI^2$. Since the inductor peak current is the same in all converters, an inductor volume ratio is simply determined by an inductance ratio. Hence, the inductor volume of the proposed converter is expected to be 56.6% [= 47/83 = 47/(27.5×3)] that of conventional ones.

VII. CONCLUSION

This article has proposed the bidirectional buck-boost converter using cascaded energy storage modules. Each module is based on the module-to-cell equalizer having a half-bridge cell. The half-bridge cell in each module is utilized not only for the module-to-cell equalization but also for the cascaded buck-boost converter. Module-level equalization is performed by adjusting the duty cycles of half-bridge cells while cell voltages in each module can be automatically equalized by the module-to-cell equalizers. Thus, the half-bridge cells in energy storage modules are utilized for cell- and module-level equalization, in addition to the cascaded buck-boost converter.

Detailed operation analysis for the proposed converter comprising three energy storage modules was performed. Three cascaded modules are driven 120° out of phase to equivalently

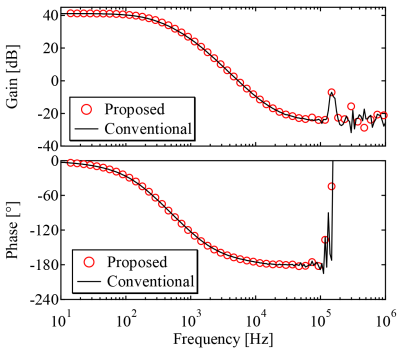

Fig. 16. Simulated control-to-output transfer functions of proposed and conventional buck-boost converter in discharging mode.

triple the switching frequency. At the same time, the left-hand cascaded cells and right-hand half-bridge cell are driven 180° out of phase. This dual interleaving operation realizes a lower inductor current ripple than conventional buck-boost converters in a wide range of voltage conversion ratios.

The experimental charge-discharge cycling test using three EDLC modules was performed from the voltage-imbalanced condition. The module voltage imbalance gradually disappeared as cycling progressed while the cell voltages in each module were automatically equalized.

APPENDIX

Control-to-output transfer functions of the proposed and conventional (see Fig. 3) buck-boost converters in discharging modes were measured in simulation analyses, as shown in Fig. 16. Component values in Table II and an actual internal resistance (10 mΩ/cell) of EDLCs were used for the analysis. Both converters operated with $V_m = 12$ V, $d = 0.6$ at $f_s = 150$ kHz, and the same component values were used. The proposed and conventional converters showed nearly identical characteristics, suggesting that their dynamic characteristics would be nearly identical.

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