Letters

An Active Power Ripple Mitigation Strategy for Three-Phase Grid-Tied Inverters Under Unbalanced Grid Voltages

Cheng-Yu Tang, *Member, IEEE*, and Jia-He Jheng

***Abstract*—This letter proposes an active power ripple mitigation strategy for the three-phase three-wire grid-tied inverter. Under the unbalanced grid voltage scenarios, the double-line frequency oscillation will have occurred on the inverter output power and the dc-link voltage. Traditionally, the three-phase four-wire or the three-phase four-leg topology could be adopted to deal with this issue. Besides, the negative and the zero-sequence current component can be controlled to cancel out the power ripple. However, the circuit cost and control complexity might be increased. Therefore, a virtual phase-current regulation (VPCR) method is developed by adding compensation to the current feedback of the fault voltage. The compensation value is consistent with the voltage drop ratio, which can effectively offset the actual power ripple. The main feature of the VPCR is its simplicity, whereas it can be realized via the digital signal processor without adding extra circuit components. Theoretical analysis and mathematical derivations of the VPCR will also be revealed. Finally, a 3 kW prototype circuit with both simulation and experimental results verify the performance and feasibility of the proposed strategy. The experimental results show that the output power ripple can be eliminated with 64.3% via the proposed VPCR.**

***Index Terms*—Power ripple mitigation, three-phase three-wire inverter, unbalanced grid voltages.**

I. Introduction

RECENTLY, because of the global warming issue, energy saving and the development of green energies have been paid highly addressed. Photovoltaic (PV) power is one of the most popular green energies. In order to transfer the PV energy to the power system, power electronic technologies should be included. Generally, the PV power system consists of two parts. The front-end maximum power point tracker (MPPT) ensures maximum PV energy harvesting. The rear-end inverter transfers the PV energy to the ac grid [1], [2], [3].

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The PV system is usually connected to the three-phase power system in medium and high power levels. Therefore, the three-phase grid-tied inverter should be included. However, under unbalanced grid voltage scenarios, the double-line frequency oscillation will have occurred on the inverter output power. Consequently, the dc-link voltage might have fluctuated whereas the PV output power will be unstable [4], [5]. Some methodologies are developed to deal with this issue. First, the three-phase four-wire inverter topology could be adopted. The zero-sequence current component on the fourth wire can be controlled to cancel out the active power ripple [6]. But the split dc-link capacitor voltage will be oscillated because of the zero-sequence current injection. Therefore, large dc-link capacitances are required. On the other hand, the three-phase four-leg topology could be adopted [7]. The dc-link voltage ripple could be suppressed via the control of the fourth leg. However, extra circuit components and control are required.

Some literatures focused on the three-phase three-wire topology under unbalanced grid voltage conditions [8], [9], [10], [11], [12]. In [8], five control strategies are proposed and analyzed under unbalanced grid voltages. The active and reactive power ripple can be eliminated via the five strategies. In other words, this letter proposed flexible power control under unbalanced grid faults. From the analysis of this literature, there might be a tradeoff between the current total harmonic distortion (THD) and the active/reactive power ripple cancellation capability. A control method of PV grid-connected inverter under grid voltage unbalanced drops was proposed in [9]. The negative sequence current is controlled to suppress the double-line frequency power oscillation. In [10], an improved direct power control (DPC) strategy of grid-connected inverters under unbalanced and harmonic grid conditions was developed. In this literature, the fifth and seventh harmonic voltage components are considered to regulate the average output power. Besides, both negative and harmonic current components were controlled to achieve alternative targets of the balanced/sinusoidal current and to smooth active/reactive output power. In addition, the negative sequence current was also considered in [11] for the grid-connection converter under the unbalanced grid condition. This literature revealed that the negative sequence current can reduce the current THD but significant double-line frequency oscillation will have occurred on the output power. In [12], a control strategy of grid-connected PV inverter under unbalanced voltage conditions

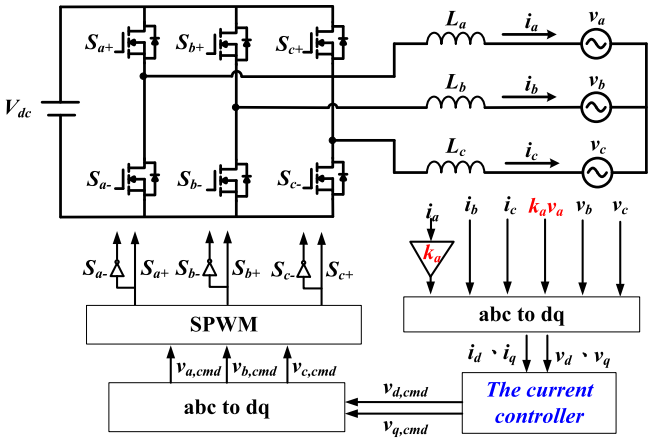

Fig. 1. Circuit diagram and control blocks of the proposed strategy.

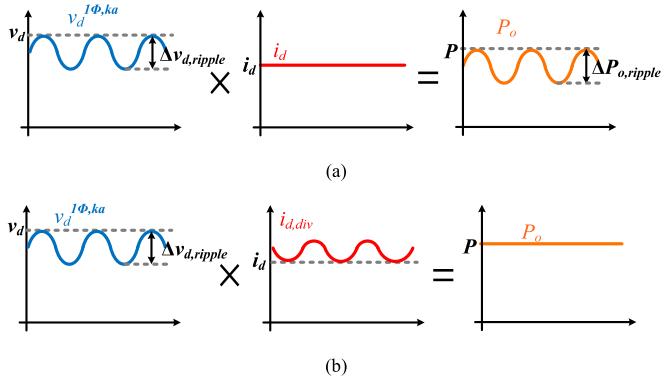

Fig. 2. Relations between the v_d, i_d, and P_o. (a) Without the active power ripple mitigation. (b) With the active power ripple mitigation.

was proposed. The active power ripple, reactive power ripple, and the current THD are taken into account. However, simulation results revealed that the suppressing of power ripple increases the current THD. The above methodologies can effectively solve the double-line frequency oscillation on the inverter output power and the dc-link voltage. Unfortunately, these methods might increase the circuit cost and control complexity, whereas the system stability might be decreased. Besides, there might be a tradeoff between the current THD and the power ripple cancellation performance.

In view of this, an active power ripple mitigation strategy is proposed in this letter. This strategy can be utilized for the conventional three-phase three-wire inverters. In addition, a virtual phase-current regulation (VPCR) method is developed in this strategy. With the VPCR, a feedback current gain will be included in the fault phase, whereas the gain ratio should be set the same as the grid voltage fault ratio. Eventually, the double-line frequency power oscillation can effectively be eliminated without complex control. The novelty and contributions of this letter can be summarized as: first, there is no need to modify the original control loop with the proposed VPCR. Second, the positive and negative sequence components are not necessary to be considered and controlled. Third, the VPCR can be realized by the digital signal processor (DSP) without adding extra circuit components. Fourth, output currents will not be distorted with the VPCR. In other words, the VPCR is developed with the feature of simplicity, whereas additional circuit cost and control complexity are not necessary. Theoretical analysis and mathematical derivations of the VPCR will also be revealed. Finally, the 3 kW prototype circuit with both simulation and experimental results verify the performance and feasibility of the proposed strategy.

II. Three-Phase Three-Wire Converter With VPCR

Fig. 1 shows the circuit diagram and control blocks of the proposed strategy. The three-phase three-wire inverter topology is adopted. The traditional direct-quadrature (d-q) transformation is utilized to control the inverter output active/reactive power. The three-phase voltages, v_a, v_b, v_c, and the three-phase currents, i_a, i_b, i_c, will be converted as v_d and i_d via the d-q transformation. Under unbalanced voltage scenarios, v_a, v_b, and v_c will not be equal to each other. Therefore, the double-line frequency oscillation will be occurred on v_d and P_o, as shown in Fig. 2(a). In order to cancel out the power ripple, i_d should be controlled as the inverted signal of v_d, as shown in Fig. 2(b). However, the magnitude and phase of i_d should precisely be controlled, which will be relatively complex. In order to simplify control, the VPCR is proposed. In this method, a virtual phase current gain, k_a, is included in the current feedback loop, whereas k_a is set the same as the phase voltage dropping ratio, as indicated in Fig. 1. Then, the compensated i_d signal will be automatically regulated by the VPCR. Eventually, the double-line frequency power ripple can be eliminated. In the following, detailed analysis and descriptions of the VPCR will be presented.

First, the d-axis voltage component, ${v_d}^{1\varphi,ka}$, under unbalanced grid voltages can be expressed as

$$
\begin{aligned}
{v_d}^{1\varphi,ka} &= \begin{bmatrix} k_a v_a \\ v_b \\ v_c \end{bmatrix} \left[P_k^d\right] = \begin{bmatrix} k_a v_d \cos(\omega t + \theta) \\ v_d \cos(\omega t + \theta - \frac{2\pi}{3}) \\ v_d \cos(\omega t + \theta + \frac{2\pi}{3}) \end{bmatrix} \\
&\times \left[\cos(\omega t) \cos\left(\omega t - \frac{2\pi}{3}\right) \cos\left(\omega t + \frac{2\pi}{3}\right)\right],
\end{aligned} \tag{1}
$$

where k_a is the voltage dropping ratio of a-phase. V_d is the d-axis voltage under normal condition. v_a, v_b, and v_c are the three-phase voltages under normal condition. $[P_k{}^d]$ is the park transformation matrix for the d-axis. Equation (1) can be simplified as (2).

$$
{v_d}^{1\varphi,ka} = \frac{k_a + 2}{3} v_d + \frac{k_a - 1}{3} v_d \cos(2\omega t). \tag{2}
$$

From (2), it can be confirmed that there will be both dc and ac components on v_d. In other words, P_o will be oscillated because of the fluctuated v_d and the constant i_d. In order to cancel out the power ripple, i_d should be regulated as the inverted signal of ${v_d}^{1\varphi,ka}$, as $i_{d,div}$ has shown in Fig. 2. It is possible to directly control the magnitude and phase of $i_{d,div}$. However, the control complexity will be increased while the system performance

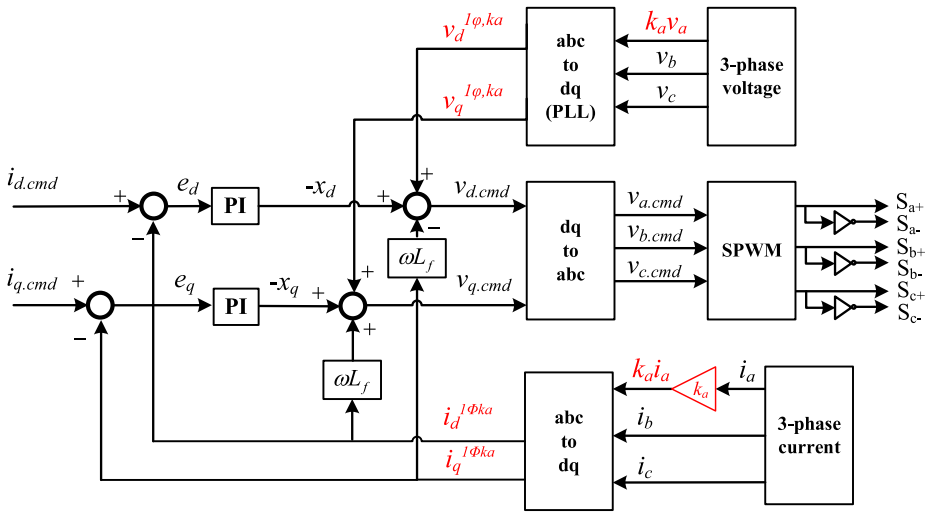

Fig. 3. Overall control block of the proposed VPCR.

might be decreased. On the other hand, with the proposed VPCR, it is no need to control $i_{d,div}$.

The overall control block of the VPCR is depicted in Fig. 3. In Fig. 3, it is assumed that v_a is the fault-phase, whereas the a-phase voltage is dropped and measured with the coefficient, k_a. With the VPCR, a virtual phase current gain, k_a, will be injected into the current feedback loop of the a-phase. Therefore, the controller will observe unbalanced three-phase currents on the feedback loop. On the other hand, because that $i_{d,cmd}$ and $i_{q,cmd}$ remain unchanged. Therefore, balanced three-phase current comments will be generated. To satisfy the balanced current commends, the a-phase current magnitude will be regulated with the ratio of $1/k_a$ (Because that k_a is included in the feedback loop in advance, the actual output current must be $1/k_a$ times to maintain balanced currents). Consequently, if the fault-phase voltage is decreased, the fault-phase current will be increased. On the contrary, if the fault-phase voltage is increased, the fault-phase current will be decreased. As a result, the power of the fault phase will be the same as the power of the two normal phases. That is to say, the output power of the three phases will be balanced while the active power ripple can be eliminated. In the following, the compensated current signals, ${i_d}^{1\varphi,ka,}$ and ${i_q}^{1\varphi,ka}$ will be pointed out for analysis.

The compensated current command on the d-axis, ${i_d}^{1\varphi,ka}$, can be expressed as (3).

$$
\begin{aligned}
{i_d}^{1\varphi,ka} &= \begin{bmatrix} i_{a,\text{gain}} \\ i_{b,\text{gain}} \\ i_{c,\text{gain}} \end{bmatrix} \left[P_k^d\right] = \begin{bmatrix} \frac{i_d}{k_a}\cos(\omega t) \\ i_d \cos(\omega t - \frac{2\pi}{3}) \\ i_d \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \\
&\times \left[\cos(\omega t)\cos\left(\omega t - \frac{2\pi}{3}\right)\cos\left(\omega t + \frac{2\pi}{3}\right)\right],
\end{aligned} \tag{3}
$$

where i_d is the origin current commend, $i_{a,\text{gain}}$, $i_{b,\text{gain}}$, and $i_{c,\text{gain}}$ are the ratios of i_d and k_a. It is worth mentioning that the k_a in (1) and (3) can be different to mitigate the ripple power. Besides, it is very simple to adjust the k_a value. Under the grid fault scenarios, the k_a value should be set the same as the voltage dropping ratio of the fault phase. If the fault-phase voltage reduces to 0.9 p.u., k_a should be 0.9. If the fault-phase voltage reduces to 0.7 p.u., k_a should be 0.7. If a-phase voltage reduces to 0.9 p.u. and b-phase voltage reduces to 0.7 p.u., k_a should be 0.9 for a-phase and 0.7 for b-phase.

After the rearrangement, (3) can be modified as follows:

$$
{i_d}^{1\varphi,ka} = \frac{2k_a+1}{3k_a} i_d + \frac{1-k_a}{3k_a} i_d \cos(2\omega t). \tag{4}
$$

With the combination of (2) and (4), the output power, P_o, can be calculated as follows:

$$
P_o = \frac{3}{2} {v_d}^{1\varphi,ka} \times {i_d}^{1\varphi,ka}. \tag{5}
$$

After the rearrangement of (2), (4), and (5), Po can be expressed as follows:

$$
\begin{aligned}
P_o &= \frac{3}{2} v_d i_d + \frac{(k_a-1)^2}{6k_a} v_d i_d \left[2 - \cos(2\omega t) - \cos^2(2\omega t)\right] \\
&= P + p_{o,VPCR},
\end{aligned} \tag{6}
$$

where $p_{o,\text{VPCR}}$ is the ripple power component with the proposed VPCR, which is the nonideal factor of P_o. In order to further analyze the effect of $p_{o,\text{VPCR}}$, the computer software, MATLAB, is utilized to depict $p_{o,\text{VPCR}}$, as shown in Fig. 4. It can be seen that there is a 2.25 times difference between the maximum and minimum value of $p_{o,\text{VPCR}}$. Besides, with the consideration of the non-ideal factor, $p_{o,\text{VPCR}}$, the diagram in Fig. 2(b) should be modified as Fig. 5.

III. Quantitative Analysis of the VPCR

The proposed VPCR can effectively mitigate the output power ripple under unbalanced grid voltages. However, the nonideal component, $\Delta P_{o,\text{VPCR}}$, cannot be neglected, whereas $\Delta P_{o,\text{VPCR}}$ might decrease the performance of the proposed strategy. Therefore, the quantitative analysis of the VPCR will be presented in this section. First, the ratio of the output power

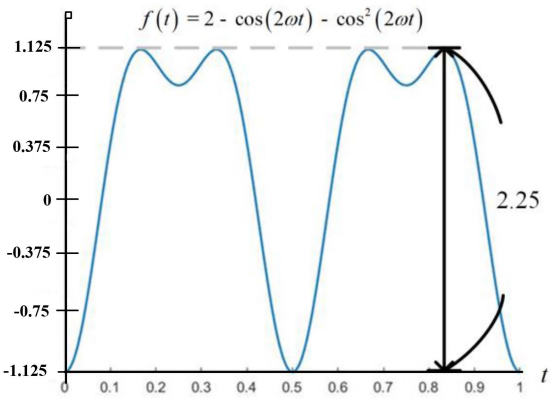

Fig. 4. Conceptual diagram of $p_{o,\mathrm{VPCR}}$ function.

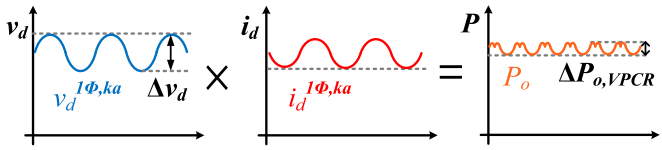

Fig. 5. Relations between v_d, i_d, and P with the VPCR.

TABLE I
K_{ERROR}, K_{VPCR}, AND K_{IMPROVE} UNDER DIFFERENT VOLTAGE FAULT CONDITIONS

k_a (p.u.)	0.9	0.8	0.7	0.6	0.5
k_{error} (%)	6.7	13.3	20	26.7	33.3
k_{VPCR} (%)	0.28	1.25	3.21	6.67	12.5
$k_{improve}$ (%)	95.8	90.6	83.9	75	62.5

ripple, $\Delta P_{o,\mathrm{ripple}}$ and the average output power, P_{avg}, without the VPCR is defined as follows:

$$k_{\mathrm{error}} = \frac{\Delta P_{o,\mathrm{ripple}}}{P_{\mathrm{avg}}} \times 100\% = 2 \times \frac{(1-k_a)}{3} \times 100\%. \quad (7)$$

Besides, the ratio of the output power ripple, $\Delta P_{o,\mathrm{VPCR}}$ and P with the VPCR can be expressed as follows:

$$k_{\mathrm{VPCR}} = \frac{\Delta P_{o,\mathrm{VPCR}}}{P_{\mathrm{avg}}} \times 100\% = 2.25 \times \frac{(k_a-1)^2}{9k_a} \times 100\%. \quad (8)$$

After combining (7) and (8), the improvement percentage of the VPCR, k_{improve}, can be written as follows:

$$k_{\mathrm{improve}} = \frac{k_{\mathrm{error}} - k_{\mathrm{VPCR}}}{k_{\mathrm{error}}} \times 100\%. \quad (9)$$

Table I and Fig. 6 show detailed analysis of k_{error}, k_{VPCR}, and k_{improve} under different voltage fault conditions. It can be seen that the power ripple mitigation capability of the VPCR will be related to k_a. In slight voltage fault scenario ($k_a = 0.9$ p.u.), k_{error} and k_{VPCR} are 6.7% and 0.28%, respectively, whereas k_{improve} will be 95.8%. During severe voltage fault ($k_a = 0.5$ p.u.), k_{error} and k_{VPCR} are 33.3% and 12.5%, respectively. In this case, k_{improve} will be decreased to 62.5%.

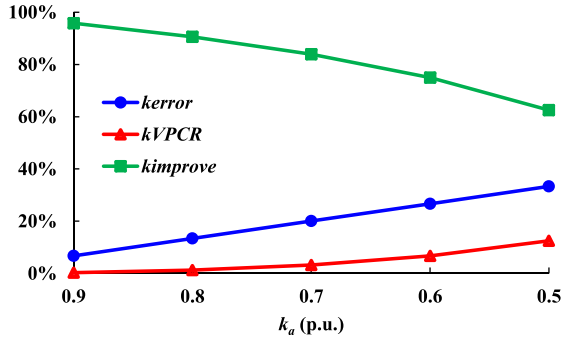

Fig. 6. K_{error}, K_{VPCR}, and K_{improve} under different voltage fault conditions.

It should be noticed that when the sag/swell happens in two phases, the analysis progress will be the same as in the one-phase voltage fault scenario. The only difference is that during the two-phase voltage fault scenario, it is necessary to include extra compensating factors (e.g., k_a for a-phase voltage and k_b for b-phase voltage). On the other hand, with the proposed VPCR, there is no need to include extra circuits and components. Even if the grid fault conditions are not considered, it is necessary to detect and locate the grid voltages for grid-tied inverters. The main reasons are as follows:

1) Under normal operation, the grid voltages should be measured and detected for protection.
2) The three-phase grid voltages (v_a, v_b, v_c) should be feedbacked and converted to V_d, V_q signals to control the inverter.
3) The phase-locked loop (PLL) is an essential function for grid-tied inverters, whereas PLL signals are generated from three-phase ac voltages. In other words, the three-phase voltages should be detected and located no matter whether the grid fault happens or not. The complexity of the proposed method will not be increased.

On the other hand, the mitigation of the output power ripple can reduce the dc-link voltage ripple. In other words, the dc-link capacitance can be minimized via the VPCR. In the following, the quantity contribution to the dc-link capacitance reduced by the VPCR will be analyzed. First, the energy storage in the dc0link capacitance, ΔE_C can be defined as follows:

$$\begin{aligned}\Delta E_C &= \frac{1}{2}C_{\mathrm{dc}}\left(V_H^2 - V_L^2\right) \\ &= \frac{1}{2}C_{\mathrm{dc}}\left[\left(V_{\mathrm{dc,avg}} + \frac{1}{2}\Delta V_{\mathrm{dc}}\right)^2 - \left(V_{\mathrm{dc,avg}} - \frac{1}{2}\Delta V_{\mathrm{dc}}\right)^2\right]\end{aligned} \quad (10)$$

where C_{dc} is the dc-link capacitance. V_H and V_L represent the highest and lowest values of the dc-link voltage, respectively. $V_{\mathrm{dc,avg}}$ is the average dc-link voltage. ΔV_{dc} is the ripple voltage on the dc-link, which can be defined as follows:

$$\Delta V_{\mathrm{dc}} = V_H - V_L. \quad (11)$$

TABLE II
COMPARISONS OF THE POWER RIPPLE AND THEORETICAL REQUIRED DC-LINK CAPACITANCE UNDER DIFFERENT VOLTAGE FAULT CONDITIONS

k_a(p.u.)	0.9	0.8	0.7	0.6	0.5
ΔV_{dc}	7.5V (1% of the $V_{dc,avg}$)				
$\Delta P_{o,ripple}$ (W)	200	400	600	800	1000
$\Delta P_{o,VPCR}$ (W)	8.33	37.5	96.43	200	375
$C_{dc,without\ VPCR}$ (μF)	188.6	377.3	565.9	754.5	943.1
$C_{dc,with\ VPCR}$ (μF)	7.9	35.4	90.9	188.6	353.7

TABLE III
CIRCUIT SPECIFICATIONS

Parameters	Value
Rated power	3kW
Input voltage	750 V
Line-to-line grid voltage (Normal phase)	220V_{rms}/60Hz
Line-to-line grid voltage (Fault phase)	198V_{rms}/60Hz (Scenario I) 154V_{rms}/60Hz (Scenario II)
DC-link capacitance	0.825mF
Output inductance	2mH
Switching frequency	50 kHz

With the combination of (10) and (11), ΔE_C can be modified as follows:

$$\Delta E_C = C_{\rm dc} \times V_{\rm dc,avg} \times \Delta V_{\rm dc}. \tag{12}$$

According to [4], the relationship between ΔE_C and the output power ripple, ΔP, can be expressed as follows:

$$\Delta E_C = \int_{\pi/2\omega}^{\pi/\omega} \Delta P \sin(2\omega t)\, dt = \frac{2\Delta P}{\omega} \tag{13}$$

where ω is the angular frequency of the grid voltage. After combining (12) and (13), $C_{\rm dc}$ can be calculated, as:

$$C_{\rm dc} = \frac{2\Delta P}{\omega \times V_{\rm dc,avg} \times \Delta V_{\rm dc}}. \tag{14}$$

It is worth mentioning that the ΔP shown in (13) and (14) can replaced as $\Delta P_{o,\rm ripple}$ or $\Delta P_{o,\rm VPCR}$.

Comparisons of the power ripple and theoretical required dc-link capacitance under different voltage fault conditions are shown in Table II. In this analysis, the dc-link voltage ripple, $\Delta V_{\rm dc}$, is set as 1% of the average dc-link voltage. Table II reveals that under different k_a values, the power ripple can effectively be mitigated with the VPCR. Besides, the theoretical required dc-link capacitance can also be minimized via the proposed strategy. In order to further demonstrate the quantity contribution of the dc-link capacitance minimization, Fig. 7 illustrates the comparison of the theoretical required dc-link capacitance.

From the quantitative analysis, it can be confirmed that both the active power ripple and the dc-link capacitance can be decreased with the VPCR. As a result, the circuit size and cost can be reduced.

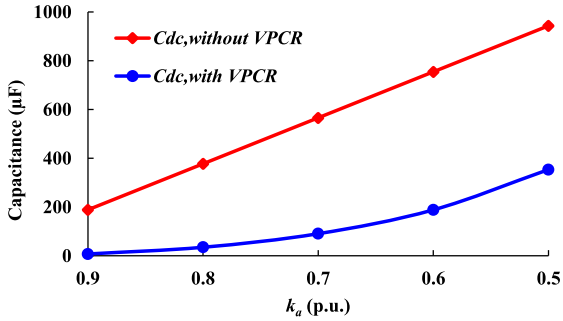

Fig. 7. Comparison of the required capacitance under different voltage fault conditions.

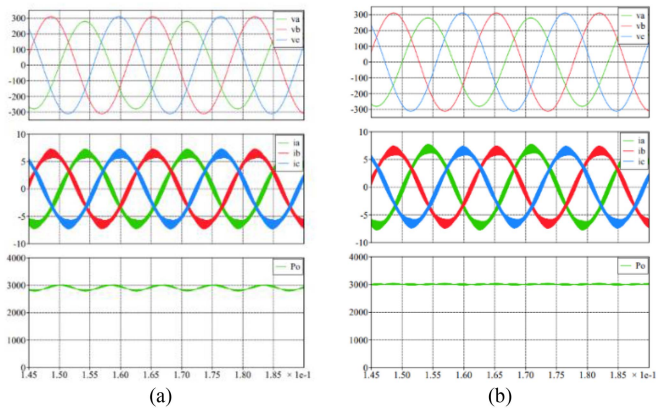

Fig. 8. Simulation waveforms of the grid voltages, output currents and the output power under scenario I (a-phase voltage reduces to 0.9 p.u.) (a) Without the VPCR. (b) With the VPCR.

IV. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the proposed strategy, a 3 kW prototype circuit with specifications shown in Table I is built. The input voltage is set as 750 V. The grid voltages are 220 $V_{\rm rms}$ under normal conditions. To verify the VPCR, four unbalanced grid fault scenarios will be established. Scenarios I and II demonstrate one-phase grid fault situations. Scenarios III and IV demonstrate the two-phase grid fault situations. For scenario I, a-phase voltage is set as 0.9 p.u. (198 $V_{\rm rms}$). For the scenario II, a-phase voltage is set as 0.7 p.u. (154 $V_{\rm rms}$). For scenario III, both the a-phase and b-phase voltage are set as 0.7 p.u. (154 $V_{\rm rms}$). For scenario IV, a-phase voltage is set as 0.7 p.u. (154 $V_{\rm rms}$), whereas b-phase voltage is set as 0.5 p.u. (110 $V_{\rm rms}$).

A. Computer Simulations

The computer simulation software, PLECS, is utilized for strategy verifications. Simulation waveforms are shown in Figs. 8 and 9. First, Fig. 8 shows waveforms of the three-phase voltages and currents, and the output power under Scenario I, whereas Fig. 8 shows similar waveforms under Scenario II. In

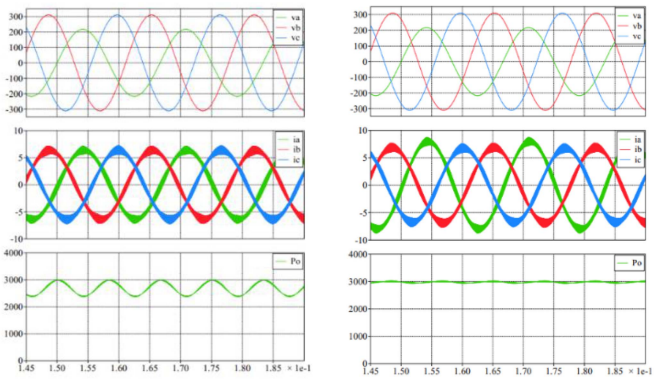

Fig. 9. Simulation waveforms of the grid voltages, output currents and the output power under scenario II (a-phase voltage reduces to 0.7 p.u.) (a) Without the VPCR. (b) With the VPCR.

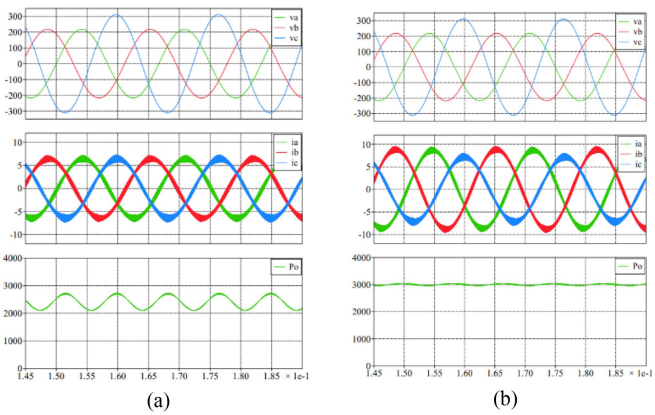

Fig. 10. Simulation waveforms of the grid voltages, output currents and the output power under scenario III (a-phase and b-phase voltage reduce to 0.7 p.u.) (a) Without the VPCR. (b) With the VPCR.

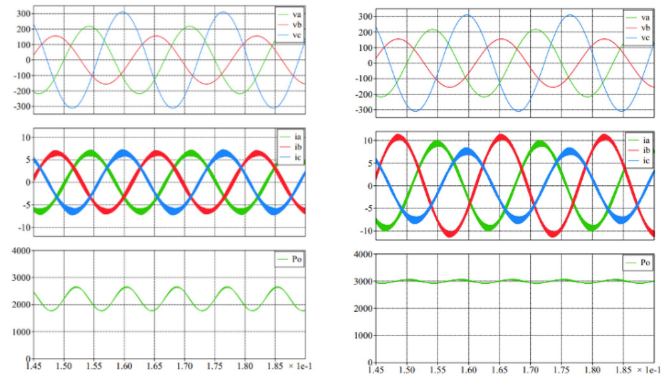

Fig. 11. Simulation waveforms of the grid voltages, output currents and the output power under scenario IV (a-phase voltage reduces to 0.7 p.u. and b-phase voltage reduces to 0.5 p.u.) (a) Without the VPCR. (b) With the VPCR.

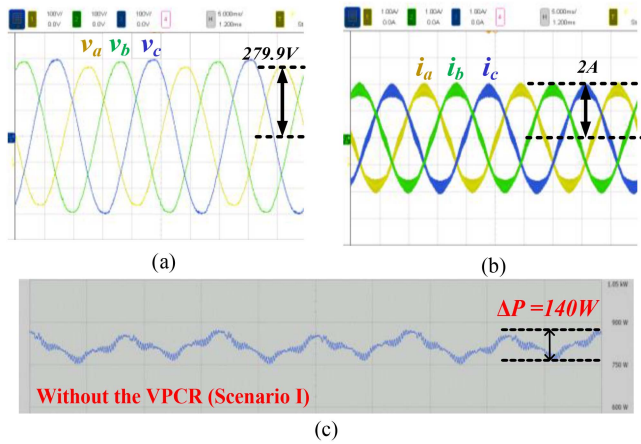

Fig. 12. Experimental results without VPCR under Scenario I. (a) Grid voltages. (b) Output currents. (c) Output power.

Figs. 8(a) and 9(a), the VPCR is not included while the VPCR is adopted in Figs. 8(b) and 9(b).

On the other hand, Figs. 10 and 11 show waveforms of the three-phase voltages and currents, and the output power under Scenarios III and IV, respectively. It can be confirmed that the proposed VPCR can effectively eliminate the power ripple under the one-phase and two-phase unbalanced grid faults.

B. Hardware Experiments

In this section, performances of the proposed VPCR are verified via hardware experiments. First, Figs. 9 and 10 show experimental results of the grid voltages, output currents, and the output power under Scenario I. In this scenario the a-phase voltage is set as 0.9 p.u. Therefore, the peak voltage of a-phase is reduced to 279.9 V, as shown in Figs. 9(a) and 10(a). In Fig. 9, the VPCR is not included; the oscillated power ripple can be calculated as 140 W, as shown in Fig. 9(c). However, the VPCR is adopted in Fig. 10. The output power ripple is decreased to 50 W according to Fig. 10(c).

On the other hand, experimental waveforms of the grid voltages, output currents and the output power under Scenario II are shown in Figs. 11 and 12 . In this scenario, the a-phase voltage is set as 0.7 p.u. The peak voltage of a-phase is reduced to 217.7V, as shown in Figs. 11(a) and 12(a). In Fig. 11, the VPCR is not adopted; the oscillated power ripple is calculated as 200 W, as shown in Fig. 11(c). If the VPCR is utilized, as shown in Fig. 12(c), the output power ripple is decreased to 100 W. From the experimental results, it can be confirmed that under the one phase grid fault of 0.9 and 0.7 p.u., the output power ripple can be eliminated with 64.3% and 50%, respectively.

It is worth mentioning that the power ripple mitigation performance is slightly lower than the theoretical analysis shown in Section III and the simulation results. The main factor impacting the VPCR performance will be the quality of grid voltages. In simulations, ideal ac voltages are adopted, whereas these voltages are with pure sinusoidal waveforms. Therefore, the THD of voltages will be equal to zero in simulations. On the other hand, in the experimental setup, the output ports of the inverter are directly connected to the grid. Unfortunately, the grid voltage characteristics will be affected by the power quality.

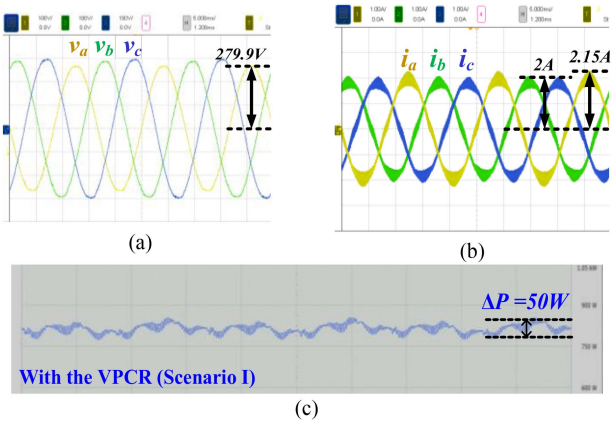

Fig. 13. Experimental results with VPCR under Scenario I. (a) Grid voltages. (b) Output currents. (c) Output power.

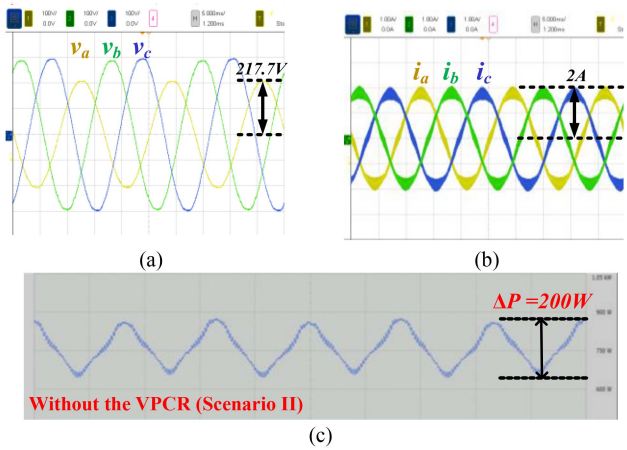

Fig. 14. Experimental results without VPCR under Scenario II. (a) Grid voltages. (b) Output currents. (c) Output power.

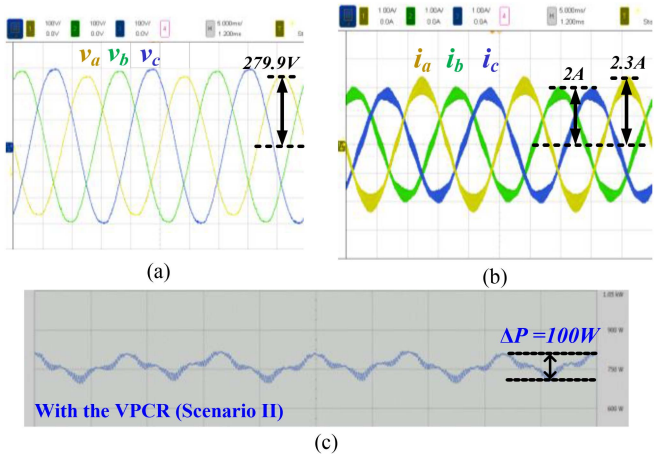

Fig. 15. Experimental results with VPCR under Scenario II. (a) Grid voltages. (b) Output currents. (c) Output power.

THD of grid voltages will be increased when the power quality is decreased. Therefore, the gird voltages in our laboratory are not with pure sinusoidal waveforms. Consequently, higher voltage THD produces an unexpected power ripple of the inverter. As a result, the performance of the proposed VPCR will be decreased by the nonideal characteristics of grid voltages.

V. Conclusion

This letter proposes an active power ripple mitigation strategy for a three-phase inverter under unbalanced grid voltages. Simplicity is the main feature of this strategy. With the proposed VPCR strategy, the power oscillation can effectively be suppressed without adopting complex circuit structures or control methods. Theoretical analysis and mathematical equations of the proposed method are also presented. Finally, both simulation and experimental results obtained from a 3 kW circuit demonstrate the feasibility of the proposed strategy.

References

[1] N. Beniwal, H. D. Tafti, G. G. Farivar, S. Ceballos, J. Pou, and F. Blaabjerg, "A control strategy for dual-input neutral-point-clamped inverter-based grid-connected photovoltaic system," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 9743–9757, Sep. 2021.

[2] M. A. Ghasemi, H. M. Foroushani, and F. Blaabjerg, "Marginal power-based maximum power point tracking control of photovoltaic system under partially shaded condition," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5860–5872, Jun. 2020.

[3] C.-Y. Tang, P.-T. Chen, and J.-H. Jheng, "Bidirectional power flow control and hybrid charging strategies for three-phase PV power and energy storage systems," *IEEE Trans. Power. Electron.*, vol. 36, no. 11, pp. 12710–12720, Nov. 2021.

[4] F. Deng, J. Zhao, C. Liu, Z. Wang, X. Cai, and F. Blaabjerg, "Temperature-balancing control for modular multilevel converters under unbalanced grid voltages," *IEEE Trans. Power. Electron.*, vol. 37, no. 4, pp. 4614–4625, Apr. 2022.

[5] C. Tang, L. Kao, Y. Chen, and S. Ou, "Dynamic power decoupling strategy for three-phase PV power systems under unbalanced grid," *IEEE Trans. Sustain. Energy*, vol. 10, no. 2, pp. 540–548, Apr. 2019.

[6] T. Yueh, T. Tsai, Y. Chen, Y. Lee, and Y. Chang, "The reverse zero-sequence current compensation strategy for back-to-back active power conditioners," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–6.

[7] E. Espina, R. Cárdenas-Dobson, M. Espinoza-B., C. Burgos-Mellado, and D. Sáez, "Cooperative regulation of imbalances in three-Phase four-wire microgrids using single-phase droop control and secondary control algorithms," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1978–1992, Feb. 2020.

[8] P. Rodriguez, A. V. Timbus, R. Teodorescu, M. Liserre, and F. Blaabjerg, "Flexible active power control of distributed power generation systems during grid faults," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2583–2592, Oct. 2007.

[9] L. Shang, W. Zhu, and Z. Li, "A control method of PV grid-connected inverter under grid voltage unbalanced drops," in *Proc. Chin. Control Decis. Conf.*, 2018, pp. 6482–6486.

[10] Y. Shen and H. Nian, "Improved DPC strategy of grid-connected inverters under unbalanced and harmonic grid conditions," in *Proc. Int. Conf. Elect. Mach. Syst.*, 2013, pp. 1566–1570.

[11] X. Du and R. Wang, "Control strategy of negative sequence current for the grid-connection converter under the unbalanced grid condition," in *Proc. 34th Chin. Control Conf.*, 2015, pp. 9066–9071.

[12] W. Cao and Y. Xu, "A control strategy of grid-connected photovoltaic inverter under unbalanced voltage conditions," in *Proc. 17th Int. Conf. Harmon. Qual. Power*, 2016, pp. 209–213.