An Active Gate Driver of SiC MOSFET Module Based on PCB Rogowski Coil for Optimizing Tradeoff Between Overshoot and Switching Loss

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***Abstract*—The superior characteristics of the silicon carbide metal-oxide-semiconductor field-effect transistor (SiC MOSFET) allow its wide use for improving the efficiency and power density of power electronic systems. However, the higher switching speed exacerbates the problems of overshoot, oscillation, and electromagnetic interference (EMI), which need to be properly addressed. In this article, a novel stage-detection closed-loop active gate driver (AGD) based on the printed-circuit-board (PCB) Rogowski Coil is proposed for optimizing the switching performance of SiC MOSFETs. And its stage identification threshold design can weaken the influence of the varying nonlinear parameters, especially for the turn-ON process. First, the gate driver trajectory and the switching process of the SiC MOSFET are analyzed. The optimal driver parameter dynamic configuration among the existing stage-control schemes is defined and unified, which aims to optimize the tradeoff between the overshoot and switching loss. Then, the parameter design of the PCB Rogowski Coil is illustrated. And the operation principle and working process of the proposed AGD are introduced. Finally, the performance of the proposed AGD and the effectiveness of the stage-control schemes are verified in the double-pulse test under different conditions. The experimental results show that the proposed AGD can not only reduce the overshoot and suppress the oscillation but also optimize the compromise of the switching loss and switching time.**

***Index Terms*—Active gate driver, EMI, overshoot, switching loss, silicon carbide metal-oxide-semiconductor field-effect transistor (SiC MOSFET).**

I. Introduction

In RECENT years, with the continuous development of wide bandgap semiconductor technology, the silicon carbide metal-oxide-semiconductor field-effect transistor (SiC MOSFET) with its higher breakdown voltage, smaller on-state resistance, higher thermal conductivity, and higher switching speed [1], [2], [3], is widely used in an increasing number of industrial applications [4], [5]. The SiC MOSFET can improve the efficiency and power density of power electronic systems, but it also introduces some problems. Due to ubiquitous parasitic inductances and junction capacitances, the higher switching speed of SiC MOSFETs inevitably leads to more severe overshoot and oscillation [6], [7]. These problems aggravate the voltage and current pressure of SiC MOSFETs and the electromagnetic interference (EMI), resulting in lower system reliability [8], [9]. Therefore, it is a major challenge to make full use of the superior characteristics of SiC MOSFETs.

To mitigate the overshoot and oscillation, the most fundamental method is optimizing the package of power devices and the layout of the printed circuit board (PCB) [10], [11]. But the effects are often limited by structure, cost, power, etc. Furthermore, the snubber circuits and the larger gate resistance are commonly used in practical applications to reduce the overall switching speed of SiC MOSFETs [12], [13], [14]. However, these ways compromise the switching time and switching loss to a major extent in fact, which is contradictory to the superior characteristics of SiC MOSFETs [8], [15], [16].

Therefore, the active gate driver (AGD) technology is proposed in [7], [8], [9], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], for the purpose of mitigating the overshoot and oscillation, while minimizing the compromise of the switching speed and switching loss during the switching process. Different from the conventional gate driver (CGD), the AGD is invented as a technology to adjust the gate driver parameters dynamically during the switching process and optimize the switching performance of power devices. When the AGD is applied to Si devices at first, the commonly used control scheme is the complete closed-loop feedback control which demonstrates a high degree of freedom for controlling [17], [18], [19]. The AGD presented in [18] realizes switching transition control of power devices by modulating the optical intensity of the optically triggered transistor. However, tuning the feedback controller parameters for every device is a cumbersome process, thus making it less attractive for industrial applications [9]. Furthermore, it is difficult to realize the real-time feedback adjustment of the switching trajectory for SiC MOSFETs, because of the increase in the switching speed and the limit of the feedback controller response speed [7].

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Thus, the concept of the stage-control scheme is proposed in [20] and [21], which controls the gate driver parameters of different stages, respectively, during the switching process. The open-loop parameter design scheme is used to achieve this purpose at first [7], [8], [9], [15], [16], [22], [23], [24], [25], [26], [27], [28], [29], such as the 63-level gate driver integrated circuit without feedback loop proposed in [22] and [23]. Specifically, the open-loop scheme realizes the adjustment of the gate driver dynamic trajectory with the advance driver parameter design. The design of the dynamic parameters is commonly based on a precise and complex theoretical calculation, and its effect depends on the accuracy of the varying nonlinear parameter models and circuit parasitic parameters extraction. Furthermore, the effect of the determined open-loop parameter varies with the load, device, circuit, and environmental conditions. However, the switching performance under unsuitable dynamic parameters can even be worse than that of the CGD [24], [25]. Then, authors in [7], [9], [26] realized online calculation of the dynamic driver parameter by detecting the load current and voltage, which improve the applicability of the AGD to a certain extent under different load conditions.

The stage-detection closed-loop control scheme is proposed in [6], [20], [21], [30], [31], [32], [33], [34], [35], [36]. In these schemes, the gate driver parameters are adjusted accordingly based on the stage of the switching transient behavior during the switching process, so as to realize the switching performance optimization of SiC MOSFETs. To identify the switching transient stage, the detection method is crucial. The gate-source voltage is detected to indirectly identify the switching transient stage in [6], [30], [31], [32]. However, the detection value of the gate-source voltage is affected by the switching oscillation. And it is a challenge to define a correspondence between the gate-source voltage and the switching transient stage of a SiC MOSFET. There are some other detection methods to locate the switching transient stage, such as the drain-source voltage detection in [33], [34], [35], [36] and the common-source inductance voltage detection in [20], [21], and [36]. These methods increase the difficulty of the interface circuit design because the detection circuits are close to the high-voltage position of the power stage [37].

In addition, for the common objective of reducing the overshoot, there is a discrepancy in the driver parameter dynamic configurations among the different AGDs in the references, which leads to different compromises of the switching loss. Specifically, the existing stage-control schemes for the turn-ON process in [6], [8], [9], and [28], are not the most suitable schemes for SiC MOSFETs, as they mostly ignore the characteristic differences between Si and SiC devices. Therefore, it is very important to design an optimal driver parameter configuration for each stage of the switching process for the SiC MOSFET.

In this article, the influences of the gate driver dynamic trajectory on the voltage and current change rate, overshoot, and switching loss at different stages during the switching process are analyzed at first. The optimal stage-control scheme for the SiC MOSFET is defined and unified, where the different stage-control schemes for the turn-ON process are compared by experiment. Then, a novel stage-detection closed-loop AGD of SiC MOSFETs based on the PCB Rogowski coil is proposed, which is in line with the designed stage-control scheme. The advantages of solid signal isolation, high bandwidth, wide measurement range, and less temperature sensitivity make the PCB Rogowski coil an attractive current detector for SiC devices, and it used to be adopted only for current reconstruction and protection [38], [39], [40]. The utilization of the Rogowski coil for switching performance optimization is conducive to the integrated design of the multifunctional driver. And the stage identification threshold design process of the proposed AGD weakens the influence of the varying nonlinear parameters, where the threshold design for the turn-ON process is basically only related to the load current. At last, the performance of the proposed AGD is verified by experiment. The results show that the optimization of the tradeoff between the overshoot and switching loss during the switching process is achieved. This article is organized as follows. The gate driver trajectory and switching performance of SiC MOSFETs are analyzed in Section II. The parameters design of the PCB Rogowski coil and the principle of the proposed AGD are introduced in Section III. The experimental validation and performance analysis of the proposed AGD are shown in Section IV. Finally, Section V concludes this article.

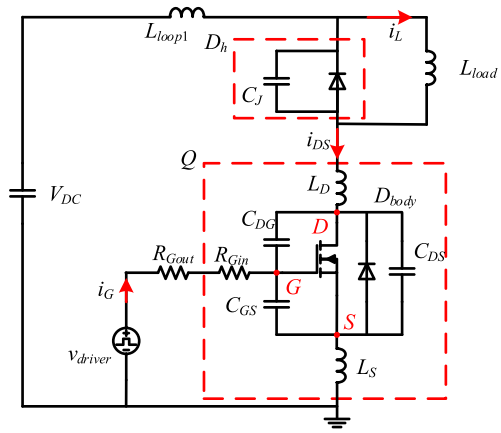

Fig. 1. Double pulse test (DPT) circuit with inductive load considering parasitic parameters.

II. Analysis of Gate Driver Trajectory and Switching Performance

The double pulse test (DPT) circuit with inductive load considering parasitic parameters is shown in Fig. 1. V_{DC} is the dc bus voltage. v_{driver} is the output voltage of a voltage source gate driver. L_{load} is the inductive load. R_{Gout} is the gate driver resistance. The SiC MOSFET Q with body diode D_{body} and parasitic parameters inside the package is in the lower red box. The internal parasitic parameters include drain parasitic inductance L_D, common source parasitic inductance L_S, gate-source junction capacitance C_{GS}, drain-source junction capacitance C_{DS}, drain-gate junction capacitance C_{DG}, and internal gate resistance R_{Gin}. The diode D_h with junction capacitance C_J

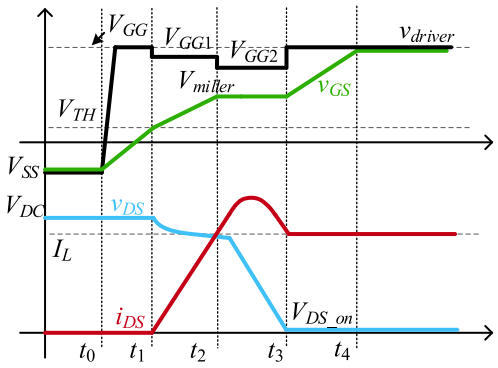

Fig. 2. Gate driver trajectory and corresponding idealized turn-ON waveforms of a SiC MOSFET.

is in the higher red box. L_{loop1} is the interconnection parasitic inductance of the power stage loop.

A. Gate Driver Trajectory and Switching Performance of the Turn-ON Process

As shown in Fig. 2, the idealized turn-ON process of the SiC MOSFET is typically divided into four stages, including turn-ON delay stage $(t_0 - t_1)$, current rising stage $(t_1 - t_2)$, voltage falling stage $(t_2 - t_3)$, and gate remaining charging stage $(t_3 - t_4)$. At t_0, v_{driver} rises to the positive supply voltage V_{GG}, which initiates the turn-ON process of the SiC MOSFET, and then v_{GS} starts to rise. This stage ends when v_{GS} reaches the threshold voltage V_{TH} at t_1. The turn-ON delay stage has little effect on the switching loss, but a higher V_{GG} is conducive to improving the switching speed. The turn-ON loss E_{on} is mainly generated in the subsequent current rising stage and voltage falling stage. Starting from t_1, as v_{GS} continues to rise, the drain-source current of the SiC MOSFET i_{DS} rises as well. The differential equations of the circuit during this stage can be expressed as

$$V_{GG1} = R_G i_G + v_{GS} + L_S \frac{di_{DS}}{dt} \tag{1}$$

$$i_{DS} = g_m (v_{GS} - V_{TH}) \tag{2}$$

$$i_G = C_{\text{iss}} \frac{dv_{GS}}{dt} \tag{3}$$

where V_{GG1} is the driver supply voltage during the current rising stage, g_m is the transconductance of the SiC MOSFET, the gate resistance $R_G = R_{\text{Gout}} + R_{\text{Gin}}$, and the input capacitance $C_{iss} = C_{GS} + C_{DG}$. At t_2, i_{DS} reaches the load current I_L, v_{GS} rises to the Miller plateau voltage V_{miller}, and this stage ends. The average current change rate of i_{DS} during the current rising stage can be approximately expressed as

$$\frac{di_{DS}}{dt} = \frac{V_{GG1} - \left(\dfrac{I_L}{2g_m} + V_{TH}\right)}{\dfrac{R_G C_{\text{iss}}}{g_m} + L_S}. \tag{4}$$

The duration of this stage T_{s2} can be expressed as

$$T_{s2} = \frac{I_L}{di_{DS}/dt} = \frac{I_L \left(\dfrac{R_G C_{\text{iss}}}{g_m} + L_S\right)}{V_{GG1} - \left(\dfrac{I_L}{2g_m} + V_{TH}\right)}. \tag{5}$$

The drain-source voltage v_{DS} decreases and remains at $V_{DC} - L_{\text{loop}}(di_{DS}/dt)$ during this stage considering the effect of parasitic inductance, where $L_{\text{loop}} = L_{\text{loop1}} + L_D + L_S$. The switching loss E_{on_s2} of this stage can be obtained as

$$\begin{aligned} E_{on\_s2} &= \frac{I_L^2}{2} \frac{V_{DC} - L_{\text{loop}}(di_{DS}/dt)}{di_{DS}/dt} \\ &= \frac{I_L^2}{2} \left(\frac{V_{DC}}{di_{DS}/dt} - L_{\text{loop}}\right). \end{aligned} \tag{6}$$

After t_2, the overshoot of i_{DS} appears. The obvious difference in the switching behavior between SiC and Si devices should be noted here. For the Si device, the reverse recovery process of the freewheeling diode (FWD) D_h is the main source of the current overshoot. The reverse recovery charge Q_{rr} of the FWD is determined by the device characteristics and the load current I_L. The reverse recovery time T_{rr} and the maximum value of the reverse recovery current I_{rrm} are affected by the current change rate at the end time of the current rising stage. The equations can be expressed as [8], [41], [42]

$$Q_{rr} = \frac{Q_{rr\_\text{data}}}{I_{SD\_\text{data}}} I_L, \tag{7}$$

$$I_{\text{rrm}} = \sqrt{Q_{rr} \frac{di_{DS}}{dt}} = \frac{1}{2} T_{rr} \frac{di_{DS}}{dt} \tag{8}$$

$$T_{rr} = 2\sqrt{\frac{Q_{rr}}{di_{DS}/dt}} \tag{9}$$

where Q_{rr_data} is the reverse recovery charge under the test condition in the datasheet, I_{SD_data} is the load current in the datasheet. Accordingly, the switching loss caused by the reverse recovery process of the FWD E_{rr} can be expressed as

$$E_{rr} = \left(I_L \sqrt{\frac{Q_{rr}}{di_{DS}/dt}} + Q_{rr}\right) \left(V_{DC} - L_{\text{loop}} \frac{di_{DS}}{dt}\right). \tag{10}$$

On the other hand, for SiC devices, the SiC diode and the SiC MOSFET intrinsic diode have been proved to have a little reverse recovery [43], [44], [45]. Therefore, the effect of the reverse recovery process of D_h on the switching loss and current overshoot is very small. After t_2, it is the voltage falling stage. The drain-source voltage of the SiC MOSFET v_{DS} keeps falling during this stage, while the gate-source voltage v_{GS} remains at V_{miller}. The equations of this stage can be expressed as

$$v_{GS} = V_{\text{miller}} = \frac{I_L}{g_m} + V_{TH} \tag{11}$$

$$i_G = \frac{V_{GG2} - V_{\text{miller}}}{R_G} \tag{12}$$

where V_{GG2} is the driver supply voltage during the voltage falling stage. v_{DS} drops from $V_{DC} - L_{\text{loop}}(di_{DS}/dt)$ to the conduction voltage drop V_{DS_on}. The average voltage change rate of v_{DS} during this stage can be obtained based on (12), which can be approximately expressed as

$$\frac{dv_{DS}}{dt} = -\frac{i_G}{C_{DG}} = -\frac{V_{GG2} - V_{\text{miller}}}{C_{DG}R_G}. \tag{13}$$

The duration T_{s3} and switching loss E_{on_s3} of this stage can be expressed as

$$T_{s3} = \frac{Q_{GD\_s3}}{i_G} = \frac{R_G Q_{GD\_s3}}{V_{GG2} - V_{\text{miller}}} \tag{14}$$

$$E_{on\_s3} = \frac{I_L[V_{DC} - L_{\text{loop}}(di_{DS}/dt)]}{2} \frac{R_G Q_{GD\_s3}}{V_{GG2} - V_{\text{miller}}} \tag{15}$$

where Q_{GD_s3} is the gate-drain charge of the SiC MOSFET in this stage. Moreover, whether it is a Si device or a SiC device, the voltage across the FWD v_{D_h} is rising rapidly during this stage. This behavior leads to the charging process of C_J, which results in the current overshoot of i_{DS}. The variation process of v_{D_h} can be divided into two sections, the voltage drop of L_{loop} during the current rising stage transfers to D_h at the initial time of the voltage falling stage, and then the drain-source voltage of the SiC MOSFET transfers to D_h. When v_{D_h} reaches V_{DC}, this stage ends. The value of the current overshoot can be expressed as

$$i_{os} = -C_J \frac{dv_{DS}}{dt}. \tag{16}$$

The switching loss caused by the charging current of C_J can also be divided into two parts, and the sum of these two parts can be expressed as

$$E_{C_J} = \frac{1}{2} C_J \{V_{DC}^2 - [L_{\text{loop}}(di_{DS}/dt)]^2\}. \tag{17}$$

Furthermore, the voltage change process can be equivalent to a step signal to the *LC* resonant circuit composed of C_J and L_{loop}, which leads to an oscillation. And the intensity of the oscillation is positively correlated with the voltage change rate. At t_3, the voltage falling stage ends, and v_{GS} continues to rise to the driver supply voltage V_{GG}. The gate supply voltage in the gate remaining charging stage has little effect on the switching loss and oscillation, but a higher V_{GG} is helpful for improving the switching speed and reducing the ON-state loss. The total turn-ON loss E_{on} can be expressed as

$$E_{on} = E_{on\_s2} + E_{on\_s3} + E_{rr} + E_{C_J}. \tag{18}$$

It should be noted that the turn-ON loss of SiC MOSFETs does not include E_{rr} that is caused by the reverse recovery process of the diode.

Besides, the transconductance and the junction capacitances of the device are actually variable nonlinear parameters, which are usually fitted by nonlinear equations. The description of the relationship between the gate-source voltage v_{GS} and the channel current i_{CH} is a quadratic formula, which can be expressed as

$$i_{CH} = \begin{cases} 0 & v_{GS} < V_{TH} \\ k_{fs}(v_{GS} - V_{TH})^2 & v_{GS} > V_{TH}. \end{cases} \tag{19}$$

However, the linear formula is often used in the analysis process for simplicity, which is similar to (2)

$$i_{CH} = \begin{cases} 0 & v_{GS} < V_{TH} \\ g_m(v_{GS} - V_{TH}) & v_{GS} > V_{TH}. \end{cases} \tag{20}$$

Therefore, for the parameters calculation of a duration period in the switching process with continuously changing nonlinear parameters, such as the stage duration, the average current or voltage change rate, and the stage loss, the average value is required. According to the results in [46], the equivalent average value of transconductance g_{avr} in the switching process is related to the load current I_L. The average transconductance g_{avr} under the determined working temperature can be expressed as

$$g_{\text{avr}} = \frac{2(k^2 + 3k + 3)}{3k(1 + k)} \sqrt{k_{fs} I_L} \tag{21}$$

where $k = \sqrt{6}$. Furthermore, the nonlinear fitting equations of the parasitic junction capacitances C_{DG}, C_{DS}, and C_J under variable voltage v can be expressed as

$$C = \frac{C_0}{(1 + v/V_b)^r} + C_1 \tag{22}$$

where C_0 and C_1 can be extracted from the capacitances curves in the datasheet, and V_b and r are the parameters to be fitted. For C_{DG} and C_{DS}, v is the drain–source voltage v_{DS}. For C_J, v is the reverse voltage of D_h. The equivalent average value of junction capacitances during the switching process can be expressed by [46]

$$C_{\text{avr}} = \begin{cases} \dfrac{C_0 V_b}{(1-r)(V_1 - V_2)} \left[\left(1 + \dfrac{V_1}{V_b}\right)^{1-r} - \left(1 + \dfrac{V_2}{V_b}\right)^{1-r} \right] & r \neq 1 \\ \dfrac{C_0 V_b}{V_1 - V_2} \ln \dfrac{V_1}{V_2} + C_1 & r = 1 \end{cases} \tag{23}$$

where V_1 and V_2 are the variation range of v.

In general, the above analysis shows that the value of R_G for the CGD can be changed to realize an overall adjustment of the switching speed, overshoot, and switching loss, which should be designed reasonably according to the system requirements. But for the AGD with dynamic gate driver trajectory, the switching performance of different stages can be controlled, respectively, by V_{GG}, V_{GG1}, and V_{GG2}. The higher V_{GG1} during the current rising stage contributes to a higher current change rate during the turn-ON process. The higher V_{GG2} during the voltage falling stage contributes to a higher voltage change rate with increasing the oscillation intensity as well. In terms of the switching loss, ceteris paribus, the increase in V_{GG1} or V_{GG2} would reduce the turn-ON switching loss, the former significantly reducing E_{on_s2} and E_{rr}; and the latter reducing E_{on_s3}. Furthermore, the contributory factors of the current overshoot are different for Si devices and SiC devices. The decrease of V_{GG2} contributes

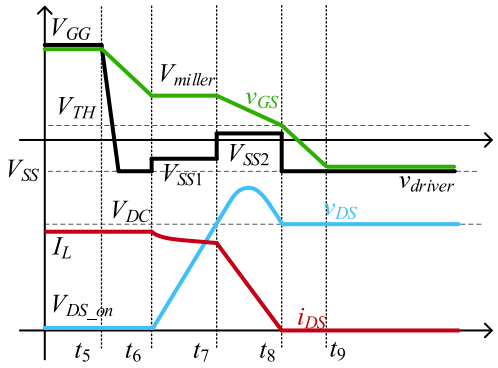

Fig. 3. Gate driver trajectory and corresponding idealized turn-OFF waveforms of a SiC MOSFET.

to the reduction of the current overshoot and oscillation for SiC MOSFETs. But for Si devices, the reverse recovery current of the FWD is the main source of the current overshoot during the turn-ON process, which is mainly affected by the current change rate. Thus, V_{GG1} also needs to be reduced for effectively mitigating the current overshoot of Si devices. At present, the driver parameter dynamic configurations adopted in literature to mitigate the current overshoot and oscillation are more suitable for Si devices, i.e., the gate charging speed of the current rising stage and voltage falling stage are both reduced [6], [8], [9], [28]. However, when this scheme is applied to SiC MOSFETs, it compromises the turn-ON loss and switching time to a great extent. Therefore, for the control objective of mitigating the current overshoot and oscillation while reducing the compromise of the turn-ON loss and switching time, the optimal scheme for SiC MOSFETs should be reducing the gate charging speed only in the voltage falling stage while increasing the gate charging speed in other stages.

B. Gate Driver Trajectory and Switching Performance of the Turn-OFF Process

As shown in Fig. 3, the idealized turn-OFF process of the SiC MOSFET is also typically divided into four stages, including turn-OFF delay stage ($t_5 - t_6$), voltage rising stage ($t_6 - t_7$), current falling stage ($t_7 - t_8$), and gate remaining discharging stage ($t_8 - t_9$). When v_{driver} goes to the negative supply voltage V_{SS} at t_5, v_{GS} begins to decrease. When v_{GS} drops to V_{miller} at t_6, the turn-OFF delay stage ends. This stage generates little switching loss, but lower V_{SS} contributes to a higher switching speed. The turn-OFF loss E_{off} is mainly generated in the subsequent voltage rising stage and current falling stage. After t_6, v_{DS} begins to rise, while v_{GS} remains at V_{miller}, which is similar to the voltage falling stage in the turn-ON process. The average change rate of v_{DS} during this stage can be approximately expressed as

$$\frac{dv_{DS}}{dt} = -\frac{i_G}{C_{DG}} = -\frac{V_{SS1} - V_{\text{miller}}}{C_{DG}R_G} \tag{24}$$

where V_{SS1} is the driver supply voltage of this stage. When v_{DS} rises from V_{DS_on} to V_{DC}, the voltage rising stage ends. The duration of this stage can be expressed as

$$T_{s6} = \frac{Q_{GD\_s6}}{i_G} = \frac{R_G Q_{GD\_s6}}{|V_{SS1} - V_{\text{miller}}|} \tag{25}$$

where Q_{GD_s6} is the gate-drain charge of the SiC MOSFET in this stage. Given the effect of the junction capacitance in the voltage variation process, i_{DS} falls and remains as $I_L - C_J(dv_{DS}/dt)$ during this stage. The switching loss $E_{\text{off\_s6}}$ of this stage can be obtained as

$$E_{\text{off\_s6}} = \frac{V_{DC}[I_L - C_J(dv_{DS}/dt)]}{2} \frac{R_G Q_{GD\_s6}}{|V_{SS1} - V_{\text{miller}}|}. \tag{26}$$

After t_7, it is the current falling stage, which is the reverse of the current rising stage in the turn-ON process. v_{GS} drops from V_{miller} to V_{TH}, while i_{DS} decreases to zero at the end time of this stage t_8. The average change rate of i_{DS} during this stage can be approximately expressed as

$$\frac{di_{DS}}{dt} = \frac{V_{SS2} - \left(\dfrac{I_L}{2g_m} + V_{TH}\right)}{\dfrac{R_G C_{iss}}{g_m} + L_S} \tag{27}$$

where V_{SS2} is the designed driver supply voltage of this stage. Thus, the duration and switching loss $E_{\text{off\_s7}}$ of this stage can be expressed as

$$T_{s7} = \frac{\left(I_L - C_J\dfrac{dv_{DS}}{dt}\right)\left(\dfrac{R_G C_{\text{iss}}}{g_m} + L_S\right)}{\left|V_{SS2} - \left(\dfrac{I_L}{2g_m} + V_{TH}\right)\right|} \tag{28}$$

$$E_{\text{off\_s7}} = \frac{V_{DC}}{2} \frac{\left[I_L - C_J\dfrac{dv_{DS}}{dt}\right]^2}{\left|V_{SS2} - \left(\dfrac{I_L}{2g_m} + V_{TH}\right)\right|} \left(\frac{R_G C_{\text{iss}}}{g_m} + L_S\right). \tag{29}$$

Moreover, there is a large negative voltage drop on L_{loop} because of the sharp current variation during the current falling stage, which causes the overshoot of v_{DS}. In fact, the current transfer process also includes two sections, the first one is i_{DS} drops to $I_L - C_J(dv_{DS}/dt)$ in the voltage rising stage, and the latter one is in the current falling stage. The value of the voltage overshoot in the current falling stage can be expressed as

$$v_{os} = -L_{\text{loop}}\frac{di_{DS}}{dt}. \tag{30}$$

The switching loss caused by the overvoltge can also be divided into two parts, and the sum of these two parts can be expressed as

$$E_{L_{\text{loop}}} = -\frac{1}{2}L_{\text{loop}}\left[I_L^2 - \left(C_J\frac{di_{DS}}{dt}\right)^2\right]. \tag{31}$$

At t_8, the current variation process is over, and v_{GS} continues to discharge until reaching V_{SS}. The lower V_{SS} is conducive to improving the switching speed. The total turn-ON loss E_{off} can be expressed as

$$E_{\text{off}} = E_{\text{off\_s6}} + E_{\text{off\_s7}} + E_{L_{\text{loop}}}. \tag{32}$$

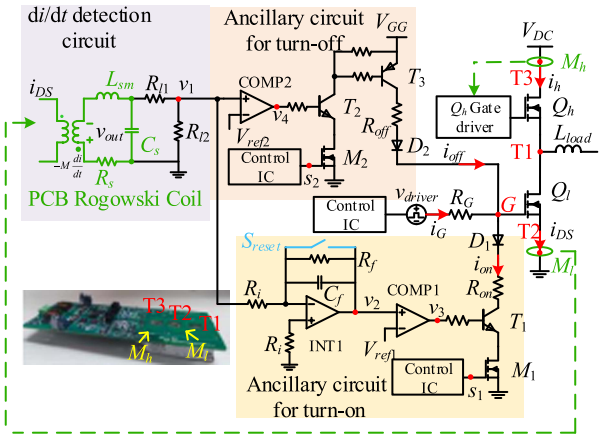

Fig. 4. Circuit schematic diagram and installation structure of the proposed AGD.

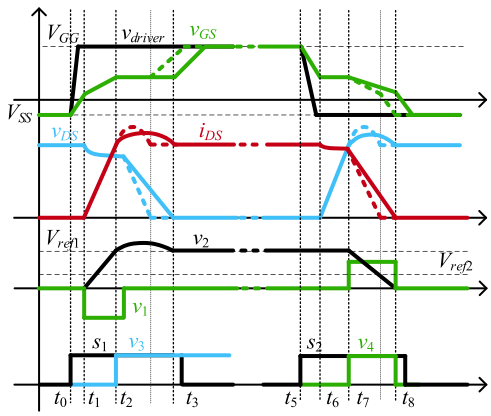

Fig. 5. Idealized switching waveforms of a SiC MOSFET and signals of the proposed AGD (dashed line: switching behavior without the auxiliary circuit, solid line: switching behavior under the auxiliary circuit).

According to the above equations, the driver supply voltage during the voltage rising stage V_{SS1} can be increased to lower the voltage change rate, and V_{SS2} can be increased to reduce the current falling rate during the turn-OFF process. For the switching loss, the decrease in V_{SS1} or V_{SS2} would reduce the turn-OFF switching loss, the former significantly reducing $E_{\text{off\_s6}}$, and the latter reducing $E_{\text{off\_s7}}$. In order to optimize the compromise of the turn-OFF loss and switching time under the premise of reducing voltage overshoot, the optimal turn-OFF gate driver scheme of SiC MOSFETs should be reducing the gate discharging speed only in the current falling stage while increasing the gate discharging speed in other stages.

III. Operation Principle of the Proposed AGD

The half-bridge circuit with the circuit schematic diagram of the proposed AGD for the lower device is shown in Fig. 4. The key waveforms of the SiC MOSFET and the corresponding signals of the AGD are shown in Fig. 5. The proposed AGD consists of four major function sections: 1) the control integrated chip (IC), 2) the di/dt detection circuit, 3) the ancillary circuit for the turn-ON process, and 4) the ancillary circuit for the turn-OFF process. A complex-programmable-logic-device (CPLD) is used as the control IC to receive switching signals and control the switching state of the SiC MOSFET. And the ADA4817 with a bandwidth of 1 GHz is chosen as the amplifier, and the comparators are the LT1711 with a typical propagation delay of 4.5 ns. The proposed AGD is independent of the original CGD push-pull circuit v_{driver}, which can realize the adjustment of the gate charging and discharging speed by stage-detection closed-loop control.

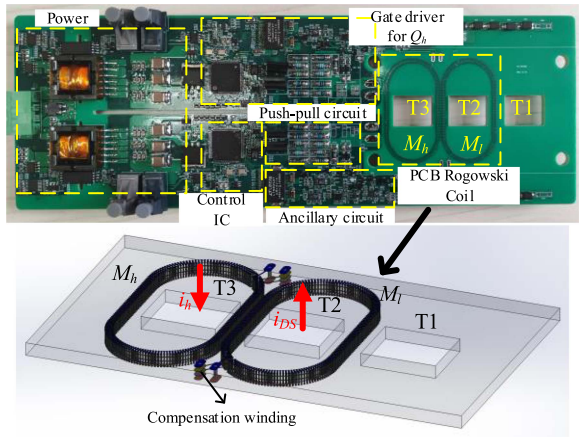

Fig. 6. Prototype of the proposed AGD and 3-D model of the Rogowski coil.

A. Current Change Rate Sensor Based on PCB Rogowski Coil

The PCB Rogowski coil is used as the di/dt detection sensor in the proposed AGD. The PCB Rogowski coil is a kind of induction coil constructed by traces and vias of the PCB. The ideal Rogowski coil is a high-load-impedance current transformer that equivalently performs as an inductor with the value of mutual inductance. A di/dt voltage scaled by the mutual inductance M is induced at the output of the transformer, where i is the current through the coil. The prototype of the proposed AGD and the 3-D model of the designed PCB Rogowski coil are shown in Fig. 6. The adopted module is the 1700 V/300 A SiC MOSFET CAS300M17BM2 from CREE, Inc. The two PCB Rogowski coils are installed on the drain of the higher device (Terminal 3-T3) and the source of the lower one (Terminal 2-T2) of the SiC MOSFET module, respectively. The power stage currents of the two SiC MOSFETs pass through their own coil. As shown in the 3-D model, the Rogowski coil is constructed by the top layer traces, the bottom layer traces, the vias, and the compensation windings in the second and third layers. The compensation winding can mitigate the effect of the external magnetic field which is perpendicular to the PCB [47]. And the Rogowski coil of a closed and symmetrical shape can mitigate the effect of the external magnetic field which is parallel to the PCB [47]. According to the design considerations in [40], a higher mutual inductance value is conducive to dealing with a high-EMI environment. Therefore, the Rogowski coil is designed as the horseshoe shape in this article for more turns and higher mutual inductance, and the plan sketch is shown in Fig. 7. The single-turn winding in the

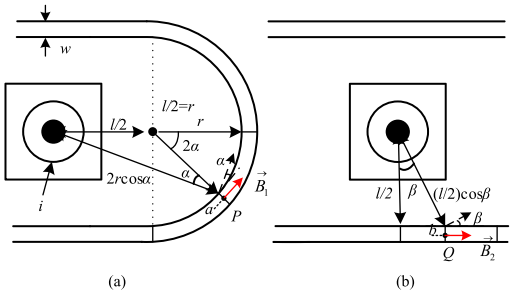

Fig. 7. Plane diagram of the Rogowski coil. (a) Type I winding. (b) Type II winding.

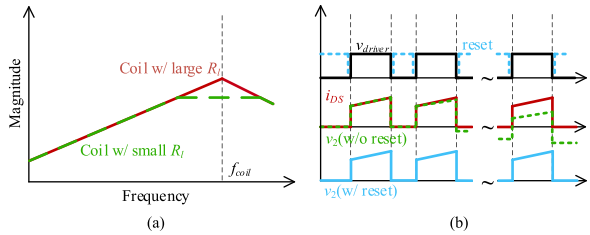

Fig. 8. Characterization of the Rogowski coil and INT1. (a) Bode diagram of the coil under different load damping. (b) Function of the reset switch S_{reset}.

horseshoe shape coil can be divided into two types, i.e., the type I in the circular edge and the type II in the rectangular edge. For any single-turn type I winding in Fig. 7(a), the magnetic field intensity $\vec{B}_1$ perpendicular to the cross section of the winding produced by the measured current i at any point P inside the winding can be expressed as

$$\vec{B}_1 = \cos\alpha \frac{\mu_0 i}{2\pi(2r\cos\alpha + a\cos\alpha)} \tag{33}$$

where μ_0 is vacuum permeability, a is the distance between point P and the inner diameter of the coil. The magnetic flux of the single-turn winding can be obtained by integrating. Accordingly, the induced voltage of the single-turn winding under the changing current i can be expressed as

$$v_{\text{out1\_}n} = \cos\alpha \frac{\mu_0 h}{2\pi} \ln \frac{2r\cos\alpha + w\cos\alpha}{2r\cos\alpha} \frac{di}{dt} \tag{34}$$

where h is the height of the via. Further, the total output induced voltage of all the N_1 turns type I winding can be expressed as

$$v_{\text{out1}} = \text{Re}\left[e^{\frac{\pi}{N_1}} \frac{e^{\frac{\pi}{N_1}} - e^{\frac{\pi}{4}}}{1 - e^{\frac{\pi}{N_1}}} \right] \frac{4\mu_0 h}{2\pi} \ln \frac{2r + w}{2r} \frac{di}{dt}. \tag{35}$$

Furthermore, the induced voltage of the single-turn type II winding and all the N_2 turns type II winding under the changing current i can be expressed as

$$v_{\text{out2\_}n} = \cos\beta \frac{\mu_0 h}{2\pi} \ln \frac{(l/2)\cos\beta + w\cos\beta}{(l/2)\cos\beta} \frac{di}{dt} \tag{36}$$

$$v_{\text{out2}} = \text{Re}\left[e^{\frac{\pi}{N_2}} \frac{e^{\frac{\pi}{N_2}} - e^{\frac{\pi}{4}}}{1 - e^{\frac{\pi}{N_2}}} \right] \frac{4\mu_0 h}{2\pi} \ln \frac{(l/2) + w}{l/2} \frac{di}{dt}. \tag{37}$$

Based on (35) and (37), the theoretical mutual inductance M of the designed Rogowski coil can be obtained by

$$M = \frac{v_{\text{out1}} + v_{\text{out2}}}{di/dt}. \tag{38}$$

With the design parameters of $N_1 = 120$, $N_2 = 70$, $l/2 = r = 12$ mm, $w = 1.1$ mm, and $h = 3$ mm, M can be obtained as 6.37 nH. Besides, the simulation value of M obtained by the Ansoft Q3D is 6.26 nH. According to the standard analytical mutual inductance solutions of the regular shapes given in [40], the theoretical value of M increases by about 20% at the same turn-number density.

As shown in Fig. 4, except for the mutual inductance M, the practical lumped model of the PCB Rogowski coil also includes the self-inductance L_{sm}, the internal resistance R_s, and the equivalent parallel capacitance C_s. Considering the effect of the load damping R_l ($R_l = R_{l1} + R_{l2}$), the transfer function of the Rogowski coil stage can be expressed as

$$G_0 = \frac{U(s)}{I(s)} = \frac{-sMR_l}{s^2 R_l L_{sm} C_s + s(L_{sm} + R_l R_s C_s) + R_l + R_s} \tag{39}$$

where $U(s)$ is the output of the practical coil. If the design value of R_l is suitable, the coil behaves as a mutual inductance M with the magnitude rising at 20dB/dec below the resonant frequency f_{coil}, as the red solid line shown in Fig. 8(a). Thus, v_1 can be expressed approximately as

$$v_1 \approx -\frac{MR_{l2}}{R_{l1} + R_{l2}} \frac{di_{DS}}{dt} \tag{40}$$

where the ratio of R_{l1} and R_{l2} is used to adjust the range of v_1. Furthermore, the magnitude descends at -20dB/dec above f_{coil} because of the two pole points. However, if the two poles are all real solutions, the coil behaves as the green dashed line with constant magnitude in a wide frequency domain. In fact, the coil works in the self-integral state but not the differential state under this condition. Therefore, R_l needs to be reasonably designed to adjust the poles of the transfer function. The eigenvalues Δ of (39) should be less than zero to ensure that the poles have imaginary parts

$$\Delta = (L_{sm} + R_l R_s C_s)^2 - 4(R_s + R_l) R_l L_{sm} C_s. \tag{41}$$

Then, the range of the load damping can be obtained as

$$R_l > \sqrt{\frac{L_{sm}^2}{4L_{sm}C_s - R_s^2 C_s^2}}. \tag{42}$$

where $4L_{sm}C_s > R_s^2 C_s^2$ must be satisfied.

Moreover, in order to reduce the effects of parasitic parameters and improve the dynamic performance of the coil, it is necessary to further optimize the load damping value. If the equivalent transformer output voltage v_{out} is taken as the input of the second-order circuit composed of the parasitic parameters, the transfer function can be expressed as

$$G_1 = \frac{U(s)}{U_{\text{out}}(s)} = \frac{R_l}{s^2 R_l L_{sm} C_s + s(L_{sm} + R_l R_s C_s) + R_l + R_s}. \tag{43}$$

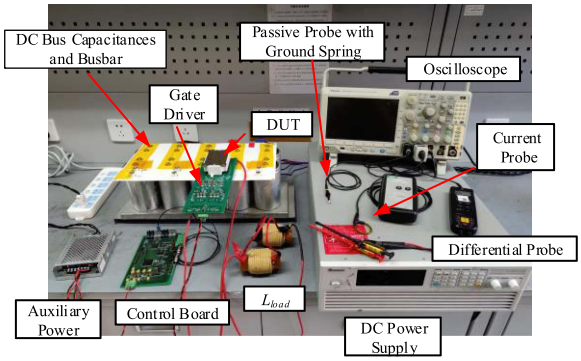

Fig. 9. Experiment platform of the proposed AGD.

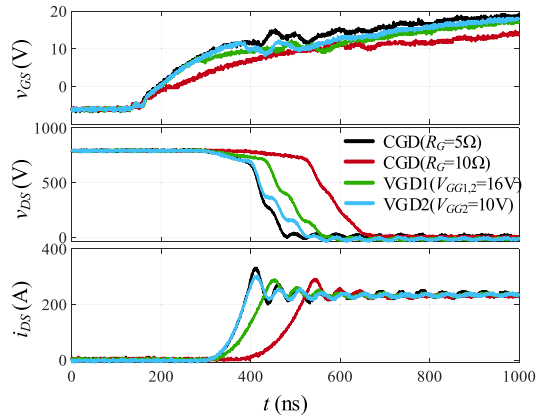

Fig. 10. Comparison of measured turn-ON waveforms under different gate drivers.

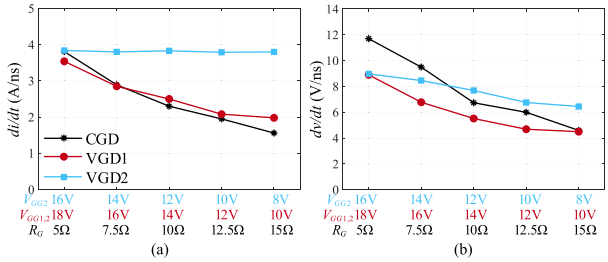

Fig. 11. Comparison of experimental results under different gate drivers. (a) Driver parameters and di/dt. (b) Driver parameters and dv/dt.

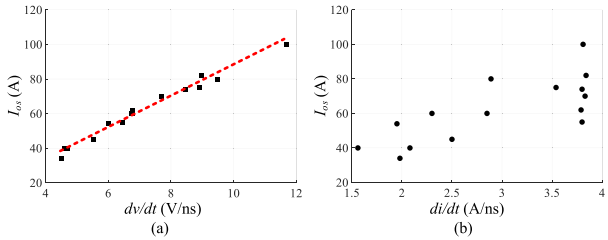

Fig. 12. Statistics of the relationship between the experimental change rate parameters and current overshoot I_{os}. (a) dv/dt and I_{os}. (b) di/dt and I_{os}.

As a typical second-order system, its damping ratio ξ can be expressed as

$$\xi = \frac{L_{sm} + R_l R_s C_s}{2\sqrt{R_l L_{sm} C_s (R_l + R_s)}}. \tag{44}$$

When ξ is designated as the optimal damping ratio 0.707, the value of R_l can be obtained as

$$R_l = \sqrt{\frac{L_{sm}^2}{2L_{sm}C_s - R_s^2 C_s^2}}. \tag{45}$$

where $2L_{sm}C_s > R_s^2 C_s^2$ must be satisfied. Based on the simulation result of the Ansoft Q3D, $L_{sm} = 1618$ nH, $C_s = 1.49$ pF, and $R_s = 1.71\Omega$, R_l can be obtained as 750Ω.

B. Ancillary Circuit for the Turn-ON Process

The signal conditioning circuit includes active integrator INT1, reset switch circuit S_{reset}, and comparator COMP1. The active integrator converts the value of v_1 into v_2, and realizes the reconstruction of i_{DS}. If S_{reset} remains OFF , the transfer function of INT1 is

$$H_s = -\frac{1}{1 + R_f C_f} \frac{R_f}{R_i} \approx -\frac{1}{R_i C_f s} \tag{46}$$

where $R_f \gg R_i$ must be satisfied. Then, v_2 can be expressed as

$$v_2 = -\frac{1}{R_i C_f} \int v_1 dt \approx \frac{1}{R_i C_f} \frac{M R_{l2}}{R_{l1} + R_{l2}} i_{DS}. \tag{47}$$

In addition, as shown in Fig. 8(b), the nonideal characteristics of the amplifier may cause the accumulated offset of INT1. To address this problem, switch S_{reset} is used to reset the active integrator when the SiC MOSFET is in the OFF-state every cycle. The control signal of S_{reset} is synchronously complementary to the gate driver signal v_{driver}. In this way, the initial value of the active integrator is ensured to be zero before the turn-ON process at each cycle, and the accumulated offset problem is satisfactorily solved. Furthermore, the pull-down circuit includes the ancillary gate resistance R_{on}, diode D_1, and switch T_1 and M_1. T_1 is controlled by the output voltage of COM1, while M_1 is controlled by the control IC.

According to the proposed driver parameter dynamic configuration in Section II, the gate charging speed of the SiC MOSFET during the voltage falling stage should be reduced to achieve better turn-ON switching performance. The proposed ancillary circuit for the turn-ON process identifies the voltage falling stage by detecting the moment that the device current reaches the load current I_L. The turn-ON waveforms of the SiC MOSFET and signals of the ancillary circuit are shown in Fig. 5, where the dashed lines of the device's voltages and currents waveforms represent the switching process without the auxiliary circuit, while the solid lines represent the behavior under the effect of the auxiliary circuit. When the SiC MOSFET is turned-on by v_{driver} at t_0, the control signal of M_1 s_1 is turned to high by the control IC so that the auxiliary circuits can be connected to the gate of the SiC MOSFET. After the turn-ON delay stage, i_{DS} begins to rise, and the active integrator begins to integrate at the same time. According to (47), v_2 is proportional to the devices' power

TABLE I
COMPARISON OF TURN-ON SWITCHING PERFORMANCE BETWEEN CGD AND VGDS

	I_{os} (A)	E_{on} (mJ)	dv_{DS}/dt (V/ns)	di_{DS}/dt (A/ns)	T_{on} (ns)
Original CGD ($R_G = 5\Omega$)	100	11.26	11.7	3.81	359
CGD ($R_G = 10\Omega$)	60	19.46	6.74	2.3	563
VGD1 ($V_{GG1,2} = 16V$)	60	17.78	6.78	2.85	453
VGD2 ($V_{GG2} = 10V$)	62	13.8	6.76	3.79	415

TABLE II
COMPARISON OF TURN-ON SWITCHING PERFORMANCE BETWEEN CGD AND AGD

	I_{os} (A)	E_{on} (mJ)	dv_{DS}/dt (V/ns)	di_{DS}/dt (A/ns)	T_{on} (ns)
Original CGD ($R_G = 5\Omega$)	100	11.26	11.7	3.81	359
AGD ($R_{on} = 3.6\Omega$)	42	16.31	4.61	3.8	410
CGD ($R_G = 15\Omega$)	40	26.79	4.6	1.56	1057
AGD ($R_{on} = 10\Omega$)	60	13.8	6.78	3.8	398
CGD ($R_G = 10\Omega$)	60	19.46	6.74	2.3	563

stage current. Therefore, the reference voltage V_{ref1} of COMP1 can be designated according to the value of v_2 coming from the actual load current I_L, which can be expressed as

$$V_{\text{ref1}} = \frac{1}{R_i C_f} \frac{M R_{l2}}{R_{l1} + R_{l2}} I_L. \tag{48}$$

However, considering the operation delay of COMP1 and T1, the corresponding current of the practical reference voltage must be lower than I_L. When v_2 reaches the reference voltage, the output voltage of COM1 v_3 reaches high to switch ON T_1. Then, i_G is shunted by the auxiliary circuit current i_{on}, which realizes the function of decreasing the gate charging speed, and i_{on} can be expressed as

$$i_{on} = \frac{V_{\text{miller}} - V_{F\_D_1} - V_{F\_T_1} - V_{F\_M_1}}{R_{on}} \tag{49}$$

where $V_{F\_D_1}$, $V_{F\_T_1}$, and $V_{F\_M_1}$ is the ON-state forward voltage of D_1, T_1, and M_1. According to (13) and (16), the drain-source voltage change rate during the voltage falling stage is reduced and the current overshoot during the turn-ON process is mitigated, and the reduced drain-source voltage change rate can be expressed as

$$\frac{dv'_{DS}}{dt} = -\frac{V_{GG} - V_{\text{miller}}}{C_{DG} R_G} + \frac{i_{on}}{C_{DG}}. \tag{50}$$

It can be seen that the degree of the auxiliary circuit's influence can be adjusted by changing the value of R_{on}. The smaller the R_{on}, the greater the effect of the auxiliary circuit on the gate charging speed. In order to ensure the normal operation of the voltage falling stage, i_{on} and R_{on} must satisfy that

$$i_{on} < i_G = \frac{V_{GG} - V_{\text{miller}}}{R_G} \tag{51}$$

$$R_{on} > R_G \frac{V_{\text{miller}} - V_{F\_D_1} - V_{F\_T_1} - V_{F\_M_1}}{V_{GG} - V_{\text{miller}}}. \tag{52}$$

After the voltage falling stage, M_1 should be turned OFF to disconnect the auxiliary circuit.

C. Ancillary Circuit for the Turn-OFF Process

The ancillary circuit for the turn-OFF process mainly consists of comparator COMP2 and pull-up circuit, as shown in Fig. 4. The pull-up circuit includes the ancillary gate resistance R_{off}, diode D_2, and switch T_2, T_3, and M_2. T_2 is controlled by the output voltage of the COM2, while M_2 is controlled by the control IC. According to the proposed driver parameter dynamic configuration in Section II, the gate discharging speed of the SiC MOSFET during the current falling stage should be reduced to mitigate the overvoltage. The proposed ancillary circuit for the turn-OFF process identifies the current falling stage by detecting the beginning of the current falling behavior. The turn-OFF waveforms of the SiC MOSFET and signals of the ancillary circuit are shown in Fig. 5, where the dashed lines of the device's voltages and currents waveforms represent the switching process without the auxiliary circuit while the solid lines represent the behavior under the effect of the auxiliary circuit. When the SiC MOSFET is turned-OFF by v_{driver} at t_5, the control signal of M_2 s_2 is turned to high by the control IC so that the auxiliary circuits can be connected to the gate of the SiC MOSFET. After the turn-OFF delay stage and the voltage rising stage, i_{DS} begins to decrease sharply, and the Rogowski coil outputs a positive voltage that can be used to drive COMP2. The reference voltage V_{ref2} of COMP2 can be designated according to the current change rate at the initial moment of the current falling stage, which can be expressed as

$$V_{\text{ref2}} = \frac{M R_{l2}}{R_{l1} + R_{l2}} \frac{V_{\text{miller}} - V_{SS}}{L_S + (R_G C_{GS})/g_m}. \tag{53}$$

The device in this process is in the state of complete conduction, and g_m can take the constant value g_{m_ln} of the region where the channel current and v_{GS} have a linear relationship in the transfer characteristic curve. Similarly, considering the operation delay of COMP2 and T3, the practical reference voltage must be less than the theoretical value. With the toggle of COMP2, T_2 is

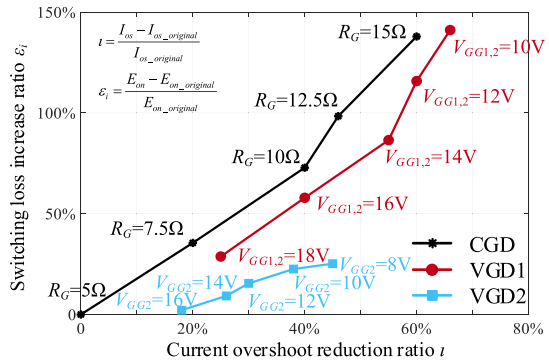

Fig. 13. Comparison of the turn-ON switching performance adjustment efficiency with different gate drivers (I_{os} and E_{on} are the experimental results under VGD1, VGD2, or changed CGD conditions, $I_{os\_original}$ and $E_{on\_original}$ are the experimental results under the original CGD condition).

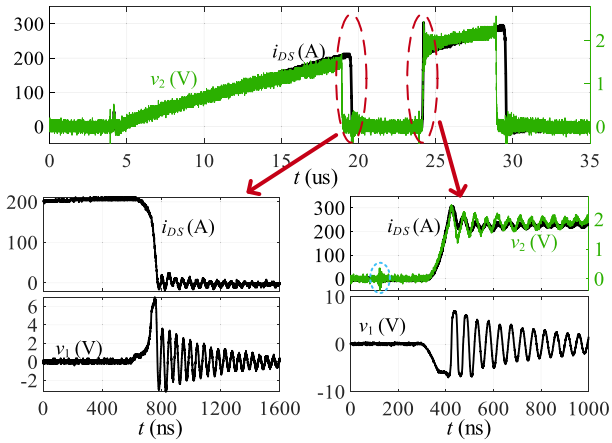

Fig. 14. Experimental characterizations of the Rogowski coil and INT1.

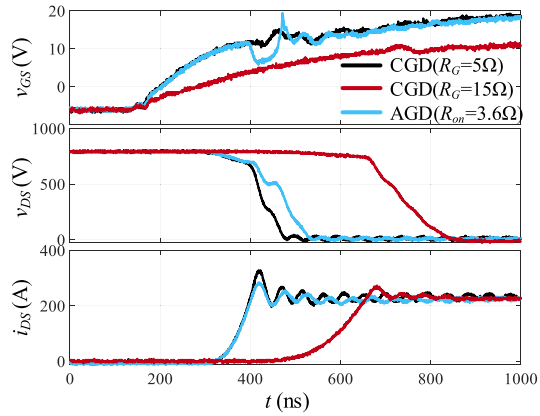

Fig. 15. Comparison of measured turn-ON waveforms between CGD and AGD ($R_{on} = 3.6\Omega$).

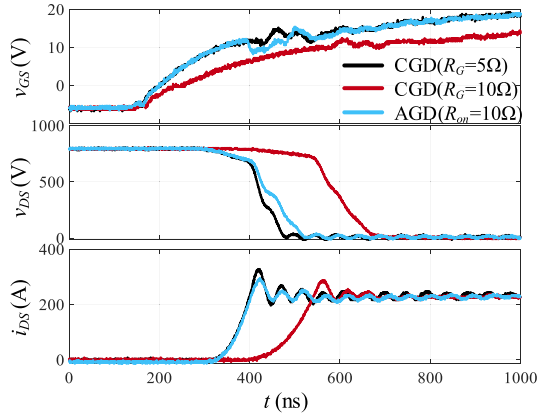

Fig. 16. Comparison of measured turn-ON waveforms between CGD and AGD ($R_{on} = 10\Omega$).

turned ON, and i_G is shunted by the auxiliary circuit current i_{off}. Then, the gate discharging speed and power stage current change rate of the SiC MOSFET are reduced. And the voltage overshoot of the turn-OFF process is mitigated as well. i_{off} can be expressed as

$$i_{\text{off}} = \frac{V_{GG} - V_{\text{miller}} - V_{F\_D_2} - V_{F\_T_3}}{R_{\text{off}}} \tag{54}$$

where $V_{F\_D_2}$ and $V_{F\_T_3}$ is the ON-state forward voltage of D_2, T_3. The reduced average current change rate of i_{DS} can be approximately expressed as

$$\frac{di'_{DS}}{dt} = \frac{V_{SS} - \left(\frac{I_L}{2g_m} + V_{TH}\right) + R_G i_{\text{off}}}{(R_G C_{\text{iss}})/g_m}. \tag{55}$$

Similarly, the affected gate discharging speed can be adjusted by changing the value of R_{off}. The smaller the R_{off}, the more obvious the effect of the auxiliary circuit on the gate discharging speed. In order to ensure the normal operation of the turning OFF process, i_{off} and R_{off} need to satisfy that

$$i_{\text{off}} < |i_G| = \left|\frac{V_{SS} - V_{\text{miller}}}{R_G}\right| \tag{56}$$

$$R_{\text{off}} > R_G \left|\frac{V_{GG} - V_{\text{miller}} - V_{F\_D_2} - V_{F\_T_3}}{V_{SS} - V_{\text{miller}}}\right|. \tag{57}$$

After the current falling stage, v_4 reaches low to switch OFF T_2, and M_2 also can be turned OFF at an appropriate point of time to disconnect the auxiliary circuit.

IV. Experimental Verification and Performance Analysis

A double-pulse test platform is established to verify the proposed driver parameter dynamic configuration and the AGD circuit, as shown in Fig. 9. The SiC MOSFET tested in this article is the 1700 V/300 A SiC MOSFET CAS300M17BM2 from CREE, Inc. The lower device serves as the SiC MOSFET under test and the upper one serves as the freewheeling diode. Two parallel air-core inductors serve as the inductive load. The total value of L_{load} is 40 uH. The dc bus voltage is 800 V, I_L is 230 A. The CGD with fixed gate resistance and driver voltage is denoted as the original condition, where $R_G = 5\Omega$, V_{GG} is 20 V, and V_{SS} is -5 V. In addition, a Tektronix MDO3034 oscilloscope is used for the measurement, and a Tektronix TPP0500B passive probe with flex ground spring, a Tektronix THDP0200 high

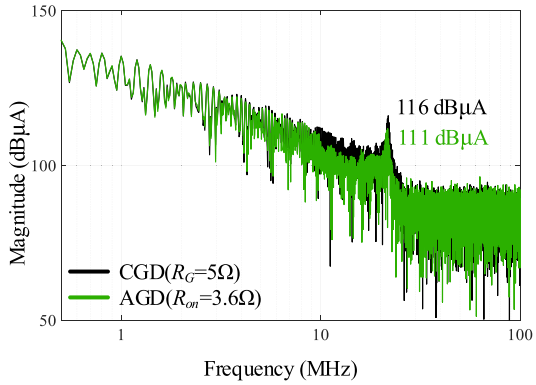

Fig. 17. Comparison of current spectrums between CGD and AGD ($R_{on} = 3.6\Omega$).

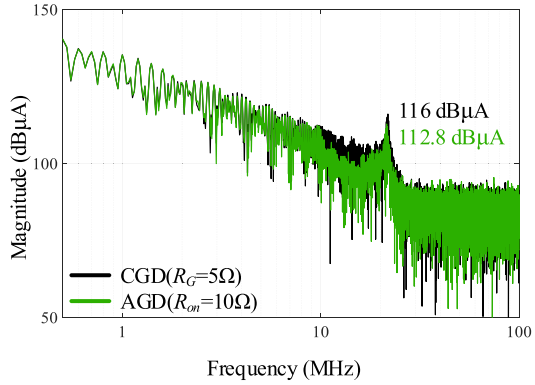

Fig. 18. Comparison of current spectrums between CGD and AGD ($R_{on} = 10\Omega$).

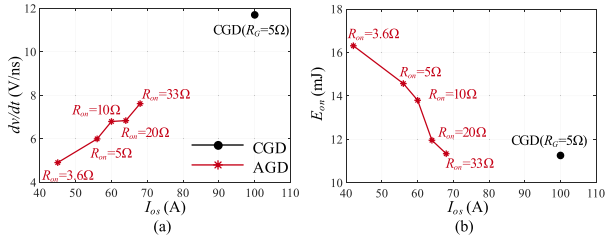

Fig. 19. Turn-ON switching performance of AGD with different parameters. (a) I_{os} and dv/dt. (b) I_{os} and turn-ON switching loss.

voltage differential probe, and a PEM CWTMini 3B Rogowski Coil current probe are used to measure v_{GS}, v_{DS}, and i_{DS}, respectively.

A. Performance Comparison of Different Gate Driver Trajectory for the Turn-ON Process

Three gate drivers are compared to verify the influences of the gate driver configurations on the current overshoot and switching loss of the turn-ON process. In addition to the CGD with different gate resistances, two stage-control schemes by the open-loop parameter design are also carried out. Specifically, reducing the driver supply voltage during the current rising stage and voltage falling stage (i.e., V_{GG1} and V_{GG2}) is denoted as VGD1, reducing the driver supply voltage during the voltage falling stage (i.e., only V_{GG2}) is denoted as VGD2, and R_G is retained as 5Ω in these two schemes. The method of reducing the driver supply voltage is adjusting the linear region of the switching device in the totem pole by changing the input voltage of the push–pull circuit.

The waveforms of the original condition and three other gate drivers with the same current overshoot reduction are shown in Fig. 10, where $R_G = 10\Omega$ for the CGD of changing R_G, $V_{GG1} = V_{GG2} = 16$ V for the VGD1, and $V_{GG2} = 10$ V for the VGD2. Furthermore, the detailed experimental switching performances under the four different gate drivers are shown in Table I, where T_{on} is the total time of t_0 to t_3. It can be seen that, compared with the original condition, the current overshoots of the three conditions are reduced to a similar level, but their compromises of the switching loss and switching time are inconsistent. For the CGD with $R_G = 10\Omega$ and the VGD1, the switching losses increase by 73% and 58%, respectively, while that of VGD2 only increases by 22%. Meanwhile, the CGD with $R_G = 10\Omega$ has the most obvious influence on the switching time. It is worth noting that for the three experimental results at a similar current overshoot, their voltage change rate are also at a similar level, which supports the above analysis, i.e., the current overshoot of the SiC MOSFET on the turn-ON process is mainly affected by the voltage change rate.

Moreover, the experiment results of the current change rate and voltage change rate under the three gate drivers with different parameters are shown in Fig. 11. It can be seen that, different from the CGD and VGD1, which affect the voltage and current change rate simultaneously, VGD2 realizes the reduction of the voltage change rate while having almost no effect on the current change rate. As shown in Fig. 12, the statistics of the corresponding relationship between the change rate parameters and the current overshoot in the experiments can further illustrate the key factor that affects the current overshoot of the turn-ON process. There is an obvious linear relationship with an asymptotic line between the voltage change rate and current overshoot, while the relationship and distribution between the current change rate and current overshoot are chaotic. These also indirectly prove that the reverse recovery of the SiC MOSFET intrinsic diode has little effect on the current overshoot during the turn-ON process.

In addition, in order to compare the performance of different gate drivers in the tradeoff between the current overshot and switching loss, the experimental results of the switching performance adjustment efficiency are normalized in Fig. 13. Based on the experimental results of the original condition $I_{os\_original}$ and $E_{on\_original}$, current overshoot reduction ratio ι and the corresponding switching loss increase ratio ε_i under other experimental conditions are calculated, respectively, where ι and ε_i can be expressed as

$$\iota = \frac{I_{os} - I_{os\_original}}{I_{os\_original}} \tag{58}$$

$$\varepsilon_i = \frac{E_{on} - E_{on\_original}}{E_{on\_original}}. \tag{59}$$

Obviously, as a better scheme, the VGD2 can optimize the compromise of the switching loss and switching time on the premise of the same current overshoot reduction.

B. Performance of the AGD for the Turn-ON Process

The experimental characterizations of the Rogowski coil and the active integrator INT1 are shown in Fig. 14. It can be seen that the Rogowski coil realizes the differential of the current i_{DS}. And the output voltage of INT1 v_2 realizes a good reconstruction of i_{DS}. The actual mutual inductance M can be obtained as 6.16 nH by matching v_2 with i_{DS}, and considering the value of R_i and C_f. It is worth mentioning that the oscillation of v_2 before the current rising stage in the dashed blue oval is caused by the synchronous turn-OFF of the reset switch S_{reset} at the beginning of the turn-ON process. And S_{reset} is turned ON when the control IC sends the turn-OFF signal, so the integral result v_2 has been cleared at the beginning of the turn-OFF process. In addition, the current oscillation during the turn-ON process cannot be perfectly matched in the integral result because of the leakage current of the amplifier and the measurement error.

The comparisons of the turn-ON waveforms between the CGD and the proposed AGD with different parameters are shown in Figs. 15 and 16. The dc bus voltage is 800 V, and the load current is 230 A. The CGD with $R_G = 5\Omega$ is also set as the original condition, where the current overshoot is 100 A, and R_G remains as 5Ω in the AGD conditions. As shown in Fig. 15, both the CGD with $R_G = 15\Omega$ and the AGD with $R_{on} = 3.6\Omega$ reduce the current overshoot to about 40 A. It can be observed that, compared to the original condition, the turn-ON delay stage, the current rising stage, and the current change rate are almost unaffected under the AGD condition, while the overall switching speed of the turn-ON process with the CGD of $R_G = 15\Omega$ is reduced obviously. The phenomenon in Fig. 16 is similar, except that the current overshoot is 60 A. In order to further compare the turn-ON switching performance with different drivers, the detailed experimental results of the turn-ON process are shown in Table II. Based on the original condition, when the current overshoot is reduced from 100 to 60 A, the CGD increases the turn-ON loss by 73%, while the AGD only increases the turn-ON loss by 23%. Furthermore, when the current overshoot is reduced to 40 A, the CGD increases the turn-ON loss by 138%, while the AGD increases the turn-ON loss by 45%. Moreover, considering the impact of the CGD on the turn-ON delay stage and the current rising stage of the turn-ON process, the corresponding total duration of the first three stages is increased by an additional 47% and 180%, respectively. The spectrums of i_{DS} in these two comparisons are shown in Figs. 17 and 18. The amplitude of the spectrums from 10 to 20 MHz are effectively mitigated with the AGD. And the EMI induced by the overshoot and oscillation of i_{DS} is suppressed as well.

Besides, in order to illustrate the relationship between R_{on} and the effect of the AGD, the experimental results of the AGD with other R_{on} are shown in Fig. 19. With the increase of R_{on}, the current overshoot and voltage change rate are increased, while the turn-ON loss is reduced. But the current overshoot is always less than that of the original CGD. To further evaluate the performance of the proposed AGD, the normalized current overshoot reduction ratio ι and the corresponding switching loss increase ratio ε_i of the proposed AGD and other literature are shown in Fig. 20. It can be seen that the proposed AGD has significantly better performance than the AGDs used in other literature in terms of reducing the current overshoot while optimizing the compromise of the switching loss. Furthermore, it also proves the effectiveness of the proposed optimized driver parameter dynamic configuration for the turn-ON process of the SiC MOSFET.

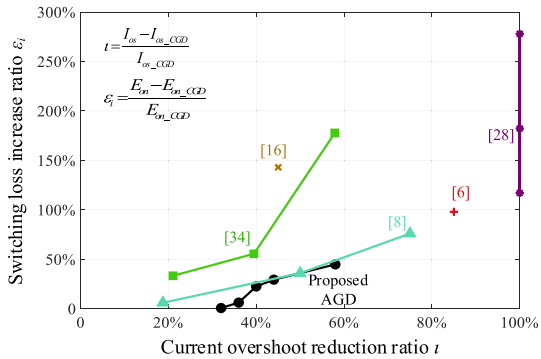

Fig. 20. Comparison of the turn-ON switching performance adjustment efficiency between the proposed AGD and AGDs in other literature (I_{os} and E_{on} are the experimental results under the AGD conditions, I_{os_CGD} and E_{on_CGD} are the experimental results under the corresponding CGD condition).

TABLE III
COMPARISON OF TURN-ON SWITCHING PERFORMANCE BETWEEN CGD AND AGD UNDER DIFFERENT LOAD CURRENT CONDITIONS

	I_{os} (A) CGD	I_{os} (A) AGD	E_{on} (mJ) CGD	E_{on} (mJ) AGD
$I_L = 230$A	100	42	11.26	16.31
$I_L = 200$A	76	36	9.43	15.74
$I_L = 150$A	72	36	7.32	12
$I_L = 100$A	65	41	5.23	7.91
$I_L = 50$A	55	40	3.46	5.08

In addition, the turn-ON waveforms between the CGD and AGD under different load currents are shown in Fig. 21. And the specific experimental data are shown in Table III. R_G of the CGD and AGD are all set to 5Ω, R_{on} of the AGD is set to 3.6Ω, and V_{ref1} varies with the load currents in these experiments. It can be observed that the proposed AGD can reduce current overshoot and suppress oscillation intensity compared to the CGD under different load current conditions.

C. Performance of the AGD for the Turn-OFF Process

The comparisons of the turn-OFF waveforms between the CGD and AGD with different parameters are shown in Figs. 22 and 23. The dc bus voltage and load current retain at their

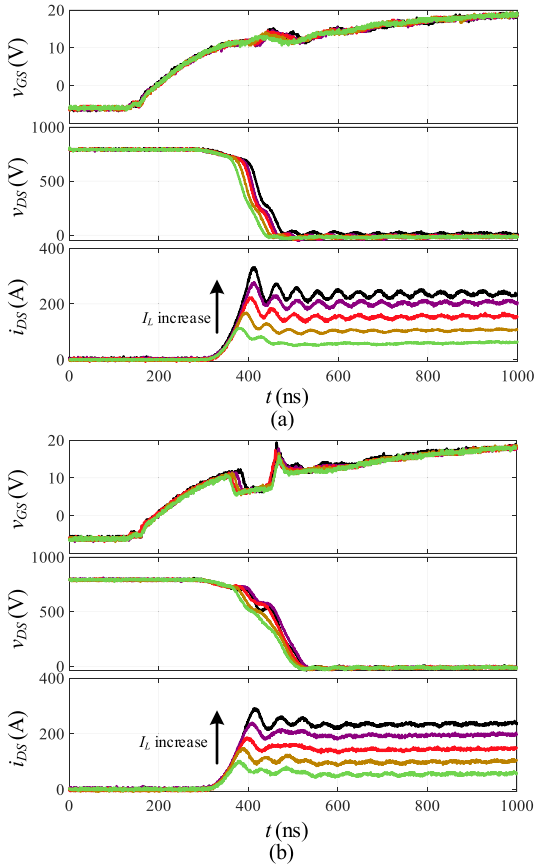

Fig. 21. Measured turn-ON waveforms for CGD and AGD under different load current I_L. (a) CGD. (b) AGD.

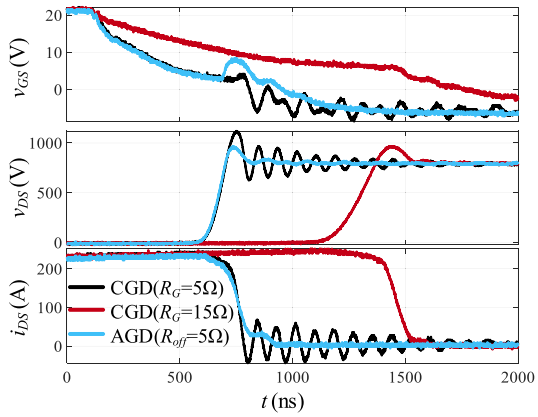

Fig. 22. Comparison of measured turn-OFF waveforms between CGD and AGD ($R_{\text{off}} = 5\Omega$).

original values. The CGD with $R_G = 5\Omega$ is denoted as the original condition as well, and R_G remains the same under the AGD conditions. As shown in Fig. 22, both the CGD with $R_G = 15\Omega$ and the AGD with $R_{\text{off}} = 5\Omega$ reduce the voltage overshoot from 320 to about 160 V. Similarly, the turn-OFF delay stage, the voltage rising stage, and the voltage change rate are almost unaffected under the AGD condition, while the overall switching speed of the turn-OFF process with the CGD

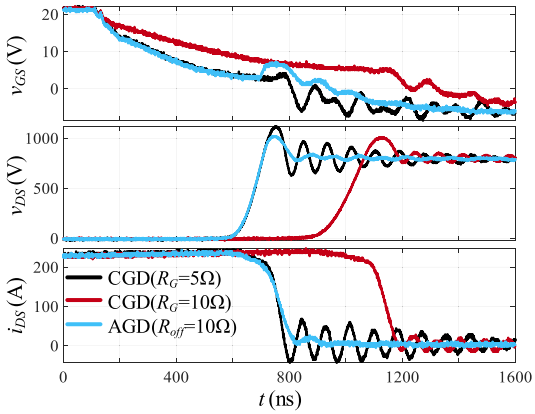

Fig. 23. Comparison of measured turn-OFF waveforms between CGD and AGD ($R_{\text{off}} = 10\Omega$).

TABLE IV
COMPARISON OF TURN-OFF SWITCHING PERFORMANCE BETWEEN CGD AND AGD

	V_{os} (V)	E_{off} (mJ)	dv_{DS}/dt (V/ns)	di_{DS}/dt (A/ns)	T_{off} (ns)
Original CGD ($R_G = 5\Omega$)	320	18.99	8.76	2.76	674
AGD ($R_{off} = 5\Omega$)	160	20.8	8.76	1.25	814
CGD ($R_G = 15\Omega$)	160	40.46	3.96	1.22	1535
AGD ($R_{off} = 10\Omega$)	200	19.3	8.74	1.8	715
CGD ($R_G = 10\Omega$)	200	28.95	4.22	1.78	1135

of $R_G = 15\Omega$ is reduced obviously. The phenomenon in Fig. 23 is also similar, except that the voltage overshoot is reduced to 200 V. The detailed experimental results of the turn-OFF process with these drivers are shown in Table IV, where T_{off} is the total time of t_5 to t_8. Based on the original condition, when the voltage overshoot is reduced from 320 to 200 V, the CGD increases the turn-OFF loss by 52%, while the AGD only increases the turn-OFF loss by 1.6%. Furthermore, when the voltage overshoot is reduced to 160 V, the CGD increases the turn-OFF loss by 113%, while the AGD increases the turn-OFF loss by 9.5%. Moreover, the corresponding total duration of the first three stages in the turn-OFF process is increased by an additional 62% and 127% considering the impact of CGD in the turn-OFF delay stage and the voltage rising stage. The spectrums of v_{DS} in these two comparisons are shown in Figs. 24 and 25. The amplitude of the spectra from 10 to 20 MHz are effectively mitigated with

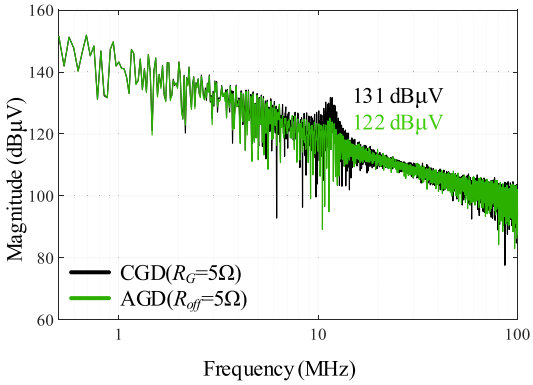

Fig. 24. Comparison of voltage spectrums between CGD and AGD ($R_{\text{off}} = 5\Omega$).

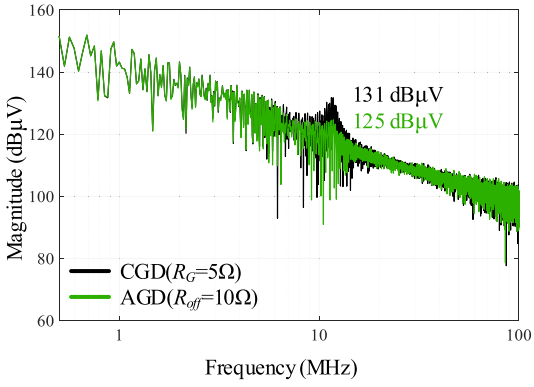

Fig. 25. Comparison of voltage spectrums between CGD and AGD ($R_{\text{off}} = 10\Omega$).

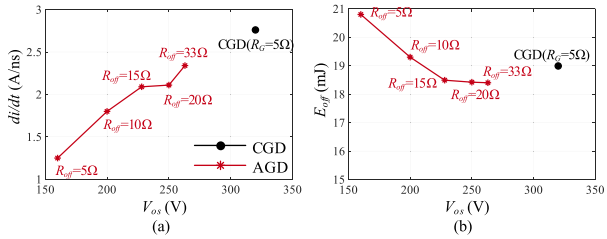

Fig. 26. Turn-OFF switching performance of AGD with different parameters. (a) V_{os} and di/dt. (b) V_{os} and turn-OFF switching loss.

the AGD. And the EMI induced by the overshoot and oscillation of v_{DS} is suppressed as well.

Besides, the experimental results of the AGD with other R_{off} are shown in Fig. 26, which indicates the relationship between R_{off} and the effect of the AGD. With the increase of R_{off}, the voltage overshoot and current change rate are increased, while the turn-OFF loss is reduced. But the voltage overshoot is always less than that of the original CGD. Different from the experimental results of the turn-ON process, when the effect of the AGD is slight, the turn-OFF loss is reduced. The normalized voltage overshoot reduction ratio υ and the corresponding switching loss influence ratio ε_υ of the proposed AGD and those used in other literature are shown in Fig. 27. The expression of υ and ε_υ can

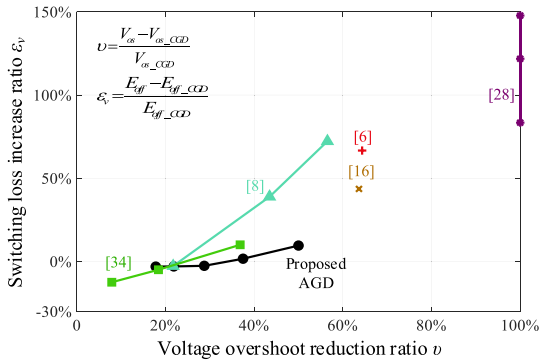

Fig. 27. Comparison of the turn-OFF switching performance adjustment efficiency between the proposed AGD and AGDs in other literature (V_{os} and E_{off} are the experimental results under the AGD conditions, V_{os_CGD} and $E_{\text{off\_CGD}}$ are the experimental results under the corresponding CGD condition).

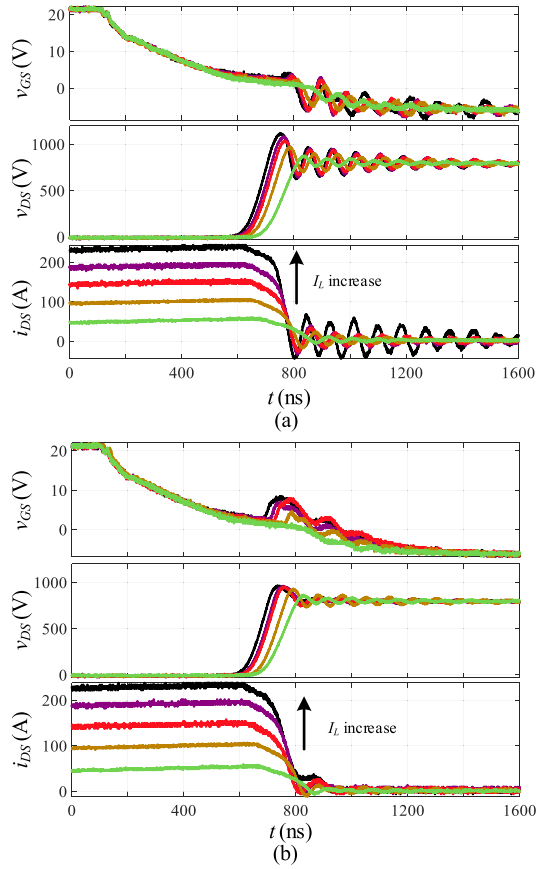

Fig. 28. Measured turn-OFF waveforms for CGD and AGD under different load current I_L. (a) CGD. (b) AGD.

refer to (58) and (59). The proposed AGD has better performance than the AGDs of other literature in terms of reducing voltage overshoot while optimizing the compromise of the switching loss.

The turn-OFF waveforms between the CGD and AGD under different load currents are shown in Fig. 28. And the specific experimental data are shown in Table V. R_G of the CGD and AGD are all set to 5Ω, R_{off} of the AGD is set to 5Ω. It can be

TABLE V
COMPARISON OF TURN-OFF SWITCHING PERFORMANCE BETWEEN CGD AND AGD UNDER DIFFERENT LOAD CURRENT CONDITIONS

	V_{os} (V) CGD	V_{os} (V) AGD	E_{off} (mJ) CGD	E_{off} (mJ) AGD
$I_L = 230$A	320	160	18.99	20.8
$I_L = 200$A	284	156	13.17	13.56
$I_L = 150$A	236	160	9.1	8.76
$I_L = 100$A	171	140	5.31	4.96
$I_L = 50$A	76	65	2.47	2.24

seen that the AGD can reduce voltage overshoot and suppress oscillation intensity compared to the CGD under different load current conditions.

V. CONCLUSION

A novel stage-detection closed-loop control AGD for SiC MOSFETs is proposed in this article, which realizes the isolated switching stage identification based on the PCB Rogowski coil. And the influence of the parasitic parameters on the stage identification threshold design is weakened, especially for the turn-ON process, where the threshold design is basically only related to the load current. For the control objective of mitigating the overshoot and oscillation while reducing the compromise of the switching loss and switching time, the optimal gate driver trajectory for the turn-ON process should be reducing the gate charging speed only in the voltage falling stage, since the current overshoot of the SiC MOSFET in the turn-ON process only has high relevancy with the voltage change rate but not with the current change rate. Furthermore, the optimal scheme for the turn-OFF process is reducing the gate discharging speed only in the current falling stage. Moreover, the proposed AGD can not only effectively reduce the overshoot of the switching process but also suppress the oscillation intensity and the induced EMI. And the AGD significantly reduces the compromise of the switching loss and switching time on the premise of reducing overshoot, which has an outstanding performance in terms of balancing the tradeoff between the overshoot and the switching loss.

Besides, the present circuit can be further expanded if the proposed AGD needs to realize the self-adaptive application under variable load conditions or ac conditions. Specifically, the reference voltages of the auxiliary circuits can be defined and adjusted by the control IC every switching period according to the control signal of the host computer or the sampling result of the load current, where the sampling of the load current has been realized by the active integrator.

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